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Design Oriented Analysis of Switched Capacitor DC–DC Converters

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ABSTRACT A novel approach to the design of switched capacitor (SC) converters is presented in this article. By recognizing the relationship between three design parameters in SC converters, namely capacitance, switching frequency, and switch on-resistance, this work is able to align the design method of SC more closely with conventional power converters. Using the charge-multiplier framework for design, capacitor sizes can be related to one another and subsequently to output voltage ripple, a key design parameter of converters. Optimization tools are used to take the equations developed for hand calculation and enable a more broad generalization of how SC converters can be designed. Typically it is thought that the larger the voltage ripple in SC converters is, the less efficient the converter is. However, this design method shows that this is not necessarily the case. Experimental prototypes are designed with these tools to show the validity of the proposed method.

INDEX TERMS Power electronics, switched capacitor design, capacitive energy transfer, design oriented analysis.

I. INTRODUCTION

Switched Capacitor (SC) converters have been investigated as solutions in a number of space constrained battery-powered and power harvesting applications [1], [2]. They have been increasingly used in novel multi-stage power management systems [3] and as parts of emerging hybrid converter topologies [4], [5].

They are also available as products where they are able to provide increased power density compared to the conventional buck and boost solutions, typically at lower cost and lower complexity. Examples include LED drivers (Texas Instruments LM2753), power supplies for op-amps (Linear Technologies LTC1517-3.3) and power supplies for gate-drivers (Maxim Integrated MAX619).

SC converters have significantly higher power density than conventional inductive based converters in integrated, low-power applications while maintaining high power processing efficiency [6], [7]. This increased power density [8], [9], [10] is a result of much larger energy storage capacity per unit volume of capacitors compared to inductors [11]. Along with this, the development of CMOS based trench capacitors has created opportunities for cost-effective full on-chip integration of SC converters by utilizing deep-trench capacitors [12], [13].

The fundamental principles of SC converter operation have been described in a general way by at least 1995 [14] and various methods of understanding SC operation have been proposed [15], [16], [17], [18]. However, compared to the large body of work and practical methods developed for design and analysis of conventional inductive topologies [19], the equivalent methods for SC converters are relatively sparse and do not provide a complete understanding of design trade-offs. As a result, the design and analysis of the SC topologies remains challenging.

A pioneering work on design-oriented SC analysis is presented in [8]. There, a practical design methodology for DC-DC SC converters is given. Several SC topologies are investigated and a method to analyse and optimize them is provided. However, this optimization is limited in the sense that it is a single objective optimization over losses with the total capacitance/capacitor volume and die area of the system are fixed. In [17] and [18], particular SC converters are designed taking into account trade-offs between volume and efficiency, but conclusions drawn from those specific applications do not

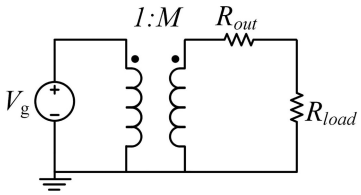

FIGURE 1. Transformer model of a SC converter.

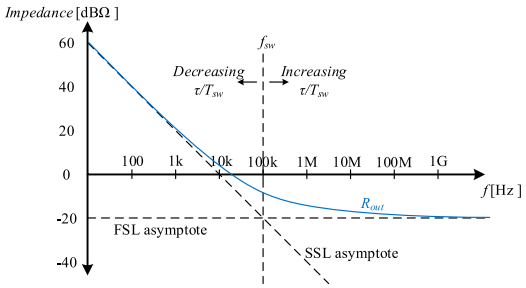

FIGURE 2. Output impedance of an arbitrary SC converter for reference. R_{out} is defined here by the root of the sum of the squares of R_{SSL} and R_{FSL}.

appear to generalize easily to other SC topologies. The work to be presented in this paper builds on the fundamental results shown [6] and [8]. The main goal is to give a more general framework for designing DC-DC SC converters, providing a better understanding of the relation between the main converter parameters and various design trade-offs along with a straightforward way of selecting these variables.

The work introduces an analysis and design methodology that produces equations relating the fundamental design variables of SC converters (capacitance, switching frequency and switch on-resistance) to the switch capacitor topology, output voltage ripple, desired power processing efficiency, and switch parameters. These equations not only give a better understanding of design trade-offs compared to previously presented methods, but also create practical guidelines for designing DC-DC SC converters.

This paper is organized as follows: First a brief explanation of previous SC analysis presented in [8] is provided. Loss and volume models for SC converters are shown to provide a framework over which a converter is to be optimized. From the previous analysis in [8] and loss models developed here, explicit equations for SC capacitors, switch on-resistances and switching frequency are derived. Next, a design example of 1:5 SC converter is given to demonstrate the design algorithm using these equations. Area of the converter is then taken into account and a multi-objective convex optimization technique based on [20] is developed. The effectiveness of both the design algorithm and the volume/efficiency optimization technique is demonstrated with experimental prototypes. The design algorithm is applied to the 1:5 Fibonacci converter and multi-objective optimization is applied to the 1:2 SC converter to demonstrate an increase in efficiency with increased voltage ripple.

II. SWITCHED CAPACITOR CONVERTER BACKGROUND

The methodology for the design of SC converters presented in [8] starts with the general DC model shown in Fig. 1. This basic model includes a DC transformer with turns ratio $1 : M$, which represents the nominal (unloaded) gain of the SC, and an output impedance R_{out}. As the load increases, the output voltage tends to drop based on the product of the load current and the output impedance.

It has been shown that this output impedance is frequency dependent and has two limits, referred to as the slow switching limit (SSL) and the fast switching limit (FSL) [6], [8], [14]. Intuitively, these limits represent what limits the charging/discharging of the capacitors. In SSL, the switching frequency is low relative to the time-constants of the capacitive networks in the system. This means the capacitor voltages tend to settle to their final values and current flow is limited by the capacitance. Because of this, the converter appears capacitive from the perspective of the load. In FSL, the switching frequency is high with respect to the time-constants within in the SC and the capacitors do not charge to their final value. In this case, the on-resistances of the switches limit the current flow. From the perspective of the load, the converter appears resistive. A bode plot of an example SC output impedance is shown in Fig. 2.

The concept of a charge multiplier vector is introduced in [8] to develop equations for the SSL and FSL impedances. The capacitor charge multiplier vector represents the charge that flows in and out of each capacitor in each switching state. For simplicity, the analysis presented here is restricted to SC converters with two switching states. An example 2:1 SC converter with charges flowing into and out of each capacitor in each switching state can be seen in Fig. 3.

These charges flowing in each capacitor in a single switching state are components of the charge multiplier vector organized from the output to the input and are normalized to the output charge. The vector takes the form

$$a_{c,j} = [q_{out,j} \quad q_{C,n,j} \quad \cdots \quad q_{C,1,j} \quad q_{in,j}]/q_{out}, \qquad (1)$$

where $q_{out,j}$ is the charge going to the load in jth switching state, $q_{C,n,j}$ is the charge going into the nth capacitor in the jth switching state, $q_{C,1,j}$ is the charge going into the first capacitor in the jth switching state, $q_{in,j}$ is the charge coming from the input in the jth switching state and q_{out} is the total output charge over the full switching cycle. Intuitively, this vector is related to the current each capacitor sees and the total input and output current.

From capacitor charge balance, the average capacitor voltage is constant and thus the total charge going into and coming out of each capacitor is zero in steady state. For two switching state SC converters, this means $q_{C,n,1} = -q_{C,n,2}$. Furthermore, the total output charge is the sum of the output charges in each phase, $q_{out,1} + q_{out,2} = q_{out}$ and the total

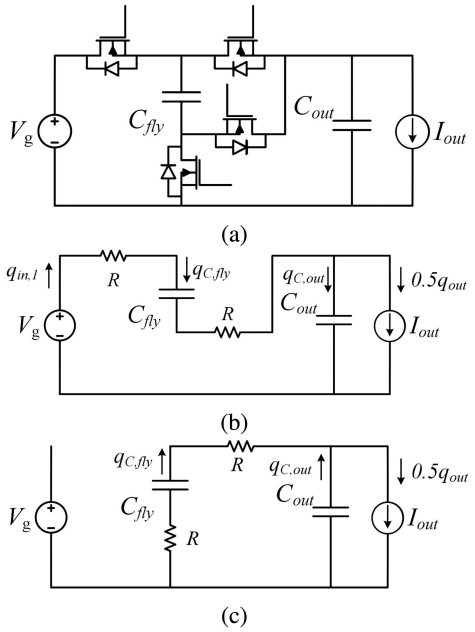

FIGURE 3. Circuit diagrams of the 2-1 SC converter. The complete circuit is shown in (a), the equivalent circuit in first switching state in (b) and the equivalent circuit in the second switching state in (c).

input charge is the sum of the input charges in each phase, $q_{in,1} + q_{in,2} = q_{in}$.

In an ideal converter, the input power is equal to the output power in steady state. Similarly, if we integrate over a switching cycle, the input energy is equal to the output energy.

$$q_{in}V_{in} = q_{out}V_{out} \tag{2}$$

Rearranging, the conversion ratio $M = \frac{V_{out}}{V_{in}}$ can be found

$$M = \frac{V_{out}}{V_{in}} = \frac{q_{in}}{q_{out}} \tag{3}$$

Let's take the 2:1 step-down SC converter shown in Fig. 3 as an example. For simplicity, a current source as a load will be assumed.

The first step is to find the charge multiplier vectors and voltages of the capacitors (as in [8]). As can be seen by the states of the SC, the sum of the capacitor voltages is the input voltage, and the two capacitor voltages are equal nominally. Thus $V_{C,fly} = V_{C,out} = V_g/2$. To find the charge multiplier vectors, we can write KCL equations in both states of the switching cycle. First, if the converter operates at a 50% duty ratio, then the load will draw equal current in both states, namely $q_{out}/2$. In the first state, we have

$$q_{C,fly} = q_{in,1} = q_{C,out} + \frac{q_{out}}{2}, \tag{4}$$

and in the second state

$$q_{C,fly} + q_{C,out} = \frac{q_{out}}{2}, \quad q_{in,2} = 0. \tag{5}$$

Summing these two equations we can see

$$q_{C,fly} = \frac{q_{out}}{2}, \quad q_{C,out} = 0. \tag{6}$$

The charge vectors are then

$$a_{c,1} = [0.5 \quad 0 \quad 0.5 \quad 0.5], \; a_{c,2} = [0.5 \quad 0 \quad -0.5 \quad 0] \tag{7}$$

These vectors make some intuitive sense. The conversion ratio is 2:1, and the input charge (or current) is half the output charge while the output voltage is half the input voltage. An unintuitive result for the 2:1 converter is that charge of the output capacitor, $q_{C,out}$, is zero, meaning is charge multiplier vector and thus it's required capacitance is zero.

Similarly to the capacitor charge multiplier vectors, there are transistor charge multiplier vectors, which represent the charges flowing through each switch. These vectors are expressed in the same way as the capacitor charge multiplier vectors.

$$a_{r,j} = [q_{SW1,j} \quad q_{SW2,j} \quad \cdots \quad q_{SWN,j}]/q_{out}. \tag{8}$$

When a switch is off, it should have a charge of zero flowing through it and when it is on, it should have some combination of capacitor charges flowing through it. As an be seen in Fig. 3, the charges flowing through each resistor (which represent the switches when they are on) are each $q_{C,fly}$. This means the switch charge multiplier vectors are

$$a_{r,1} = [0.5 \quad 0 \quad 0.5 \quad 0], \; a_{r,2} = [0 \quad 0.5 \quad 0 \quad 0.5]. \tag{9}$$

In this case, the sign of the components is not too important as these values are related to resistive loss and there is no difference to whether the charge is flowing one way or another through the switches.

It is shown by the authors of [16] that this framework of normalized charge multipliers can be used to generate equations for the output impedance of SC converters. The equations derived for the output impedances are shown here.

$$R_{SSL} = \sum_{i \in caps} \frac{a_{c,i}^2}{C_i f_{sw}}, \tag{10}$$

$$R_{FSL} = 2 \sum_{i \in switches} R_{on,i} a_{r,i}^2, \tag{11}$$

$$R_{out} = \sqrt{R_{FSL}^2 + R_{SSL}^2}, \tag{12}$$

where R_{SSL} is the SSL impedance, R_{FSL} is the FSL impedance, $a_{c,i}$ is the charge multiplier of the ith capacitor, C_i is the capacitance of the ith capacitor, f_{sw} is the switching frequency, $R_{on,i}$ is the resistance of the ith switch, $a_{r,i}$ is the normalized charge flowing through the ith switch, and R_{out} is the total output impedance of the converter. Intuitively, these limits are found by finding the ratio of output voltage to output current and taking the limit as the switching frequency approaches 0 for SSL and the limit as the switching frequency approaches infinity for FSL.

With the use of some optimization techniques, an equation for the sizing of capacitors in a SC converter is provided in [8]:

$$C_i = \frac{a_{c,i}}{v_{c,i(rated)}} \frac{2E_{tot}}{\sum_{i \in caps} a_{c,i} v_{c,i(rated)}}, \tag{13}$$

where E_{tot} is the total energy stored in all the capacitors. This is a very interesting result, but it stops just short of being implementable because there are too many unknowns. In particular, how does one find the total energy? Summing all $(1/2)CV^2$ requires that we know all capacitor values and integrating output power over a switching cycle requires we know the switching frequency.

This work investigates these equations more deeply to enable SC design. The derivations of these equations can be seen in [8] but are not required. To build upon this framework a loss model, a volume model, and an expression for output voltage ripple are needed.

A. CAPACITOR SIZING

An equation for the capacitance of the flying capacitors in a switched capacitor converter is shown in Eq. 13. The derivation of this equation provided in [8] assumes that the output capacitor is large such that output voltage ripple is small. However, with both efficiency and volume in mind, the output capacitor volume should be taken into account. In fact, the output capacitance should be determined from the ripple specifications of the system. The capacitor sizing equation eq. 13 only gives a method to select the capacitors based on charge multipliers and total energy E_{tot}. Again, it doesn't not appear that the total energy is well defined. It could be based on output power integrated over a switching cycle, but the switching frequency hasn't yet been determined. It could also be based on the energy stored in all the capacitors, but the capacitances haven't yet been determined.

A simplification can be made by including the output capacitor in the equations and looking at the relative values of the capacitors because the term $2E_{tot}/\sum_{i \in caps} a_{c,i} v_{c,i(rated)}$ in Eq. 13 is constant for all capacitors. The reason this term is constant can be understood by inspecting each term individually. The energy E_{tot} is defined as the total energy of the system and thus should be constant for a given design and operating point. The denominator of this term sums over all capacitors and thus is also constant regardless of which capacitor is being inspected. Rewriting Eq. 13 with this in mind, we get:

$$C_i = \frac{a_{c,i}}{v_{c,i(rated)}} k, \tag{14}$$

Where C_i is the capacitance of a particular capacitor, $a_{c,i}$ is the normalized charge multiplier vector of that capacitor, $v_{c,i(rated)}$ is the nominal voltage of that capacitor, and k is some arbitrary constant for a particular SC topology. This means the relative capacitance of each capacitor is determined by the normalized charge flowing through it and the voltage across it. Once C_{out} is determined by a ripple requirement, the flying capacitors can be determined by a simple scaling of the output capacitance depending on the topology. We've avoided the issue of not knowing what E_{tot} is and can instead find relative capacitances, bringing us closer to sizing capacitances based on voltage ripple.

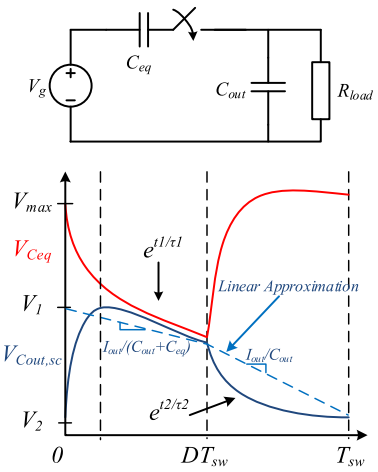

FIGURE 4. Diagram showing the charging mechanism of a step-up SC converter in the slow switching limit. A linear approximation for the output voltage is shown with a dashed line.

We begin the derivation of SC ripple by inspecting an example waveform of the output voltage of a step-up SC converter with a resistive load. This waveform can be seen in Fig. 4. The circuit in this figure lumps all the Cs into an equivalent capacitance C_{eq}. Because all capacitances can be related to the output capacitance, this C_{eq} is just some scaled version of the output capacitance. The maximum voltage $V_{\max}$ shown on the graph is the voltage of the capacitor network about to charge the output capacitor just before it is connected, which is approximately equal to the SC conversion ratio times the input voltage. Based on the discharging of the output capacitor, a relationship can be found between the maximum and minimum values of the output voltage, V_1 and V_2 of Fig. 4.

$$V_2 \approx V_1 e^{\frac{-DT_{sw}}{\tau_1} - \frac{(1-D)T_{sw}}{\tau_2}} \tag{15}$$

where V_1 is the peak output voltage, $V_{\max}$ is the conversion ratio times the input voltage, V_2 is the minimum output voltage, and T_{sw} is the switching period of the SC converter. τ_1 is the time constant when the equivalent capacitance C_{eq} and the output capacitor C_{out} are discharged by the load R_{load} and t_2 is the time constant when C_{out} alone is discharged by R_{load}.

Another equation relating V_1 and V_2 can be derived by inspecting the charge redistribution between the C_{eq} and C_{out} when the capacitor network charges the output capacitor. The final voltage of this charge redistribution is somewhere between the minimum voltage of the output capacitor and the maximum voltage of the capacitor network and is determined by the inverse of the two capacitances. Formally

$$V_1 = \frac{C_{eq}}{C_{out} + C_{eq}} (V_{\max} - V_2) + V_2. \tag{16}$$

Note that for some SC topologies, there can be a $C_{eq,1}$ for the first phase and a $C_{eq,2}$ for the second phase, both connected to the output capacitor. Both equivalent capacitances can be found in relation to the output capacitance. The discharge of the output voltage in second phase becomes related to $C_{out} + C_{eq,2}$.

Now V_1 can be found in terms of $V_{\max} = MV_g$ and the capacitances of the SC.

$$V_1 = MV_g \frac{C_{eq}}{C_{eq} + C_{out} - C_{out} e^{\frac{-DT_{sw}}{\tau_1} - \frac{(1-D)T_{sw})}{\tau_2}}}. \tag{17}$$

Finally, the difference between V_1 and V_2 is the output voltage ripple ΔV_{out}. Taking this difference produces a relation between C_{out} and ΔV_{out}:

$$C_{out} = \frac{\frac{2+\alpha}{1+\alpha}}{2R_{load} f_{sw} ln\left(\frac{\Delta V_{out} - \alpha M V_g}{\Delta V_{out}(1+\alpha) - \alpha M V_g}\right)}, \tag{18}$$

Where α is the ratio of C_{eq}/C_{out} and M is the desired conversion ratio of the SC converter and ΔV_{out} is the output voltage ripple. A linear approximation of the output voltage is shown by the dotted line in Fig. 4. The corresponding linear approximation equation is

$$C_{out} = \frac{I_{out}}{2\Delta V_{out} f_{sw}} \frac{2+\alpha}{1+\alpha}, \tag{19}$$

which is the output voltage when the load is a current source.

This analysis was done with the assumption that the charging time of the output capacitor is much shorter than the discharging time. However, if the charging time is on the order of discharging time, then the ripple is less than what is predicted by these equations. Removing the factor $\frac{2+\alpha}{1+\alpha}$ accounts for this effect because the ripple can be derived from the discharge of the output capacitor.

This shows that ripple is determined by capacitance and switching frequency. What we also know is that the output impedance (specifically the SSL factor) is also related to capacitance and switching frequency. By finding this connection between output voltage, switching frequency and capacitance, we see that there is a connection between output impedance and ripple specifications. This means that output voltage ripple effects the conduction losses of a SC converter and thus C and frequency are directly linked for a design with a given efficiency.

B. SWITCH ON RESISTANCE

As mentioned in [6] and [14], optimal efficiency and volume of an SC converter is achieved at the knee point between FSL and SSL. Looking at Fig. 2, we can image that this means we've selected the switching frequency (vertical line) to intersect the FSL and SSL asymptotes at a single point. This means for a given selection of any two of capacitance, switching frequency and switch on-resistance, the other is determined because all three of these lines intersect. Intuitively, the knee-point makes sense as an ideal operating point. If the converter operates deep in SSL, increasing the on-resistances of the switches has little effect on increasing the output impedance. Increasing the on-resistances means the switches can be smaller and thus the overall size can be smaller for nearly the same efficiency, giving an objectively better converter. Conversely, if the converter operates deep in FSL, decreasing the capacitance has little effect on increasing the output impedance because we are far from the knee-point. Decreasing capacitance then allows the capacitor volume to decrease, resulting in a smaller converter with similar efficiency giving an objectively better converter again. Practically, this means the resistances of the switches in an SC converter are determined once both C_{out} and f_{sw} are selected such that the converter operates at or near the knee point between FSL and SSL.

A simple equation for on resistance can be determined by looking at the individual charging loops within the SC converter. Multiplying the equivalent resistance and capacitance of the loops together yields an *RC* time constant. The designer has the choice of how many time constants should occur in each charging/discharging phase.

$$R_{loop} = \frac{T_{sw}}{2nC_{loop}} \tag{20}$$

Some SCs may have switches which are part of multiple loops. The on resistance of such a switch needs to operate for the loop with the largest equivalent series capacitance. Use the lowest resistance of the possible choices and substitute into subsequent loop equations.

This formulation of switch on-resistance allows us to recast a three variable problem into a two variable problem. Now all that is needed is to solve for C_{out} and f_{sw}. One equation to solve these two variables is provided in the capacitor sizing section and the other will be derived from losses in the next section.

C. LOSSES IN SWITCHED CAPACITOR CONVERTERS

SC converters have an inherent trade-off between efficiency and size. A siginificant portion of loss in an SC converter comes from its output impedance [6], [8], [14] which takes the form shown in eq. 12.

One factor the output impedance model does not take into account is switching loss, which can be significant when a large number of switches are used. Although there is no continuous current flowing in SC converters, the switch output capacitance does still cause switching loss. This means increasing switching frequency to reduce capacitor size runs into the issue of eventually requiring larger capacitors to reduce the output impedance to make up for the loss caused by the increased switching frequency. A simple model of the switching loss is just related to the output capacitance of the switches, the switching frequency and the voltage across the switch at the time of turn on.

$$P_{sw} = f_{sw} \sum_{i \in switches} C_{oss,i} V_{sw,i}^2, \tag{21}$$

where $C_{oss,i}$ is the output capacitance of ith switch and $V_{sw,i}$ is the voltage across the ith switch when it is off. This model can be adjusted to include the input capacitance and gate drive voltage. Here we assume that the output capacitance of the switches are charged capacitively and therefore they lose one half of the energy when charged and the other half is discharged.

The conduction loss is the square of the output current multiplied by the output impedance R_{out} from eq. 12

$$P_{conduction} = I_{out}^2 \sqrt{\left(\sum_{i\in caps} \frac{a_{c,i}^2}{C_i f_{sw}}\right)^2 + \left(2\sum_{i\in switches} R_{on,i} a_{r,i}^2\right)^2} \tag{22}$$

Here R_{out} is shown here explicitly as a function of the capacitances, switch on-resistances and switching frequency of the SC converter. These two equations provide a simplified loss model of SC converters which can be used to design a converter based on efficiency requirements.

D. SELECTING SWITCHING FREQUENCY

Now that equations for the resistances and capacitances of SC converters have been developed and loss models have been derived, selecting the switching frequency of the converter must be done. As will be explained later, multi-objective optimization must be done followed by selection of a design from a set of Pareto optimal designs. If there is a desired efficiency or volume, parameter selection can be done by hand based on the set of equations provided above.

The charge multiplier vectors, the relation between the flying capacitors and the output capacitance, the FOM for a certain set of switches to be used, the desired output voltage ripple, the maximum output current of the converter and the input voltage of the converter are required before the design algorithm can be performed.

By expanding the losses above, we can find a relation between f_{sw} and C_{out}. First we look at conduction loss, which is seen in eq. 22. From Eqs. 12 and 20, we can see that each R_i in R_{FSL} is actually related to f_{sw} and C_{out}. Replacing R_is with the expressions derived from eq. 20, C_{out} and f_{sw} can be factored out of the output impedance. This gives

$$P_{conduction} = I_{out}^2 \frac{1}{f_{sw} C_{out}} \times \sqrt{\left(\sum_{i\in caps} j_i a_{c,i}^2\right)^2 + \left(\left(2\sum_{i\in switches} \frac{r_i a_{r,i}^2}{2n}\right)^2\right)} \tag{23}$$

where n is the number of charging/discharging time constants per half switching cycle, j_i represents the relative capacitance of the ith capacitor to output capacitor and r_i is the factor which relates each switch on-resistance to C_{out} and f_{sw}. The square root term can be lumped into a constant, k_{cond} because it only varies with SC topology and not with C and f_{sw}. This gives

$$P_{conduction} = I_{out}^2 \frac{k_{cond}}{f_{sw} C_{out}}. \tag{24}$$

where k_{cond} is a constant related to charge multipliers and relative capacitances of the SC converter. For the switching loss given in Eq. 21, C_{oss} is inversely proportional to R_{on} to the first order. Typically there are nonlinearities in C_{oss} due to blocking voltage, amongst other variables. Here we approximate

$$C_{oss} = \frac{k_{C,oss}}{R_{on}}, \tag{25}$$

where $k_{C,oss}$ is a constant that relates the on-resistance of the switch to its output capacitance. Each R_{on} is itself inversely proportional to C_{out} and f_{sw} as in eq. 20. Subbing these expressions for C_{oss} and R_{on} into $P_{switching}$ gives

$$P_{switching} = f_{sw} k_{C,oss} \sum_{i\in switches} f_{sw} C_{out} \frac{2nV_{sw,i}^2}{r_i}, \tag{26}$$

where again, r_i relates each switch on-resistance to C_{out} amd f_{sw}. Again, this can be simplified as the switch voltages and r_is are only topology dependent. Factoring the above expression and lumping terms static with topology into a single term, $k_{switching}$ gives

$$P_{switching} = k_{switching} V_g^2 f_{sw}^2 C_{out}, \tag{27}$$

Here we have absorbed the constant $k_{C,oss}$ into the $k_{switching}$ constant. It is interesting to see here that the switching loss appears related to the square of the switching frequency. In the end, if one had chosen all components and began varying f_{sw}, there would only be a linear increase in switching loss, not quadratic. This square factor arises because C_{out}, f_{sw}, and R_{on} are all related. Switching loss is proportional to switching frequency and the size of the switch. The size of the switch is related to the on-resistance, but we constrain the design such that the on resistance is related to the switching frequency. V_g appears here because all the switch blocking voltages can be related back to the input voltage. $k_{switching}$ accounts for the scaling factors after the switching losses of all the switches are summed together.

As shown in Section II-A, there is another relation between C_{out} and f_{sw} which is the output voltage ripple from Eqs. 18 or 19. These relate the product of C_{out} and f_{sw} to the output voltage ripple. This relation can be substituted into the loss equation just derived to eliminate the dependence on two variables. For convenience, the product of C_{out} and f_{sw} are equation to some function of ΔV_{out} at a specific load current,

$$C_{out} f_{sw} = f(\Delta V_{out}). \tag{28}$$

Substituting this function into the total loss equation gives

$$P_{loss,total} = I_{out}^2 \frac{k_{cond}}{f(\Delta V_{out})} + k_{switching} V_g^2 f_{sw} f(\Delta V_{out}). \tag{29}$$

Now $P_{loss,total}$ depends only on f_{sw}. Solving for f_{sw} gives

$$f_{sw} = \frac{P_{loss,total} - I_{out}^2 \frac{k_{cond}}{f(\Delta V_{out})}}{k_{switching} V_g^2 f(\Delta V_{out})}, \tag{30}$$

or,

$$f_{sw} = \frac{P_{out}\left(\frac{1}{\eta} - 1\right) - I_{out}^2 \frac{k_{cond}}{f(\Delta V_{out})}}{k_{switching} V_g^2 f(\Delta V_{out})}, \tag{31}$$

Where η is the desired power processing efficiency. Thus, for a desired loss (or efficiency) and a desired output voltage ripple, the switching frequency, output capacitance, flying capacitances and switch on resistances can all be calculated directly. Clearly there is a limitation here, namely that frequency cannot be negative. What this limitation is saying is there is a lower limit on the total loss achievable: the "conduction" loss of the SC converter. Looking at Eq. 30 we can see that this "conduction" loss is related to our design parameter ΔV_{out}, so for some desired loss, there is a limitation on how much ripple is possible. A more detailed loss model could be developed and correlation between design and experiment would improve. The loss models developed here demonstrate a particular design method and highlight the correlation between relevant design parameters. More complex loss models would only serve to make the understanding of the trade-offs in SC design more difficult. Improving the loss model for more specific implementations (i.e. fully integrated) presents opportunity for future work.

III. A 1:5 SC CONVERTER DESIGN EXAMPLE

A 1:5 step-up Fibonacci SC converter is investigated here as an example of the design algorithm. For simplicity, a current source as a load will be assumed. A diagram of this converter including switching states can be seen in Fig. 5.

The first step is to find the charge multiplier vectors and voltages of the capacitors (as in [8]). In state 2 we can see $C_{fly,3}$ is charged to V_g. In state 1, $C_f, 2$ is charged to $V_g + V_{Cf,3} = 2V_g$. In state 2, $C_{fly,1}$ is charged to $V_{Cfly,3} + V_{Cfly,2} = 3V_g$. Finally, in state 1, C_{out} is charged to $V_{Cfly,2} + V_{Cfly,1} = 5V_g$. To find the charge multiplier vectors, we can write KCL equations in both states of the switching cycle for all nodes. Assuming the converter operates at a 50% duty ratio, then the load will draw equal current in both states, $\frac{q_{out}}{2}$. The charge multiplier vectors are

$$a_{c,1} = [-0.5 \quad 1 \quad -1 \quad 2 \quad 3],$$
$$a_{c,2} = [0.5 \quad -1 \quad 1 \quad -2 \quad 2]$$

The charge multiplier vector for the switches is

$$a_r = [3 \quad 2 \quad 2 \quad 2 \quad 1 \quad 1 \quad 1 \quad 1 \quad 1 \quad 1]$$

These vectors make some intuitive sense. The conversion ratio is 1:5, and the input charge (or current) is 5 times the output charge (or current). Using these charge multiplier vectors, the relative capacitances of the flying capacitors can be found.

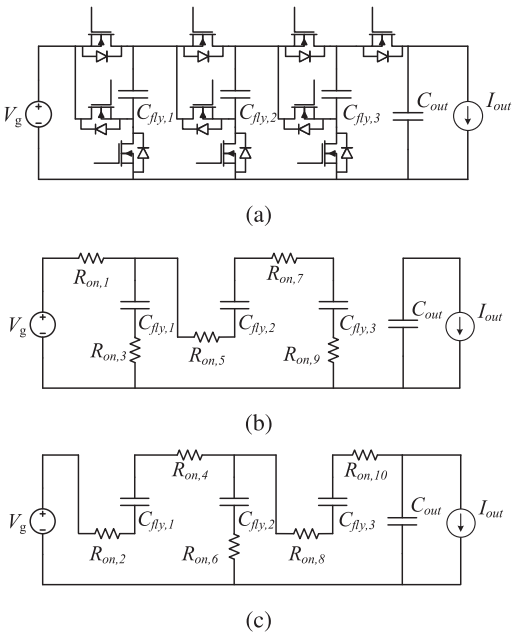

FIGURE 5. Circuit diagrams of the 1:5 Fibonacci SC converter. The complete circuit is shown in (a), the equivalent circuit in first switching state in (b) and the equivalent circuit in the second switching state in (c).

$$C_{fly,3} = \frac{10}{3} C_{out}, \quad C_{fly,2} = 5C_{out}, \quad C_{fly,1} = 20C_{out}.$$

Now α can be found by expressing the equivalent capacitance connected to C_{out} in terms of C_{out}.

$$C_{eq} = C_{fly,3} || (C_{fly,1} + C_{fly,2}),$$
$$\rightarrow C_{eq} = \frac{50}{17} C_{out} \rightarrow \alpha = \frac{50}{17}$$

Using equation eq. 19 the ripple of this capacitor for a current load is

$$\Delta V_{out} = \frac{42}{67} \frac{I_{out}}{f_{sw} C_{out}}$$

rearranging

$$C_{out} f_{sw} = \frac{42}{67} \frac{I_{out}}{\Delta V_{out}}, \tag{32}$$

Next, the on-resistances must be found. From Fig. 5(b) and 5(c), there are four loops. The resulting r vector, the vector used in eq. 23 which relates switch on-resistance to $\frac{1}{f_{sw} C_{out}}$ is

$$r_{1:5} = \left[\frac{1}{40} \quad \frac{1}{12} \quad \frac{1}{40} \quad \frac{1}{12} \quad \frac{7}{40} \quad \frac{1}{12} \quad \frac{7}{40} \quad \frac{17}{24} \quad \frac{7}{40} \quad \frac{17}{24}\right]$$

R_{on}s are then designed using $n = 2$, two times constants per half switching cycle.

Now k_{cond} and $k_{switching}$ must be found. Assuming there are two time constants in one half-switching cycle of the SC, k_{cond}

can be found by factoring out $\frac{1}{C_{out} f_{sw}}$ from R_{out}. This gives

$$k_{cond} = \sqrt{\left(\frac{19}{20}\right)^2 + \left(\frac{181}{120}\right)^2} \approxeq 1.78257$$

Relating C_{oss} to the R_{on} of the switch using eq. 25 and substituting in the expression for R_{on}, $k_{switching}$ can be found

$$k_{switching} = \frac{127328}{119} k_{C,oss}.$$

Substituting this all back into eq. 30, we get

$$f_{sw} = \frac{1139}{763968} \Delta V_{out} \frac{P_{loss,total} - 2.84362 I_{out} \Delta V_{out}}{k_{C,oss} V_g^2 I_{out}}$$

The constraint on ΔV_{out} can be clearly seen

$$\Delta V_{out} < \frac{P_{loss,total}}{2.84362 I_{out}}. \tag{33}$$

In other words, there is a constraint on the minimum SC loss achievable due to the non-adiabatic charging nature of the system. C_{out} can be solved using eq. 32.

A more complex model involving more losses can be developed. This process provides a hand calculation algorithm for SC design.

One piece not directly covered in the above algorithm is determining the coefficient k_{Coss}, which is used here as a figure-of-merit for a given MOSFET. For integrated designs, this relation could be extracted from the process. For a discrete implementation, determining this factor across different manufacturers is effectively impossible. Once the equations are determined, substituting in different k_{Coss} values can be done until solutions which include readily available devices are produced.

IV. VOLUME AND EFFICIENCY OPTIMIZATION OF SC CONVERTERS

When optimizing a converter in general, often we are concerned with multiple variables at once (e.g. power loss, volume of the final solution, or cost), and may have some constraints for a particular application. If we want to make the "best" SC converter, we then have to take these variables into account. Typically, designing converters for maximum power density is desirable. However, as will be explained later, power density is not necessarily a convex function, which prevents the use of convex optimization tools. Instead, we try to minimize the volume of a converter, which increases power density for a fixed output power. The loss model to be used has been shown in the previous section and now a volume model for capacitors and switches is needed to perform a multi-objective optimization. Assuming that the volume of capacitors is proportional to the energy storage [19], the total passive volume of the capacitors in an SC converter is simply

$$Vol_{caps} = \frac{1}{2} k_{caps} \sum_{i \in capacitors} C_i V_i^2, \tag{34}$$

Where C_i is the capacitance of a specific capacitor in the circuit and V_i is the voltage across that capacitor and k_{caps} relates the energy storage to energy density. In real applications, capacitor sizes are discretized and fit into specific package sizes, meaning this model is a continuous approximation of an inherently discontinuous function. Furthermore, this model does not factor in the cost of the capacitors. If volume is of major concern, a more expensive material with higher permittivity could be used to decrease size. This model assumes the same technology for all capacitors in the converter.

Switch size presents a different issue and depends on the type of implementation. For discrete implementations, MOSFETs also fall into discrete package sizes, making volume a discontinuous function. For integration, we are usually interested in silicon area and the area of the switch is usually described as being proportional to the square of the blocking voltage and inversely proportional to the on resistance of the switch [21]. To be able to sum the volume of capacitors and areas of switches together we assume that the height is constant, implying area and volume are proportional.

$$Vol_{sw} = k_{MOSFET} \sum_{i \in switches} \frac{V_{DS,i}^2}{R_{on,i}}, \tag{35}$$

where k_{MOSFET} is a constant which relates the sum to volume in mm^3, $V_{DS,i}$ is the blocking voltage of ith MOSFET and $R_{on,i}$ is the on-resistance of the ith switch.

Using equations 21, 22, 18, 34, and 35, optimal SC converters can be designed using the optimization technique applied in [20], where loss and volume equations for a buck converter, a 3-level Flying Capacitor Multilevel converter and a 4-level Flying Capacitor Multilevel converter are expressed in posynomial and monomial form. These forms, which are polynomials with strictly positive coefficients, allow the optimization problem of loss and volume to be cast as a geometric program, which has been shown to be convex [22]. Convexity guarantees an optimal solution if it exists.

At its core, the method of convex optimization described here is the same as [20]. Multi-objective convex optimization itself is not novel. The main result of [20] is the application multi-objective optimization to multi-level dc-dc converters as it turns out such problems can be casts as geometric programs. That paper goes further to include a much more detailed modelling of inductors (which involves extracting data from magnetics manufacturers and fitting convex curves to that data), a comparison between continuous (i.e. integrated) and discrete implementations of MOSFETs, and the inclusion of temperature increase as a constraint (whose implementation involved some novelty to achieve convergence). The use of convex optimization presented in this paper is much simpler. For one, there are no inductors and two temperature variation is not included. Finally, all variables are continuous. The loss and volume modeling of SC converters provided here results in equations which are all posynomial. This is an important because it allows SC optimization to be cast as a geometric program, allowing convex optimization tools be used.

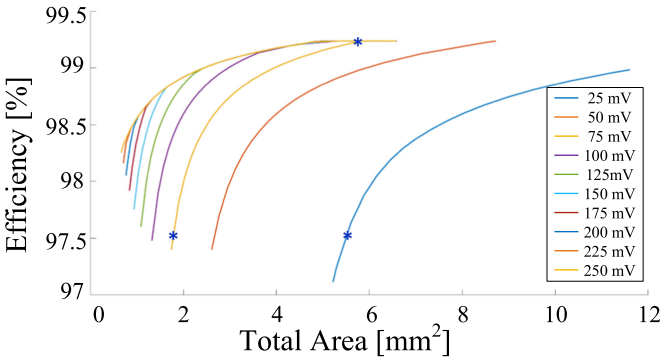

FIGURE 6. Families of Pareto optimal solutions over efficiency and area for different output voltage ripple constraints of a 1:2 SC converter.

TABLE 1. 1:5 SC Converter Parameters

Parameter	Optimized Value(s)	Practical Values(s)
V_{in}	$3.7\ V$	$3.7\ V$
I_{out}	$200\ mA$	$200\ mA$
ΔV_{out}	$400\ mV$	$470\ mV$ measured, $479\ mV$ recalculated
$P_{loss,desired}$	$250\ mW$	$290\ mW$
$k_{c,oss}$	$1000\ m\Omega pF$	N/A
f_{sw}	$1.175\ MHz$	$1.171\ MHz$
C_{out}	$0.223\ \mu F$	$0.2\ \mu F$
$C_{fly,1}$	$0.742\ \mu F$	$0.82\ \mu F$
$C_{fly,2}$	$1.11\ \mu F$	$1.2\ \mu F$
$C_{fly,3}$	$4.45\ \mu F$	$4.7\ \mu F$
$SW_{1,3}$	$23.898\ m\Omega, 209\ pF$	AO3404A $28\ m\Omega,\ 120\ pF$
$SW_{2,4,6}$	$79.66\ m\Omega, 62.8\ pF$	DMN3110 $50\ m\Omega, 70\ pF$
$SW_{5,7,9}$	$167.285\ m\Omega, 29.9\ pF$	SSM3K339R $140\ m\Omega, 30\ pF$
$SW_{8,10}$	$677.107\ m\Omega, 7.38\ pF$	SSM3K339R $140\ m\Omega, 30\ pF$
Gate Driver		LTC4440 (HS), MAX15013 (Half Bridge)

As mentioned previously, power density is an important factor. For low power, integrated applications, volume of the converter is typically determined by total PCB area and the maximum allowed height of the converter. For a given output power, the power density is simply inversely proportional to the volume. The volume models used here are posynomials, meaning the power density function would be the inverse of a posynomial which is strictly not a posynomial function. This means if we wish to use convex optimzation tools, we are forced to minimise volume instead of maximize power density in the optimization.

The specific optimization of an SC converter takes the form

$$\begin{aligned} \min_{f_{sw},C_{sc}} \quad & \gamma \frac{P_{loss,sc}}{P_{loss,\max}} + (1-\gamma)\frac{Vol_{sc}}{Vol_{\max}} \\ \text{subject to} \quad & f_{\min} \le f_{sw} \le f_{\max} \\ & C_{\min} \le C_{sc} \le C_{\max} \\ & \Delta V_{sc} \le \Delta V_{sc,\max} \end{aligned} \tag{36}$$

Loss and volume are normalized because the absolute values of loss and area are very different. For some applications total loss may be on the order of watts and total area may be on the order of square mm and either loss or area would dominate the optimization regardless of the scaling factor γ. The factor γ is swept from 0 to 1 to vary the weight between loss and area. A γ of 1 optimizes only for efficiency and a γ of 0 optimizes only for area.

A 1:2 doubler SC was optimized over loss and volume while varying the constraint on output voltage ripple. The result of these optimizations can be seen in Fig. 6. As ΔV_{out} relaxes and more ripple on the output voltage is allowed, the family of solutions become better in the sense that they have higher efficiency and smaller volume. As ΔV_{out} relaxes further, some of the Pareto fronts begin to converge. Pareto fronts that lie on top of one another have identical switching frequency, capacitor size and switch on-resistance. Conventional intuition of SC converters indicates that lower ripple is better. Why this is not the case in this situation is due to the design methodology itself. By constraining the on-resistance of the switches to be related to the switching frequency and the capacitors, we effectively determine the size of switches and thus the switching loss through ΔV_{out}. Looking at eq. 29 and subbing in eq. 19 for $f(\Delta V_{out})$, we can see how $P_{loss,total}$ depends on ΔV_{out}.

$$P_{loss,total} = k'_{conduction}\Delta V_{out} I_{out}^2 + \frac{k'_{switching} f_{sw}}{\Delta V_{out}}, \tag{37}$$

where the conduction and switching loss equations have been simplified with constants $k'_{conduction}$ and $k'_{switching}$ respectively, to show the relationship more clearly. This linear plus inverse function tends to infinity as output voltage ripple tends to either infinity or zero with a minimum in between these two extremes.

While constraining the output voltage ripple may be a system requirement, this constraint may prevent the optimizer from finding solutions that are both smaller and more efficient. In some cases, relaxing the ripple constraint maybe yield better results as eq. 37 has a minimum with respect to ΔV_{out}.

V. EXPERIMENTAL RESULTS

Two experimental setups were prepared to show the effectiveness of the proposed method. A 1:5 Fibonacci SC converter was designed using the analysis in Section III and several 1:2 doubler SCs were implemented using the convex optimization technique described in Section IV. While power density is important, these prototypes were implemented in an effort to demonstrate the design method.

A. 1:5 FIBONACCI SC EXPERIMENTAL PROTOTYPE

Following the design outlined in the Section III, an experimental prototype of a 1:5 Fibonacci converter was designed. The input voltage is 3.7 V, output current 200 mA, a desired output voltage ripple of 400 mV and a desired total loss of 250 mW.

The input and output specifications, desired components and selected components are provided in Table 1.

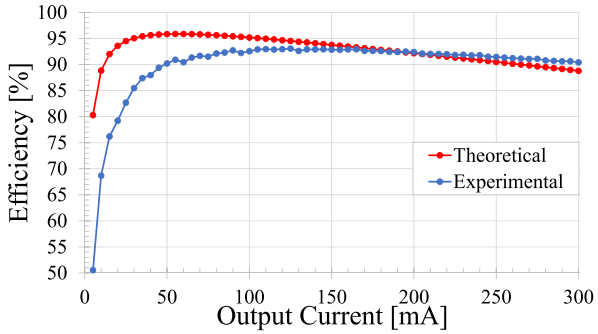

FIGURE 7. Power processing efficiency of the 1:5 SC converter versus load current.

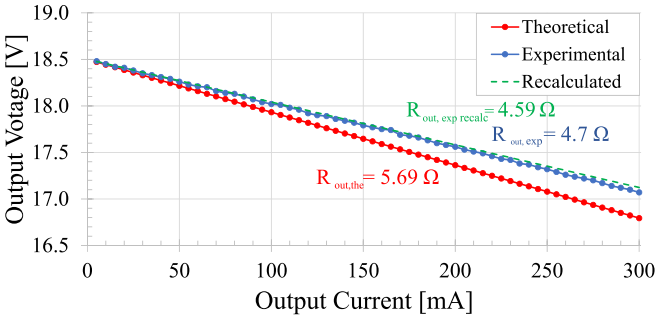

FIGURE 8. Output voltage of the 1:5 SC converter versus load current.

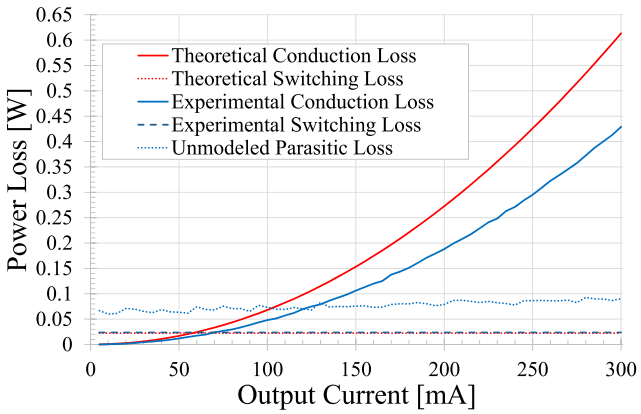

FIGURE 9. Loss breakdown of the 1:5 SC converter versus load current.

The limited selection of practical components makes matching the values suggested by the algorithm difficult. Components were selected as close as possible.

The 1:5 Fibonacci converter was tested from 5−300 mA at 1.171 MHz and compared against the theoretical results of the algorithm. The converter efficiency can be seen in Fig. 7, the output voltage can be seen in Fig. 8 and the loss breakdown can be seen in Fig. 9. The experimental efficiency is lower than the theoretical efficiency at light load. This is mostly due to unmodelled or parasitic capacitance on the PCB along with the differences between theoretical and practical

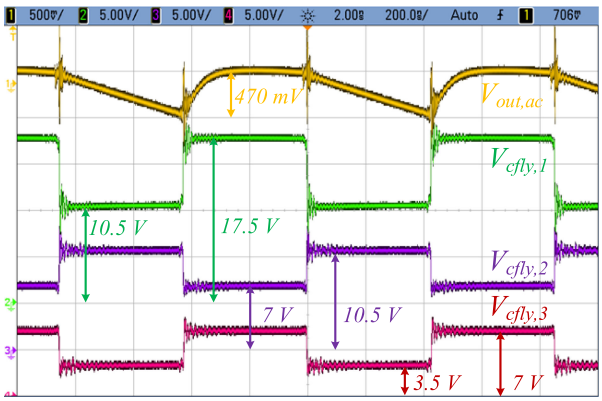

FIGURE 10. Experimental waveforms of the 1:5 Fibonacci SC converter. Ch.1 (yellow) (500 mV/div): AC coupled Output voltage. Ch.2 (green) (5 V/div): Top node of $V_{cfly,1}$. Ch.3 (purple) (5 V/div): Top node of $V_{cfly,2}$. Ch.3 (red) (5 V/div): Top node of $V_{cfly,3}$. Timescale is 200 ns/div and the output current is 200 mA.

component selection. The output voltage indicates that the experimental output impedance of the SC converter is lower than the output impedance predicted by the model. Again, the component selection has an impact on this. Recalculating the output impedance using the practical values matches well with the slope of the output voltage. The output voltage ripple is approximately 70 mV higher than expected. Recalculating the expected output voltage ripple given the selected components using the linear equation gives 479 mV output voltage ripple. The loss breakdown is intended to align with the loss models developed previously. Losses were broken down by observing the drop in output voltage over load current to derive the output impedance. Conduction loss was calculated by multiplying the square of the load current by the output impedance. Experimental switching loss was calculated from the output capacitance of the MOSFETs used in the practical setup. The remaining loss is the unmodeled parasitic loss in the practical setup. Clearly this is not perfectly accurate, but it does illustrate that these remaining losses are roughly flat with respect to load current, which implies there is extra capacitance in the practical implementation. The recalculated switching loss matches closely with the intended design despite the differences in both switching frequency and individual output capacitances.

Experimental waveforms of the 1:5 Fibonacci SC converter can be seen in Fig. 10. The output voltage ripple matches well with the output voltage ripple at the designed current of 200 mA when recalculated with the practical values.

B. 1:2 OPTIMIZATION DESIGN

An experiment was set up to verify the effect of output voltage ripple on efficiency and area as well as demonstrate the effectiveness of the optimization technique. A 1:2 SC converter was designed using the optimization technique described in Section IV with a variable output voltage ripple constraint. The converter was optimized for an output current of 50 mA

TABLE 2. 1:2 SC Converter Parameters

Parameter	Optimized Value(s)	Practical Values(s)
	75 mV Ripple: Small Area Design	
f_{sw}	2.185 MHz	2.2 MHz
C_{out}	415 nF	470 nF
C_{fly}	1.6 μF	1.2 μF
$SW_{1,3}$	70.3 $m\Omega$, 91 pF	Si3442BDV 50 $m\Omega$, 100 pF
$SW_{2,4}$	187.5 $m\Omega$, 34.1 pF	QS5U34 130 $m\Omega$, 25 pF
	25 mV Ripple: Comparison Design	
f_{sw}	1.875 MHz	1.875 MHz
C_{out}	1.4 μF	1.2 μF
C_{fly}	5.6 μF	5.6 μF
$SW_{1,3}$	23.4 $m\Omega$, 273.1 pF	BSL202SN 22 $m\Omega$, 400 pF
$SW_{2,4}$	62.5 $m\Omega$, 102.4 pF	Si3442BDV 50 $m\Omega$, 100 pF
	75 mV Ripple: High Efficiency Design	
f_{sw}	250 kHz	250 kHz
C_{out}	3.5 μF	3.3 μF
C_{fly}	14.4 μF	14.7 μF
$SW_{1,3}$	70.3 $m\Omega$, 91 pF	Si3442BDV 50 $m\Omega$, 100 pF
$SW_{2,4}$	187.5 $m\Omega$, 34.1 pF	QS5U34 130 $m\Omega$, 25 pF
Gate Driver		LTC4440 (HS), MAX15013 (Half Bridge)

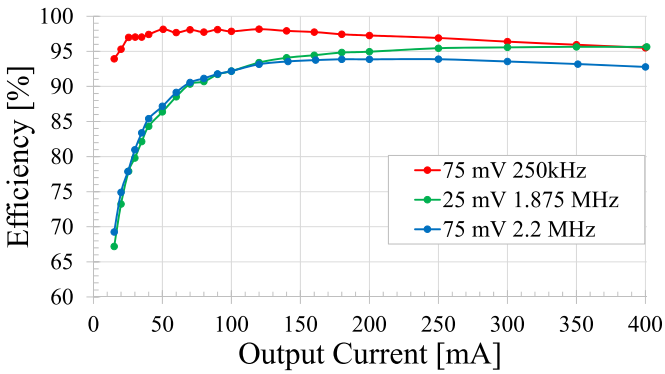

FIGURE 11. Efficiency results for three 1:2 SC converters. The green curve shows the reference 25 mV ripple design, blue curve shows the small 75 mV ripple design and the red shows the high efficiency 75 mV ripple design.

and and input voltage of 3.7 V. A plot of the families of Pareto optimal designs for the output voltage ripple constraint varying from 25 mV to 250 mV can be seen in Fig. 6. The 25 mV design is the reference design and the 75 mV designs were selected to show that a converter with larger output voltage ripple can be made with higher efficiency and similar area or smaller area and similar efficiency. The converter parameters of these designs can be seen in Table 2.

Efficiency results for these converters are shown in Fig. 11. The efficiency results vary significantly from the efficiency predicted by the optimizer. This is due to unaccounted for parasitics in the loss model. The PCB has significant parasitic capacitances at the switch nodes which results in increased losses, especially for the converters operating at a high switching frequency. The high efficiency 75 mV design operates much closer to the expected efficiency because these parasitics have less impact due to the lower switching frequency. Improving the model to include PCB parasitics would result in designs which more closely match the predictions of

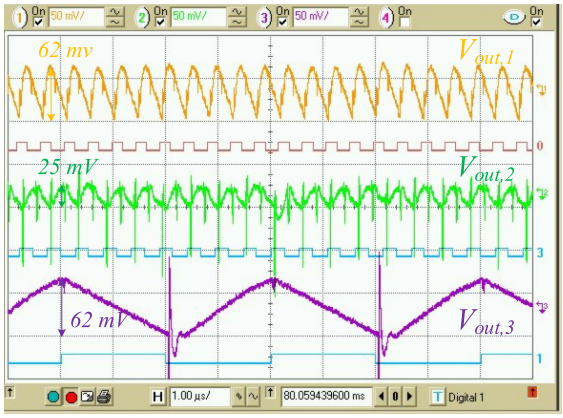

FIGURE 12. Experimental waveforms of the three SC converters. Ch.1 (yellow) (50 mV/div): Output voltage of the small area 75 mV output voltage ripple design. Ch.2 (green) (50 mV/div): Output voltage of the 25 mV output voltage ripple design. Ch.3 (purple) (50 mV/div): Output voltage of the high efficiency 75 mV output voltage ripple design. The digital signal D0 shows the control signal for low volume 75 mV design, D3 shows the control signal for the 25 mV design and D1 shows the control signal for the high efficiency 75 mV design.

the optimizer. The ripples of the 75 mV designs are slightly lower than predicted. For the small area design, the selected components and switching frequency are slightly higher than desired, decreasing the output voltage ripple. For the high efficiency design, the values are relatively close, but the flying capacitance is slightly higher than the optimized value.

These waveforms also exhibit relatively large voltage spikes at the switching transitions. These spikes occur when the flying capacitor is connected to the output capacitor and arise from a combination of the deadtime and parasitic inductance in the practical implementation of the circuit. The high efficiency 75 mV design has larger ringing due to the proportionally larger deadtime for its period. The voltage spikes could be decreased by selecting a more appropriate deadtime between switching states along with optimizing the layout to reduce parasitic inductance. Snubbing the voltage ringing is possible, but would result in efficiency reduction.

These results experimentally verify the prediction that an SC converter with a larger voltage ripple can have higher efficiency than an SC converter with a smaller voltage ripple. Experimental output voltage waveforms of the three SC converters can be seen in Fig. 12.

VI. CONCLUSION

Practical design techniques for SC converters have been shown. Beginning from the work presented in [8], the observation that all capacitances in SC converters can be related to one another through the total energy of the system. This observation allows the designer to relate switching frequency and capacitance to output voltage ripple, which is typically a constraint in conventional SMPS design. This connection had been previously missing and resulted in a circular dependence between capacitance, frequency and energy which had been

solved through brute force. Utilizing the relationship to output voltage ripple, SC design has been explained in depth with equations for finding the pertinent design variables provided.

With this perspective on SC design, some unusual properties of SC converters have been shown. The first is that switching loss appears related to the square of the switching frequency. The second is that the solutions found through convex optimization tend to improve as the constraint on output voltage ripple relaxes. Both these results are not intuitive, but their origin comes from the design process, not the physics of the circuit itself.

A 1:5 Fibonacci SC was implemented to demonstrate the effectiveness of the hand design method. Differences between the calculated and experimental output impedance and output voltage ripple was shown to be due to component selection and parasitics. Three 1:2 SC converters were implemented as discrete prototypes to verify the effect of output voltage ripple on SC performance. Experimental results differed from predicted results due to unaccounted for parasitics in PCB implementation and being unable to select devices specified by the optimizer. The results confirm the prediction of the model, namely that increased output voltage ripple does not necessarily result in reduced efficiency.

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