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Operational Verification of Gate Drive Circuit With Condition Monitoring Function for Gate Oxide Degradation of SiC MOSFETs

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ABSTRACT This paper proposes a gate drive circuit with a condition monitoring function for detecting the gate oxide degradation in silicon carbide (SiC) metal–oxide–semiconductor field-effect transistors (MOSFETs). Trapped charges in the gate oxide can cause fluctuations in the on-resistance and gate threshold voltages. These phenomena affect the long-term reliability of power conversion circuits. The proposed condition monitoring function detects the degradation of the gate oxide by measuring the input capacitance C_{iss} versus the gate–source voltage v_{GS} characteristics (C_{iss}–v_{GS} characteristics) of SiC MOSFETs implemented in power conversion circuits. Experiments on the proposed gate drive circuit were conducted using a 400 W-rated buck converter circuit in which a SiC MOSFET is implemented. The experimental results show that the gate drive circuit is capable of online measurement of C_{iss}–v_{GS} characteristics and gate drive at 20 kHz. The online measurement of the C_{iss}–v_{GS} characteristics corresponds to the offline measurement with a measurement instrument, indicating the effectiveness of the gate drive circuit.

INDEX TERMS Condition monitoring, gate drive circuit, gate oxide, long-term reliability, SiC MOSFET.

I. INTRODUCTION

Silicon carbide (SiC) metal–oxide–semiconductor field-effect transistors (MOSFETs) exhibit excellent performance as power devices due to their higher breakdown voltage compared to that of Si MOSFETs [1], [2], [3], [4], [5]. However, the gate oxide of SiC MOSFETs has been reported to degrade with long-term use [6], [7], [8], [9], [10], [11]. In addition, reports on the causes of power conversion circuit failures indicate that one-third to one-half of the failures are caused by power devices [12], [13]. Therefore, condition monitoring systems have been developed to improve the long-term reliability of power devices [14], [15]. Table 1 summarizes the characteristics of aging precursors of power devices for condition monitoring that have been proposed in previous studies. On-voltage, body diode forward voltage, gate threshold voltage, and switching waveforms (e.g., Miller platform voltage and switching time) have been proposed as aging precursors for in-situ condition monitoring systems [13], [16], [17], [18], [19], [20], [21], [22], [23], [24], [25], [26], [27], [28]. However, these aging precursors are temperature-dependent, and it is difficult to distinguish temperature-induced fluctuations from degradation-induced fluctuations. A temperature-dependent degradation detection method has been proposed that is effective in detecting package degradation by measuring the case temperature of the power device at two points [29], [30]. However, detecting bare die degradation is difficult because the bare die temperature must be accurately estimated. In [31], [32], [33], although gate leakage current has been proposed as an aging precursor, gate oxide degradation does not always cause gate leakage current.

In this paper, a gate drive circuit with a condition monitoring function is proposed to measure the input capacitance C_{iss} versus gate–source voltage v_{GS} characteristics (C_{iss}–v_{GS} characteristics) as an aging precursor, which has almost no temperature dependence. Fluctuations in the C_{iss}–v_{GS} characteristics are caused by trapped charges in the gate oxide and at the oxide–semiconductor interface. The trapped charges also cause fluctuations in the on-resistance and gate

TABLE 1. Features of Aging Precursors of Power Devices for Condition Monitoring

Aging precursors	Targets	Temperature dependence	Other comments	References
On-voltage	Bare die and package	✓	Depending on operating conditions	[16]–[22]
Body diode forward voltage	Bare die and package	✓	–	[23]
Gate threshold voltage	Bare die	✓	–	[24]
Switching waveforms	Bare die and package	✓	Depending on operating conditions	[13], [25]–[28]
Temperature-related	Bare die and package	–	Difficult to estimate die temperature	[29], [30]
Gate leakage current	Bare die	Negligible	Not always fluctuating due to degradation	[31]–[33]
C_{iss}–v_{GS} characteristic	Bare die	Negligible	–	–

threshold voltage [34], [35], [36], [37]. Therefore, the proposed condition monitoring system is effective for improving the long-term reliability of power conversion circuits. This paper is organized as follows. First, the suitability of C_{iss}–v_{GS} characteristics as the aging precursor for condition monitoring of SiC MOSFETs with planar-gate structure is evaluated theoretically and experimentally. Next, the working principle, design method, and operation sequence of the condition monitoring function capable of measuring the C_{iss}–v_{GS} characteristics of SiC MOSFETs implemented in a power conversion circuit are described. Finally, using a 400 W-rated buck converter circuit implementing a SiC MOSFET, the gate drive circuit was demonstrated to drive the gate and to conduct online measurements of the C_{iss}–v_{GS} characteristics. The results of the online measurement of the C_{iss}–v_{GS} characteristics correspond to the results of the offline measurement using a measurement instrument. The results support the hypothesis that fluctuations in C_{iss}–v_{GS} characteristics due to degradation can be measured.

II. GATE OXIDE DEGRADATION AND CHARACTERISTICS FLUCTUATION

A. THEORETICAL CONSIDERATIONS

The gate oxide of MOSFETs degrades over time due to the effects of temperature and electric field strength. As the degradation progresses, the oxide charge Q_{ox} appearing at the gate oxide–semiconductor interface changes [38]. Changes in the oxide charge Q_{ox} cause various fluctuations in the electrical characteristics of the MOSFET. For example, the gate threshold voltage V_{th} is given by the following equation [39]:

$$V_{th} = \frac{\sqrt{4\varepsilon_s kTN_A \ln(N_A/n_i)}}{C_{ox}} + \frac{2kT}{q}\ln\left(\frac{N_A}{n_i}\right) - \frac{Q_{ox}}{C_{ox}}, \quad (1)$$

where ε_s is the dielectric constant of the semiconductor, k is the Boltzmann constant, T is the absolute temperature, N_A is the acceptor density in the P-base region, n_i is the intrinsic carrier density, C_{ox} is the parasitic capacitance due to the gate oxide, and q is the elementary charge. Equation (1) shows that the gate threshold voltage V_{th} fluctuates as the oxide charge Q_{ox} changes. In addition, the on-voltage of the MOSFET also fluctuates due to the fluctuation of the gate threshold voltage V_{th}.

On the contrary, (1) includes the absolute temperature T, which indicates that the gate threshold voltage V_{th} also fluctuates owing to temperature changes. Similarly, the on-voltage have a temperature dependence [38]. Therefore, the gate threshold voltage V_{th} and the on-voltage are affected by both the gate oxide degradation and temperature change. Therefore, it is necessary to distinguish these factors when monitoring the conditions. However, it is difficult to accurately measure the junction temperature of a bare power semiconductor die.

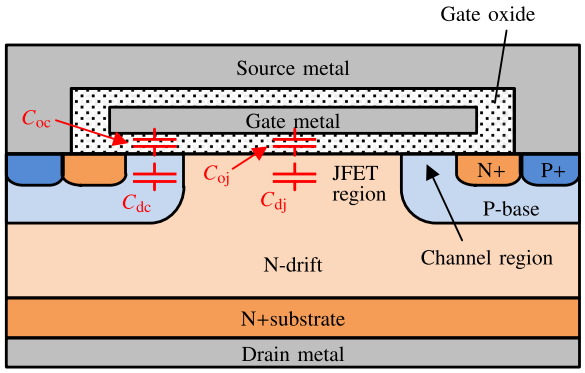

FIGURE 1. Typical MOSFET with planar-gate structure and the parasitic capacitors that compose the input capacitance.

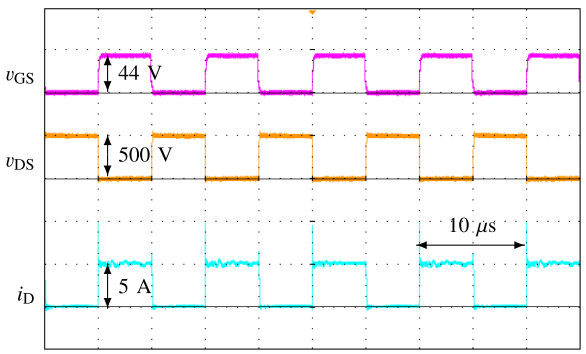

FIGURE 2. Experimental waveforms of accelerated aging test by advanced high-temperature gate bias test.

The C_{iss}–v_{GS} characteristic is another electrical characteristic that fluctuates as the oxide charge Q_{ox} changes. Fig. 1 shows the structure of a typical MOSFET with planar-gate and the parasitic capacitors that compose the input capacitance C_{iss}. The input capacitance C_{iss} is composed of C_{oc} formed by the gate oxide capacitance between the gate electrode and

the P-base region, C_{oj} formed by the gate oxide capacitance between the gate electrode and the JFET region, C_{dc} formed by the depletion layer capacitance in the P-base region, and C_{dj} formed by the depletion layer capacitance in the JFET region [36], [40].

The capacitances C_{oc} and C_{oj} are determined by the gate oxide structure and are found to be independent of voltage and temperature. The depletion layer capacitances C_{dc} and C_{dj} are given by the following equation, assuming that they are the depletion layer capacitance of a MOS capacitor [38]:

$$C_{dc} = C_{dj} = \frac{C_{ox}}{\sqrt{1 + \frac{2C_{ox}^2(v_{GS}+Q_{ox}/C_{ox})}{qN\varepsilon_s}} - 1}. \quad (2)$$

where N is the density of the majority carrier. Equation (2) considers the case of an ideal MOS capacitor where there is no work function difference between the metal and the semiconductor, and all doped impurities are ionized.

Equation (2) shows that when the oxide charge Q_{ox} changes due to gate oxide degradation, the depletion layer capacitances C_{dc} and C_{dj} are affected not only by the applied gate–source voltage v_{GS} but also by the oxide charge Q_{ox}. However, the oxide charge Q_{ox} does not interact electrically with the semiconductor. Therefore, the C_{iss}–v_{GS} characteristic fluctuates parallel to the v_{GS} axis as the oxide charge Q_{ox} changes. However, (2) does not include the absolute temperature T, indicating that there is no temperature dependence. From the above analysis, the C_{iss}–v_{GS} characteristics characteristic fluctuates parallel to the v_{GS} axis due to gate oxide degradation and has no temperature dependence, making it one of the suitable aging precursors for condition monitoring.

B. EXPERIMENTAL VERIFICATION

The C_{iss}–v_{GS} characteristics of a 1.2 kV SiC MOSFET with planar-gate structure (C2M0280120D, CREE) used as the device under test (DUT) in this paper were measured for temperature and degradation-related characteristic fluctuations, respectively. The DUT is a discrete device packaged in TO-247 type. The C_{iss}–v_{GS} characteristics were measured using a high-voltage C–V measurement system (CS-603 A, Iwatsu) under the conditions that the measurement signals were 25 mV and 1 MHz. To clarify the characteristic fluctuations due to temperature, measurements were conducted at ambient temperatures of 25 °C and 150 °C for the DUT.

In this study, the "advanced high-temperature gate bias (HTGB) test" was conducted for the accelerated aging test, thereby enabling the accelerated aging of the gate oxide under the continuous switching condition of the DUT [37], [41], [42]. One of the features of the advanced HTGB test is that it enables accelerated aging under conditions similar to those in the actual use of power devices, compared to the conventional accelerated aging of gate oxide under static conditions. Fig. 2 shows the switching waveforms of the DUT over the course of the advanced HTGB test. Fig. 2 shows that the DUT is switching continuously at 500 V, 5 A, and 100 kHz (duty ratio was 0.5). At this time, a higher voltage (44 V) than the maximum rated voltage (25 V) specified in the datasheet was applied to the gate–source to accelerate the gate oxide aging. The test duration was set to 30 minutes, and a naturally air-cooled heat sink was attached to the DUT to keep the junction temperature from exceeding the maximum rating (150 °C) during the test.

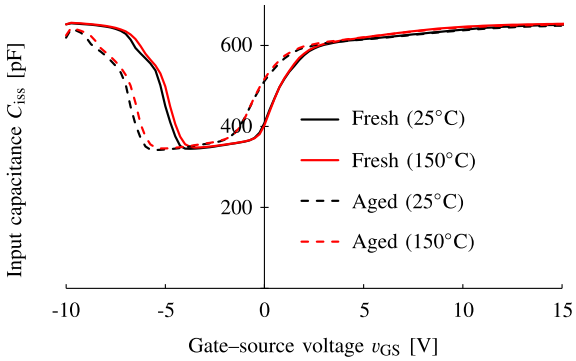

FIGURE 3. Temperature and degradation dependence of C_{iss}–v_{GS} characteristics.

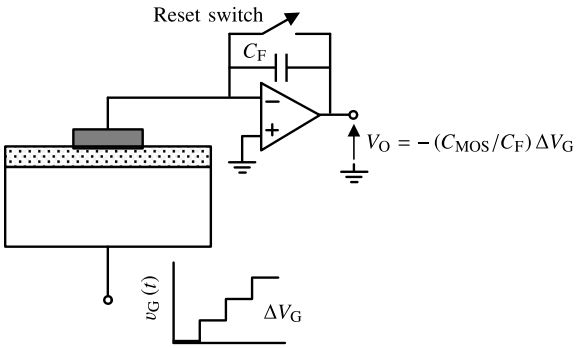

FIGURE 4. Principle of measurement by the quasi-static method (charge–voltage method).

Fig. 3 shows the measurement results of the C_{iss}–v_{GS} characteristic. From Fig. 3, there is a characteristic fluctuation where the C_{iss}–v_{GS} characteristic shifts parallel to the v_{GS} axis due to degradation, while the characteristic fluctuation due to temperature is almost negligible. The measurement results suggest that the experimental results are similar to the theoretical considerations. Furthermore, it has been reported that even when repetitive short-circuit tests and repetitive UIS (Unclamped Inductive Switching) tests are conducted as accelerated aging tests, the C_{iss}–v_{GS} characteristic shifts parallel to the v_{GS} axis due to degradation [36], [43]. Therefore, from both theoretical and experimental points of view, the C_{iss}–v_{GS} characteristic is considered one of the suitable aging precursors for condition monitoring of gate oxide degradation in SiC MOSFETs.

III. GATE DRIVE CIRCUIT WITH CONDITION MONITORING FUNCTION

A. MEASUREMENT METHOD OF C_{iss}–v_{GS} CHARACTERISTICS

Many methods have been established in the field of semiconductor devices to measure the input capacitance C_{iss}–v_{GS} characteristics of MOSFETs. In this study, the quasi-static

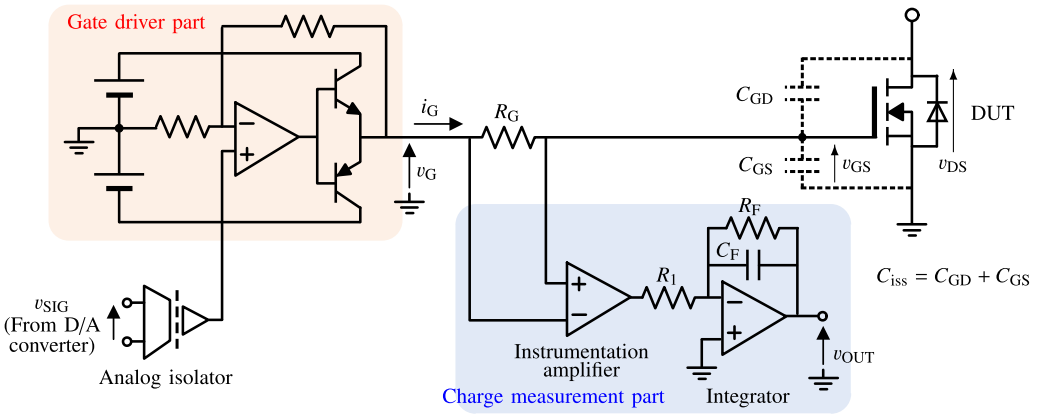

FIGURE 5. Circuit diagram of the proposed gate drive circuit.

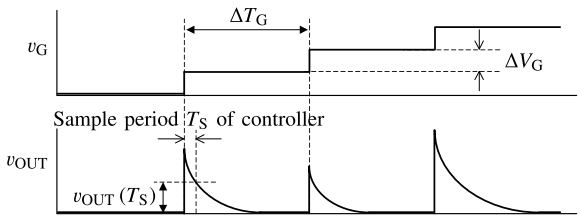

FIGURE 6. Schematic waveforms of the output voltages of the gate driver part and charge measurement part.

method (charge–voltage method) is selected from among these methods, based on the perspective of implementing the measurement circuit in power conversion circuits. Fig. 4 shows the principle of measuring the gate voltage v_G characteristic of MOS capacitors using the quasi-static method (charge–voltage method). In the quasi-static method (charge–voltage method), a stepwise voltage with a voltage width ΔV_G and time width ΔT_G is applied to the gate, and the charge charged to the MOS capacitor ΔQ is measured at each step. The voltage-dependent capacitance C_{MOS} of the MOS capacitor is given by the following equation:

$$C_{MOS} = \frac{\Delta Q}{\Delta V_G}. \tag{3}$$

In the measurement circuit shown in Fig. 4, the output voltage V_O of the operational amplifier (integrator) is given by the following equation [35].

$$V_O = -\frac{C_{MOS}}{C_F}\Delta V_G. \tag{4}$$

B. GATE DRIVE CIRCUIT CONFIGURATION

To measure the input capacitance C_{iss}–v_{GS} characteristics of MOSFETs using the quasi-static method (charge–voltage method), a stepwise voltage source is required to apply the stepwise voltage to the gate–source. In addition, a charge measurement circuit is required to measure the charge charged in the input capacitance C_{iss}. In this study, these functions were added to the gate drive circuit. Fig. 5 shows the circuit diagram of the proposed gate drive circuit. The circuit shown in Fig. 5 can be broadly divided into the "gate driver part" which outputs the stepwise voltage and "charge measurement part" which measures the charge charged in the input capacitance C_{iss} using an integrator. In a conventional gate drive circuit, the output signal from the controller has a binary value of Hi or Lo. In contrast, the gate drive circuit uses a D/A converter to generate an analog output signal v_{SIG} from the controller. The analog output signal v_{SIG} is isolated by an analog isolator and input to the gate driver part. The gate driver part amplifies the input signal using a push–pull circuit in the same way as the conventional gate drive circuit. Therefore, the gate driver part can output not only the square-wave voltage required to drive the gate of the DUT but also the stepwise voltage required to measure the C_{iss}–v_{GS} characteristic as the output voltage v_G.

The charge measurement part consists of an instrumentation amplifier and integrator using an operational amplifier. The charge charged to the input capacitance C_{iss} of the DUT is calculated by measuring the voltage across the gate resistance R_G in the charge measurement part. Where, the gate resistor R_G plays the role of a shunt resistor for measuring the gate current. However, in applications where the gate resistor R_G is not used, a current sensor can be used instead. The charge measurement accuracy depends on the frequency bandwidth of the instrumentation amplifier and integrator. The required frequency bandwidth depends on the time it takes for the charge to follow the DC bias of the stepwise voltage. The following time is expected to be different for each type of device and should be designed to meet the requirements. The output voltage v_{OUT} is sensed by the controller.

Fig. 6 shows a schematic of the output voltage of the gate driver part v_G and charge measurement part v_{OUT}. When the output voltage v_G of the gate driver part changes in the stepwise manner by ΔV_G, the output voltage of the charge measurement part after time T_S seconds $v_{OUT}(T_S)$ is given by the following equation:

$$v_{OUT}(T_S) = \frac{GR_G C_{iss}\Delta V_G}{R_I C_F}\exp\left(-\frac{T_S}{R_F C_F}\right), \tag{5}$$

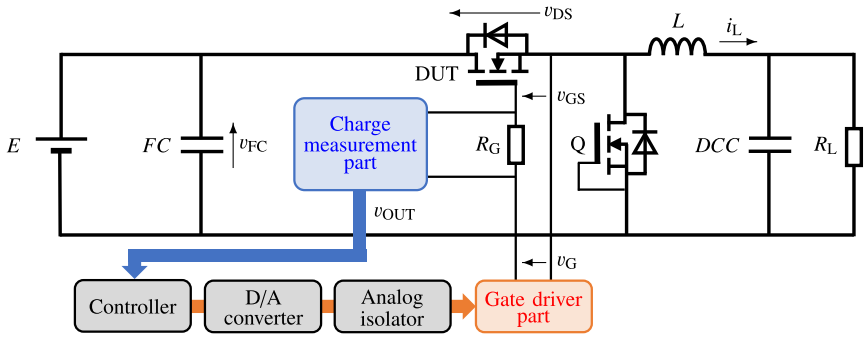

FIGURE 7. Schematic of the proposed condition monitoring system in a conventional buck converter.

where G is the gain of the instrumentation amplifier. However, in deriving (5), the charging time to the input capacitance C_{iss} is ignored, assuming that the time constant $C_{iss}R_G$ is sufficiently small. As shown in (5), when the output voltage v_G of the gate driver part changes in the stepwise manner, the charge measurement part outputs a voltage v_{OUT} proportional to the input capacitance C_{iss}. The output voltage v_{OUT} of the charge measurement part decreases gradually as the charge charged in the integrator capacitor C_F is discharged by a resistor R_F. Considering that the output voltage v_{OUT} of the charge measurement part is detected by the controller, v_{OUT} is detected after one sampling period (e.g., T_S) from the time when the stepwise voltage is changed. If the sampling period T_S is known, the input capacitance C_{iss} can be calculated. If multiple sampling cycles occur before the integrator capacitor C_F is sufficiently discharged, a more accurate measurement can be obtained by averaging the input capacitance C_{iss} calculated for each sampling cycle. Furthermore, by setting the time width ΔT_G of the stepwise voltage to be longer than the time at which the integrator capacitor C_F is sufficiently discharged, the reset switch of the integrator becomes unnecessary.

C. OPERATION SEQUENCE

As an example, the operation sequence when the gate drive circuit is implemented in a buck converter is described here; Fig. 7 shows a schematic of the condition monitoring function implemented in the buck converter circuit. The gate drive circuit monitors the condition of the power device at the time of the filter capacitor voltage $v_{FC} = 0$ V of the buck converter circuit. That is, the gate drive circuit can be used in a circuit configuration that can separate the power conversion circuit from the input voltage E. Such a circuit configuration is also used in the drive systems of electrical vehicles, rolling stock, and so on [44], [45].

Fig. 8 shows the operation sequence, i.e., the buck converter circuit starting up, outputting voltage, and shutting down, in the circuit shown in Fig. 7. As can be seen in Fig. 8, when the buck converter starts up before the input voltage E is applied to the main circuit, the gate drive circuit outputs the stepwise voltage as a "condition monitoring mode" and measures the input capacitance C_{iss}–v_{GS} characteristic. Subsequently, the input voltage E is applied to the main circuit, and the gate

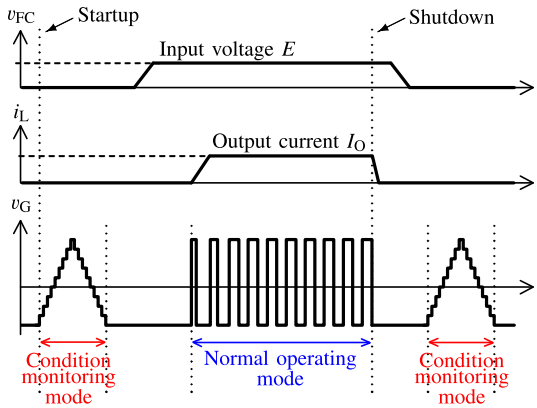

FIGURE 8. Operation sequence of the proposed gate drive circuit.

drive circuit outputs the square wave voltage as a "normal operation mode". In the normal operation mode, the operation is the same as that of a conventional buck converter circuit. When the buck converter shuts down, after the filter capacitor voltage v_{FC} and output capacitance DCC voltage have been discharged to approximately 0 V, the gate drive circuit outputs the stepwise voltage as the "condition monitoring mode" and measures the input capacitance C_{iss}–v_{GS} characteristic again. That is, there are two opportunities to monitor the condition of the DUT, once at starting up and once at shutting down. Of course, it is enough to monitor the condition on only one of the two opportunities.

IV. OPERATIONAL VERIFICATION BY EXPERIMENT

It is verified that the gate drive circuit can monitor the condition of the C_{iss}–v_{GS} characteristics and drive the gate of SiC MOSFETs experimentally. The experimental circuit was the buck converter circuit shown in Fig. 7. Fig. 9 shows the detailed circuit diagram of the gate drive circuit used in the experiment and Fig. 10 shows the experimental circuit. Table 2 lists the circuit parameters. The frequency bandwidths of the operational amplifiers (OPAmp1, 2) and instrumentation amplifier used in the experimental circuit were 18 MHz and 2 to 10 MHz (depending on gain), respectively. The DUT was the 1.2 kV SiC MOSFET (C2M0280120D, CREE). The operating conditions of the buck converter circuit were input

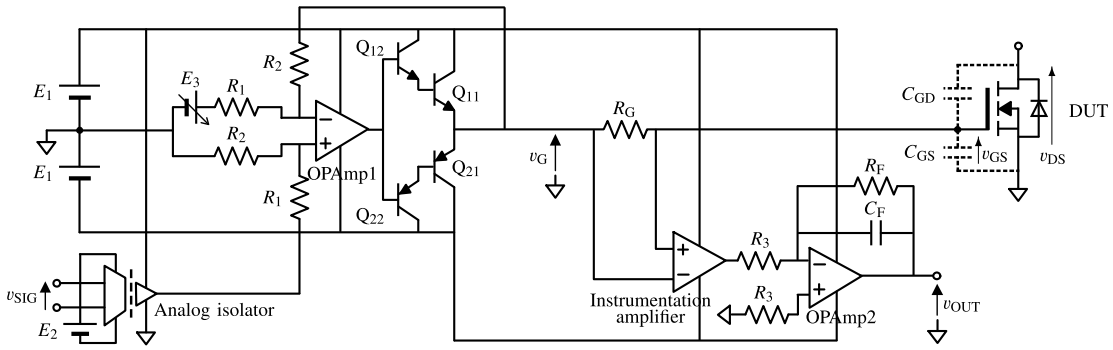

FIGURE 9. Detailed circuit diagram of the proposed gate drive circuit used in the experiment.

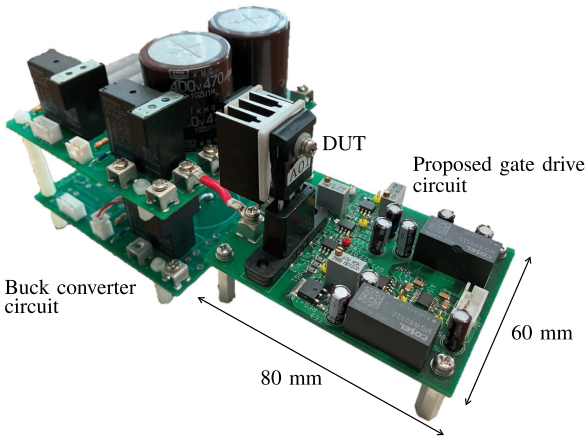

FIGURE 10. Prototype of the proposed gate drive circuit and buck converter circuit.

TABLE 2. Parameters Used in the Experimental Circuit

Parameters	Value
Resistance R_L	100 Ω
Capacitance FC, DCC	470 μF
Inductance L	720 μH
DC voltage E_1	18 V
DC voltage E_2	5 V
DC voltage E_3	0.9 V
Gate resistance R_G	19 Ω
Gain of instrumentation amplifier G	20
Resistance R_1	1 kΩ
Resistance R_2	30 kΩ
Resistance R_3	2 kΩ
Resistance R_F	20 kΩ
Capacitance C_F	1 nF
Analog isolator	ADUM3190B
OPAmp1, 2	ADA4625-1
Instrumentation amplifier	AD8421A

voltage $E = 400$ V and output current $I_O = 2$ A. Table 3 summarizes the specifications of the output voltage v_G of the gate driver part in the condition monitoring mode and normal operating modes. The maximum output voltage of the gate driver was set to 15 V, and the minimum output voltage was set to −15 V. The voltage width ΔV_G of the stepwise voltage in the condition monitoring mode was set to 1 V, and the time width ΔT_G was set to 1 ms. The square wave voltage in the normal operating mode was set to ±15 V and 20 kHz (duty ratio was 0.5).

TABLE 3. Specification of Output Voltage v_G of Gate Driver Part

Parameters	Condition Monitoring and Operating	Normal
Maximum voltage	15 V	15 V
Minimum voltage	−15 V	−15 V
Voltage width ΔV_G	1 V	–
Time width ΔT_G	1 ms	25 μs (20 kHz)

Fig. 11 shows the experimental waveforms of the DUT's drain–source voltage v_{DS}, inductor current i_L, and gate–source voltage v_{GS}. The magnified waveforms of v_{DS}, i_L, and v_{GS} in normal operating mode show that the buck converter is operating according to specification. The waveform of v_{GS} in the condition monitoring mode is shown magnified along with the waveform of the output voltage v_{OUT} of the charge measurement part. In this experiment, the stepwise voltage is output in both rising and falling patterns. In principle, it is possible to measure the C_{iss}–v_{GS} characteristic not only when the stepwise voltage is rising, but also when it is falling. Fig. 12 shows the further magnified waveform of the condition monitoring mode in Fig. 11. The gate driver part outputs the stepwise voltage as specified. The output voltage v_{OUT} of the charge measurement part is output according to the change in the stepwise voltage.

Fig. 13 shows the calculation results of the C_{iss}–v_{GS} characteristics monitored by the gate drive circuit. In Fig. 13, the average of the measured C_{iss}–v_{GS} characteristics as the stepwise voltage rises and falls is shown. Since the purpose of this experiment is to verify the basic operation, the output voltage v_{OUT} of the charge measurement part was measured with an oscilloscope instead of the controller. Based on the measured v_{OUT}, the input capacitance C_{iss} was calculated using (5). Fig. 13 shows that the C_{iss}–v_{GS} characteristic of the condition monitoring (online measurement) corresponds to

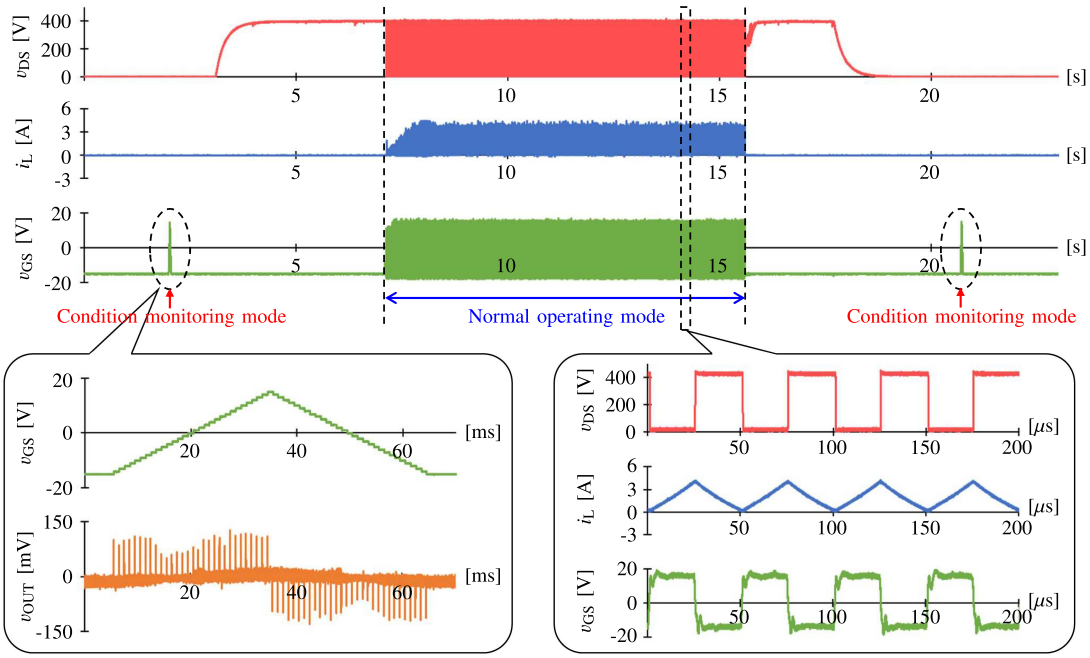

FIGURE 11. Experimental waveforms of the buck converter with the proposed gate drive circuit.

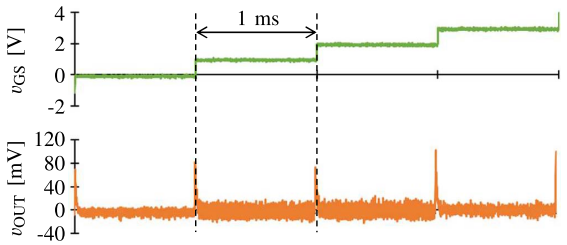

FIGURE 12. Enlargement of experimental waveforms in condition monitoring mode.

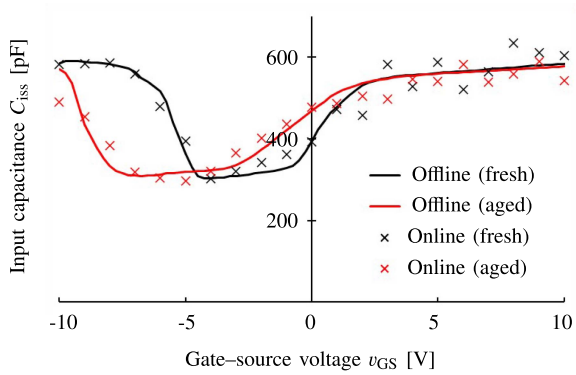

FIGURE 13. Comparison of the C_{iss}–v_{GS} characteristics between the measured values and condition monitoring.

the characteristic measured by the high-voltage C–V measurement system (offline measurement by measuring instrument). Furthermore, the experimental results for a fresh DUT and an aged DUT show that the fluctuations in the C_{iss}–v_{GS} characteristics can be condition monitored. In the region of gate–source voltage $v_{GS} > 0$ V, there are some errors between the condition monitoring and the measurement by the high-voltage C–V measurement system. One possible reason for this is the effect of channel formation. In the measurement by the high-voltage C–V measurement system, the drain–source is shorted, making the C_{iss}–v_{GS} characteristic measurement unaffected by channel formation. On the other hand, in the condition monitoring, the C_{iss}–v_{GS} characteristic measurement is affected by channel formation. However, the purpose of the C_{iss}–v_{GS} characteristics measurement by condition monitoring is not to measure the true value but to detect fluctuations of the C_{iss}–v_{GS} characteristics. Therefore, these errors are not considered to be a major issue. The results of measuring the C_{iss}–v_{GS} characteristics of the DUT before and after aging by condition monitoring and a method to improve the measurement resolution of the gate–source voltage v_{GS} has been described in detail in [46].

The following are possible methods for determining the degradation of SiC MOSFETs from the fluctuation of C_{iss}–v_{GS} characteristics.

- Calculate the fluctuation of the gate threshold voltage from the fluctuation of the C_{iss}–v_{GS} characteristics based on (1) and (2).
- The gate drive circuit can obtain the process of trapping and de-trapping oxide charge because daily condition monitoring can be conducted. Therefore, the degradation caused by repeated trapping and de-trapping can be estimated.

In order to study these methods in detail, it is necessary to analyze by device simulation and data analysis by machine learning. If the gate drive circuit detects degradation of the SiC MOSFET, it may be possible to try fine tune of the gate drive

voltage to offset aging-induced performance degradation [47]. These investigations will be presented in another paper.

V. CONCLUSION

In order to detect the degradation of the gate oxide of SiC MOSFETs, a gate drive circuit with a condition monitoring function has been proposed. In this study, the input capacitance C_{iss}–v_{GS} was used as the aging precursor for condition monitoring. It has been shown both theoretically and experimentally that the C_{iss}–v_{GS} characteristics fluctuate due to gate oxide degradation, and that the C_{iss}–v_{GS} characteristics have no temperature dependence.

The gate drive circuit can measure the C_{iss}–v_{GS} characteristics using the quasi-static method (charge–voltage method). To demonstrate the validity of the gate drive circuit, the operation of the circuit has been verified by experiments using a 1.2 kV SiC MOSFET as a DUT that was implemented in a buck converter circuit. It has been confirmed that the buck converter circuit with the gate drive circuit operates according to the specifications. In addition, the C_{iss}–v_{GS} characteristics measured by the condition monitoring mode correspond to the results measured by the high-voltage C–V measurement system. These results indicate that the gate drive circuit can be used to monitor the degradation of the gate oxide of SiC MOSFETs.

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