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Analytical Benchmarking of Direct Hybrid Switched-Capacitor DC-DC Converters

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ABSTRACT Hybrid switched-capacitor converters (HSCCs) have gained attention due to their promising efficiency and power density compared to traditional inductor- or capacitor-based converters. However, with the recent development of various HSCC topologies, it has become increasingly challenging to choose the most suitable one for a particular application. To address this challenge, this paper proposes a benchmarking framework that enables direct comparison of direct HSCC topologies based on various performance metrics such as passives volume and bandwidth. The proposed approach, which compares all topologies at the same efficiency and output voltage ripple, provides guidelines for topology selection and optimization, ultimately contributing to wider industrial adoption and exploration of new topologies. Downloadable open-access code is also provided to recreate presented results and expand to other topologies not discussed in the paper.

INDEX TERMS DC-DC converter, hybrid converter topology, switching converters.

I. INTRODUCTION

Many non-isolated step-down DC-DC converter applications, such as microprocessor power delivery, USB charging, and automotive systems, require large voltage conversion ratios (VCRs). In such cases, the passive components, typically capacitors and inductors, often dominate the size of the converter. To reduce the volume of these passive components, recent efforts have focused on increasing the switching frequency [1], using resonant topologies [2], introducing inductorless piezoelectric structures [3], [4], [5], using alternative flying components [6], [7], and high density Silicon capacitor components [8], [9]. Among all of these solutions, hybrid switched-capacitor converters (HSCCs) are considered amongst the most promising [10], [11] and have received significant attention over the last decade. Initially, these efforts were driven by a few research groups [12], [13], [14].

The root reasons for HSCC supremacy are mostly due to technological limitations on: i) passive components, specifically the relative low inductor energy density compared to capacitors [8], [15], and ii) on active devices, namely the negative impact of the blocking voltage on switch performance [16], [17], [18], [19]. HSCCs utilize a switched-capacitor network to block a portion of the input voltage across capacitors, and then an inductor-based stage completes the conversion, as illustrated in Fig. 1. Since HSCCs do not usually suffer from inherent charge-sharing losses that appear in pure switched-capacitor converters (SCCs) due to inductors soft-charging the flying capacitor networks, performance can be significantly higher than the baseline SCC [20]. For example when operating in a soft-charged mode, the ripple across the flying capacitors can be significantly increased without experiencing the impedance issues typically associated with the slow-switching limit (SSL) observed in pure SCC [19]. Additionally, HSCCs offer a lossless voltage control capability not possible in baseline SCCs [17].

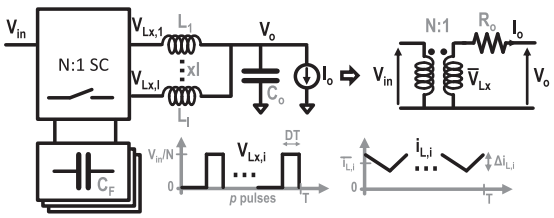

FIGURE 1. Overview of the general scheme employed by hybrid switched-capacitor converters (HSCCs).

The topological zoology of HSCCs is mainly derived from SCCs, influenced by formalization in the 2000s [19]:

TABLE 1. Table of Comparison of Previously Published Non-Resonant Hybrid Converters

	Unit	TPEL'22 [47]	TPEL'23 [48]	TPS54A20 TI Product	ISSCC'19 [49]	TCAS'22 [50]	JSSC'20 [23]	CICC'20 [51]	JSSCC'22 [52]	ISSCC'17 [53]	JSSC'21 [54]
Topology name	-	3L buck	3L buck	DSD	4L buck	Dual-branch SP	SMML	5L buck	Cascaded SC	4:1 Dickson	Tri-State DSD
Nominal voltage ratio	-	2	2	2	3	3	3	4	4	4	4
# phase	-	1	1	2	1	1	1	1	1	1	2
Input voltage	V	3.5-4.5	2.7-4.5	12	3.7-5	3.6	3-5.0	4-5.5	4-6.0	3-4.5	12-24.0
Output voltage	V	1-3.3	0.6-1.3	1.2	0.8-1.8	0.55-1	0.3-1.2	0.4-1.2	0.4-1.2	0.3-1	1
Peak output current	A	0.9	1.6	10	10	0.5	0.43	1.4	1	1.5	3
Technology	nm	55	65		22	3	180	180	180	65	180
Die area	mm^2	0.8	2.07		6.9	65	5.5		7.8	4.1	6.3
Area (die, passive)	mm^2		13.3		75.6	1.01	7		11		
Inductor	µH	0.33	0.47	2x0.22	10	0.1	0.22	0.24	0.24	0.18	2x0.56
Flying capacitor	µF	1x2.2	1x1	1x2.2	2x13.2	4x0.47	4x1	3x4.7	2x4.7 + 1x10	3x22	2x1
Output capacitor	µF	2.2	10	2x4.7	18	0.94	1	10	14.4	22	10
Switching frequency	MHz	3-3.5	2.5		4.4-11.8	5	4		1.4-1.6	1	0.2-2
Max power density	W/mm^2		0.15		0.95		0.52	0.11	0.1		
Peak power density	W/mm^3		0.061@3.5		0.198		0.52@4.2		0.18@4.5	0.24@4.4	0.06@12
Peak Efficiency	%@- [CR]	95@1.3	88.6@3.5		93.8@2.77	82@4	89.5@4.2	92.4@4.6	96.9@4.2	94.2@4.4	91.2@12
Max VCR	-@% [Eff.]			10@85	6.25@85.8		16.7@74.0	8.8@86.5	12.5@85.5		

Dickson [20], [21], series-parallel [13], Fibonacci [22], ladder [23], multi-level [24] and others [25], [26]. The concept of HSCCs can be expanded to multiple inductors [27], [28] placed at the input [29], [30], output [25], or in the middle [31] of capacitor networks. Moreover, certain proposed topologies such as those in [32], [33], [34], [35], [36], [37] incorporate the concept of dual-current paths, where simultaneous soft-charging and hard-charging operations are implemented primarily to minimize the current flowing into the inductor. Finally, HSCCs topologies can be combined with other well-known topologies such as dual active bridge to create high-performance DC-DC converters [38].

There are two main HSCC subsets divided by the energy transfer mode: resonant [2] or non-resonant [13]. Although resonant operation enables zero current switching, it is worth noting that operating a HSCC above resonance has the advantage of significantly reducing the circulating current. This reduction leads to a decrease in the RMS current through the switches, effectively mitigating switching losses and resulting in improved efficiency [39], [40]. Additionally, non-resonant operation is preferred for its advantages in regulating the output voltage and in less susceptibility to component and timing mismatch [41], [42], [43].

To further diminish the size of the inductor, prior studies have suggested the utilization of coupled inductors, which yield notable enhancements in transient response compared to uncoupled counterparts [44]. The advantages of coupling multiple inductors become particularly pronounced with an increase in the number of phases. However, designing a multiphase coupled inductor configuration that achieves simultaneously small current ripples, rapid transient response, and a compact inductor size poses significant challenges [45]. Due to the distinct inductor sizing procedure [46], our paper concentrates solely on structures utilizing non-coupled inductors.

This paper focuses only on non-resonant "direct" (as defined in [40]) HSCC topologies where the inductors are located at the output. In this configuration, the inductors act as current sources to soft-charge the capacitors located in the first conversion stage, which helps to reduce the capacitors' values compared to their baseline SCC counterparts. Thanks to the first stage introducing a natural N:1 voltage conversion ratio, the second stage can be seen as a traditional buck converter powered by a reduced intermediate power supply, V_{in}/N, to achive the desired VCR, named M here. Moreover, by interleaving the pulse train, it can have a higher rate than the switching frequency [24], reducing further the inductor voltage-second balance, which is an attractive benefit.

Choosing the right HSCC topology for a given application is crucial, as the topological choice distributes the constraints over the three main converter components (switches, capacitors, and inductors). Table 1 provides experimental data obtained by different research groups who have experimented with non-resonant HSCC using integrated Silicon power stages and inductors at the output with full soft-charging operations [23], [47], [48], [49], [50], [51], [52], [53], [54]. The data suggests that for most cases with MHz switching frequency, the inductor and flying capacitor are in the 100 s of nH and μF range, respectively. However, due to the different input voltage levels and IC choices used in various Silicon technologies, it is difficult to isolate the benefits of the HSCC topology itself, making inference of which topology is best suited for which application difficult. This is the main motivation for this work.

Previous studies have introduced various methods to predict the achievable output resistance [18], [39], [55], largely relying on models developed for SCCs [19], [56]. However, the proposed approach sets itself apart by establishing a direct link between the inherent performance of both passive and active components, leveraging parameters such as switch area and switching frequency across diverse topologies. This methodology allows for a comprehensive comparison of all topologies while ensuring consistent conduction and switching losses, including those from inductor. Additionally, it guarantees uniform inductor current and output voltage ripples, enhancing the fairness and accuracy of the evaluation process.

Our previous work [57] proposed a normalized benchmarking framework for fully soft-charging non-resonant direct

HSCC topologies, comparing various topologies to a baseline 2-level buck converter operating at the same power efficiency and output voltage ripple. This paper expands on [57] by presenting a comprehensive analytical framework with tractable equations and offering a broad overview of HSCC performance in various expanded design contexts, including regulated HSCCs where voltage regulation is achieved through duty cycle adjustment. The comparison is dimensionless, which ensures that any conclusions drawn are broadly applicable to various input/output voltage and current levels, as long as current and voltage ripples remain negligible in the calculation of RMS values and not impact the switch voltage rating. Recently, [43] introduces a comprehensive analysis that considers the impact of voltage ripple and introduces metrics to assess switch stress and passive volume for hybrid converters both at and above resonance.

The paper is structured as follows: we begin by presenting the modeling framework, including the assumptions made and the method for determining converter parameters from a small set of topological parameters. Next, we compare our benchmark to previous works. Then, we provide analytical expressions for converter parameters, such as silicon area, switching frequency, and total volume using the aforementioned method. Based on this framework, we offer recommendations for selecting the best topology for various design contexts, such as for a given voltage conversion ratio, and discuss the effect of switch and inductor scaling laws.

II. MODELING FRAMEWORK

A. INITIAL ASSUMPTIONS AND NOTATIONS

The proposed approach has certain limitations and assumptions. It is only valid in continuous mode, in periodic steady-state operation, without core saturation or hysteresis effects, and assumes equally-valued inductors, L, at the outputs for perfect output current sharing between phases [58]. The energy transfer through flying capacitance is considered to be in a fully soft-charging mode, with no charge-sharing loss in any state, and the frequency operation, F, is far above the self-resonance formed by L, C_F as in [14], [59], [60]. The resonant-based HSCC is not addressed in this paper due to its distinct loss mechanism, which significantly differs from non-resonant approaches [39], [40].

The methodology also assumes that the inductor series resistance (DCR) remains relatively constant within the studied switching frequency range, which is less than ten times in the following. Moreover, for the sake of simplicity, all flying capacitors are assigned an identical value, denoted as C_F.

The framework remains applicable under the condition of small voltage ripple across capacitors, as it does not consider the impact of voltage ripple on the voltage stress experienced by the switches, as also presumed in [19], [55], [61]. We have also assumed that the RMS current conveyed through all switches is solely due to the DC current. In other words, the contribution of current ripple in the switches conduction loss is neglected in this analysis. However, the effect of current ripple is included to calculate the conduction loss in the inductor. It's important to note that all these assumptions are uniformly applied to all topologies, potentially mitigating the impact of these assumptions in the later normalized benchmark results.

To enhance clarity, further assumptions, including passive component sizing, are introduced later in the paper. A summary of assumptions introduced later in the paper can be found in Appendix A.

Practical converter designs involve several considerations beyond just sizing of power transistors and passive components. These include factors such as VCR (DC gain) range, number of switches, gate driving, level shifters, capacitor charge balancing [33], [50], [62], voltage stress during the starting phase [52], feedback control [47], [48], [63], PCB routing, input capacitor [64] and EMI. While these considerations may make the low N topology an appealing choice, a final decision must take into account all relevant factors with appropriate weighting depending on the application.

To distinguish between dimensionless (x) and dimensional ($\widetilde{x}$) values, the paper uses tilde notation ($\widetilde{x}$). We also define three main variable types: i) the "input" variables defining the design context (e.g., desired VCR, switch performance), ii) the "topological" variables describing the HSCC, and iii) the "design" variables resulting of the framework (e.g., switching frequency, inductor volumes). Regarding the notation for voltage and volume, this paper names them V and U, respectively.

B. METHOD FOR SIZING A CONVERTER WITH CONSTANT LOSS AND CONSTANT RIPPLES

The core of the proposed framework involves comparing a HSCC referenced by a topology index, k, to a 2-level single-phase buck converter (1B) *at the same power dissipation level and at same inductor current and output voltage ripples*. The losses considered are the switch conduction loss, P_{cond}, the gate driving (i.e., switching) loss, P_{drive}, the inductor loss, P_{ind}, from the inductor's DCR, and the loss induced by the current ripple, ΔI_L. The total HSCC loss is expressed as:

$$\begin{aligned}\widetilde{P_{loss,k}} &= \widetilde{P_{cond,k}} + \widetilde{P_{drive,k}} + \widetilde{P_{ind,k}} \\ &= \widetilde{R_{o,k}}\widetilde{I_o^2} + \widetilde{E_{dr,k}}\,\widetilde{F_k} + \sum_i^{\#ind} R_L \frac{\widetilde{I_o^2}}{I_k^2}\left(1+\frac{\varepsilon}{12}\right) \end{aligned} \quad (1)$$

where k is the topology index, $\widetilde{R_o}$ is the equivalent output impedance, $\widetilde{I_o}$ is the output current, $\widetilde{F_k}$ is the switching frequency, $\widetilde{E_{dr,k}}$ is the total energy consumed by all switches during one cycle to commute, ε is the relative inductor current ripple (with respect to $\widetilde{I_L}$), l_k is the number of inductors, and $\widetilde{R_L}$ is the series resistance of each inductor (DCR).

For a given set of input parameters (voltage conversion ratio, switch scaling law, etc.), the method involves three steps:

1) Finding the total switch area, $\widetilde{A_k}$, to achieve the same output impedance as the basedline 1B buck converter ($\widetilde{R_{o,k}} = \widetilde{R_{o,1B}}$), meaning $\widetilde{P_{cond,k}} = \widetilde{P_{cond,1B}}$;

2) From $\widetilde{A_k}$, deducing the total energy, $\widetilde{E_{dr}}$, to commute during one cycle and adjusting the switching frequency $\widetilde{F_k}$, to obtain $\widetilde{P_{drive,k}} = \widetilde{P_{drive,1B}}$;
3) Adapting the inductor value, $\widetilde{L_k}$, to equalize inductor ripple, and thus losses: $\widetilde{P_{ind,k}} = \widetilde{P_{ind,1B}}$.

The output capacitor, $\widetilde{C_{o,k}}$, is then adjusted such that the HSCC and the 1B buck converter produce the same amount of output voltage ripple. By ensuring that the inductor current and output voltage ripples are the same for both topologies, the comparison becomes more meaningful, since any differences in performance can be attributed to the topology itself.

The value of the flying capacitors, $\widetilde{C_{F,k}}$, is then chosen such that the operating frequency of the HSCC is significantly above the resonance frequencies formed by $\{\widetilde{L_k}, \widetilde{C_{F,k}}\}$ and $\{\widetilde{L_k}, \widetilde{C_{o,k}}\}$ tanks compared to the chosen switching frequency, $\widetilde{F_k}$. This ensures that the flying capacitors operate in a fully soft-charging mode and ensures that each current is a constant value during each state. Hence, the RMS value is close to the DC value, restricting the framework to small-signal analysis, as in most existing benchmarks [19], [55].

To ensure consistent conduction loss in the inductor ($\widetilde{P_{\text{ind},k}}$) across various topologies, the DC resistance (DCR) of each inductor is chosen to be proportional to the number of inductors, as indicated by the topological parameter l defined later in Section II-E. For instance, single-inductor topologies like the baseline or Dickson share the same DCR for their inductor. In the case of topologies with two inductors, such as the double step-down (DSD) [12], the DCR is doubled compared to single-inductor topologies.

The method provides dimensionless design parameters, which are relative to those of the 1B converter. The output parameters include the switch area A_k, the switching frequency F_k, and passive component values (L_k, C_{ok}, and C_{Fk}) relative to those of the 1B converter (e.g., $\widetilde{F_k} = F_k \text{x} \widetilde{F_{1B}}$).

From these parameters, the method can determine the relative gain in switch area, passive component size (inductor and capacitor) and maximal cutoff frequency of the output LC filter BW compared to the 1B converter. This allows for a more direct comparison between the HSCC and 1B converter in terms of power density at the same power efficiency and inductor current and output voltage ripples.

C. COMPARISON TO PREVIOUS BENCHMARKS

The proposed methodology stands apart from prior studies by fully normalizing the design to a reference case and optimizing the triptych parameters A_k, F_k, L_k to achieve consistent overall losses, as shown in (1). Additionally, the optimization process encompasses adjustments to $C_{o,k}, C_{F,k}$ to ensure equivalent output ripple and maintain non-resonant operation. In contrast to [19], [65], our approach involves the comprehensive optimization of switch sizing. Each switch is tailored to minimize conduction loss at the targeted voltage conversion ratio, M. Furthermore, M does not necessarily correspond to the inherent Voltage Conversion Ratio (VCR) of the SCC network preceding the inductor (referred to as $1/N$). Consequently, our analysis focuses on comparing HSCCs with regulation capability. Our method distinguishes itself from previous approaches by establishing a connection between the intrinsic performance of passive and active components through switch area and switching frequency across different topologies. This facilitates a comparison of all topologies while maintaining consistent conduction and switching losses, including inductor losses. Moreover, it ensures uniform inductor current and output voltage ripples for a fair evaluation.

D. SELECTED TOPOLOGIES

In this paper, we have constrained our analysis to three flying capacitors to maintain a reasonable number of passive devices. Most of the referenced papers for 12-to-1 V in the IC context use three or fewer flying capacitors. If a higher VCR is targeted, the framework and the open-access code [66] can be easily extended to accommodate a greater number of flying capacitors. As mentioned earlier when discussing assumptions, we only consider HSCC topologies where the inductors are placed at the output, and exclude topologies from [29], [30], [31], as they require more nuanced analysis. Furthermore, we only consider HSCCs that exhibit fully soft-charging operation, which limits the selection of common SCC topologies, as not all of them are compatible with soft-charging. This excludes some topologies from our benchmarking scope, such as those in [32], [33], [34], [35], [36], [37]. While coupled-inductor topologies demonstrate noteworthy enhancements in certain use cases, we have excluded them from our comparison due to differences in the inductor sizing procedure.

For a single inductor at the output, previous work in [65] has already formally revealed configurations that satisfy this requirement without infinite flying capacitor values, namely the series-parallel (SP) and Fibonacci (FB) topologies. Direct deployment of the Dickson SCC topology in a HSCC does not provide soft-charging operation, but it can be modified to be compatible by introducing a splitting state [60], which we refer to as DS. The ladder [23] and doubler topologies are not included in our benchmark, as they are generally not amenable to soft-charging without major modifications. Based on our modeling assumptions, we compare the SP, FB, and DS topologies in the following. Additionally, flying capacitor multilevel converters (ML) are also added to the benchmark as they satisfy the soft-charging constraint [41], [49], [51], [67], [68]. These topologies align with the direct-conversion distinction proposed in [40].

For two inductors at the output, we have considered the well-known two-phase 2-L buck (1B2), the double step-down (2DSD) [12], and the tri-state DSD (2DSD3) [54] topologies, all of which offer full soft-charging operation.

The N prefix is used in this paper to indicate the N:1 natural SCC voltage conversion ratio for the topology name. The number of flying capacitors is N-1, except for 5FB (which follows the Fibonacci series) and 2DSD3. For instance, 3DS refers to the Dickson topology with unregulated 3:1

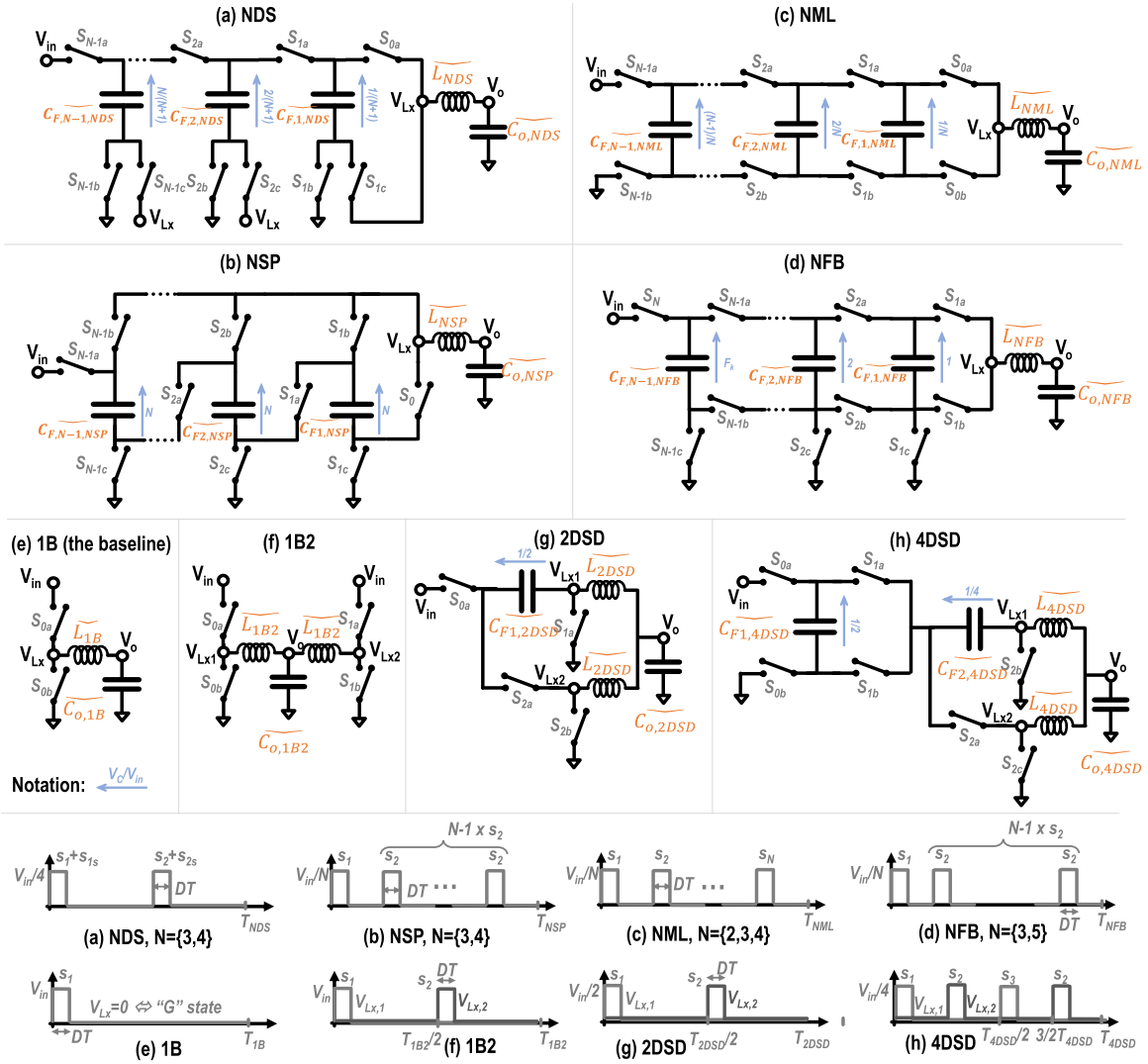

FIGURE 2. Selected topologies: Schematic diagrams and V_{Lx} waveforms, (a) Dickson, (b) series-parallel, (c) multi-level, (d) Fibanocci, (e) buck (the baseline), (f) 2-phase buck, (g) double-step-down, and (h) tri-state double-step-down.

TABLE 2. Terminology for Topologies in This Article

Topology	Terminologies found in literature	References
1B	1-phase 2-level Buck	[69]
1B2	2-phase 2-level Buck	[69]
NML	N:1 Flying-Capacitor Multi-Level	[24], [47], [49], [51]
NSP	N:1 Series-Parallel	[13], [25], [65]
NFB	N:1 Fibonacci Hybrid Converters	[22], [65]
NDS	N:1 Hybrid Dickson Switched-Cap.	[20], [21], [25], [60], [65]
2DSD	Double Step Down	[12], [70], [71]
4DSD	Tri-State Double Step Down	[54]

conversion capability. Table 2 aims to provide clarity on the naming conventions.

As we investigate the HSCC for achieving a targeted voltage ratio M that differs from the natural N:1 given by the flying capacitors network, we introduce the ground state (G), where the inductor is demagnetized. The duration of the G state is modulated according to the targeted VCR. Fig. 2 shows the schematics of all the screened topologies in this paper. Table 3 describes the states by giving the normalized current flowing into each switch in each state ($I_{sw,i}/I_O$).

E. TOPOLOGY DESCRIPTION

First, topologically defining vectors for each HSCC structure under consideration need to be derived through analysis and deduction. The framework utilizes only nine "topological" parameters (C, S, V_s, V_c, m, d, l, p, s) obtained from circuit inspection as inputs:

- The current multiplication vector, C, represents the RMS current flowing through each switch during the entire switching period T and is referenced to I_O. This concept is akin to the charge multiplier utilized in [19].
- The switching rate activity is given by the vector S, where each entry in the vector represents the number of times each switch in a given topology commutes during time T.

TABLE 3. Normalized Current Flowing in Each Switch for All States in 13 Selected Topologies

topo	1B	2ML			3ML				4ML					3SP			4SP			3FB			5FB			3DS					4DS					1B2			2DSD			4DSD			
state	1	1	2	1	2	1	2	3	1	2	3	4	1	2	1	2	1	2	1	1	2	1	1	2	1	1	1s	2	2s	1	1	1s	2	2s	1	1	2	1	1	2	1	1	2	3
T	D	1-D	D	D	1-2D	D	D	D	1-3D	D	D	D	D	1-4D	D	2D	1-3D	D	3D	1-4D	D	2D	1-3D	D	4D	1-5D	2/3D	1/3D	2/3D	1/3D	1-2D	¾D	1/4D	¾D	1/4D	1-2D	D	D	1-2D	D	D	1-2D	D	2D	D	1-4D
0a	1		1			1				1					1		1	1		1							1/2			1		2/3					1			1/2			1/2			
0b		1		1	1		1	1	1		1	1	1	1																						1	1						1/2		
1a				1				1			1		1					1			1/2	1		1/3	1		1					1/3	1				1						1/2		
1b			1		1	1	1		1	1		1	1		1/2			1/3			1			1			1/2			1	1			1/2	1	1		1			1/2				
1c															1/2	1		1/3	1	1		1	1		1			1					1	1	1/2									
2a						1						1	1					1			1			1/2			1/2	1				1/3	1								1/2				
2b						1		1	1	1	1			1	1/2			1/3		1				1				1			1/2			1/3	1	1/2					1	1/2		1		1/2
2c															1/2			1/3			1/2			1/3			1/2	1			1/2	1/3	1		1/2				1/2		1/2	1/2		1/2	1/2
3a										1								1			1/2			1/3										2/3										
3b									1		1	1	1					1/3						1/3																						
3c																		1/3						1/2																						
4a																								1/2																						

TABLE 4. Topological Parameters of Selected Hybrid Switched-Capacitor Converter Topologies

Topo	#ind.	#cap.	#switch	m	d	p	l	s	C^2	S	V_s (DSV)	V_s (TV)	V_c
				V_{Lx}/V_{in}	D/M	V_{Lx} pulses	#ind.		current multiplication vector	Switch activity	DS Blocking volt.	Term. Blocking volt.	Cap. volt.
									$S_0;S_{1a};S_{1b};S_{1c};S_{2a};S_{2b};S_{2c};S_{3a};S_{3b};S_{3c}$				$C_1;C_2;C_3$
1B	1	0	2	1	1	1	1	-	M,1-M	1;1	1;1	1;1	-
2ML		1	4	1/2	1	2	1	1	M;1-M;M;1-M	1;1;1;1	1/2;1/2;1/2;1/2	1;1/2;1;1/2	1/2
3ML		2	6	1/3	1	3	1	2	M;1-M;M;1-M;M;1-M	1;1;1;1;1;1	1/3;1/3;1/3;1/3;1/3;1/3	2/3;1/3;1;1/3;1;1/3	1/3;2/3
3SP			7	1/3	1	3	1	2	1-2M;M;M/2;1-5/2M;M;M/2;M/2	2;1;2;1;1;1;2	1/3;1/3;1/3;1/3;2/3;2/3;2/3	1/3;1/3;2/3;1/3;1;1;2/3	1/3;1/3
3FB			7	1/3	1	3	1	2	1-5/2M;2M;1-2M;M;M;M/2;M/2	1;2;2;1;1;1;2	1/3;1/3;1/3;1/3;2/3;2/3;1/3	1/3;2/3;1/3;1/3;1;2/3;1	1/3;2/3
3DS			7	1/3	3/2	2	1	2	3/4M;M;1/4;1/4+M/4;3/4M;1/4+M/4;1/4	2;1;1;2;1;1;1	1/3;2/3;1/3;1/3;1/3;1/3;1/3	2/3;1;1/3;1/3;1;1/3;1/3	1/3;2/3
4ML		3	8	1/4	1	4	1	2	M;1-M;M;1-M;M;1-M;M;1-M	1;1;1;1;1;1;1;1	1/4;1/4;1/4;1/4;1/4;1/4;1/4;1/4	1/2;1/4;3/4;1/4;1;1/4;1;1/4	1/4;1/2;3/4
4SP			10	1/4	1	4	1	3	1-3M;M;M/3;1-11/3M; M;M/3;M/3;M/3;M;M/3	3;1;3;1;1;1;3;1;1;3	1/4;1/4;1/4;1/4;1/4; 1/2;1/2;3/4;3/4;3/4	1/4;1/4;1/2;1/4;1/4;3/4; 1/2;1;1;3/4	1/4;1/4;1/4
5FB			10	1/5	1	5	1	2/3	1-14/3M;3M;1-3M;M/2; 2M;M/3;M/3;M/3;M/2;M/2	2;3;3;2;2;3;3;3;2;2	1/5;1/5;1/5;1/5;2/5; 2/5;2/5;3/5;3/5;2/5	1/5;2/5;1/5;1/5;3/5;2/5; 2/5;1;3/5;1	1/5;2/3;3/5
4DS			8	1/4	2	2	1	2	2/3M;2/3M;1/4+M;1/4+M; 2/3M 1/4-M/3;1/4-M/3;2/3M	1;1;1;1;1;1;1;1	1/4;1/2;1/4;1/4;1/2; 1/4;1/4;1/4	1/2;3/4;1/4;1/4;1;1/4;1/4;1	1/4;1/2;3/4
1B2	2	0	4	1	1	2	2	-	M/4;(1-M)/4;M/4;(1-M)/4	1;1;1;1	1;1;1;1	1;1;1;1	-
2DSD		1	4	1/2	2	2	2	1	M/2;1/4+M;M/2;1/4-M/2	1;1;1;1	1/2;1/2;1;1/2	1;1/2;1;1/2	1/2
4DSD		2	7	1/4	2	4	2	2	M/2;M/2;M/2;M/2;M;1/4+2M;1/4-M	1;1;1;1;2;2;2	1/2;1/2;1/2;1/2;1/2;1/4;1/4	1;1/2;1;1/2;1/2;1/4;1/4	1/2;1/4

- The vector V_s illustrates the maximal voltage experienced by each switch during all states. The voltage can be defined by referencing drain and source voltages to the bulk (TV), or alternatively the drain-to-source voltage (DSV). All components are normalized with respect to $\widetilde{V_{in}}$.
- The voltage handled by each flying capacitor is described in the vector V_c, where each element is the normalized voltage referenced to $\widetilde{V_{in}}$. A unity value means the DC voltage across the capacitor is $\widetilde{V_{in}}$.
- The scalar m_k represents the normalized V_{Lx} voltage (Fig. 1) by dividing the maximal $\widetilde{V_{Lx}}$ by $\widetilde{V_{in}}$. m_k is equal to $1/N$.
- The relationship between the desired VCR M and the duty cycle D is illustrated by the normalized duty-cycle $d_k = \frac{D}{M}$. DT represents the duration of each pulse where V_{Lx} is not equal to zero, as illustrated in Fig. 1.
- The scalar l is equal to the number of inductors.
- The switch rate of V_{Lx} is given by the scalar p. Here, a value of n means V_{Lx} switches n times during time T.
- The scalar s is utilized to ascertain the ratio of the effective capacitor value seen by L_k. It is used to calculate the out-of-resonance condition and is derived by determining the minimum value of the equivalent flying capacitor network at the V_{Lx} node throughout all states.

The vector size of C, S and V_s is equal to the number of switches. The length of V_c is determined by the number of flying capacitors. The term "state" pertains to the various switch configurations within one switching period, whereas the term "phase" is employed to signify the interconnection between different power stages that converge at the output node V_o through inductors. The topological parameters of all screened topologies are given in Table 4.

F. INPUTS DETERMINATION USING DSD AS AN EXAMPLE

This section describes how to find the topological parameters for a 2:1 HSCC in the DSD configuration (2DSD) using the schematic and state sequence shown in Fig. 2 and Table 3, respectively.

In the 2DSD configuration, featuring two inductors, under steady-state operation with ideal charge balancing, the capacitor network produces a V_{LX} pulse train oscillating between 0 and $V_{in}/2$ with a duty cycle of D, consequently resulting in $m = 1/2$. The connection between VCR and the duty cycle is expressed as $D = 2M$, setting d to 2. The total count of pulses observed by the output from both V_{Lx} is 2, yielding $p = 2$.

Table 3 gives the normalized current flowing in each state with respect to the output current, which allows us to determine the dimensionless current multiplication vector, C (Table 4). The RMS current flowing can be deduced in each switch during the period using Table 3, and then C_i can be calculated as:

$$C_i = \sqrt{\sum_j^{\#state} C_{i,j}^2 D_j} = f(M) \tag{2}$$

Here, D_j is the duty cycle of the jth state, and $C_{i,j}$ is the normalized DC current passing through the ith switch.

In 2DSD [12], three switches see half of the input voltage, and the third one sees the entire voltage ($V_{s,j} = 1/2$, $j\varepsilon\{1, 2, 4\}$ and $V_{s,3} = 1$). In some contexts, the voltage referenced to the bulk is the limiting factor, and this is given in the V_S vector in Table 4 (terminal voltage column). For 2DSD,

two switches see the entire voltage, and the others see half of the input voltage. In this case, V_s is equal to [1,1/2,1,1/2].

As the topology has one flying capacitor biased at half of the input voltage, V_c is a scalar vector equal to 1/2.

The switching activity of all switches is equal unity as every switch commutes once during one period. Thus, S is equal to the unity vector [1,1,1,1].

The parameters of all screened topologies are given in Table 4, and Fig. 2 shows the labeling of all screened HSCCs. The reader can also be referred to the 4ML topology example given in [57]. For charge balancing and soft-charging operation, the operation of the 13 topologies may require some small modifications compared to their baseline SCC counterparts. For example, the Dickson NDS includes the splitting state (called 1 s, 2 s) as introduced in [60], and the series-parallel NSP topology has one charging state and N-1 discharging states for charge balancing purpose [18]. Other state sequence could be considered to have a charge balanced process, but we try to keep the most favorable sequence for each topology.

G. LINK BETWEEN EXISTING PROXIES AND THE PROPOSED TOPOLOGICAL PARAMETERS

In the proposed topological parameters used in this paper, we can draw some parallels with a conventional figure of merit commonly found in the literature. For example, [43] has previously introduced a method for comparing topologies based on the product of the maximum voltage stress ($V_{\max}$) and the root mean square (RMS) current (I_{rms}) experienced by each switch. The sum of these products, considering each element in the vector of $V_s \times C$, forms the basis of this figure of merit (FoM).

III. BENCHMARKING FRAMEWORK PROCEDURE DESCRIPTION

A. ACTIVE-DEVICES SCALING MODELS

Before explaining each step in detail, it is worth noting the general trade-off in switch performance versus voltage rating. Common cost-scaling models have already been introduced to create a relationship between the size, on-state resistance, switching energy, and voltage rating in prior work [16], [17], [18], [19]. Applicable to both integrated and discrete transistors using a planar structure, this constraint can be expressed as:

$$A_i \propto G_i V_{s,i}^{\alpha} \tag{3}$$

Where G_i and $V_{s,i}$ are the conductance and the rated voltage of the switch, labelled i, respectively. α is a coefficient representing the cost depending on the scenario (cascade arrangement, constant field, high-voltage, etc.), varying from 0 to 2.

We also introduce an additional relationship to link the energy consumed $E_{dr,i}$ to commute the ith switch to the blocking voltage $V_{s,i}$ using β:

$$E_{dr,i} \propto A_i V_{s,i}^{\beta} \tag{4}$$

TABLE 5. Coefficient for Switch Scaling Law

Scenario name	G-V [18]	G-V^2 [18], [19]	Constant field [17]	Cascode arrang. [17]	GaN [17]
α	1	2	2	1	-
β	0	0	1	1	-
$\alpha+\beta$	1	2	3	2	1.3

The Table 5 summarizes some values for different scenarios found in previous works. To maintain the generality of the model, the framework keeps α and β as input variables, given the various options available.

B. TOTAL SWITCH AREA

The first step of the benchmarking framework looks to minimize the total switch area, A, to obtain a given output impedance, R_o. Following the switch scaling law given in Section III-A, the denormalized switch area $\widetilde{A_k}$ can be expressed as:

$$\widetilde{A_k} \propto \sum_{i}^{\#sw} \widetilde{G_{i,k}} \widetilde{V_{s,i,k}}^{\alpha} \tag{5}$$

where $\widetilde{G_{i,k}}$ is the on-state conductance of each switch of the topology k, and the sum is over the switches included in the topology k.

The output impedance of the converter is defined as follows:

$$\widetilde{R_{o,k}} = \sum_{i}^{\#sw} \frac{C_{i,k}^2}{\widetilde{G_{i,k}}} \tag{6}$$

where C_i is the portion of RMS current referenced to I_O through the i^{th} switch, as defined previously and formally defined in (2).

Similarly to [19], but without presuming the G-V^2 switch scaling law, a Lagrange optimization function $\mathcal{L}$ is formed to find the minimal output impedance while satisfying the constraint in (5):

$$\mathcal{L} = \sum_{i}^{\#sw} \frac{C_{i,k}^2}{\widetilde{G_{i,k}}} + \lambda \left(\sum_{i}^{\#sw} \widetilde{G_{i,k}} \widetilde{V_{s,i,k}}^{\alpha} - \widetilde{A_k} \right) \tag{7}$$

The minimization is performed by taking the partial derivative of (7) and setting it to zero:

$$\frac{\partial \mathcal{L}}{\partial \widetilde{G_{i,k}}} = -\frac{C_{i,k}^2}{\widetilde{G_{i,k}}^2} + \lambda V_{s,i,k}^{\alpha} = 0 \tag{8}$$

Equation (8) defines the optimal conductance of the i^{th} switch with a coefficient g:

$$\widetilde{G_{i,k}} = g \left| \frac{C_{i,k}}{\widetilde{V_{s,i,k}}^{\alpha/2}} \right| \tag{9}$$

Combining with (5), the optimal partition of switch conductance for a given switch area $\widetilde{A_k}$ can be found:

$$\widetilde{G_{i,k}} = \frac{\widetilde{A_k}}{\sum_i^{\#sw} \left| C_{i,k} \widetilde{V_{s,i,k}}^{\alpha/2} \right|} \left| \frac{C_{i,k}}{\widetilde{V_{s,i,k}}^{\alpha/2}} \right| \tag{10}$$

The output impedance is obtained by combining (6) and (10):

$$\widetilde{R_{o,k}} \propto \frac{1}{\widetilde{A_k}} \left(\sum_i^{\#sw} C_{i,k} \widetilde{V_{s,i,k}}^{\alpha/2} \right)^2 \tag{11}$$

This analytical expression allows for the comparison of various HSSC topologies without any assumptions on the active device scaling law described in Section III-A.

From the topological parameters given in Table 4, the switch area of the baseline 1B can be deduced:

$$\widetilde{A_{1B}} \propto \frac{1 + 2\sqrt{M(1-M)}}{\widetilde{R_{o,1B}}} \tag{12}$$

In our framework, each topology is compared to the baseline two-level buck converter topology (1B). From (11) and (12), the switch area $\widetilde{A_k}$ of a k-indexed topology is compared to $\widetilde{A_{1B}}$ with the same $\widetilde{R_o}$ ($\widetilde{R_{o,k}} = \widetilde{R_{o,1B}}$).

$$A_k = \frac{\widetilde{A_k}}{\widetilde{A_{1B}}} = \frac{\left(\sum_i^{\#sw} C_{i,k} V_{s,i,k}^{\alpha/2} \right)^2}{1 + 2\sqrt{M(1-M)}} \tag{13}$$

Now, the normalized switch area A_k is independent of $\widetilde{V_{in}}$ and $\widetilde{R_o}$, in contrast to (11).

C. SWITCHING FREQUENCY

The gate driving power loss of each switch is proportional to its switching rate activity S_k, switch area $A_{i,k}$, the switching frequency F_k, and the scaling law coefficient β from (4). The total gate driving power for the topology is given by:

$$\widetilde{P_{drive,k}} = \widetilde{F_k} \sum_i^{\#sw} S_{i,k} \widetilde{A_{i,k}} \widetilde{V_{s,i,k}}^{\beta} = \widetilde{F_k} \sum_i^{\#sw} S_{i,k} \widetilde{G_{i,k}} \widetilde{V_{s,i,k}}^{\alpha+\beta} \tag{14}$$

In order to obtain the same driving loss as the baseline buck topology (1B), we introduce an dimensionless power loss variable, P_{drive}, which represents the switching loss overhead of the k^{th} topology relative to 1B (for the same $\widetilde{A}$):

$$P_{\text{drive,k}}(A_k = 1) = \frac{\widetilde{P_{drive,k}}}{\widetilde{P_{drive,1B}}} = F_k \sum_i^{\#sw} \frac{S_{i,k} C_{i,k} V_{s,i}^{\frac{\alpha}{2}+\beta}}{\sum_i^{\#sw} C_{i,k} V_{i,k}^{\alpha/2}} \tag{15}$$

As defined in Section III-B, the total switch area is different between the topology k and the baseline 1B by a factor A_k to keep the same output impedance.

To equalize the switching loss at the same output impedance, the relationship needs to be satisfied:

$$P_{drive,k}(A_k = 1) \times A_k = 1 \tag{16}$$

Using this expression, the normalized frequency determination can be given by:

$$F_k = \frac{1 + 2\sqrt{M(1-M)}}{\sum_i^{\#sw} S_{i,k} C_{i,k} V_{s,i}^{\frac{\alpha}{2}+\beta} \sum_i^{\#sw} C_{i,k} V_{s,i}^{\frac{\alpha}{2}}} \tag{17}$$

D. INDUCTOR VALUE

Only four topological parameters $\{m, d, l, p\}$ are required to analytically express the inductor current ripple in any HSCC studied in this paper. As shown in Fig. 1, any HSCC generates a pulse train V_{Lx} with a reduced amplitude compared to a two-level buck thanks to the input capacitive network (i.e., the N:1 SCC). The normalized output amplitude of the SCC is defined by $m = \widetilde{V_{Lx}}/\widetilde{V_{in}}$. Depending on the topology, the output filter is formed by l inductors connected at the l SC outputs. To regulate the desired voltage ratio $M = \widetilde{V_o}/\widetilde{V_{in}}$, the duty cycle of the pulse train D is adjusted. For normalization, the duty cycle d is defined as $d = D/M$. During the switching period T, the pulse train of all V_{Lx} combined consists of p pulses, each having a duration of D.

According to these coefficients, the relative inductor current ripple of a k-indexed HSCC can be expressed as:

$$\Delta_R \widetilde{I_{L,k}} = \frac{\Delta \widetilde{I_{L,k}}}{< \widetilde{I_{L,k}} >} = (m_k - M) d_k l_k M \frac{\widetilde{V_{in}}}{\widetilde{L_k} \widetilde{F_k} \widetilde{I_o}} \tag{18}$$

By comparing the ripple to the baseline 1B, the *normalized* inductor current ripple is given by:

$$\Delta_R I_{L,k} = \frac{\Delta_R \widetilde{I_{L,k}}}{\Delta_R \widetilde{I_{L,1B}}} = \frac{(m_k - M)}{(1-M)} d_k l_k \frac{1}{L_k F_k} \tag{19}$$

As described in the framework development procedure, we compare the topology at the same inductor ripple, meaning $\Delta_R I_{L,k} = 1$. Equation (19) gives L_k when F_k is found in Section III-C:

$$L_k = \frac{d_k l_k (m_k - M)}{(1-M) F_k} \tag{20}$$

Combined with (17), the inductor value can be found only from the topological parameters, independently of input/output current/voltage values:

$$L_k = \frac{d_k l_k (m_k - M) \sum_i^{\#sw} S_{i,k} C_{i,k} V_{s,i}^{\frac{\alpha}{2}+\beta} \sum_i^{\#sw} C_{i,k} V_{s,i}^{\frac{\alpha}{2}}}{(1-M)(1 + 2\sqrt{M(1-M)})} \tag{21}$$

E. OUTPUT CAPACITOR VALUE

Following the same notations as in the inductor current ripple determination, the output voltage ripple can be expressed as:

$$\Delta_R \widetilde{V_o} = \frac{\Delta \widetilde{V_o}}{< \widetilde{V_o} >} = (m_k - l_k M) \frac{d_k M}{p_k} \frac{\widetilde{V_{in}}}{8 \widetilde{L_k} \widetilde{C_{o,k}} \widetilde{F_k}^2} \tag{22}$$

The *normalized* output voltage ripple can be expressed as follows by using the previously defined coefficients:

$$\Delta_R V_{o,k} = \frac{\Delta_R \widetilde{V_{o,k}}}{\Delta_R \widetilde{V_{o,1B}}} = \frac{d_k (m_k - l_k M)}{p_k (1-M)} \frac{1}{L_k C_{o,k} F_k^2} \tag{23}$$

To obtain the same output voltage ripple as the baseline topology, the normalized output voltage ripple has to be equal to unity. Combining this constraint in (23) with (17) and (21), we get:

$$C_{o,k} = \frac{m_k - l_k M}{p_k l_k (m_k - M)} \frac{\sum_i^{\#sw} S_{i,k} C_{i,k} V_{s,i}^{\frac{\alpha}{2}+\beta} \sum_i^{\#sw} C_{i,k} V_{s,i}^{\frac{\alpha}{2}}}{1 + 2\sqrt{M(1-M)}} \tag{24}$$

The previous expression does not depend on any denormalized value such as $\widetilde{V_{in}}$, $\widetilde{I_o}$, or $\widetilde{F}$. C_k should be understood as the ratio of the output capacitor value of the topology k to that of 1B to obtain the same output voltage ripple. If C_k is less than one, the value required in the topology k is lower than in 1B.

F. FLYING CAPACITOR VALUE

In most cases, the flying capacitors volume is lower than the inductors volume [72], [73]. Thus, the flying capacitor value can be directly derived from the inductor value L_k. As the flying capacitor value cannot be referenced to the non-existent flying capacitor in the 1B topology, we choose to refer the value to the well-known 3-level buck converter, namely 2ML here.

In contrast to [65], where the voltage ripples across each C_F are maintained constant, in this study, the flying capacitor values are determined by ensuring that the operation remains out-of-resonance with the same ratio K_F. It is worth noting that voltage ripple does not impact power loss in the analyzed topologies, as they are fully soft-charged. The equation below links the flying value to switching frequency and inductor values to maintain F far above the self-resonance F_{res} formed by L_K and the series or parallel combination of $C_{F,k}$.

$$\widetilde{F_k} >> \widetilde{F_{res}} \propto \frac{1}{\widetilde{L_k}\widetilde{C_{F,k}}} \Rightarrow C_{F,k} = \frac{s_k d_k^2}{L_k F_k^2} \tag{25}$$

Where s_k is the minimum ratio value of the flying capacitor observed from the capacitance network at the V_{Lx} node throughout all states, the normalized value $C_{F,k}$ is referenced to the 2ML topology, serving as a reference (as 1B has no flying capacitor).

The ratio K_F between F and F_{res} does not play a role in determining the normalized value of the flying capacitor. However, this ratio will influence the determination of the total passive volume, as described later in Section III-I.

Once the values of L_k and F_k are determined for a given topology from (17) and (21), the values of C_F can be directly calculated:

$$C_{F,k} = \frac{s_k d_k (1-M) \sum_i^{\#sw} S_{i,k} C_{i,k} V_{s,i}^{\frac{\alpha}{2}+\beta} \sum_i^{\#sw} C_{i,k} V_{s,i}^{\frac{\alpha}{2}}}{l_k (m_k - M)(1 + 2\sqrt{M(1-M)})} \tag{26}$$

Again, the value of the flying capacitors can be determined without the need for any specific input or output voltage or current values, which makes the design process more generalizable.

In certain scenarios, particularly when the number of flying capacitors increases, the contribution of capacitors to the overall volume of the converter cannot be overlooked. To ascertain whether we are in such a situation, it is imperative to first express the total volume U_T. Section III-I will delve into these cases where capacitors cannot be deemed negligible in determining the total volume.

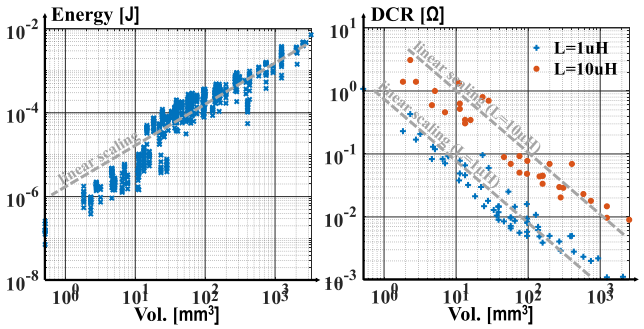

FIGURE 3. Analysis of inductor volume trends.

G. INDUCTOR VOLUME

Fig. 3 presents a survey of compact commercial inductors extracted from datasheets of a major supplier (TDK, Murata). The inductor volume scales linearly with the square root of the saturation current. Sometimes, in the right part of Fig 3, for high-current application, the series resistor of the inductor (DCR) has to be very low and the inductor size is more ditacted by DCR than by the saturation current [74]. In this case, a clear linear relationship between the inductor volume and DCR, R_L, can be observed for the same inductor value. For these two cases, where the inductor volume is limited by its saturation current (i) or by the DCR value (ii), the total inductor volume U_L can be expressed as follows, respectively:

$$\text{(i) } \widetilde{U_{L,k}} \propto l_k \widetilde{L_k} \widetilde{I_{L,k}}^2; \text{ (ii) } \widetilde{U_{L,k}} \propto l_k \frac{\widetilde{L_k}}{\widetilde{R_L}} \widetilde{I_o}^2 \tag{27}$$

Under the assumption of ideal components, equal inductor values and small inductor ripple current, the inductors connected in parallel exhibit identical current flow. Therefore, the current through each inductor in a topology with l output inductors is simply the output current divided by the number of inductors:

$$\widetilde{I_{L,k}} = \frac{\widetilde{I_o}}{l_k} \Rightarrow I_{L,k} = \frac{1}{l_k} \tag{28}$$

If we assume the same DCR for each inductor, the *normalized* power dissipated in all inductors can be calculated:

$$P_{ind,k} = \sum_j^{\#inductor} R_{L,j} I_{L,j,k}^2 = \frac{R_L}{l_k^2} \tag{29}$$

To compare all topology, the same conduction loss $\widetilde{P_{ind}}$ in the inductor has to be obtained, meaning $P_{ind} = 1$. Combining (27) and (29) with the previous constraint, the total inductor

volume is proportional to the inductor value L_k:

$$U_{L,k} = \frac{\widetilde{U_{L,k}}}{\widetilde{U_{L,1B}}} = \frac{L_k}{l_k^{\gamma}} \tag{30}$$

where γ is equal to unity or zero when the inductor volume is dictated by the saturation current (case i) or DCR value (case ii), respectively.

To explore the implications of these two hypotheses, we have focused on the 1B2 topology. If we choose case (i), the combined volume of the two inductors in 1B2 is equivalent to that of 1B (i.e., $U_{L,1B2} = 1$). Conversely, if we choose case (ii), the volume of 1B2 will be twice that of 1B ($U_{L,1B2} = 2$), since the inductor cannot benefit from the reduction in the saturation current in each of the two inductors, as they will be constrained by the DCR.

H. CAPACITOR VOLUME

When calculating the volume of capacitors, we assume it is dictated by the energy stored in the capacitor, not by ESR requirements. Here, the normalized volume of the output decoupling capacitor (referred to the two-level buck converter 1B) is given by:

$$U_{C_o,k} = \frac{\widetilde{U_{Co,k}}}{\widetilde{U_{Co,1B}}} = C_{o,k} V_{o,k}^2 = C_{o,k} \tag{31}$$

where $V_{o,k}$ is the normalized output voltage ($V_{o,k} = \widetilde{V_{o,k}}/\widetilde{V_{o,1B}}$), which is equal to unity by definition (i.e., all topologies are compared at the same output voltage).

The same consideration is done to determine the volume of the total flying capacitors. The total volume of the flying capacitors referred to 2ML is determined by:

$$U_{C_{F,k}} = \frac{\widetilde{U_{C_{F,k}}}}{\widetilde{U_{C_{F,2ML}}}} = C_{F,k} \sum_{j}^{\#cap} V_{s,j,k}^2 \tag{32}$$

I. TOTAL PASSIVE VOLUME

Based on previous experimental works on HSCC [72], we make the initial assumption that the volume of the output capacitor (U_{C_O}) can be considered negligible compared to the volumes of the flying capacitors (U_{C_F}) and inductors (U_L). However, it is important to note that the total passive volume cannot be obtained simply by summing the normalized volumes of the inductors (U_L) and flying capacitors (U_{C_F}) since they are normalized with respect to different baselines. Therefore, a process of denormalization becomes necessary using ρ_L and ρ_C the volumetric energy density factors of inductors and capacitors, respectively.

The denormalized flying capacitor volume $\widetilde{U_{C_F}}$ is given by:

$$\begin{aligned}\widetilde{U_{C_{F,k}}} &= U_{C_{F,k}} \widetilde{U_{C_{F,2ML}}} = U_{C_{F,k}} \frac{1}{2} \widetilde{C_{F,2ML}} \sum_{j}^{\#cap} \widetilde{V_{c,j,2ML}}^2 \\ &= \frac{C_{F,k} \widetilde{C_{F,2ML}} \widetilde{V_{in}}^2 \sum_{cap} V_{c,i,k}^2}{8\rho_C}\end{aligned} \tag{33}$$

The out-resonance ratio K_F is defined as:

$$K_F = \frac{\widetilde{T_{res,k}}}{\widetilde{T_{st,k}}} = \frac{2\pi d_k M \sqrt{(\widetilde{L_k} \widetilde{C_{F,k}}/s_k)}}{\widetilde{F_k}} \tag{34}$$

where T_{st} is the maximal duration of the states (DM/F), excluding the ground state, and T_{res} is the minimal resonant period of the electrical oscillator formed by L and the combination of C_F network in any state ($2\pi\sqrt{LC_F/s_k}$).

The flying capacitor volume for the 2ML topology is expressed as:

$$\widetilde{C_{F,2ML}} = \frac{M^2 K_F^2}{4\pi^2 \widetilde{L_{2ML}} \widetilde{F_{2ML}}^2} s_{2ML} d_{2ML}^2 \tag{35}$$

where $\widetilde{L_{2ML}}$ is defined as $L_{2ML}\widetilde{L_{1B}}$, with $L_{2ML} = \frac{M(1-M)\widetilde{V_{in}}}{\delta \widetilde{F_{1B}} \widetilde{I_o}}$, and $\widetilde{F_{2ML}}$ is defined as $F_{2ML}\widetilde{F_{1B}}$. Additionally, d_{2ML} and s_{2ML} are set to 1 by the definition of the topological parameters for 2ML.

The overall volume of the flying capacitor is reciprocally related to L_k:

$$\widetilde{U_{C_{F,k}}} = \frac{\delta K_F^2 M}{16\pi^2 \rho_c (1-M)} \frac{d_k^2 s_k \sum_{cap} V_{c,i,k}^2}{F_k^2 F_{2ML}^2 L_{2ML}} \frac{\widetilde{I_o} \widetilde{V_{in}}}{\widetilde{F_{1B}}} \frac{1}{L_k} \tag{36}$$

The denormalized total inductor volume ($\widetilde{U_T}$) varies in direct proportion to L_k:

$$\widetilde{U_{L_k}} = U_{L_k} \widetilde{U_{L_{1B}}} = \frac{M(1-M)}{\rho_L \delta l_k^{\gamma}} \frac{\widetilde{I_o} \widetilde{V_{in}}}{\widetilde{F_{1B}}} L_k \tag{37}$$

where the baseline inductor is defined as $\widetilde{L_{1B}} = \frac{M(1-M)\widetilde{V_{in}}}{\delta \widetilde{F_{1B}} \widetilde{I_o}}$, incorporating the current ripple constraint $\delta = \frac{\Delta I_L}{I_L}$ and the expression for voltage-second balance.

By adding the two previous denormalized expressions the total normalized volume (U_T) is expressed as follows:

$$U_T = \frac{M \widetilde{I_o} \widetilde{V_{in}}}{\rho_c \widetilde{F_{1B}}} \widetilde{U_T} = a L_k + \frac{b}{L_k} \tag{38}$$

where:

$$\begin{aligned} a &= \frac{\rho_C (1-M)}{\rho_L \delta l_k^{\gamma}} \\ b &= \frac{\delta K_F^2}{16\pi^2 (1-M)} \frac{1}{F_{2ML}^2 L_{2ML}} \frac{d_k^2 s_k \sum_{cap} V_{c,i,k}^2}{F_k^2} \end{aligned} \tag{39}$$

By introducing only two dimensionless design parameters, δ and K_F, an expression of total volume removing most of the design-level dimensional parameters such as $\widetilde{V_{in}}$, $\widetilde{L_{1B}}$ or $\widetilde{I_o}$.

The expression for U_T in (38) is dimensionless and has a minimum at $L_{k,opt} = \sqrt{\frac{b}{a}}$. If the inductor value L_k found in (21) equals $L_{k,opt}$, the volume of flying capacitors will be the same as that of inductors. If $L_k < L_{k,opt}$, meaning the capacitor volume can no longer be negligible as in some practical implementations [41], the framework will select the optimal value $L_{k,opt}$ for the inductor to minimize the overall passive volume.

Moreover, the normalized coefficient in (38) reaffirms the scaling characteristics of the converter volume. For instance, the total volume exhibits a linear scaling with output power and an inverse proportionality with the switching frequency. This observation emphasizes the advantageous volume reduction achieved by hybrid converters, especially as the voltage conversion ratio (VCR) decreases, corresponding to lower values of M.

J. POWER DENSITY

Power density is a key metric in DC-DC converter comparisons. In this framework, the power density gain is analogous to $1/U_T$ since all topologies are compared at the same output power.

K. CUTOFF FREQUENCY DETERMINATION

From the expressions for the passive components in (21) and (24), and similarly to [75], we can deduce the normalized 3 dB bandwidth of the converter, BW_k, which is dictated by the cutoff frequency of the small-signal model of the output filter:

$$BW_k = \frac{1}{\sqrt{L_k C_{o,k}}} = \sqrt{\frac{p_k l_k (1-M)}{d_k (m_k - l_k M)}} \frac{1 + 2\sqrt{M(1-M)}}{\sum_i^{\#sw} S_{i,k} C_{i,k} V_{s,i}^{\frac{\alpha}{2}+\beta} \sum_i^{\#sw} C_{i,k} V_{s,i}^{\frac{\alpha}{2}}} \tag{40}$$

IV. BENCHMARK RESULTS

A. INPUT VARIABLES

The framework requires certain input variables to be chosen before starting the topological benchmark. These variables include:

- the voltage conversion ratio (M);
- the active device scaling law (α and β);
- the definition of the blocking voltage vector (V_s): the maximal drain-source voltage (DSV), or the voltage referred to the bulk (TV);
- the relative energy density ratio between inductors (ρ_L) and capacitor (ρ_C), as expressed in (39), namely ρ;
- the inductor sizing case (γ): 0 if DCR is the limiting factor, 1 otherwise.

In this study, we set $K_F = 10$ to be out-of-resonance and $\delta = 0.3$ to have 30% relative inductor ripple. By default, when these variables do not vary, the VCR is fixed to 0.1, the switch follows the G-V^2 scaling law, the energy density ratio is 100, DCR is considered as the limited factor ($\gamma = 0$), and the drain-source voltage is considered to be the blocking voltage.

Exploring the impact of varying input variables while holding others constant, we conducted a sensitivity analysis to determine how different combinations of these variables might affect optimal topologies. Table 6 provides a summary of the benchmarks across multiple dimensions for quick reference.

TABLE 6. Benchmarks Across Multiple Dimensions

Section	M	α	β	V_s	ρ	γ
B	0.1	2	0	DSV	100	0
D	[0.1;0.5]	2	0	DSV	100	0
E	[0.1;0.5]	[0;2]	0	DSV	100	0
F	[0.05;0.15]	[1.5;2]	0	{DSV;TV}	100	0
G	0.1	[0;2]	0	DSV	[5;100]	0
H	[0.05;0.15]	[1.5;2]	0	DSV	100	{0;1}

B. DEFAULT INPUT VARIABLES

Fig. 4 presents the results of the benchmarking framework with default values for all input variables. In the 1B topology, the bottom switch (S_2) accounts for 75% of the overall switch area (Fig 4(a)) due to the majority of current flowing through it. Fig 4(b) displays the values of each design variable (A, F, L, C_o, C_F) necessary to achieve the same power efficiency and ripples as the baseline 1B.As an example, the 4DS topology only requires half of the switch area compared to 1B ($A_{4DS} = 0.54$), allowing for a substantial increase in the switching frequency ($F_{4DS} = 1.8$) while maintaining the same driving loss. Using (21), the inductor value for 4DS is 0.17 times that of 1B. By using all the design variables, we calculate the total volume U_T from (38) and the maximal cutoff frequency of the output LC filter from (40) and plot them in Fig 4(c). For this particular input variables case, 4ML and 4DS have the smallest volume, with a 5x reduction compared to 1B. As U_T and power density (PD) link explained earlier Section III-J, the power density is also boosted by 5x. The 4DSD topology is superior to the others in maximizing bandwidth.

C. VALIDATION THROUGH SPICE-LEVEL SIMULATIONS

To validate the accuracy of the analytical equations, we conducted SPICE-level simulations, implementing all HSCC topologies using switches from analogLib in Cadence (with finite R_{ON}) and inductors including DCR. For a fixed set of input variables (default values), we documented on-state resistances $R_{on,i,k}$, switching frequencies F_k, inductor L_k, and capacitor $C_{F,k}, C_{o,k}$ values, as provided by the framework (mainly from (17), (21), (24)). Subsequently, we verified that the output impedances $R_{o,k}$, inductor current ripples $\Delta I_{L,k}$, and output voltage ripples $\Delta V_{o,k}$ of each topology were consistent with each other, as illustrated in Fig. 5(a).

For instance, the output resistance of each topology was indeed equal to the baseline two-level buck, 1B, within a 5% error. The inductance current oscillation and output voltage ripple were also similar for all topologies, demonstrating that the topologies can be compared at the same efficiency and ripple levels. We verified that each converter was operating well above the resonance frequency with the C_F values given by the framework (26), indicating that the current is mostly constant in each state. By introducing switching loss linked to the on-state of each switch, the overall efficiencies are also checked to ensure the validity of your assumptions and derivations.

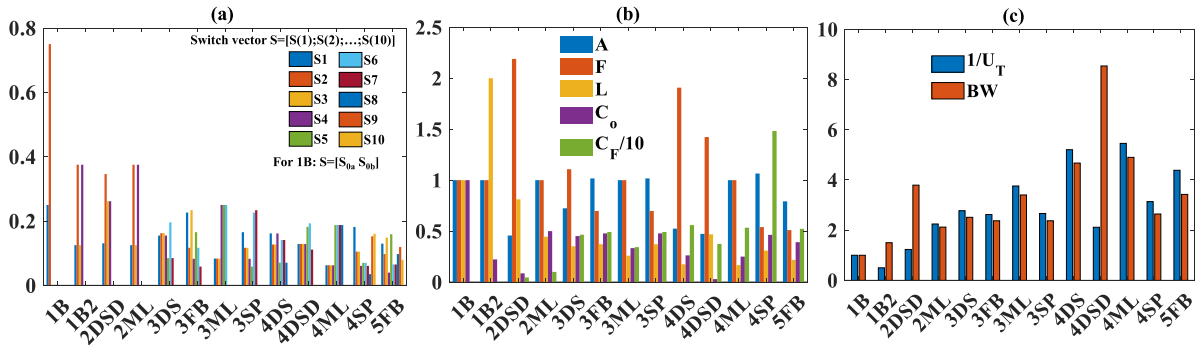

FIGURE 4. Topological benchmark when all design variables are equal to the default values (a) relative contribution of each switch area to the total area A, (b) all optimal design variables given from the framework, and (c) total volume of each converter and bandwidth.

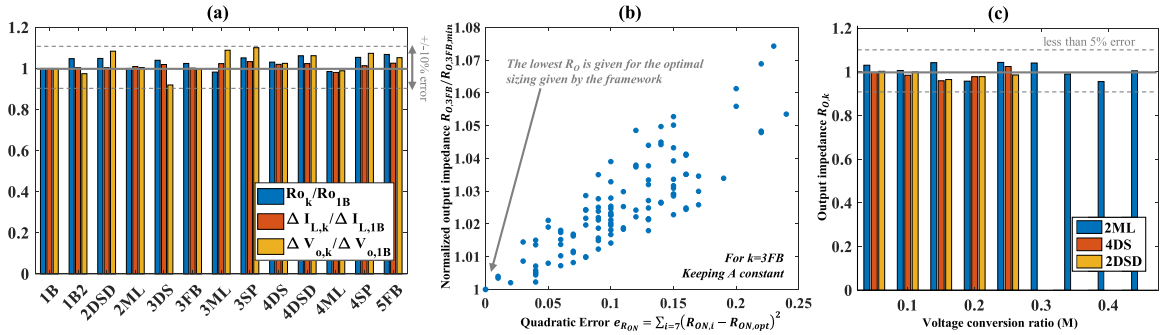

FIGURE 5. Framework validation using SPICE transient simulations (a) The relative output impedance, inductor current ripple and output voltage ripples with default variable values given in Section IV-B, (b) the output impedance if R_{on} diffres from the optimal sizing given by the framework (10), and (c) Comparison of the output impedances of 1*B* and 2*DSD* in respect to VCR (*M*).

To confirm the validity of the analytical equation in finding the lowest output impedance for a given switch area, we conducted SPICE transient simulations. In each simulation, we slightly varied the R_{on} distribution over the switches from the optimal one given by the framework (10). Fig. 5(b) illustrates the normalized output impedance of the topology 3FB against how far it deviates from the optimal point. We defined a quadratic error to measure the distance from the optimal point: $e_{Ron} = \sum (R_{ON,i} - R_{on,opt,i})^2$, where $R_{on,opt,i}$ is the optimal on-state value of switch i for a given area, and $R_{ON,i}$ is a value deviating from the optimal point where the summation of each switch area gives the same total switches area.

We also verified that the output impedances are always equal when the input variables vary. Fig. 5(c) illustrates the case where M varies from 0.05 to 0.45 for three selected topologies. For each M, the framework provides new design variables, which are then used in the SPICE schematic ($R_{ON,i}$, L, etc.). Transient simulations are performed to compare the output impedance to the baseline (R_O). We observed less than a 5% error, confirming once again the validity of the analytical equations presented in this paper.

As the considered topologies have previously undergone practical validation, we find it unnecessary to furnish additional demonstrations. The primary aim of this article is to introduce an idealized comparison framework, facilitating the juxtaposition of various topologies to showcase their potential within specified assumptions. As outlined in Section II-A, it is crucial to recognize that additional implementation constraints should be considered, thereby augmenting the difficulty of a practical validation at this comparative level.

D. EFFECT OF VOLTAGE CONVERSION RATIO

It is important to highlight that the choice of the optimal topology is significantly influenced by the voltage conversion ratio (VCR), M, as it plays a crucial role in all analytical expressions. Fig. 6 demonstrates the performance of each topology when each data point is optimized for different values of M. As each topology has a limited VCR range, the curves are not defined everywhere. The results highlight the importance of selecting the appropriate topology based on the VCR range of the application. Additionally, the curves show that there is no one-size-fits-all solution for HSCCs.

Regarding switch area (Fig. 6(a)), SP topologies are the worst in terms of switch utilization ($A_{NSP} > 1$ in most cases), as already known in SCC literature [19], though this analysis confirms this remains the case for HSCCs.

To analyze the fundamental factors influencing the performance of each topology, readers should delve into the

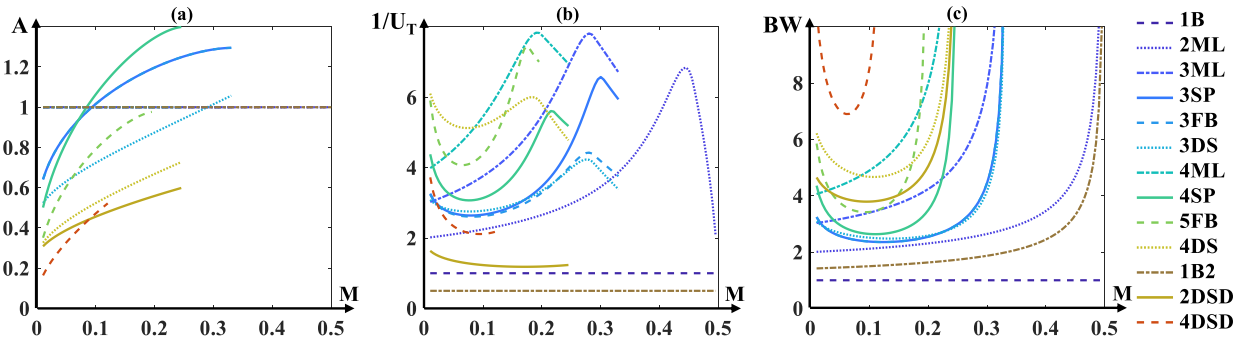

FIGURE 6. Topological benchmark when M varies (a) the total switch area A, (b) volume gain ($1/U_T$), and (c) the maximal cutoff frequency of the LC filter.

analytical equations governing key performance metrics such as A, U_T, and BW. For instance, the expression for total volume in (38) relies on a relatively small set of input and topological parameters. Assuming the flying capacitor is negligible, U_T is primarily proportional to L_k. In (21), L_k is directly proportional to the topological parameters d_k and l_k. This implies that topologies with the lowest d_k are better positioned for volume reduction. By scrutinizing the analytical equations, readers can infer trends simply by examining the topological variables. However, some topological variables are physically interconnected, making it challenging to achieve the lowest d_k simultaneously with other parameters. Nonetheless, a careful examination of the equations can inspire the creation of new HSCC topologies.

In Fig. 6(b), all the $1/U_T$ curves exhibit a maximum volume gain. HSCC topologies in general show a significant improvement in volume, with up to an 8× reduction, making them an attractive choice for applications where space is a critical factor. However, their performance varies depending on the value of M. For M values between 0.1 and 0.5, ML topologies are the best option, while for M values below 0.1, 4DS is the best option. Each volume reduction gain has a maximum point, just before their natural VCR (N). Beyond this point, the flying capacitor volume becomes dominant (to maintain out-resonance condition), and the inductor is reduced accordingly to minimize the overall volume (see Section III-I).

If the bandwidth is taken into consideration (Fig. 6(c)), 4DSD is dominant in the achievable VCR range. The four flying capacitor topologies (4ML, 5FB, and 4DS, excluding 4SP), provide advantageous bandwidth. Once again, significant bandwidth improvement can be achieved using HSCCs. The bandwidth curves exhibit an asymptotic behavior near their natural VCR (N) because, theoretically, no inductor is required at this ratio, as shown in (20) where $M = m_k$.

E. EFFECTS OF COMBINING VOLTAGE CONVERSION RATIOS AND SWITCH SCALING LAW

The input parameters α and β, which define the switch scaling law, also have a significant impact on the analytical equations. Since β behaves similarly to α, we have opted to focus on varying α in this study.

In Fig. 7, we present the best topology over the 2D input space $\{M, \alpha\}$ regarding silicon area (A), volume gain ($1/U_T$), and the required cutoff frequency of the output LC filter (BW). At a glance, there is no clear winner in all categories. For low α, i.e., low area penalty vs. blocking voltage, the baseline 1B or its sister, the two-phase 1B (1B2), are always the best topology. The result makes sense as one of the main arguments for introducing HSCCs is to reduce the blocking voltage across the switches to boost their performance. Above $\alpha = 1$ and for low M, 1B disappears in favor of various HSCC topologies. Concerning A, the DSD family is the best solution to reduce the silicon area occupied by the switches. To minimize the total volume U_T, 4DS is the best topology for extreme VCRs (e.g., M<0.15). For moderate VCRs, less flying capacitor topologies, such as 2ML or 3ML, are more suitable to minimize the overall volume. To maximize BW, reducing the constraint of the output capacitor value, 2-inductors architectures (1B2, 2DSD, 4DSD) are more suitable.

It is important to note that while the best topology is selected in this analysis, there may be cases where other topologies perform similarly. To illustrate this, Fig. 8(a) (blue case) shows the relative volume reduction of each topology compared to the best one selected over the range of α and M values, given in Table 6. For instance, 4DS achieves, in average, 90% of the volume reduction $1/U_{T,4DS}$ achieved by the best topology $1/U_{T,BT}$, and no lower than 80% in the worst case (blue case). Once again, 4ML and 4DS are the most effective topologies among the selected HSCCs for reducing the converter volume in average.

F. EFFECT OF BLOCKING VOLTAGE

In Section II-E, we have described two main choices to define the blocking voltage vector V_s, by considering i) the drain-source voltage experienced by each switch, or ii) the voltage across drain or source (DSV) referenced to the bulk voltage, namely the terminal voltage (TV) here. In Fig. 8(a), it is interesting to note that the choice of the blocking voltage vector can have a significant impact on the volume reduction achieved by the different topologies. Using the drain-source voltage (DSV) as a reference results in a higher volume reduction compared to using the terminal voltage (TV) as a

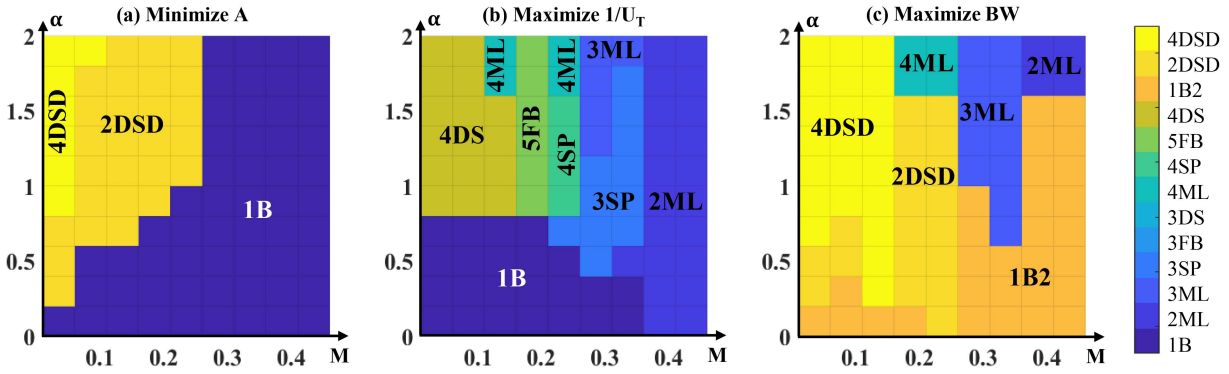

FIGURE 7. The best topology to (a) minimize the total switch area A, (b) minimize volume gain ($1/U_T$), and (c) maximize the cutoff filter frequency BW, when M and α varies.

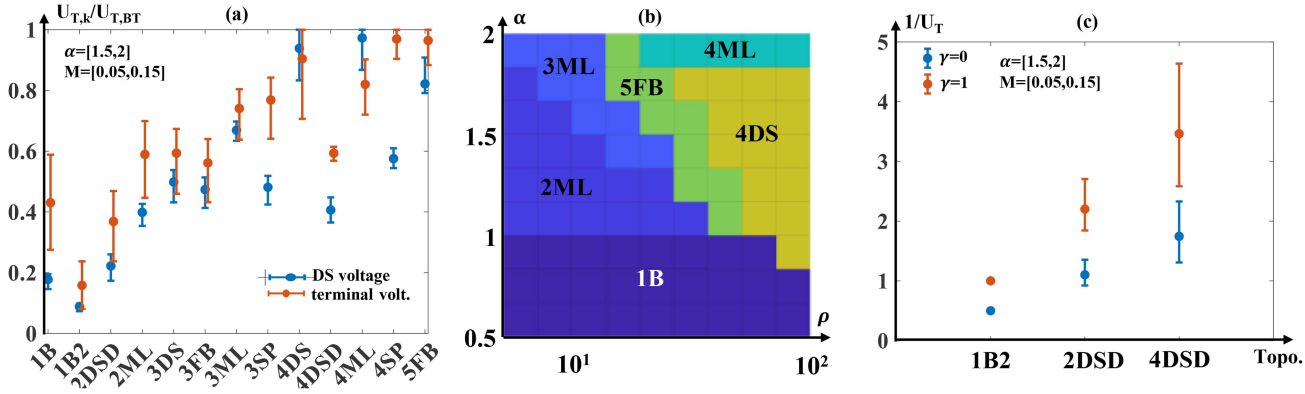

FIGURE 8. (a) The volume reduction range compared to the best topology over α and M ranges, (b) the most compact topologies for different α and ρ combination, and (c) volume reduction (compared to 1B) of the two-inductors topologies for two inductor scaling law (γ).

reference. The best topology achieves an 8x volume reduction with DSV and only 2x with TV ($U_{T,1B}/U_{T_{BT}}$). The 4DS topology maintains a significantly better volume reduction than 4ML when using the TV, but the 4SP and 5FB topologies outperform both of them. It is important to carefully consider the choice of the blocking voltage, which depends on the technology choice (discrete component, integrated circuit, transistor type), when designing HSCCs.

G. EFFECTS OF SWITCH SCALING AND RELATIVE VOLUMETRIC DENSITY

The primary reasons for the superiority of HSCCs lie in the limitations of passive components, namely the relatively low energy density of inductors compared to capacitors (referred to as ρ) and active devices, which are negatively impacted by blocking voltage, as evidenced by high α and β values in this context [15], [18]. However, with recent advancements in inductor [76], [77], [78] and switch integration [71], [79], it is uncertain whether HSCCs will remain relevant, especially in light of progress in high-voltage switches using, for example, III-V materials. Fig. 8(b) illustrates that the HSCC topology's advantages are most pronounced in the upper-right corner of the plot, where the relative volumetric density and voltage penalty in the switch size are high. In this region, 4ML and 4DS are the most effective topologies, but as ρ decreases, the number of flying capacitors required also decreases, and topologies with fewer flying capacitors, such as 2ML, become more desirable. Conversely, in the lower-left corner of the plot, where the voltage penalty is low and the inductor density is high, the HSCC topology is no longer advantageous, and 1B becomes the optimal choice.

H. INDUCTOR SCALING EFFECTS

The performance of topologies with two inductors is heavily influenced by the value of the γ parameter, which takes on a value of 1 when the inductor volume is dependent on stored energy and 0 when the inductor volume is also determined by the DCR, as is the case for high-current applications. Fig. 8(c) depicts the reduction in volume, as represented by $1/U_T$, for these two assumptions across reasonable ranges of α and M, given in Table 6. When $\gamma = 0$, the 2-phase 1B topology (1B2) does not add to the volume cost but does increase the bandwidth. Topologies like 2DSD and 4DSD have a much greater capability to reduce volume if the inductor volume is limited only by stored energy, but this reduction is still less than that of topologies like 4DS and 4ML.

V. DENORMALIZATION PROCEDURE

To validate the benchmark HSCC topologies under denormalized conditions, we introduce here the denormalization procedure. The normalized input variables remain consistent with those described earlier in Section IV-B, except for δ, which is set to 0.15.

A. DENORMALIZATION INPUT VARIABLES

Some dimensional input variables have to be defined:

- the input voltage $\widetilde{V_i}$ (10 V),
- the output current $\widetilde{I_o}$ (1 A),
- the switching frequency of the baseline topology 1B ($\widetilde{F_{1B}}$ = 1 MHz),
- the relative output voltage ripple, targeted to be lower than 1%,
- the power efficiency (95%),
- a Silicon technology, with a 1.2 μ m length transistor supporting 10 V with a sheet resistance of $\lambda_R = 3.3\,k\Omega \cdot \mu m$, sheet gate charge $\lambda_Q = 12fC/\mu m$ and a voltage drive swing of 5 V, with lower-voltage transistors scaling as defined by the normalized inputs ($\alpha = 2$, $\beta = 0$).

B. DIMENSIONAL VALUES FOR THE BASELINE TOPOLOGIES

By combining dimensionless and dimensional input values, the key design parameters of 1B can be expressed as:

- The output voltage $\widetilde{V_o} = M\widetilde{V_i} = 1$ V.
- The inductor current ripple $\widetilde{\Delta I_L} = \delta\widetilde{I_o} = 0.15$ A.
- The closed standard inductor value to maintain the current ripple at the VCR:

$$\widetilde{L_{1B}} = \frac{M(1-M)}{\widetilde{F_{1B}}\delta\widetilde{I_o}} \approx 6.8\mu H \tag{41}$$

- The equivalent output resistance $\widetilde{R_o} = 26.3$ mΩ by estimating the converter efficiency η by its conduction efficiency and splitting equally the loss contribution between the DCR and the converter impedance $\widetilde{DCR} = \widetilde{R_o}$:

$$\eta = \frac{\widetilde{P_{o,1B}}}{\widetilde{P_{o,1B}} + \widetilde{P_{loss,1B}}} = \frac{\widetilde{R_L}}{\widetilde{R_L} + \widetilde{R_o} + \widetilde{DCR}} \tag{42}$$

- Considering the distribution of on-state resistance to obtain the minimal Silicon area from the (9), the on-state resistances of the transistors are $\widetilde{R_{on,S_{0a}}} = 2.5\widetilde{R_o} = 65.7$ mΩ and $\widetilde{R_{on,S_{0b}}} = 0.83\widetilde{R_o} = 21.8$ mΩ.
- Using the sheet resistance of 10 V transistors λ_R and their length (1.2 μm), the Silicon area is deduced: $\widetilde{A_{1B}} = 1.2\,mm^2$.
- From (4) and the sheet gate charge λ_Q, the total driving loss is found: $\sum \widetilde{E_{dr,S_i}} = \sum \lambda_Q W_i V_{gs} = 21$nJ.
- By introducing the driving loss, neglected in the first approximation earlier, in the efficiency calculation, η could be found 92.7% is close to the targeted efficiency.
- The closed standard output capacitor value $\widetilde{C_{o,1B}}$ can be deduced from:

$$\widetilde{C_{o,1B}} = \frac{1-M}{8\widetilde{L_{1B}}\widetilde{C_{o,1B}}\widetilde{F_{1B}}^2} \approx 1.5\mu F \tag{43}$$

As no flying capacitor is present in 1B, the denormalization procedure to find $\widetilde{C_{F,k}}$ is based on the flying capacitor of 2ML. Hence, the 2 M topology can also be considered as a baseline topology. As the modelization is valid far above the resonance, we can define the value considering the resonant frequency if the LC network formed by $\widetilde{C_{F,2ML}}$ and $\widetilde{L_{2ML}}$ and the switching frequency $\widetilde{F_{2ML}}$:

$$\widetilde{C_{F,2ML}} = \frac{K_F^2}{4\pi^2\widetilde{L_{2ML}}\widetilde{F_{2ML}}} = 0.84\mu F \tag{44}$$

where $\widetilde{L_{2ML}} = L_{2ML}\widetilde{L_{1B}}$ and $\widetilde{F_{2ML}} = F_{2ML}\widetilde{F_{1B}}$ by definition.

To maintain the small-signal assumption for the flying capacitor voltage, the flying capacitor is augmented to $\widetilde{C'_{F,2ML}} = 4.7\mu$F, ensuring that the flying capacitor ripple remains below 0.2 V. Noticed that $\widetilde{C_{F,2ML}}$ remains the value for denormalizing other topologies: $\widetilde{C_{F,k}} = C_{F,k}\widetilde{C_{F,2ML}}$.

C. DENORMALIZATION PROCEDURE FOR OTHER TOPOLOGIES

The dimensional values of topology k are derived from the dimensional values of $1B$ (and $2ML$ for C_F) provided in Section V-B and the dimensionless values resulting from the framework, as exemplified in Section IV-B. For instance, the inductor value is calculated as follows: $\widetilde{L_k} = L_k \times \widetilde{L_{1B}}$.

D. PASSIVE SELECTION

We have chosen real passive components for $\widetilde{L_k}$, $\widetilde{C_{F,k}}$, and $\widetilde{C_{o,k}}$ from an industrial passive database (TDK). For $\widetilde{L_k}$, we selected the smallest volume for a given inductor value while respecting the targeted DCR (here 26 mΩ, for single-inductor case) and the saturation current I_{SAT} (at least I_o/l). We also check the DCR value at the switching frequency ($\widetilde{F_k}$) are similar in all topology, and the self-resonance frequency of the selected inductors is higher than the operating frequency. Notably, we observed that the primary constraint dictating the volume is the DCR value, not I_{SAT}, affirming our hypothesis ($\gamma = 0$) by default (Section III-G). Concerning the capacitors, we also checked their self-resonant frequency to ensure all operate in the capacitive behaviour.

E. COMPARISON OF DENORMALIZED APPROACH AND NORMALIZED APPROACH

Table 7 provides all denormalized values for four topologies where the efficiency, voltage output ripple and inductor ripple are equal. By opting for real passive components, we confirm the volume scaling-down benefit $1/U_T$ of 4DS by a factor of 5. 2ML and 4DSD also exhibit a good ability to reduce the volume of the converter by a factor of 2. Some differences are observed between the results given by the framework and the

TABLE 7. Denormalized Volumes of Some Screened Topologies

	Unit	1B	2ML	4DS	4DSD
$\widetilde{A}$	mm^2	1.2	1.2	0.62	0.56
$\widetilde{F_{sw}}$	MHz	1	1.3	1.9	1.4
$\widetilde{L}$	µH	6.8	3	1.2	2x3.3
Ref.	Coilcraft	XGL5030	XGL4025	XGL3515	XGL3520
$\widetilde{U_L}$	mm^3	89.7	40	16.3	32.6
$\widetilde{C_F}$	µF	-	4.7	3x4.7	2x4.7
Ref.	TDK	-	C1005		
$\widetilde{U_{C_F}}$	mm^3	0	0.25	0.75	0.5
$\widetilde{C_o}$	µF	1.5	0.68	0.47	0.047
Ref.	TDK	C1608		C0510	
$\widetilde{U_{C_o}}$	mm^3	1.02	1.02	0.16	0.16
$\widetilde{U_T}$	mm^3	90.7	41.3	17.2	33.3
$1/U_T$	(denorm.)	1	2.2	5.1	2.7
$1/U_T$	(model)	1	2.2	5.3	2.1

denormalized procedure. This is primarily explained by TDK offering inductor families with a discrete choice of L/DCR couples that do not precisely match the desired values. For 4DSD, the denormalization procedure leads to a significant disparity between the required inductor of 3.1 μH and the closest available value in the TDK portfolio. In all cases, the desired *DCR* does not always fit perfectly, and the closest available value is selected, introducing additional constraints on the inductor. Again, the objective of the framework is not to provide exact values but to offer a useful tool to draw trends encompassing all constraints together.

VI. DISCUSSION

This paper introduces a comparative framework that evaluates different soft-charging hybrid switched-capacitor (HSCC) topologies by considering various constraints, including equal power loss and equal ripples. Building upon our previous work [57], this framework specifically focuses on non-resonant direct HSCC topologies due to their distinct loss mechanisms, excluding resonant HSCC configurations. The framework establishes correlations among intrinsic switch stress, passive volume, and topological parameters to derive an optimal set of design parameters, such as switching frequency and Silicon area. For instance, higher switch penalties (higher α) necessitate adjustments in the optimal design parameters, such as reducing the switching frequency to accommodate switch losses and increasing the inductor value to maintain consistent inductor ripple. This example elucidates how switches impact passive size in the overall design. While previous works have argued that the Dickson topology is superior due to its better active utilization, this study shows that when considering additional constraints and including splitting states in the sizing process, the Dickson topology's advantage is reduced, particularly when compared to multi-level topologies. The two-inductors topologies are also valuable for improving the bandwidth, and in certain conditions, for reducing the converter volume significantly.

To enable readers to investigate additional aspects or expand the benchmarking to new topologies, we offer the MATLAB-based source code for exploration [66].

It should be noted that the analysis assumes an ideal sizing process with access to the best specific resistance for each voltage rating, which may not be available in practice. The off-the-shelf components or Silicon integrated technology may not offer such vast voltage-rating options, limiting the potential of topologies with various values in the voltage vector. Furthermore, the switch scaling law coefficients significantly influence the conclusions, giving more space for low count flying capacitor topologies when the penality is reduced.

While the comparison framework formalizes various design aspects, it's essential to acknowledge that practical converter designs require consideration of additional factors. These factors encompass a broad range of elements, including but not limited to, the voltage conversion ratio (VCR) range, startup procedures, gate driving techniques [80], level shifting methodologies, capacitor charge balancing strategies [33], [50], [51], feedback control mechanisms [47], [63], PCB routing, methods for inductor current balancing [58], specifications of input capacitors [64], [81], and considerations for electromagnetic interference (EMI) [29]. Although the losses associated with drain and source capacitances are not explicitly addressed in the paper, they can be factored into the overall switching losses. As such, designers must evaluate all relevant factors with weighted coefficients tailored to their specific application when selecting a final topology. Additionally, it's worth noting that coupling inductors in multi-phase topologies can further improve power density with a specific inductor sizing procedure [82].

VII. CONCLUSION

This paper presents a comprehensive framework for the comparison of non-resonant hybrid switched-capacitor converters. By enabling the adjustment of design parameters such as switch area and frequency, the framework establishes a connection between the active and passive performance of each topology. This allows for the determination of the potential reduction in total volume and the increase in bandwidth while maintaining the same efficiency and ripples as a conventional 2-level buck converter. The framework is accompanied by practical guidelines for its utilization and provides access to available code [66]. It serves as a valuable tool for designers, assisting them in their decision-making process and facilitating the evaluation of the performance of newly proposed topologies.

APPENDIX A
LIST OF ASSUMPTIONS

In addition to the assumptions detailed in Section II-A, several assumptions are introduced throughout the paper for the sake of clarity. The following list provides a comprehensive summary of these additional assumptions:

1) The input decoupling capacitor is assumed to be sufficiently large, allowing the input to be considered ideal voltage source, as commonly done in existing models.
2) The switching frequency F is far above the self resonant formed by the output filter $\{L, C_o\}$ and the flying capacitors networks $\{L, C_F\}$.
3) In line with prior research, for instance, [19], [55], [61], we make the assumption that the voltage ripple across the flying capacitors is relatively small. This assumption is made to minimize the impact of voltage ripple on the stress experienced by the switches. The framework, designed primarily for small-signal analysis, has the potential for extension to large-signal analysis, a path outlined in [43]. The voltage ripple is indirectly fixed by the "far above resonant" condition, rather than aiming for equal voltage ripple across all capacitors in any topology. While this choice results in similar outcomes, it is justified for obtaining a total volume that can be normalized. It's crucial to note that this assumption may lead to undersizing of switches compared to scenarios with high ripple.
4) While (1) considers non-zero inductor current ripple when determining loss, the derivations of all equations assume that the inductor current ripple is small enough to be approximated as DC in the inductor current. However, this assumption does not apply to the inductor current ripple, which is considered non-negligible for calculating the inductor loss, as indicated by the parameters δ.
5) The overall volume of the converter is calculated by summing the volumes of flying capacitors and inductors. While the volume of the switches of the power stage is excluded, the volume of the flying capacitors is considered a significant factor in optimizing the overall volume of the converter, as described in Section III-H.
6) For conciseness, the inductor volume is assessed using two different scaling laws based on observed performance trends in commercially available inductors (Section III-G). Our evaluation does not consider effects such as saturation, hysteresis, or core losses concerning frequency. Additionally, the switching frequency for each topology is kept within the same order of magnitude (F varies up to 2x), minimizing the need to account for frequency dependence of DCR.
7) We solely focus on planar switches, where the switch areas scale proportionally with their on-state resistances. Vertical structures are beyond the scope of this study, as accounting for Silicon volume is necessary to calculate the on-state value.

These assumptions are applied uniformly to all topologies. Since the benchmark aims to compare topologies by normalizing them to a common baseline, certain assumptions have limited effects, affecting all topologies to a similar extent.

All these assumptions have been established to derive manageable analytical equations, avoiding the necessity for numerical solving, and relying solely on the inherent characteristics of the topology, including the number of states and phases, current flow vectors, and voltage stress in each switch.

REFERENCES

[1] Y. Guan, C. Cecati, J. M. Alonso, and Z. Zhang, "Review of high-frequency high-voltage-conversion-ratio DC-DC converters," *IEEE J. Emerg. Sel. Topics Ind. Electron.*, vol. 2, no. 4, pp. 374–389, Oct. 2021.

[2] K. Kesarwani and J. T. Stauth, "Resonant and multi-mode operation of flying capacitor multi-level DC-DC converters," in *Proc. IEEE 16th Workshop Control Model. Power Electron.*, 2015, pp. 1–8.

[3] J. D. Boles, J. E. Bonavia, J. H. Lang, and D. J. Perreault, "A piezoelectric-resonator-based DC-DC converter demonstrating 1 kW/cm^3 resonator power density," *IEEE Trans. Power Electron.*, vol. 38, no. 3, pp. 2811–2815, Mar. 2023.

[4] L. d. A. Pereira, A. Morel, M. Touhami, T. Lamorelle, G. Despesse, and G. Pillonnet, "Operating frequency prediction of piezoelectric DC-DC converters," *IEEE Trans. Power Electron.*, vol. 37, no. 3, pp. 2508–2512, Mar. 2022.

[5] W.-C. B. Liu and P. P. Mercier, "A series/parallel magnetic-less step-down converter based on piezoelectric resonators," in *Proc. IEEE Appl. Power Electron. Conf. Expo.*, 2023, pp. 484–489.

[6] S. Ghandour, G. Despesse, and S. Basrour, "Design of a new MEMS DC/DC voltage step-down converter," in *Proc. 8th IEEE Int. NEWCAS Conf.* 2010, pp. 105–108.

[7] E. Perez, C. A. Berlitz, Y. Moursy, B. Allard, S. Oukassi, and G. Pillonnet, "Ultra-low frequency DC-DC converters using switched batteries," in *Proc. IEEE Energy Convers. Congr. Expo.*, 2022, pp. 1–7.

[8] C. Hardy et al., "11.1 A scalable heterogeneous integrated two-stage vertical power-delivery architecture for high-performance computing," in *Proc. IEEE Int. Solid- State Circuits Conf.*, 2023, pp. 182–184.

[9] E. Perez, Y. Moursy, S. Oukassi, and G. Pillonnet, "Silicon capacitors opportunities for switched capacitor converter," in *Proc. IEEE 23rd Workshop Control Model. Power Electron.*, 2022, pp. 1–6.

[10] R. D. Middlebrook, "Transformerless DC-to-DC converters with large conversion ratios," *IEEE Trans. Power Electron.*, vol. 3, no. 4, pp. 484–488, Oct. 1988.

[11] T. A. Meynard and H. Foch, "Multi-level conversion: High voltage choppers and voltage-source inverters," in *Proc. 23rd Annu. IEEE Power Electron. Specialists Conf.*, 1992, pp. 397–403.

[12] K. Nishijima, K. Harada, T. Nakano, T. Nabeshima, and T. Sato, "Analysis of double step-down two-phase buck converter for VRM," in *Proc. 27th Int. Telecommun. Conf.*, 2005, pp. 497–502. [Online]. Available: https://ieeexplore.ieee.org/document/4134388/

[13] R. C. N. Pilawa-Podgurski, D. M. Giuliano, and D. J. Perreault, "Merged two-stage power converterarchitecture with softcharging switched-capacitor energy transfer," in *Proc. IEEE Power Electron. Specialists Conf.*, 2008, pp. 4008–4015.

[14] V. Yousefzadeh, E. Alarcon, and D. Maksimovic, "Three-level buck converter for envelope tracking applications," *IEEE Trans. Power Electron.*, vol. 21, no. 2, pp. 549–552, Mar. 2006. [Online]. Available: https://ieeexplore.ieee.org/document/1603688/

[15] D. J. Perreault et al., "Opportunities and challenges in very high frequency power conversion," in *Proc. 24th Annu. IEEE Appl. Power Electron. Conf. Expo.*, 2009, pp. 1–14.

[16] B. J. Baliga, "Power semiconductor device figure of merit for high-frequency applications," *IEEE Electron Device Lett.*, vol. 10, no. 10, pp. 455–457, Oct. 1989.

[17] J. T. Stauth, "Pathways to mm-scale DC-DC converters: Trends, opportunities, and limitations," in *Proc. IEEE Custom Integr. Circuits Conf.*, 2018, pp. 1–8.

[18] W. C. Liu, Z. Ye, and R. C. Pilawa-Podgurski, "A 97% peak efficiency and 308 A/in3 current density 48-to-4 V two-stage resonant switched-capacitor converter for data center applications," in *Proc. IEEE Appl. Power Electron. Conf. Expo.*, 2020, pp. 468–474.

[19] M. D. Seeman and S. R. Sanders, "Analysis and optimization of switched-capacitor DC-DC converters," *IEEE Trans. Power Electron.*, vol. 23, no. 2, pp. 841–851, Mar. 2008.

[20] Y. Lei and R. C. N. Pilawa-Podgurski, "Soft-charging operation of switched-capacitor DC-DC converters with an inductive load," in *Proc. IEEE Appl. Power Electron. Conf. Expo.*, 2014, pp. 2112–2119.

[21] P. Assem, W.-C. Liu, Y. Lei, P. K. Hanumolu, and R. C. N. Pilawa-Podgurski, "Hybrid Dickson switched-capacitor converter with wide conversion ratio in 65-nm CMOS," *IEEE J. Solid-State Circuits*, vol. 55, no. 9, pp. 2513–2528, Sep. 2020.

[22] Y. Yamauchi, T. Sai, K. Hata, and M. Takamiya, "0.55 W, 88%, 78 kHz, 48 V-to-5 V Fibonacci hybrid DC-DC converter IC using 66 mm3 of passive components with automatic change of converter topology and duty ratio for cold-crank transient," *IEEE Trans. Power Electron.*, vol. 36, no. 8, pp. 9273–9284, Aug. 2021.

[23] A. Abdulslam and P. P. Mercier, "A symmetric modified multilevel ladder PMIC for battery-connected applications," *IEEE J. Solid-State Circuits*, vol. 55, no. 3, pp. 767–780, Mar. 2020.

[24] Z. Ye, Y. Lei, W.-C. Liu, P. S. Shenoy, and R. C. N. Pilawa-Podgurski, "Design and implementation of a low-cost and compact floating gate drive power circuit for GaN-based flying capacitor multi-level converters," in *Proc. IEEE Appl. Power Electron. Conf. Expo.*, 2017, pp. 2925–2931.

[25] Y. Lei and R. C. Pilawa-Podgurski, "Analysis of switched-capacitor DC-DC converters in soft-charging operation," in *Proc. IEEE 14th Workshop Control Model. Power Electron.*, 2013, pp. 1–7.

[26] Z. Ye, Y. Lei, and R. C. N. Pilawa-Podgurski, "The cascaded resonant converter: A hybrid switched-capacitor topology with high power density and efficiency," *IEEE Trans. Power Electron.*, vol. 35, no. 5, pp. 4946–4958, May 2020.

[27] R. Das, G.-S. Seo, and H.-P. Le, "Analysis of dual-inductor hybrid converters for extreme conversion ratios," *IEEE Trans. Emerg. Sel. Topics Power Electron.*, vol. 9, no. 5, pp. 5249–5260, Oct. 2021.

[28] Z. Ye, R. A. Abramson, Y.-L. Syu, and R. C. N. Pilawa-Podgurski, "MLB-PoL: A high performance hybrid converter for direct 48 v to point-of-load applications," in *Proc. IEEE 21st Workshop Control Model. Power Electron.*, 2020, pp. 1–8.

[29] C. Hardy, Y. Ramadass, K. Scoones, and H.-P. Le, "A flying-inductor hybrid DC-DC converter for 1-cell and 2-cell smart-cable battery chargers," *IEEE J. Solid-State Circuits*, vol. 54, no. 12, pp. 3292–3305, Dec. 2019.

[30] G.-S. Seo and H.-P. Le, "S-hybrid step-down DC-DC converter—Analysis of operation and design considerations," *IEEE Trans. Ind. Electron.*, vol. 67, no. 1, pp. 265–275, Jan. 2020.

[31] C. Hardy and H.-P. Le, "11.5 A 21 W 94.8%-Efficient reconfigurable single-inductor multi-stage hybrid DC-DC converter," in *Proc. IEEE Int. Solid- State Circuits Conf.*, 2023, pp. 190–192.

[32] J. Huang, C.-S. Lam, Y. Lu, and R. P. Martins, "A symmetrical double step-down converter with extended voltage conversion ratio," *IEEE Trans. Circuits Syst. I: Regular Papers*, vol. 69, no. 12, pp. 4761–4773, Dec. 2022.

[33] C. Wang, Y. Lu, and R. P. Martins, "A highly integrated tri-path hybrid buck converter with reduced inductor current and self-balanced flying capacitor voltage," *IEEE Trans. Circuits Syst. I: Regular Papers*, vol. 69, no. 9, pp. 3841–3850, Sep. 2022.

[34] T. Hu, M. Huang, Y. Lu, and R. P. Martins, "A 4 A 12-to-1 flying capacitor cross-connected DC-DC converter with inserted D>0.5 control achieving >2x transient inductor current slew rate and 0.73× theoretical minimum output undershoot of DSD," in *Proc. IEEE Int. Solid-State Circuits Conf.*, 2022, pp. 1–3.

[35] K. Hata, S. Tanaka, Y. Rikiishi, and T. Matsumoto, "48 V-to-12 V always-dual-path hybrid DC-DC converter for inductor current reduction," in *Proc. IEEE Energy Convers. Congr. Expo.*, 2022, pp. 1–6.

[36] K. Hata, Y. Yamauchi, T. Sai, T. Sakurai, and M. Takamiya, "48V-to-12 V dual-path hybrid DC-DC converter," in *Proc. IEEE Appl. Power Electron. Conf. Expo.*, 2020, pp. 2279–2284.

[37] Y. Huh, S.-W. Hong, and G.-H. Cho, "A hybrid structure dual-path step-down converter with 96.2% peak efficiency using 250-m Ω Large-DCR inductor," *IEEE J. Solid-State Circuits*, vol. 54, no. 4, pp. 959–967, Apr. 2019.

[38] Y. Li, M. John, Y. Ramadass, and S. R. Sanders, "AC-Coupled stacked dual-active-bridge DC-DC converter for integrated lithium-ion battery power delivery," *IEEE J. Solid-State Circuits*, vol. 54, no. 3, pp. 733–744, Mar. 2019.

[39] S. Pasternak, C. Schaef, and J. Stauth, "Equivalent resistance approach to optimization, analysis and comparison of hybrid/resonant switched-capacitor converters," in *Proc. IEEE 17th Workshop Control Model. Power Electron.*, 2016, pp. 1–8.

[40] K. Kesarwani, R. Sangwan, and J. T. Stauth, "Resonant-switched capacitor converters for chip-scale power delivery: Design and implementation," *IEEE Trans. Power Electron.*, vol. 30, no. 12, pp. 6966–6977, Dec. 2015.

[41] N. C. Brooks, S. Coday, M. E. Blackwell, R. A. Abramson, N. M. Ellis, and R. C. N. Pilawa-Podgurski, "Operation of flying capacitor multilevel converters at and above resonance," in *Proc. IEEE 23rd Workshop Control Model. Power Electron.*, 2022, pp. 1–7.

[42] T. Urkin, G. Sovik, E. E. Masandilov, and M. M. Peretz, "Digital zero-current switching lock-in controller IC for optimized operation of resonant SCC," *IEEE Trans. Power Electron.*, vol. 36, no. 5, pp. 5985–5996, May 2021.

[43] N. M. Ellis, N. C. Brooks, M. E. Blackwell, R. A. Abramson, S. Coday, and R. C. N. Pilawa-Podgurski, "A general analysis of resonant switched capacitor converters using peak energy storage and switch stress including ripple," *IEEE Trans. Power Electron.*, early access, Jun. 21, 2023, doi: 10.1109/TPEL.2023.3285745.

[44] P.-L. Wong, P. Xu, P. Yang, and F. C. Lee, "Performance improvements of interleaving VRMs with coupling inductors," *IEEE Trans. Power Electron.*, vol. 16, no. 4, pp. 499–507, Jul. 2001.

[45] F. Zhu, X. Lou, and Q. Li, "An improved hybrid-coupled inductor structure with flux reduction and integrated controllable coupling function," *IEEE Trans. Power Electron.*, vol. 39, no. 1, pp. 1103–1114, Jan. 2024.

[46] J. Baek, Y. Elasser, and M. Chen, "MIPS: Multiphase integrated planar symmetric coupled inductor for ultrathin VRM," *IEEE Trans. Power Electron.*, vol. 38, no. 5, pp. 5609–5614, May 2023.

[47] J.-I. Seo, B.-M. Lim, W.-J. Choi, Y.-S. Noh, and S.-G. Lee, "A 95.1% efficiency hybrid hysteretic reconfigurable 3-Level buck converter with improved load transient response," *IEEE Trans. Power Electron.*, vol. 37, no. 12, pp. 14916–14925, Dec. 2022.

[48] H. A. Zadeh, H. R. Kooshkaki, K.-Y. Lee, and P. P. Mercier, "An adaptive constant-on-time-controlled hybrid multilevel DC-DC converter operating from Li-ion battery voltages with low spurious output," *IEEE Trans. Power Electron.*, vol. 38, no. 5, pp. 5763–5776, May 2023.

[49] C. Schaef et al., "8.1 A 93.8% peak efficiency, 5V-Input, 10 A max ILOAD flying capacitor multilevel converter in 22 nm CMOS featuring wide output voltage range and flying capacitor precharging," in *Proc. IEEE Int. Solid- State Circuits Conf.*, 2019, pp. 146–148.

[50] C. Wang, Y. Lu, X. Li, and R. P. Martins, "A dual-branch series-parallel hybrid buck DC-DC converter with flying capacitor voltage auto-balancing," *IEEE Trans. Circuits Syst. I: Regular Papers*, vol. 69, no. 12, pp. 4741–4750, Dec. 2022.

[51] J. S. Rentmeister and J. T. Stauth, "A 92.4% efficient, 5.5 V:0.4-1.2 V, FCML converter with modified ripple injection control for fast transient response and capacitor balancing," in *Proc. IEEE Custom Integr. Circuits Conf.*, 2020, pp. 1–4.

[52] Z. Xia and J. T. Stauth, "A cascaded hybrid switched-capacitor DC-DC converter capable of fast self startup for USB power delivery," *IEEE J. Solid-State Circuits*, vol. 57, no. 6, pp. 1854–1864, Jun. 2022.

[53] W.-C. Liu, P. Assem, Y. Lei, P. K. Hanumolu, and R. Pilawa-Podgurski, "10.3 A 94.2%-peak-efficiency 1.53 A direct-battery-hook-up hybrid Dickson switched-capacitor DC-DC converter with wide continuous conversion ratio in 65 nm CMOS," in *Proc. IEEE Int. Solid-State Circuits Conf.*, 2017, pp. 182–183.

[54] K. Wei, Y. Ramadass, and D. B. Ma, "Direct 12 V/24V-to-1 V tri-state double step-down power converter with online V_{cf} rebalancing and in-situ precharge rate regulation," *IEEE J. Solid-State Circuits*, vol. 56, no. 8, pp. 2416–2426, Aug. 2021. [Online]. Available: https://ieeexplore.ieee.org/document/9350602/

[55] Z. Ye, S. R. Sanders, and R. C. N. Pilawa-Podgurski, "Modeling and comparison of passive component volume of hybrid resonant switched-capacitor converters," *IEEE Trans. Power Electron.*, vol. 37, no. 9, pp. 10903–10919, Sep. 2022.

[56] H.-P. Le, S. R. Sanders, and E. Alon, "Design techniques for fully integrated switched-capacitor DC-DC converters," *IEEE J. Solid-State Circuits*, vol. 46, no. 9, pp. 2120–2131, Sep. 2011.

[57] G. Pillonnet, M. H. Hmada, and P. P. Mercier, "Normalized benchmarking of hybrid switched-capacitor DC-DC converters," in *Proc. IEEE 24th Workshop Control Model. Power Electron.*, 2023, pp. 1–8.

[58] J.-H. Cho et al., "A fully integrated multi-phase buck converter with on-chip capacitor dynamic re-allocation and fine-grained phase-shedding techniques," *IEEE J. Solid-State Circuits*, vol. 57, no. 12, pp. 3840–3852, Dec. 2022.

[59] R. C. N. Pilawa-Podgurski and D. J. Perreault, "Merged two-stage power converter with soft charging switched-capacitor stage in 180 nm CMOS," *IEEE J. Solid-State Circuits*, vol. 47, no. 7, pp. 1557–1567, Jul. 2012.
[60] Y. Lei, R. May, and R. Pilawa-Podgurski, "Split-phase control: Achieving complete soft-charging operation of a Dickson switched-capacitor converter," *IEEE Trans. Power Electron.*, vol. 31, no. 1, pp. 770–782, Jan. 2016.
[61] W. C. Liu, Z. Ye, and R. C. N. Pilawa-Podgurski, "Comparative analysis on minimum output impedance of fixed-ratio hybrid switched capacitor converters," in *Proc. 20th Workshop Control Model. Power Electron.*, 2019, pp. 1–7.
[62] W. Jung et al., "Dual-path three-level buck converter with loop-free autocalibration for flying capacitor self-balancing," *IEEE Trans. Power Electron.*, vol. 36, no. 1, pp. 51–55, Jan. 2021.
[63] S. Pan and P. K. T. Mok, "A 25 MHz fast transient adaptive-on/off-time controlled three-level buck converter," *IEEE Trans. Circuits Syst. I: Regular Papers*, vol. 69, no. 6, pp. 2601–2613, Jun. 2022.
[64] Y. Zhu, Z. Ye, and R. C. N. Pilawa-Podgurski, "Modeling and analysis of switched-capacitor converters with finite terminal capacitances," in *Proc. IEEE Appl. Power Electron. Conf. Expo.*, 2021, pp. 178–185.
[65] Y. Lei and R. C. N. Pilawa-Podgurski, "A general method for analyzing resonant and soft-charging operation of switched-capacitor converters," *IEEE Trans. Power Electron.*, vol. 30, no. 10, pp. 5650–5664, Oct. 2015.
[66] "The source files required to execute the benchmarking outlined in this paper," Jan. 2024. [Online]. Available: https://github.com/patmercier/DCDC
[67] S. S. Amin and P. P. Mercier, "A fully integrated Li-ion-compatible hybrid four-level DC-DC converter in 28-nm FDSOI," *IEEE J. Solid-State Circuits*, vol. 54, no. 3, pp. 720–732, Mar. 2019.
[68] W. Kim, D. Brooks, and G.-Y. Wei, "A fully-integrated 3-level DC-DC converter for nanosecond-scale DVFS," *IEEE J. Solid-State Circuits*, vol. 47, no. 1, pp. 206–219, Jan. 2012.
[69] R. W. Erickson and D. Maksimović, *Fundamentals of Power Electronics*. New York, NY, USA: Springer, 2001.
[70] P. S. Shenoy et al., "A 5 MHz, 12 V, 10 A, monolithically integrated two-phase series capacitor buck converter," in *Proc. IEEE Appl. Power Electron. Conf. Expo.*, 2016, pp. 66–72.
[71] D. Yan, X. Ke, and D. B. Ma, "Direct 48-/1-V GaN-Based DC-DC power converter with double step-down architecture and master-slave AO ^{2} T control," *IEEE J. Solid-State Circuits*, vol. 55, no. 4, pp. 988–998, Apr. 2020.
[72] Y. Lei, W.-C. Liu, and R. C. N. Pilawa-Podgurski, "An analytical method to evaluate flying capacitor multilevel converters and hybrid switched-capacitor converters for large voltage conversion ratios," in *Proc. IEEE 16th Workshop Control Model. Power Electron.*, 2015, pp. 1–7.
[73] P. H. McLaughlin, J. S. Rentmeister, M. H. Kiani, and J. T. Stauth, "Analysis and comparison of hybrid-resonant switched-capacitor DC-DC converters with passive component size constraints," *IEEE Trans. Power Electron.*, vol. 36, no. 3, pp. 3111–3125, Mar. 2021.
[74] A. Mishra, W. Zhu, B. Wicht, and V. D. Smedt, "An All-1.8-V-Switch hybrid buck-boost converter for Li-battery-operated PMICs achieving 95.63% peak efficiency using a 288-m DCR inductor," *IEEE Trans. Power Electron.*, vol. 38, no. 3, pp. 3444–3454, Mar. 2023.
[75] V. Yousefzadeh, E. Alarcon, and D. Maksimovic, "Three-level buck converter for envelope tracking in RF power amplifiers," in *Proc. 20th Annu. IEEE Appl. Power Electron. Conf. Expo.*, 2005, pp. 1588–1594. [Online]. Available: https://ieeexplore.ieee.org/document/1453248/
[76] M. Sankarasubramanian et al., "Magnetic inductor arrays for Intel fully integrated voltage regulator (FIVR) on 10th generation Intel Core™ SoCs," in *Proc. IEEE 70th Electron. Compon. Technol. Conf.*, 2020, pp. 399–404.
[77] C. A. Barros et al., "Embedded inductors using composite magnetic materials for 12-1-V integrated voltage regulators," *IEEE Trans. Compon. Packag. Manuf. Technol.*, vol. 11, no. 12, pp. 2183–2192, Dec. 2021.
[78] T. Xie, J. Zhu, D. Maksimovic, and H.-P. Le, "A highly integrated hybrid DC-DC converter with nH-Scale IPD inductors," *IEEE J. Solid-State Circuits*, vol. 58, no. 3, pp. 705–719, Mar. 2023.
[79] Y. Lei et al., "A 2 kW, single-phase, 7-level, GaN inverter with an active energy buffer achieving 216 W/in3 power density and 97.6% peak efficiency," in *Proc. IEEE Appl. Power Electron. Conf. Expo.*, 2016, pp. 1512–1519.
[80] C. Schaef and J. T. Stauth, "A highly integrated series-parallel switched-capacitor converter with 12 V input and quasi-resonant voltage-mode regulation," *IEEE Trans. Emerg. Sel. Topics Power Electron.*, vol. 6, no. 2, pp. 456–464, Jun. 2018.
[81] S. Thielemans, A. Ruderman, B. Reznikov, and J. Melkebeek, "Improved natural balancing with modified phase-shifted PWM for single-leg five-level flying-capacitor converters," *IEEE Trans. Power Electron.*, vol. 27, no. 4, pp. 1658–1667, Apr. 2012.
[82] T. Ge, R. Abramson, Z. Ye, and R. C. N. Pilawa-Podgurski, "Core size scaling law of two-phase coupled inductors — Demonstration in a 48-to-1.8 V hybrid switched-capacitor MLB-PoL converter," in *Proc. IEEE Appl. Power Electron. Conf. Expo.*, 2022, pp. 1500–1505.

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