

Three-Phase Four-Wire Step-Down Modular Converter for an Enhanced Interlinking in Low-Voltage Hybrid AC/DC Microgrids

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ABSTRACT This article proposes a three-phase four-wire bidirectional topology that serves as an interlinking converter for hybrid AC/DC microgrids, featuring a single-stage power conversion. The proposed converter configuration comprises three four-switch buck-boost modules connected in a star configuration, with the AC microgrid neutral directly linked to the positive terminal of the DC microgrid. The inclusion of the neutral wire facilitates islanded operation of the hybrid microgrid, ensuring a stable power supply for both single-phase and three-phase AC loads. Moreover, the direct connection between the AC microgrid neutral and the positive terminal of the DC microgrid allows for the grounding of both microgrids, a capability that was previously achievable only with isolated topologies. Additionally, the four-wire converters exhibit the ability to control positive, negative, and zero sequence components, providing flexible control during AC voltage imbalances to mitigate their effects and ensure optimal operation. Furthermore, the converter enables independent control of the three phases, facilitating fault-tolerant operation demonstrated in this article under single-phase faults. The performance of the converter is assessed through experimental tests conducted on a 7kW prototype. This prototype has been tested under various operating conditions, including balanced and unbalanced AC voltages, single-module disconnection, and islanded operation.

INDEX TERMS AC-DC power conversion, Four-wire converters, Hybrid microgrid, Three-phase modular converters, Three-phase rectifiers.

I. INTRODUCTION

The growing utilization of renewable energy sources (RES), energy storage systems (ESS), and electric vehicle charging stations is fueling the requirement for traditional power systems to adapt and handle larger capacities and loads. To effectively integrate distributed energy generation and meet local demand, one possible solution is the adoption of microgrids (MGs) instead of solely relying on conventional utility grids with centralized generation [1], [2], [3]. While AC MGs have the advantage of compatibility with existing utility grids and consumer loads, DC MGs have emerged as strong candidates due to their natural interface with photovoltaic and

energy storage systems, along with the increased penetration of DC loads such as electronic loads and electric vehicles [4], [5]. Therefore, hybrid AC/DC MGs can offer an optimized solution by combining the merits of both AC and DC MGs [6], [7], [8]. A power-bidirectional interface converter, interlinking the AC and DC links of the hybrid MGs, as presented in Fig. 1, is typically used for power exchange and to ensure the stable operation of the hybrid MGs.

A key criterion in the selection and design of the converter topology for hybrid MG interlinking converters (ICs) is specifying the voltage levels of both the AC and DC links, which poses a challenge in MG applications. While the AC

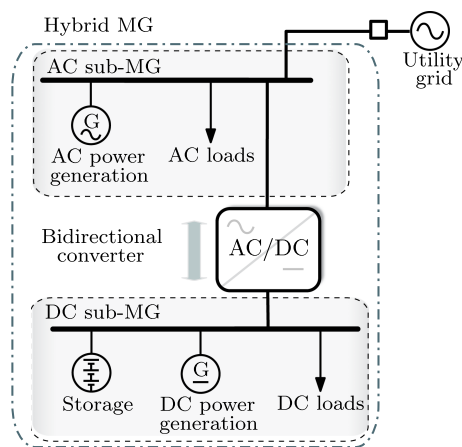


FIGURE 1. A bidirectional converter connecting a DC MG to an AC MG in hybrid MG.

link voltage level is standardized (for example, the European low-voltage (LV) grid operates with a line-to-line voltage of 400 V_{RMS}), the selection of the DC link voltage level is a significant challenge. Several voltage levels are presented in LV DC applications, ranging from 12 V up to 1500 V [9]. Toward the standardization and optimal selection of the LV DC voltage level, studies conducted in [10], [11] compared different voltage levels in terms of overall system efficiency, the number of power conversions required to connect multiple energy sources and loads, and safety and protection requirements. As a result, the 400 V DC system has been proven to result in superior performance compared to other voltage levels, specifically for residential and commercial applications.

The hybrid MG ICs can be classified in two ways: based on the DC voltage level as either buck-type or boost-type converters, or based on the incorporation of the AC neutral wire resulting in three-wire (3-W) or four-wire (4-W) converters. When connected to the LV European AC grid, buck-type converters are capable of interfacing DC systems with 490 V or lower, therefore can directly interface the 400 V DC link. In contrast, the boost-type converters are capable of interfacing DC links with 565 V or higher [12].

Optimized buck-type converters have been proposed in the literature, including the six-switch current source converter (CSC) [13], the seven-switch CSC [14], the delta-type input CSC [15], and the Swiss converter [16]. The modular buck-boost Y-connected converter, as described in [17], serves as a buck-type bidirectional PFC converter and demonstrates superior overall performance compared to the seven-switch and Swiss converters. As for boost-type converters, the conventional choice for ICs is the two-level voltage source converter (2 L VSC), acknowledged for its simple structure, control, and high power density [18], [19]. An improved overall performance can be attained with the three-level voltage source converters (3 L VSC) compared to the conventional 2 L VSC [20]. However, when interfacing the 400 V DC systems, an additional buck stage is needed which can be realized using the DC-DC buck converter [21], [22] or by isolated DC-DC converters [23]. The addition of an extra power conversion

stage and the need for an intermediate DC link capacitors degrades the overall efficiency and power density of the IC.

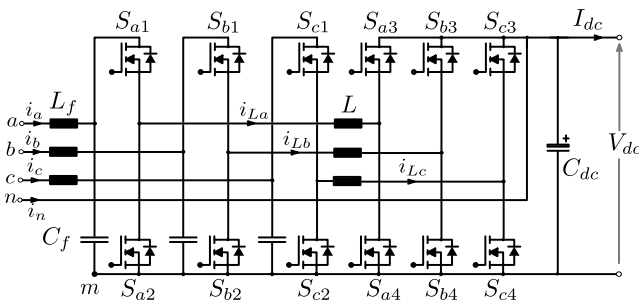
Considering 3-W and 4-W converters, the extension of the 3-W boost-type converters into 4-W converters have been extensively addressed in the literature either by adding an extra leg to the conventional 2 L and 3 L VSCs or by connecting the neutral wire to the mid-point of the split DC link [24], [25], [26], [27], [28], [29]. However four-wire buck-type converters are rarely discussed in the literature, except for some studies focusing on the suppression of common-mode voltage (CMV) and leakage current in the six-switch CSC [30], [31]. A summary of various IC topologies is presented in Table 1, where the different topologies are subcategorized based on common features. The subcategories are then highlighted based on specific aspects of each solution, such as the voltage level of the DC side, the provision of isolation, the possibility of grounding both AC and DC sides, or the allowance for partial grounding of only the AC side. Additionally, the key motivations and challenges for each topology are provided. This summary emphasizes the existing research gap in proposing a buck-type 4-W converter that facilitates a direct interlinking between the AC and DC MGs without the need for an additional power conversion stage.

Several motivations drive the adoption of 4-W converters in IC hybrid MGs. Firstly, 4-W converters can support the islanded operation of the hybrid MG, providing a stable power supply for both single-phase and three-phase AC loads [33], [34]. 3-W converters are unable to supply single-phase loads in islanded operation due to the absence of the neutral wire. Therefore, 4-W converters have gained prominence, especially due to the priority of islanded operation in hybrid MG control and the prevalence of single-phase loads in residential LV AC systems [35]. In addition, in the event of voltage imbalance in the AC MG, 3-W converters can only regulate the positive and negative sequence components of the current. This leads to a circulating current, resulting in additional power losses in the hybrid MG [27]. In contrast, 4-W converters are capable of controlling positive, negative, and zero sequence components, allowing for more flexible control to mitigate the effects of voltage imbalances and ensure optimal operation. Furthermore, 4-W converters enable independent control of the three phases, enabling fault-tolerant operation [36]. In case of a single-phase fault in the AC MG, the remaining two phases can still deliver up to two-thirds of the rated output power.

Another critical asset offered by the proposed converter is its ability to ground both the AC MG and the DC MG. While grounding the bipolar DC MG, linked to a grounded AC MG through a non-isolated converter, is achievable using split-capacitor mid-point grounding [37], grounding the unipolar DC MG presents challenges. To the best of the authors' knowledge and as indicated in previous studies [38], [39], [40], grounding both the AC MG and the DC MG is typically accomplished only through isolated converters or low-frequency transformers. In the proposed topology, grounding both sides is achieved through the direct connection

TABLE 1 Summary of the Different Topologies Proposed in the Literature for Interlinking Converters (ICs), Highlighting the Key Differences Between the Topologies, as Well as the Key Motivations and Challenges of Each

Topology	No. of wires	DC-link voltage	Isolation	Grounding	Motivations	Challenges
2L VSC [18]	3	800	NO	Partial	- Simple structure and control	- Need an additional buck stage
Four-leg VSC [24]	4	800	NO	Partial	- Continuous current at AC side - Reduced current stresses	- Intermediate DC link capacitors size - Increased voltage stresses
T-type VSC [20]	3	650	NO	Partial	- Reduced voltage stresses	- Need an additional buck stage
Neutral-point clamped (NPC) VSC [20]	3	650	NO	Partial	- Reduced voltage stresses compared to 2L VSC	- Intermediate DC link capacitors size
Four-leg T-type VSC [26]	4	800	NO	Partial	- Continuous current at AC side	- Complex structure and control
Four-leg NPC VSC [29]	4	750	NO	Partial	- Reduced current stresses	- Complex structure and control compared to 2L VSC
Six-switch CSC [13]	3	400	NO	Partial	- Single-stage power conversion	- Discontinuous current at AC side
Seven-switch CSC [14]	3	400	NO	Partial	- Reduced voltage stresses	- Inductor and input filter size
Delta-type input CSC [15]	3	400	NO	Partial	- Inherent short-circuit protection	- Complex structure and control compared to 2L VSC
Swiss converter [16]	3	400	NO	Partial		
Y-converter [17]	3	400	NO	Partial		
VSC + DC-DC buck [21], [22]	3	400	NO	Partial	- Simple structure and control - Continuous current at AC side	- Reduced efficiency and power density - Intermediate DC link capacitors size - Increased voltage stresses
VSC + DC transformer [23]	3	400	YES	YES	- Isolation between AC and DC MGs - Grounding both AC and DC MGs - Continuous current at AC side	- Reduced efficiency and power density - DC transformer size and cost - Intermediate DC link capacitors size
Power transformer + VSC [32]	3	700	YES	YES	- Isolation between AC and DC MGs - Grounding both AC and DC MGs - Continuous current at AC side	- Reduced efficiency and power density - Power transformer size and cost - Need an additional buck stage in case of 1:1 transformer
Proposed herein	4	400	NO	YES	- Single-stage power conversion - Four-wire buck-type converter - Grounding both AC and DC MGs without isolation - Reduced voltage stresses	- Discontinuous current at AC side - Inductor and input filter size


FIGURE 2. A schematic of the proposed four-wire modular converter.

between the neutral of the AC MG (n) and the positive rail of the DC MG.

The adopted approach of grounding the positive rail aligns with the requirements of the European Low Voltage Directive, LVD 2006/95/EC [41], which stipulates that the DC MG should be grounded on either the positive or negative DC rail, and the proposed topology facilitates positive rail grounding. Additionally, for DC MG, positive rail grounding is preferable compared to negative rail grounding to minimize the impact of corrosion [42]. According to [43], [44], grounding the DC MG offers numerous advantages, such as low CMV, low transient over-voltages, no grounding loss, and increased personnel safety.

This paper proposes a three-phase four-wire buck-type converter, as illustrated in Fig. 2, with the aim of enhancing the interlinking between the AC MG and the DC MG, building

upon the work presented in [45]. This enhanced interlinking is achieved through a highly efficient converter, enabled by single-stage power conversion. Additionally, optimized performance of the IC is ensured across various operating scenarios. These scenarios encompass normal power flow control under balanced conditions, operation during unbalanced conditions, fault-tolerant operation against single-phase faults, and islanded operation. Compared to state-of-the-art ICs summarized in Table 1, the key advantages of the proposed converter include:

- The proposed converter has the capability to ground both the AC microgrid and the unipolar DC microgrid without the need for isolation.
- In comparison to CSCs, the proposed converter features a 4-W configuration. This configuration enables flexible control in unbalanced conditions, improves fault tolerance, and allows for islanded operation to support both single-phase and three-phase loads.
- In contrast to VSCs, the proposed converter incorporates a single-stage power conversion. This feature potentially contributes to improved efficiency and power density. While VSCs require an additional buck stage to interface with the 400 V DC MG.

The remainder of this paper is structured as follows: Section II explains the converter operation and analysis, Section III includes an evaluation of the proposed converter, Section IV presents the converter's control structure and modulation, Section V showcases the experimental results, and finally, Section VI provides the conclusion.

II. CONVERTER'S ANALYSIS

The proposed converter extends the 3-W topology, introduced in [46] for motor drive applications, into a 4-W configuration. This section provides a discussion of both the 3-W and 4-W topologies, emphasizing the operational principles of each and highlighting the key similarities and distinctions between them.

The conventional 3-W topology is constructed by connecting three buck-boost modules at a central point known as m , which serves as the neutral point for the Y-connection of the modules. Since each module operates as a DC-DC converter, it is essential to maintain a non-negative voltage on the AC side of the module ($V_{\{a,b,c\}m} \geq 0$ V). To accomplish this, an offset voltage is required between n and m . In sinusoidal pulse width modulation (SPWM), a constant offset voltage, denoted as V_{off} , is applied and it is controlled to be greater than the peak value of the grid's AC phase voltage (\hat{V}_m). The AC-side voltages v_{am} , v_{bm} , and v_{cm} can be expressed as:

$$v_{xm} = v_x + V_{off} \quad (1)$$

where v_x , with $x = (a, b, c)$, are the phase grid voltages and ω is the AC grid frequency in rad/s.

In the case of the 4-W topology presented in Fig. 2, n is connected to the positive rail of the DC side, which leads to a fixed offset voltage equivalent to the DC-side voltage V_{dc} . To ensure the correct functioning of the four-wire converter when connected to the European distribution grid, V_{dc} needs to exceed 325 V. Therefore, this topology can be utilized to interface the 400 V DC microgrid with the European low-voltage grid. For the four-wire topology, v_{am} , v_{bm} , and v_{cm} can be expressed as:

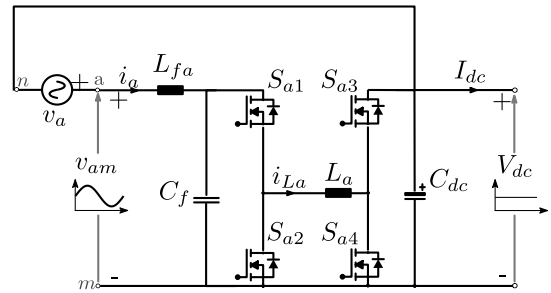
$$\begin{aligned} v_{am} &= \hat{V}_m \sin(\omega t) + V_{dc} \\ v_{bm} &= \hat{V}_m \sin\left(\omega t - \frac{2\pi}{3}\right) + V_{dc} \\ v_{cm} &= \hat{V}_m \sin\left(\omega t + \frac{2\pi}{3}\right) + V_{dc} \end{aligned} \quad (2)$$

To provide a clear and simplified analysis, a single-module analysis is provided, which can be extended similarly to the other modules. Considering phase a , displayed in Fig. 3(a), its module consists of an inductor L and two half-bridges: an AC-side half bridge (S_{a1} , S_{a2}) and a DC-side half bridge (S_{a3} , S_{a4}). These two half-bridges are controlled so that only one half-bridge is modulated at an instance and the other is kept clamped depending on the values of V_{am} and V_{dc} .

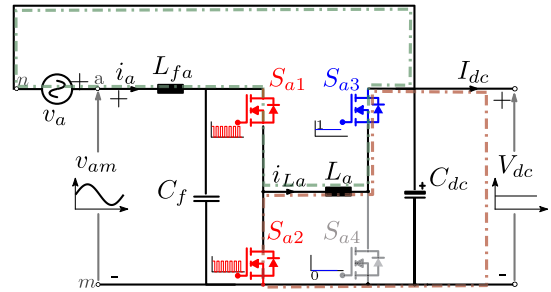
When v_{am} is greater than V_{dc} , module a works in the buck mode where the AC-side half bridge is switching, while the DC-side half bridge is clamped (S_{a3} is kept ON and S_{a4} is kept OFF) as presented in Fig. 3(b). In this mode, the duty cycle of S_{a1} , which is named $d_{buck,a}$, can be calculated as follows:

$$d_{buck,a} = \frac{V_{dc}}{v_{am}} = \frac{V_{dc}}{\hat{V}_m \sin(\omega t) + V_{dc}} \quad (3)$$

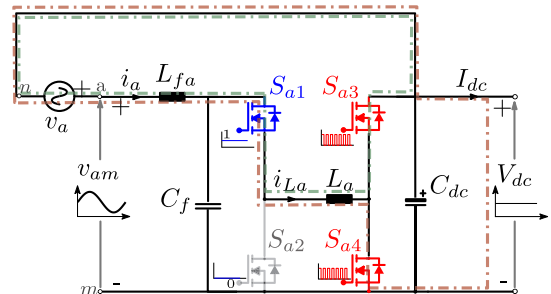
and the command of S_{a2} is the complementary of S_{a1} .



(a) Module a of the three-phase modular converter



(b) Buck mode when $v_{am} > V_{dc}$



(c) Boost mode when $v_{am} < V_{dc}$

FIGURE 3. Operation modes of one module of the proposed converter include current paths in both buck and boost modes.

Assuming sinusoidal mains current with unity power factor, the average inductor current of module a , denoted as $i_{La,av}$, can be determined as follows:

$$i_{La,av} = \frac{i_a - i_{Cf,a}}{d_{buck,a}} = \frac{\hat{I}_m \sin(\omega t) - i_{Cf,a}}{d_{buck,a}} \quad (4)$$

where i_a is the grid current of phase a , $i_{Cf,a}$ is the current of the input capacitor C_f , and \hat{I}_m is the peak grid current. By neglecting $i_{Cf,a}$ compared to i_a , $i_{La,av}$ can be simplified to be:

$$i_{La,av} = \frac{i_a}{d_{buck,a}} = \frac{\hat{I}_m \sin(\omega t)}{d_{buck,a}} \quad (5)$$

Similarly, when v_{am} is below V_{dc} , module a operates in boost mode. In this mode, the DC-side half-bridge operates in the switching mode, while the AC-side half-bridge is clamped (with S_{a1} kept ON and S_{a2} kept OFF), as illustrated in Fig. 3(c). The duty cycle of S_{a3} in this mode, denoted as

TABLE 2 Basic Equations of the Proposed Converter for Module a

	$0 \leq t \leq T/2$	$T/2 \leq t \leq T$
v_a	$\hat{V}_m \sin(\omega t)$	
v_{am}	$\hat{V}_m \sin(\omega t) + V_{dc}$	
$d_{buck,a}$	V_{dc}/v_{am}	1
$d_{boost,a}$	1	v_{am}/V_{dc}
$i_{La,av}$	$\hat{I}_m \sin(\omega t)/d_{buck,a}$	$\hat{I}_m \sin(\omega t)$

$d_{boost,a}$, can be calculated as follows:

$$d_{boost,a} = \frac{v_{am}}{V_{dc}} = \frac{\hat{V}_m \sin(\omega t) + V_{dc}}{V_{dc}} \quad (6)$$

and the command of S_{a4} is the complementary of S_{a3} .

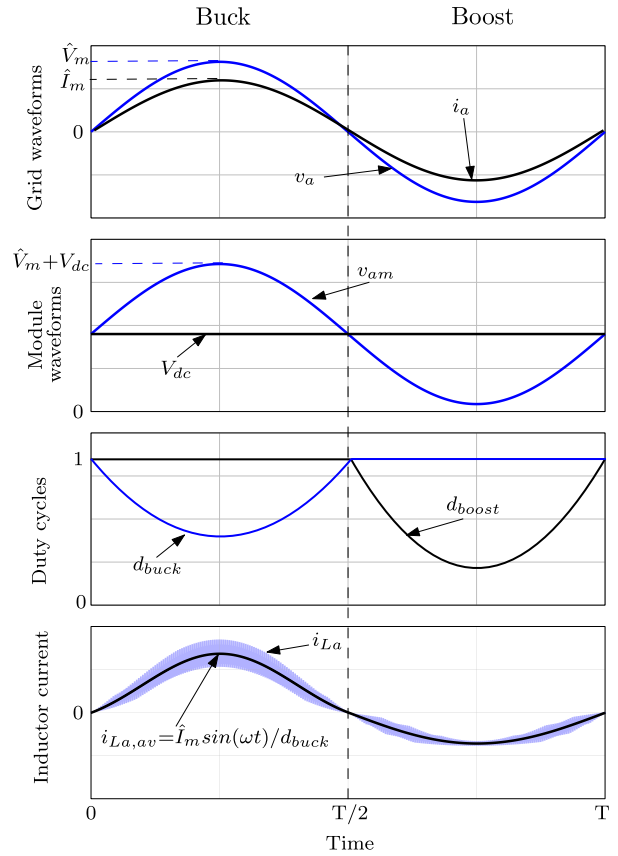
Using (5) and given that $d_{buck,a} = 1$ in boost mode, $i_{la,av}$ in boost mode equals:

$$i_{La,av} = i_a = \hat{I}_m \sin(\omega t) \quad (7)$$

The key operational differences between the 3-W and 4-W topologies are as follows. Firstly, in the 4-W topology, each module has its current return path through the neutral wire, resulting in fully independent operation of the three modules. This enhances the converter's flexibility under unbalanced conditions and improves reliability during single-phase faults, as will be demonstrated in the following sections. Secondly, the period of the buck and boost mode differs. In the 4-W topology, the fundamental period of the AC grid frequency T is equally divided between the buck and boost modes. Each module operates in the buck mode when its phase voltage is greater than zero and switches to the boost mode when its phase voltage is less than zero. In contrast, the duration of the buck and boost modes in the 3-W topology depends on both V_{dc} and V_{off} . The basic equations for phase a of the 4-W modular converter are summarized in Table 2. Additionally, the key waveforms are plotted in Fig. 4.

The performance of the 3-W topology has been thoroughly evaluated in previous studies. In [17], the 3-W topology is compared to single-stage buck-type converters, and in [47], it has been evaluated against two-stage converters. Both studies demonstrated the superior performance of the 3-W topology not only in terms of efficiency but also in overall size and power density. These findings can be extended to the 4-W topology, as it exhibits almost the same performance as the 3-W topology for the selected case study at balanced conditions.

An additional incentive for employing the proposed converter is related to its fixed CMV. Despite ongoing efforts to mitigate CMV through modifications in power converter modulation techniques, the generation of a high-frequency CMV component persists [30], [31], [48]. This CMV presents a potential threat to overall MG performance by inducing leakage current through the parasitic capacitance of PV panels


FIGURE 4. Basic waveforms of the four-wire modular converter.

to ground and causing electromagnetic interference in the high-frequency range [48]. In the proposed topology, denoted as v_{nm} , the CMV is fixed and equals V_{DC} . Consequently, the leakage current flowing through parasitic capacitances is minimized, contributing to enhanced performance.

III. TOPOLOGY EVALUATION

In this section, a comprehensive evaluation of the proposed converter is presented, comparing it to the four-leg VSC with a cascaded buck converter (4-leg VSC + buck). The 4-leg VSC + buck is chosen from the topologies discussed in Table 1 due to its resemblance to the proposed converter as a non-isolated 4-W 2 L converter. This evaluation aims to emphasize the advantages of adopting a single-stage power conversion in terms of minimizing losses and size compared to the two-stage solutions.

The comprehensive assessment of the power converters encompasses semiconductor device stresses, losses, and the overall chip area. Furthermore, an estimation of the total volume of magnetic elements in both converters is provided, taking into account main inductors and input EMI filter inductors designed to meet the CISPR 11 Class B EMI standard. The specifications and ratings guiding this evaluation are summarized in Table 3. The chosen power rating of 7kW is tailored for small-scale residential and commercial applications.

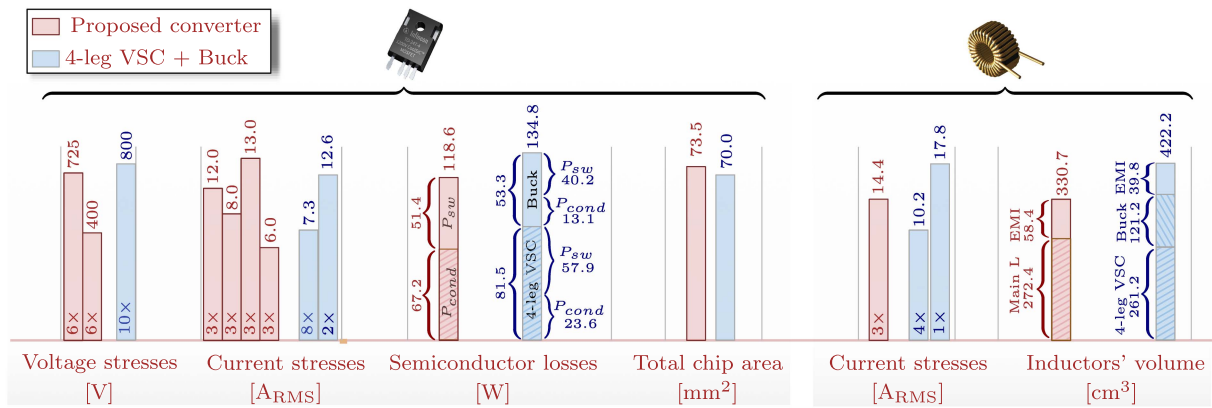


FIGURE 5. Comparison of the proposed converter with the 4-leg VSC + buck in terms of semiconductor and magnetic devices.

TABLE 3 Specifications Utilized in Converters Evaluation

Parameter	Symbol	Value
Rated power	P_r	7 kW
AC line voltage	V_{ll}	400 V
Line frequency	f	50 Hz
Switching frequency	f_{sw}	62.5 kHz
Output voltage	V_{dc}	400 V

A. SEMICONDUCTOR DEVICES EVALUATION

The evaluation of semiconductor devices begins by assessing their voltage stresses. In the case of the 4-leg VSC + buck, all devices experience a voltage stress equal to the intermediate DC-link voltage (800 V according to [24]). Consequently, 1200 V SiC devices are chosen. On the other hand, for the proposed converter, the AC-side half-bridges handle voltages with a peak value of $\hat{V}_m + V_{dc}$ (725 V), while the DC-side boost half-bridges are subjected to the DC MG voltage (400 V). Therefore, 1200 V and 650 V SiC devices are selected for AC-side and DC-side half-bridges, respectively. The CoolSiC discrete MOSFETs from Infineon are then employed in the evaluation. To assess the chip area of the devices, it is assumed that the specific on-resistance $R_{ds,sp}$, representing the on-state resistance per unit area of SiC MOSFET, remains constant for all devices with the same voltage rating. Specifically, it is set at $200 \text{ m}\Omega \cdot \text{mm}^2$ and $350 \text{ m}\Omega \cdot \text{mm}^2$ for the 650V and 1200V devices, respectively [49], [50].

The selection criterion for SiC devices is to achieve the lowest chip area. Therefore, starting from the devices with the highest on-resistance R_{ds} , the junction temperature of each device is calculated using PLECS thermal modeling simulations. The device is chosen if its junction temperature is below 120 °C; otherwise, the device with a lower R_{ds} is selected until the temperature criterion is met.

Fig. 5 summarizes the outcomes of the semiconductor devices evaluation, encompassing voltage and current stresses,

semiconductor losses, along with the total chip area for each converter. The proposed converter exhibits higher conduction losses P_{cond} due to relatively higher current stresses compared to 4-leg VSC + buck. However, the proposed converter achieves significantly lower switching losses P_{sw} due to reduced voltage stresses and the fact that not all devices are continuously commutating. This is in contrast to 4-leg VSC + buck, where all devices continuously commute at the intermediate DC-link voltage. Overall, the proposed converter exhibits lower total semiconductor losses with 118.6 W at rated power compared to 134.8 W losses of the 4-leg VSC + buck at rated power.

Additionally, the evaluation of the total chip area reveals that, despite the 4-leg VSC + buck featuring a lower number of semiconductor devices (10 devices compared to 12 devices in the proposed converter), the difference in the total chip area between both converters is minor, with only a 5% increment in the proposed converter. It is noteworthy that the theoretical limit for $R_{ds,sp}$ of 1200 V SiC devices is four times the limit for $R_{ds,sp}$ of 650 V SiC devices [50]. Therefore, advancements in SiC device manufacturing, pushing towards the theoretical limits, have the potential to positively influence the assessment outcomes in favor of the proposed converter.

B. MAGNETIC ELEMENTS EVALUATION

The magnetic components' volume of both converters is evaluated, taking into account the main converter inductors and the EMI filter inductors. The 4-leg VSC + buck includes five main inductors, four in the VSC stage and one for the buck stage. The inductance value of VSC inductors directly influences total harmonic distortion (THD) and the resulting high-frequency noise generated by the switching ripple current [51], [52]. Consequently, the maximum peak-to-peak ripple current $\Delta I_{L,pkpk}$ should be limited, and it is chosen herein to be equal to 25% of the peak grid current, resulting in four 330 μH inductors. For the buck inductor, $\Delta I_{L,pkpk}$ is set to be 60% to allow for minimized inductor volume, resulting in a 300 μH inductor.

On the other hand, the proposed converter includes only three main inductors. A minimum limit for the inductor value is defined to restrict the peak RMS value of the high-frequency ripple current I_{hf_RMS} in both buck and boost modes to the same value [53]. For the presented case study, the minimum limit for inductance is set at 100 μ H. To limit peak switching current and core losses, the inductance is chosen to be 190 μ H, allowing for a $\Delta I_{L, pkpk}$ of 60%.

The EMI filter is designed to comply with the CISPR 11 Class B EMI standard, which specifies electromagnetic emission requirements for equipment in residential areas to prevent interference. The design process for the EMI filter involves the following steps:

- The high-frequency emissions of both converters are assessed by first calculating I_{hf_RMS} at the first switching harmonic that exceeds 150 kHz, a frequency falling within the EMI standard limit.
- Subsequently, the noise emissions are calculated in dB μ V, taking into account a 50 Ω line impedance stabilization network (LISN).
- The calculation of the required attenuation by the EMI filter involves subtracting the specified noise limit at the switching harmonic from the calculated emissions. An additional margin should be considered to ensure compliance with the standard, typically adopting a 10 dB μ V margin.
- Given the required attenuation by the filter and considering a multi-stage LC filter, the product of filter inductance and capacitance can be calculated using the methodology presented in [54].
- Finally, by designing the total filter capacitance to limit its reactive power consumption to 5% of P_r , the filter inductance is calculated.

In order to estimate the inductor volume, the simplified methodology presented in [47] is adopted. The estimated total inductors' volume of both converters is illustrated in Fig. 5. In addition to the lower number of total inductors, the proposed converter yields a significantly lower inductors' volume amounting to only 78% of the 4-leg VSC + buck inductors' volume.

In addition to the reduced volume of magnetic elements in the proposed topology, it also eliminates the need for an intermediate DC-link capacitor due to its single-stage operation. In a two-stage converter like the 4-leg VSC + buck, bulky electrolytic or film capacitors are employed to smooth the DC-link voltage while being subjected to the high DC-link voltage and the high capacitor ripple current [55], [56]. The elimination of the intermediate DC-link capacitor in the proposed converter contributes to a potentially improved power density compared to two-stage converters such as the 4-leg VSC + buck

IV. CONTROL AND MODULATION

Aiming to ensure resilient and reliable operation of the hybrid MG, various control objectives are commonly categorized in a hierarchical control architecture into three different layers: primary, secondary, and tertiary [57]. The primary control

layer focuses on achieving fast load sharing among RES, ESS, and ICs. The secondary control layer is responsible for enhancing power quality, recovering the frequency and voltage deviation in the MG caused by primary level regulation errors. It also handles the resynchronization of the MG to the utility grid [58]. Lastly, the tertiary control layer aims at achieving optimal energy management, serving as a centralized function in the MG controller. Since the primary control layer handles the power balancing between generation and consumption which is the main function of the IC, the primary control will be discussed in this section along with the inner control loops of the proposed converter.

The primary control approaches can be categorized into centralized and decentralized control [59]. In centralized control, power balancing in the MG is achieved through a master–slave control approach. On the other hand, decentralized control relies on a droop control approach. The droop control strategy presents several advantages compared to master-slave control, such as increased reliability with a prompt response to load changes, reduced communication and computational burden, and enhanced flexibility that allows for easy expandability [35].

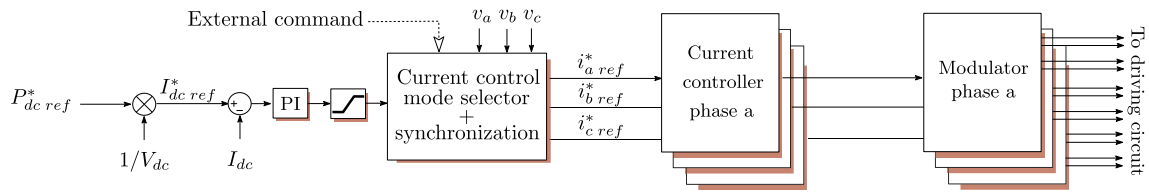
In this section, the control of the proposed converter is presented in Fig. 6 for two distinctive operating modes: the grid-following (GFL) mode and the islanded mode. The aim of this section is to highlight the converter control structure in both modes and demonstrate the converter's capabilities during balanced and unbalanced conditions.

A. GFL MODE

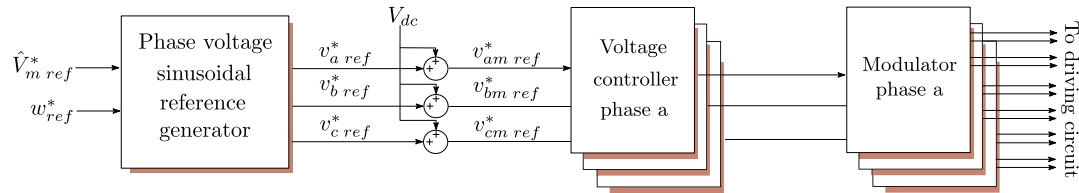
The control structure of the proposed topology in GFL mode, depicted in Fig. 6(a), comprises four main stages: outer power control loop, current control mode selector and synchronization stage, inner current control loops and finally modulators stage.

The outer power control loop is employed to regulate the power transfer between the AC MG and the DC MG. The power reference, denoted as $P_{dc_ref}^*$, is determined by the droop controller. In the proposed control structure, considering the interconnection of the AC MG with the utility grid (as depicted in Fig. 1), the DC MG droop control is designed to regulate the DC MG voltage. If the IC provides grid-supporting functions along with AC MG voltage and frequency regulation, a normalized AC-DC droop can be adopted, as discussed in [6]. With $P_{dc_ref}^*$ determined by the DC MG droop control and divided by V_{dc} , the power exchange is controlled by manipulating the DC MG current, denoted as I_{dc} , which is regulated using a PI controller.

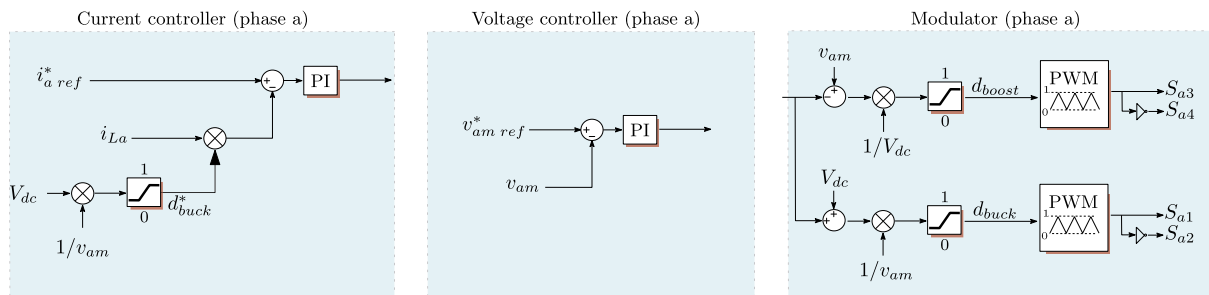
The output of the outer power control loop is directed to the current control mode selector and synchronization stage, responsible for generating grid current references for the inner current control loops. Since each module of the converter can be controlled independently, a separate current reference is generated for each module, allowing for flexible operation of the converter under unbalanced conditions. During unbalanced conditions, three current control modes are considered.



(a) Control block diagram of the proposed converter in GFL mode



(b) Control block diagram of the proposed converter in islanded mode



(c) Controllers and modulator of phase a

FIGURE 6. Block diagram of the control structure for the proposed converter.

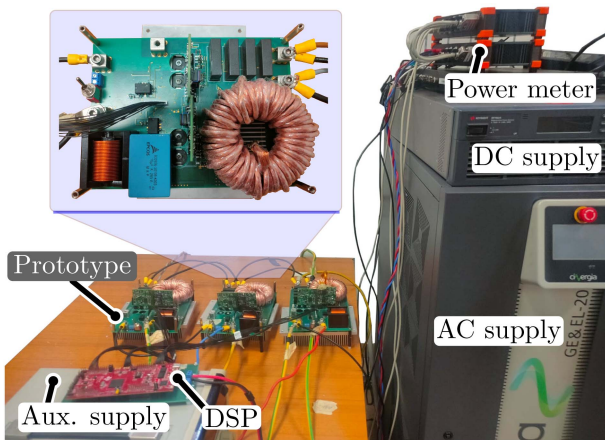


FIGURE 7. Experimental prototype of the proposed converter.

Firstly, the constant input resistance mode emulates an ohmic behavior for each module, resulting in drawn current being proportional to the measured voltage of each phase. Secondly, the constant input power mode ensures equalized power sharing between modules, causing drawn current from each phase to be inversely proportional to the measured grid voltage. Thirdly, the constant input current mode evenly distributes current between modules regardless of the grid voltage of each

phase. By measuring grid voltages and selecting the appropriate mode for current control, the grid current references for the inner current control loops are generated.

Each of the discussed current control modes has its motivations [24]. For the constant resistance mode, since the drawn current of each phase is proportional to its grid voltage, this mode helps restore balanced conditions by drawing less current from the weaker phases with lower voltages and drawing higher current from the other phases. Therefore, this mode is advantageous for the AC MG. Regarding the constant power mode, since each module delivers the same power to the DC MG, power fluctuations and low-frequency voltage ripples are minimized at the DC MG. Therefore, this mode is advantageous for the DC MG. Finally, for the constant current mode, equalized current stresses on semiconductor devices are ensured with zero current flowing in the neutral wire.

For the different current control modes, the amplitude of the generated grid current references is limited to the designed rated value. During unbalanced operation, the modules may handle different powers and currents. While the amplitudes of grid voltages do not exceed the rated values, limiting the grid current reference amplitude ensures that the power losses of each module do not exceed the designed values, ensuring a safe and reliable operation during both balanced and unbalanced conditions.

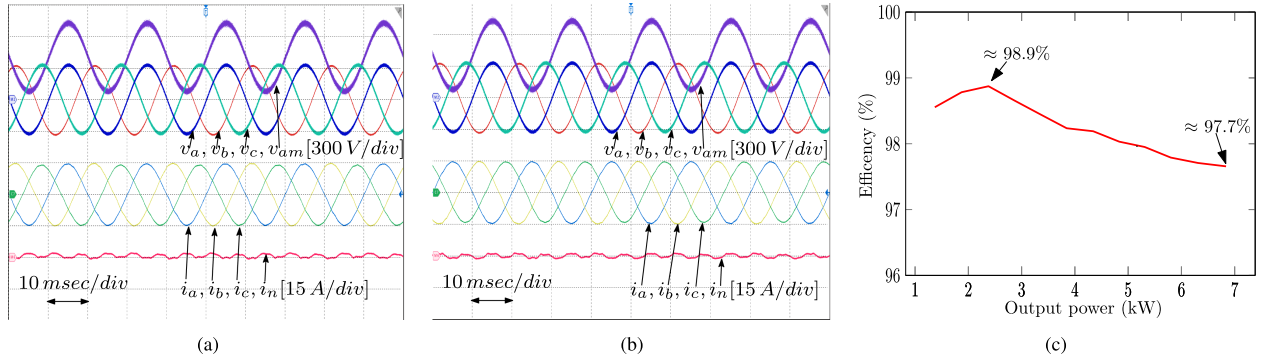


FIGURE 8. Experimental results under balanced AC grid: (a) Rectification mode at rated power, (b) Inversion mode at rated power, and (c) Efficiency curve of the experimental prototype.

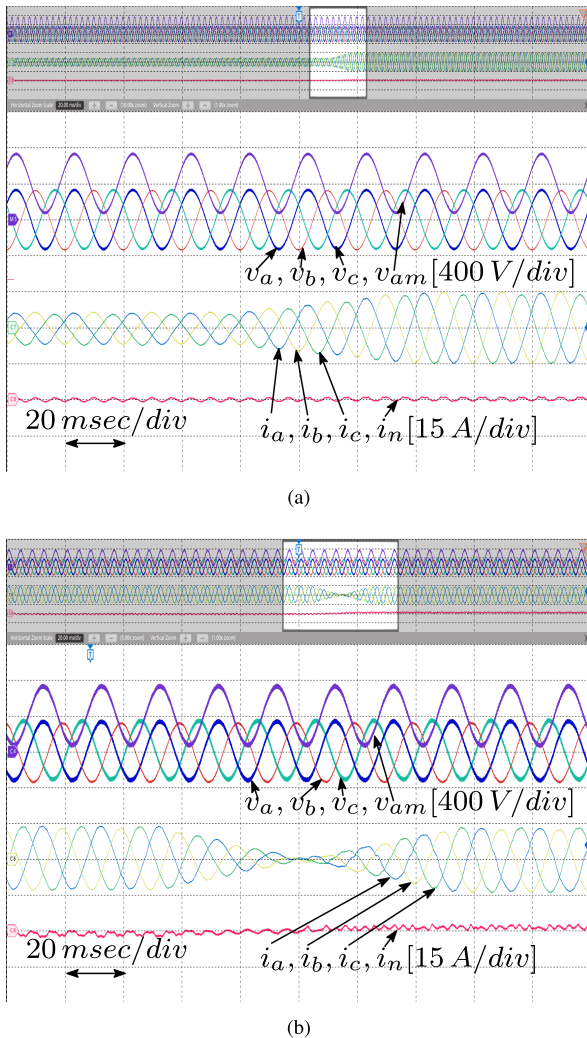


FIGURE 9. Experimental results under balanced AC grid with step changes in the load: (a) Step change in rectification mode from 50% to 100% of rated power, (b) Step change from rectification to inversion mode.

The grid current references are then sent to their respective current controllers. In the proposed control structure presented in Fig. 6(c), the feedback of the grid currents is attained through indirect measurement of the grid currents.

Based on (5) and considering phase a as an example, i_a can be calculated by multiplying $i_{La,av}$ by $d_{buck,a}$. This indirect measurement method ensures the regulation of both grid and inductor currents without the need for additional cascaded loops. The grid currents are regulated using a PI controller.

Achieving a robust operation of the ICs hinges on key factors such as precise tuning of controllers for prompt responses, minimal overshoot, and reduced steady-state error [35], [60]. Additionally, the design of the synchronization stage plays a pivotal role, ensuring sustained synchronization during transient conditions and effective rejection of noise and disturbances in the grid signal [61].

The current controllers are then connected to their respective modulators. The modulators are designed to prevent simultaneous modulation of the half-bridges in the modules, as discussed in references [53], [62]. For instance, in the case of module a during buck mode ($v_{am} > V_{dc}$), the modulator of the boost half-bridge, illustrated in Fig. 6(c), saturates to unity causing its corresponding half-bridge to be clamped, while the buck half-bridge is modulated. Similarly, during boost mode ($v_{am} < V_{dc}$), the modulator of the buck half-bridge saturates to unity while the boost half-bridge is modulated, and the corresponding buck half-bridge is clamped.

B. ISLANDED MODE

In the islanded mode, the converter is controlled to function as a voltage source, capable of providing a stable voltage for both three-phase and single-phase loads. The control structure for the islanded mode, as illustrated in Fig. 6(b), employs reference values for both the peak value of the AC voltage \hat{V}_m^* and the AC voltage frequency w_{ref}^* to generate desired sinusoidal references for the AC phase voltages v_{xref}^* . The reference values for the input module voltages v_{xmref}^* are then obtained by adding V_{dc} to v_{xref}^* . Subsequently, the generated v_{xmref}^* are connected to their respective voltage controllers and modulators. Similar to the current controller in the GFL mode, the voltage controller is implemented using a PI controller.

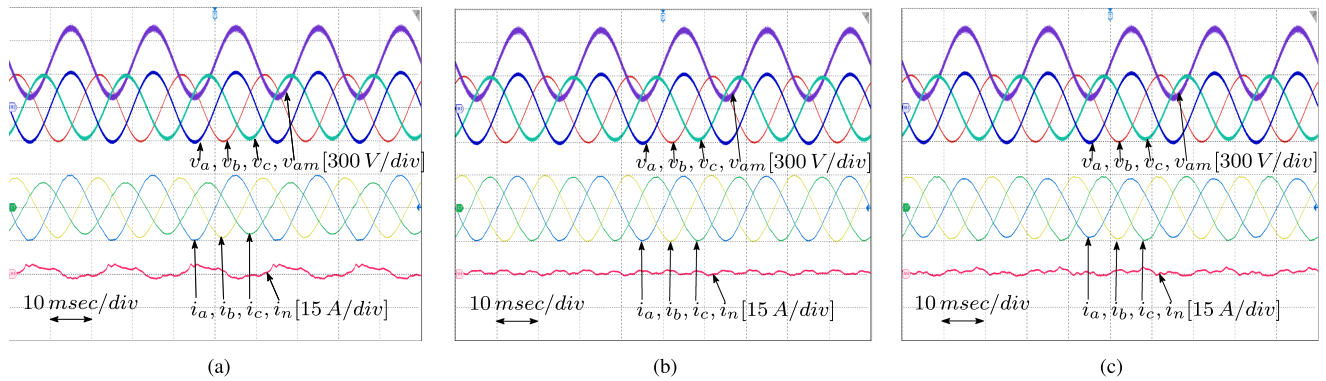


FIGURE 10. Experimental waveforms under unbalanced AC grid with different current control techniques: (a) Constant input resistance mode at rated power, (b) Constant input current mode at rated power, and (c) Constant input power mode at rated power.

TABLE 4 SiC Devices and Passive Components Utilized in the Experimental Prototype

	Parameter	Symbol	Value
SiC MOSFET	Part number	IMZ120R030M1H	
	Voltage	V_{DS}	1200 V
	Current	I_D	56 A
Inductor parameters	Inductor	L	190 μ H
	Part number	KoolMu 0079908A7	
	Magnetic path length	MPL	19.6 cm
	Core volume	V_c	43.4 cm^3
	Number of turns	N	80 Turns
Input filter	Inductor	L_f	50 μ H
	Capacitor	C_f	11.3 μ F
	Inductor DC resistance	R_{LDC}	20.3 m Ω

V. EXPERIMENTAL RESULTS

To validate the effectiveness of the proposed converter, an experimental prototype, as depicted in Fig. 7, has been constructed with a rating of 7kW. The parameters of the prototype are detailed in Table 4. Experimental waveforms were captured using an 8-channel oscilloscope and include the AC grid voltages (v_a, v_b, v_c), AC-side voltage of module a (v_{am}), and the AC grid currents (i_a, i_b, i_c, i_n). Additionally, the Dewesoft SIRIUS XHS high-speed data acquisition system is employed to accurately measure the AC grid currents' RMS values, THD, and the prototype's efficiency.

The experimental results are categorized into the following sections: performance under balanced AC grid conditions, performance under unbalanced AC grid conditions, performance when a single module is disconnected, and performance during islanded operation.

A. BALANCED AC GRID CONDITIONS

This section presents experimental waveforms under balanced AC grid conditions in both rectification and inversion modes at steady-state, as well as the transient behavior under step variations in the power reference. Additionally, efficiency curves of the experimental prototype are discussed.

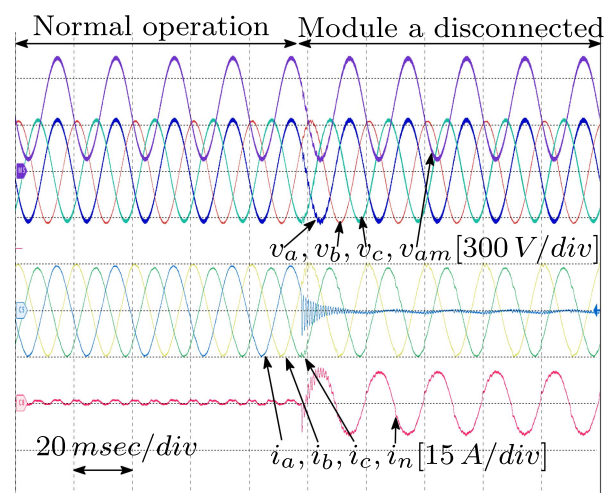


FIGURE 11. Experimental waveforms to demonstrate the fault tolerant operation under one module disconnection.

The waveforms at rated power in rectification mode are displayed in Fig. 8(a). In this mode, the AC currents are well-synchronized with the AC voltages, resulting in a measured power factor of greater than 0.99. Similarly, the inversion mode at rated power is shown in Fig. 8(b). As evident from the waveforms, the AC currents exhibit a 180-degree phase shift from the AC voltages. Additionally, the efficiency curve of the prototype is depicted in Fig. 8(c). The prototype demonstrates a peak efficiency of 98.87%, with an efficiency of 97.66% at the rated output power.

The performance of the proposed control structure is evaluated under power reference variations. Two specific cases are considered: a step change in the output power in rectification mode and a step change in the output power from rectification mode to inversion mode. In Fig. 9(a), the converter initially operates in rectification mode at 50% of its rated power. A step change is then applied to reach the rated power. The waveforms clearly demonstrate the fast and stable behavior of both i_a and i_{La} , indicating the efficient and reliable operation of the control structure.

Similarly, Fig. 9(b) illustrates the step change from rectification mode to inversion mode. The converter undergoes a transition from 100% of rated power in rectification mode to 100% of rated power in inversion mode. Once again, the waveforms exhibit a stable response, highlighting the effectiveness of the control structure.

B. UNBALANCED AC GRID CONDITIONS

The section evaluates the performance and flexibility of the converter when interfacing the DC MG with unbalanced AC voltages. Unbalances in the AC voltages may arise from uneven loading in the AC MG, such as single-phase residential loads, or single-phase distributed generation, or due to faults in the AC MG. Regardless of the source of the unbalance in the AC MG, this section focuses on the converter's operation under different current control modes. The RMS values of v_a , v_b , and v_c are adjusted to simulate AC voltage unbalance, set to 230 V, 210 V, and 190 V, respectively. Three distinct current control modes are presented for analysis.

First, the constant input resistance mode (Fig. 10(a)) demonstrates the converter's modules being controlled to exhibit ohmic behavior, resulting in grid currents proportional to the grid voltages. Second, the constant input current mode (Fig. 10(b)) showcases the converter's modules being controlled to achieve equalized current sharing among the three modules. Finally, the constant input power mode (Fig. 10(c)) illustrates the converter's modules being controlled to achieve equalized power sharing among the three modules, thereby minimizing power fluctuations on the DC MG.

C. DISCONNECTION OF A SINGLE MODULE

In this section, the fault-tolerant operation of the proposed converter under single-phase faults is verified. The study focuses on the fault-tolerant response in the event of the disconnection of a single module, attributed to potential causes such as semiconductor failure or a single feeder disconnection in the AC MG due to a single-line fault or a tripping of current protection in a single module. Given the independent control capability of each module, the converter demonstrates the capacity to sustain operation even when a single module is disconnected by redistributing power through the remaining modules.

The fault-tolerant operation is demonstrated in Fig. 11, where the converter is initially running in normal operation with a constant current reference is directly fed to the inner current control loop. The normal operation is interrupted by a sudden disconnection of module a . Despite the disconnection of module a , the operation of the other two modules remains unaffected, allowing the converter to still deliver up to two-thirds of its rated power.

D. ISLANDED OPERATION

Another valuable feature of the proposed topology is its islanded operation capability. In addition to the demonstrated performance in the previous sections under grid-following

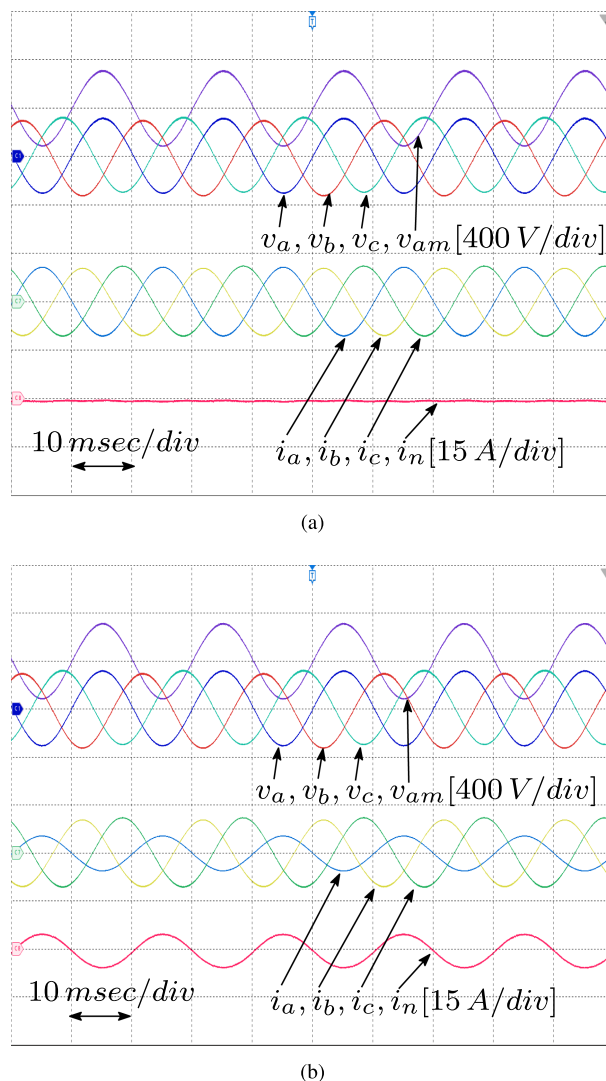


FIGURE 12. Experimental waveforms of islanded mode: (a) Balanced load, (b) Unbalanced load.

mode, the converter can control both the voltage and the frequency of the AC side for both three-phase and single-phase loads. To verify this capability, the AC supply is disconnected and replaced with a three-phase resistive load.

The operation in islanded mode is assessed under two conditions. First, when connected to a balanced resistive load of 29Ω /phase, as shown in Fig. 12(a). Second, when connected to an unbalanced three-phase load, where the resistance for phase b is changed to 58Ω while the resistances for phases a and c remain at 29Ω , as depicted in Fig. 12(b).

Based on the demonstrated waveforms, the converter proves its capability to regulate both the voltage and frequency of v_a , v_b , and v_c under both balanced and unbalanced load conditions. In the case of an unbalanced load, the zero-sequence component of the AC current will flow through the neutral wire.

VI. CONCLUSION

This article introduces a three-phase four-wire buck-type interlinking converter for hybrid AC/DC microgrids, incorporating a single-stage power conversion. The proposed configuration of the converter consists of three four-switch buck-boost modules arranged in a star configuration, where the AC microgrid neutral is directly connected to the positive terminal of the DC microgrid. The inclusion of the neutral wire enables the islanded capability of the hybrid microgrid, ensuring a stable power supply for both single-phase and three-phase AC loads. Notably, the direct link between the AC microgrid neutral and the positive terminal of the DC microgrid allows for the grounding of both microgrids, a capability previously achievable solely with isolated topologies.

Moreover, the four-wire converters are capable of regulating positive, negative, and zero sequence components, offering flexible control mechanisms during AC voltage imbalances to mitigate their impact and ensure optimal operation. This feature is demonstrated in this article by addressing three current control modes: the constant input resistance mode, which emulates an ohmic behavior for each module and then helps restore balanced conditions; the constant input current mode, which evenly distributes the current between the modules; and the constant input power mode, which minimizes power fluctuations and low-frequency ripples on the DC microgrid side.

Additionally, the converter allows for independent control of the three phases, facilitating fault-tolerant operation as demonstrated in this article under single-phase faults. The converter's performance is comprehensively evaluated through experimental tests conducted on a 7 *rmkW* prototype under diverse operating conditions, encompassing balanced and unbalanced AC voltages, single-module disconnection, and islanded operation.

REFERENCES

- [1] J. M. Guerrero, J. C. Vasquez, J. Matas, L. G. de Vicuna, and M. Castilla, "Hierarchical control of droop-controlled AC and DC microgrids—A general approach toward standardization," *IEEE Trans. Ind. Electron.*, vol. 58, no. 1, pp. 158–172, Jan. 2011.
- [2] Y. Khayat et al., "On the secondary control architectures of AC microgrids: An overview," *IEEE Trans. Power Electron.*, vol. 35, no. 6, pp. 6482–6500, Jun. 2020.
- [3] F. S. Al-Ismael, "DC microgrid planning, operation, and control: A comprehensive review," *IEEE Access*, vol. 9, pp. 36154–36172, 2021.
- [4] T. Dragičević, X. Lu, J. C. Vasquez, and J. M. Guerrero, "DC microgrids—Part II: A review of power architectures, applications, and standardization issues," *IEEE Trans. Power Electron.*, vol. 31, no. 5, pp. 3528–3549, May 2016.
- [5] M. A. Hossain, H. R. Pota, W. Issa, and M. J. Hossain, "Overview of AC microgrid controls with inverter-interfaced generations," *Energies*, vol. 10, no. 9, 2017, Art. no. 1300.
- [6] F. Nejabatkhah and Y. W. Li, "Overview of power management strategies of hybrid AC/DC microgrid," *IEEE Trans. Power Electron.*, vol. 30, no. 12, pp. 7072–7089, Dec. 2015.
- [7] Y. Xia, W. Wei, M. Yu, X. Wang, and Y. Peng, "Power management for a hybrid AC/DC microgrid with multiple subgrids," *IEEE Trans. Power Electron.*, vol. 33, no. 4, pp. 3520–3533, Apr. 2018.
- [8] E. Unamuno and J. A. Barrena, "Hybrid AC/DC microgrids—Part I: Review and classification of topologies," *Renewable Sustain. Energy Rev.*, vol. 52, pp. 1251–1259, 2015.
- [9] International Electrotechnical Commission, "LVDC: Electricity for the 21st century," IEC Technol. Report, Geneva, Switzerland, 2017. [Online]. Available: <https://www.iec.ch/basecamp/lvdc-electricity-21st-century>
- [10] L. Li, K.-J. Li, K. Sun, Z. Liu, and W.-J. Lee, "A comparative study on voltage level standard for DC residential power systems," *IEEE Trans. Ind. Appl.*, vol. 58, no. 2, pp. 1446–1455, Mar./Apr. 2022.
- [11] S. Anand and B. G. Fernandes, "Optimal voltage level for DC microgrids," in *Proc. IEEE 36th Annu. Conf. Ind. Electron. Soc.*, 2010, pp. 3034–3039.
- [12] J. W. Kolar and T. Friedli, "The essence of three-phase PFC rectifier systems—Part I," *IEEE Trans. Power Electron.*, vol. 28, no. 1, pp. 176–198, Jan. 2013.
- [13] A. Stupar, T. Friedli, J. Minibock, and J. W. Kolar, "Towards a 99% efficient three-phase buck-type PFC rectifier for 400-V DC distribution systems," *IEEE Trans. Power Electron.*, vol. 27, no. 4, pp. 1732–1744, Apr. 2012.
- [14] W. Wang, F. Gao, Y. Yang, and F. Blaabjerg, "Operation and modulation of H7 current-source inverter with hybrid SiC and Si semiconductor switches," *IEEE Trans. Emerg. Sel. Topics Power Electron.*, vol. 6, no. 1, pp. 387–399, Mar. 2018.
- [15] B. Guo, F. Wang, and E. Aeloiza, "A novel three-phase current source rectifier with delta-type input connection to reduce the device conduction loss," *IEEE Trans. Power Electron.*, vol. 31, no. 2, pp. 1074–1084, Feb. 2016.
- [16] L. Schrittwieser, M. Leibl, M. Haider, F. Thöny, J. W. Kolar, and T. B. Soeiro, "99.3% efficient three-phase buck-type All-SiC SWISS rectifier for DC distribution systems," *IEEE Trans. Power Electron.*, vol. 34, no. 1, pp. 126–140, Jan. 2019.
- [17] A. Y. Farag, T. Younis, D. Biadene, and P. Mattavelli, "AC grid-DC microgrid coupling with high-performance three-phase single-stage bidirectional converters," *Energies*, vol. 16, no. 17, 2023, Art. no. 6106.
- [18] L. Wang, X. Fu, and M.-C. Wong, "Operation and control of a hybrid coupled interlinking converter for hybrid AC/Low voltage DC microgrids," *IEEE Trans. Ind. Electron.*, vol. 68, no. 8, pp. 7104–7114, Aug. 2021.
- [19] H. Xiao, A. Luo, Z. Shuai, G. Jin, and Y. Huang, "An improved control method for multiple bidirectional power converters in hybrid AC/DC microgrid," *IEEE Trans. Smart Grid*, vol. 7, no. 1, pp. 340–347, Jan. 2016.
- [20] M. Schweizer, T. Friedli, and J. W. Kolar, "Comparative evaluation of advanced three-phase three-level inverter/converter topologies against two-level systems," *IEEE Trans. Ind. Electron.*, vol. 60, no. 12, pp. 5515–5527, Dec. 2013.
- [21] J. Xu et al., "A carrier-based two-phase-clamped DPWM strategy with zero-sequence voltage injection for three-phase quasi-two-stage buck-type rectifiers," *IEEE Trans. Power Electron.*, vol. 37, no. 5, pp. 5196–5211, May 2022.
- [22] M. Antvachis, J. A. Anderson, D. Bortis, and J. W. Kolar, "Analysis of a synergetically controlled two-stage three-phase DC/AC buck-boost converter," *CPSS Trans. Power Electron. Appl.*, vol. 5, no. 1, pp. 34–53, Mar. 2020.
- [23] J. Huang et al., "Robust circuit parameters design for the CLLC-type DC transformer in the hybrid AC–DC microgrid," *IEEE Trans. Ind. Electron.*, vol. 66, no. 3, pp. 1906–1918, Mar. 2019.
- [24] R. Zhang, V. Prasad, D. Boroyevich, and F. Lee, "Three-dimensional space vector modulation for four-leg voltage-source converters," *IEEE Trans. Power Electron.*, vol. 17, no. 3, pp. 314–326, May 2002.
- [25] K. Shi, A. Zhao, J. Deng, and D. Xu, "Zero-voltage-switching SiC-MOSFET three-phase four-wire back-to-back converter," *IEEE J. Emerg. Sel. Topics Power Electron.*, vol. 7, no. 2, pp. 722–735, Jun. 2019.
- [26] L. Zhang, H. Yang, Y. Tang, J. Pou, and L. M. Tolbert, "Decoupled modulation with common-mode load-voltage control for three-phase four-leg three-level inverter," *IEEE Trans. Ind. Electron.*, vol. 69, no. 8, pp. 8594–8598, Aug. 2022.
- [27] F. Rojas et al., "An overview of four-leg converters: Topologies, modulations, control and applications," *IEEE Access*, vol. 10, pp. 61277–61325, 2022.
- [28] Y. Yang et al., "A novel continuous control set model predictive control for LC-Filtered three-phase four-wire three-level voltage-source inverter," *IEEE Trans. Power Electron.*, vol. 38, no. 4, pp. 4572–4584, Apr. 2023.

- [29] M.-J. Tsai, H.-C. Chen, and P.-T. Cheng, "Eliminating the neutral-point oscillation of the four-wire NPC active power filter," *IEEE Trans. Power Electron.*, vol. 34, no. 7, pp. 6233–6240, Jul. 2019.
- [30] X. Guo, D. Xu, and B. Wu, "Four-leg current-source inverter with a new space vector modulation for common-mode voltage suppression," *IEEE Trans. Ind. Electron.*, vol. 62, no. 10, pp. 6003–6007, Oct. 2015.
- [31] X. Li, Y. Sun, L. Jiang, H. Wang, Y. Liu, and M. Su, "Common-mode circuit analysis of current-source photovoltaic inverter for leakage current and EMI," *IEEE Trans. Power Electron.*, vol. 38, no. 6, pp. 7156–7165, Jun. 2023.
- [32] M. Khederzadeh and M. Sadeghi, "Virtual active power filter: A notable feature for hybrid AC/DC microgrids," *IET Generation, Transmiss. Distrib.*, vol. 10, no. 14, pp. 3539–3546, 2016.
- [33] J. Zhou et al., "Distributed power sharing control for islanded single-/three-phase microgrids with admissible voltage and energy storage constraints," *IEEE Trans. Smart Grid*, vol. 12, no. 4, pp. 2760–2775, Jul. 2021.
- [34] D. I. Brandao, T. Caldognetto, F. P. Marafão, M. G. Simões, J. A. Pomilio, and P. Tenti, "Centralized control of distributed single-phase inverters arbitrarily connected to three-phase four-wire microgrids," *IEEE Trans. Smart Grid*, vol. 8, no. 1, pp. 437–446, Jan. 2017.
- [35] M. Najafzadeh, R. Ahmadihangar, O. Husev, I. Roasto, T. Jalakas, and A. Blinov, "Recent contributions, future prospects and limitations of interlinking converter control in hybrid AC/DC microgrids," *IEEE Access*, vol. 9, pp. 7960–7984, 2021.
- [36] D. T. Rodrigues, H. K. M. Paredes, C. Burgos, R. L. Lima, and J. P. Bonaldo, "Consensus-based single-phase control of three-phase inverter for current sharing in three-phase four-wire isolated AC microgrids," *IEEE Access*, vol. 10, pp. 108159–108168, 2022.
- [37] S. Rivera, R. Lizana, F. S. Kouro, T. Dragičević, and B. Wu, "Bipolar DC power conversion: State-of-the-art and emerging technologies," *IEEE Trans. Emerg. Sel. Topics Power Electron.*, vol. 9, no. 2, pp. 1192–1204, Apr. 2021.
- [38] D. Kumar, F. Zare, and A. Ghosh, "DC microgrid technology: System architectures, AC grid interfaces, grounding schemes, power quality, communication networks, applications, and standardizations aspects," *IEEE Access*, vol. 5, pp. 12230–12256, 2017.
- [39] S. Beheshtaein, R. M. Czuzner, M. Forouzesh, M. Savaghebi, and J. M. Guerrero, "DC microgrid protection: A comprehensive review," *IEEE J. Emerg. Sel. Topics Power Electron.*, early access, Mar. 12, 2019, doi: [10.1109/JESTPE.2019.2904588](https://doi.org/10.1109/JESTPE.2019.2904588).
- [40] M. Mishra, B. Patnaik, M. Biswal, S. Hasan, and R. C. Bansal, "A systematic review on DC-microgrid protection and grounding techniques: Issues, challenges and future perspective," *Appl. Energy*, vol. 313, 2022, Art. no. 118810.
- [41] European Commission, "Low voltage directive, LVD2006/95/EC," European Union Directive, Brussels, Tech. Rep. OJ L374, 2006, pp. 10–19. [Online]. Available: <http://data.europa.eu/eli/dir/2006/95/oj>
- [42] D. Salomonsson, L. Soder, and A. Sannino, "Protection of low-voltage DC microgrids," *IEEE Trans. Power Del.*, vol. 24, no. 3, pp. 1045–1053, Jul. 2009.
- [43] J. Mohammadi, F. B. Ajaei, and G. Stevens, "Grounding the DC microgrid," *IEEE Trans. Ind. Appl.*, vol. 55, no. 5, pp. 4490–4499, Sep./Oct. 2019.
- [44] D. Jayamaha, N. Lidula, and A. Rajapakse, "Protection and grounding methods in DC microgrids: Comprehensive review and analysis," *Renewable Sustain. Energy Rev.*, vol. 120, 2020, Art. no. 109631.
- [45] A. Y. Farag, D. Biadene, P. Mattavelli, and T. Younis, "Three-phase four-wire bidirectional Y-converter for an enhanced interface between the AC grid and the unipolar DC microgrid," in *Proc. IEEE 8th Workshop Electron. Grid*, 2023, pp. 1–6.
- [46] M. Antivachis, N. Kleynhans, and J. W. Kolar, "Three-phase sinusoidal output buck-boost GaN Y-inverter for advanced variable speed AC drives," *IEEE J. Emerg. Sel. Topics Power Electron.*, vol. 10, no. 3, pp. 3459–3476, Jun. 2022.
- [47] M. Antivachis, D. Bortis, D. Menzi, and J. W. Kolar, "Comparative evaluation of Y-inverter against three-phase two-stage buck-boost DC-AC converter systems," in *Proc. Int. Power Electron. Conf.*, 2018, pp. 181–189.
- [48] S.-J. Chee, S. Ko, H.-S. Kim, and S.-K. Sul, "Common-mode voltage reduction of three-level four-leg PWM converter," *IEEE Trans. Ind. Appl.*, vol. 51, no. 5, pp. 4006–4016, Sep./Oct. 2015.
- [49] M. Hofmann, "Evaluation of potentials for Infineon SiC-MOSFETs in automotive inverter applications," Fraunhofer IISB, Erlangen, Germany, 2018.
- [50] T. P. Chow, I. Omura, M. Higashiwaki, H. Kawarada, and V. Pala, "Smart power devices and ICs using GaAs and wide and extreme bandgap semiconductors," *IEEE Trans. Electron Devices*, vol. 64, no. 3, pp. 856–873, Mar. 2017.
- [51] R. N. Beres, X. Wang, M. Liserre, F. Blaabjerg, and C. L. Bak, "A review of passive power filters for three-phase grid-connected voltage-source converters," *IEEE J. Emerg. Sel. Topics Power Electron.*, vol. 4, no. 1, pp. 54–69, Mar. 2016.
- [52] J. Muhlethaler, M. Schweizer, R. Blattmann, J. W. Kolar, and A. Ecklebe, "Optimal design of LCL harmonic filters for three-phase PFC rectifiers," *IEEE Trans. Power Electron.*, vol. 28, no. 7, pp. 3114–3125, Jul. 2013.
- [53] D. Menzi, J. W. Kolar, and J. Everts, "Single-phase full-power operable three-phase buck-boost Y-rectifier concepts," in *Proc. IEEE Appl. Power Electron. Conf. Expo.*, 2021, pp. 599–606.
- [54] M. Silva, N. Hensgens, J. Oliver, P. Alou, O. Garcia, and J. A. Cobos, "New considerations in the input filter design of a three-phase buck-type PWM rectifier for aircraft applications," in *Proc. IEEE Energy Convers. Congr. Expo.*, 2011, pp. 4087–4092.
- [55] W.-J. Lee and S.-K. Sul, "DC-link voltage stabilization for reduced DC-Link capacitor inverter," *IEEE Trans. Ind. Appl.*, vol. 50, no. 1, pp. 404–414, Jan./Feb. 2014.
- [56] A. Mallik and A. Khaligh, "Intermediate DC-link capacitor reduction in a two-stage cascaded AC/DC converter for more electric aircrafts," *IEEE Trans. Veh. Technol.*, vol. 67, no. 2, pp. 935–947, Feb. 2018.
- [57] Z. Li, M. Shahidepour, F. Aminifar, A. Alabdulwahab, and Y. Al-Turki, "Networked microgrids for enhancing the power system resilience," *Proc. IEEE*, vol. 105, no. 7, pp. 1289–1310, Jul. 2017.
- [58] F. Nejabatkhah, Y. W. Li, and H. Tian, "Power quality control of smart hybrid AC/DC microgrids: An overview," *IEEE Access*, vol. 7, pp. 52295–52318, 2019.
- [59] S. K. Sahoo, A. K. Sinha, and N. K. Kishore, "Control techniques in AC, DC, and hybrid AC-DC microgrid: A review," *IEEE J. Emerg. Sel. Topics Power Electron.*, vol. 6, no. 2, pp. 738–759, Jun. 2018.
- [60] S. Vazquez, J. Rodriguez, M. Rivera, L. G. Franquelo, and M. Norambuena, "Model predictive control for power converters and drives: Advances and trends," *IEEE Trans. Ind. Electron.*, vol. 64, no. 2, pp. 935–947, Feb. 2017.
- [61] Z. Ali, N. Christofides, L. Hadjidemetriou, E. Kyriakides, Y. Yang, and F. Blaabjerg, "Three-phase phase-locked loop synchronization algorithms for grid-connected renewable energy systems: A review," *Renewable Sustain. Energy Rev.*, vol. 90, pp. 434–452, 2018.
- [62] M. Antivachis, D. Bortis, L. Schrittwieser, and J. W. Kolar, "Three-phase buck-boost y-inverter with wide DC input voltage range," in *Proc. IEEE Appl. Power Electron. Conf. Expo.*, 2018, pp. 1492–1499.



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