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Design of an Extendable High Boost Multi-Port Z-Network Converter for Small Power Grid-Connected PV Applications

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ABSTRACT Using the Z-network idea and conventional isolated power converters as its foundation, this article introduces a multi-port converter. This article proposes a topology that is called Multi-Port Z-Network Converter (MPZNC). A grid-connected inverter can include *N* input sources into a single DC bus using the suggested topology. Bypassing the input and output circuits was another capability it possessed with the boost function. Compared to traditional converters, these one-use fewer parts to integrate various energy sources. Consequently, it has better circuit properties and achieves higher conversion efficiencies. In comparison to the standard Z-Source Converter (ZSC), it improves the input-output voltage transformation ratio and provides a wider voltage control range. The circuit design, operating principle, control mechanism, and simulation data have been presented to prove technically possible. To investigate the suggested MPZNC-fed Single Phase Five Level (SPFL) inverter in the given scenario, a 1.5 kW, 230 V, 50 Hz miniature laboratory study model was created. According to the findings, the suggested converter has an efficiency of around 93% and provides double the amount of boosting time as the standard ZSC converter.

INDEX TERMS DC-DC converter, grid-connected connected PV system, high boost isolated converter, multi-port Z-netwok converter (MPZNC), photovoltaic system, single phase five level (SPFL) inverter.

I. INTRODUCTION

The power demand is rising sharply due to factors such as growing populations, more industrial operations, more office space, and more data centers. To this day, power stations that burn fossil fuels provide a major part of the world's energy consumption [1]. The combustion of fossil fuels intensifies various environmental issues. Renewable Power Generation Systems (RPGS) are the better option for reducing greenhouse gas emissions and reducing the severity of climate change [2]. When it comes to addressing energy and environmental issues on a global scale, Photovoltaic (PV) and wind power are the two most accessible, versatile, and effective renewable energy sources are indispensable [3], [4]. A lot of technical problems arise while using multi-array Photovoltaic (PV) power-producing technology on a big scale. Linking several renewable energy sources to a central DC bus is one of these challenges. Several separate power converters link different kinds of energy sources to a common DC bus in the conventional hybrid design. This leads to higher expenses, higher output volume, and worse conversion efficiency [5].

Over the last several decades, power electronic converters have been the focus of extensive study and development. Innovative methods and topologies are still needed to reduce the size, weight, and price of the conversion system while increasing its efficiency and dependability [6]. A Z-source converter is usually prepared to address the issue of input voltage fluctuations and low magnitude. In 2002, Peng set out to address the shortcomings of conventional power electronics converters by developing the Z-Source Converter (ZSC). To make this concept into a dc-dc converter, the newly added Z-source impedance network has to be short-circuited for a

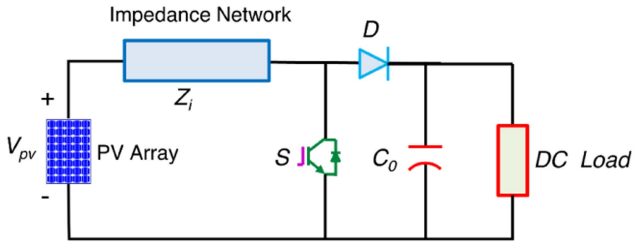


FIGURE 1. Standard Z-netwok converter with two ports.

certain duty ratio during each switching interval. Thus, the fundamental working principles are unaltered; the sole modification is a converter bridge at the back end that is designed to maximize dc-dc conversion.

Building on the popular idea of the Z-source DC connection, the series Z-source network was designed to increase the voltage output of power electronic inverters [7]. To achieve the boost and buck operation, engineers created a novel dc-dc converter with an isolated transformer that uses a distributed impedance-source network [8]. A multitude of inductors and capacitors comprise the dispersed impedance. Using switching Z-source or quasi-Z-source dc-dc converters is advised for the PV grid-connected power system [9]. By reducing the number of switches required to achieve buck and boost operation, Z-source matrix converters can get around the voltage gain constraint that traditional matrix converters have [10]. A coupled transformer-based Z-source converter with high boost gain has been designed. Increasing the turns ratio of the transformer also results in an improved gain factor [11]. It makes the converter's design simpler, which in turn lowers the production costs. A hybrid Z-source boost dc-dc converter is crafted for solar applications that necessitate high step-up dc-dc converters to elevate the low-source voltages to a specifically specified grid voltage. The boost capabilities of conventional Z-source networks can be enhanced by combining existing Z-source networks in various ways to create a hybrid converter architecture [12]. This is crucial since the boost potential of conventional Z-source networks is low. A quasi-z-source isolated bidirectional dc-dc converter has been developed for use in renewable energy applications [13]. Several upgraded Z-source dc-dc converters are made, allowing for increased voltage amplification and high-power density [14]. A high boost factor may be achieved using one of three topologies for dc-dc boost converters that use Z-source switched-capacitor technology [15]. The three-port converter has been proposed by several writers as a means to connect PV systems to the grid. When contrasted with the converter setup that is recommended, these converters have the following drawbacks.

1) Component saturation and poor performance are consequences of the conventional boost converter's low boost gain at high-duty ratios. The conventional boost converter has a limited number of input sources that it can combine with its output.
2) There is no way to separate the input and output signals.

The proposed model has the following advantages:

1) A larger boost factor can be achieved with the proposed Z-Netwok converter than the typical boost converter. This aids in providing a lower duty ratio with a larger boost factor.
2) The suggested setup could be easily modified to integrate an N-number of power sources sharing a single DC bus. It gets rid of the requirement for a DC-DC converter that is independent of the number. It contributes to lower system costs and more efficient conversions.

As shown in Fig. 1, the conventional two-port conventional Z-Netwok converter employs a diode, an impedance network, and a switch.

To connect numerous energy sources with a shared DC bus, this study delves into the creation of an innovative and effective Multi-Port Z-Netwok Converter (MPZNC). This section delves into the design, operational modes, and implementation of the Three-Port Z-Netwok Converter (TPZNC)-based Single-Phase Five-Level (SPFL) inverter. The software and hardware models of 1.5 kW, 230 V, and 50 Hz are built to confirm the proposed topology's dynamic behavior. The proposed TPZNC-based SPFL inverter outperformed the others in terms of raising the output voltage across all test scenarios. There are eight parts to this paper: After the introduction in Section I, the proposed converter-fed SPFL inverter's system description and operation are given in Section II. Section III presents the relationship between voltage gain and duty ratio. Section IV presents the control systems of the suggested paradigm. Section V presents and discusses the findings of the simulation and the experiments. Section VI presents the conclusion as a last point.

II. OPERATION OF PROPOSED MPZNC

Fig. 2 shows the grid-connected PV system that is being proposed, which is based on an N-Port Z-Netwok Converter (NPZNC) operated SPFL inverter. It consists of an impedance network with N nodes, a rectifier with voltage doubler functionality, a high-frequency transformer with multiple inputs, and an inverter using SPFL technology. The size and expense of the device are both increased by using two winding high-frequency transformers. With the multi-input high-frequency transformer, the dc-dc converter may be made smaller and cheaper. The proposed converter combines the best features of an active interleaved flyback with those of a Z-Netwok converter. The proposed converter takes electricity from many separate input ports and independently boosts each one to achieve the necessary boost factor. A two-port impedance network is being studied for implementation to decrease the design's complexity. Fig. 3, presents the three-port Z-Netwok converter that was thought of for the study and implementation.

A. TPZNC UNDER POSITIVE HALF CYCLE

At t_0 in Fig. 4(a), the capacitors C_{a1} and C_{a2} are charged by the input source V_{pv1}, the inductors L_{a1} and L_{a2} of the

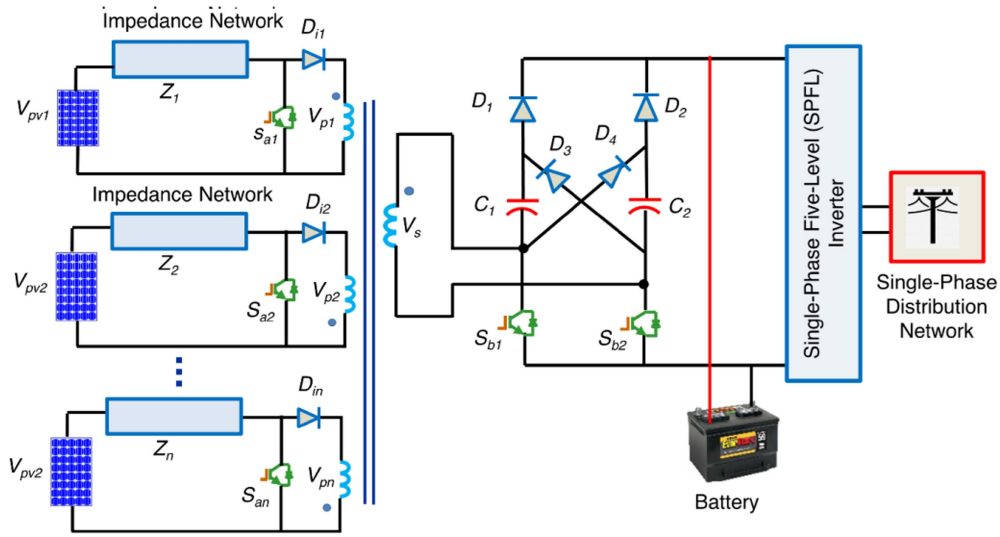


FIGURE 2. Proposed *N*-port *Z*-network converter.

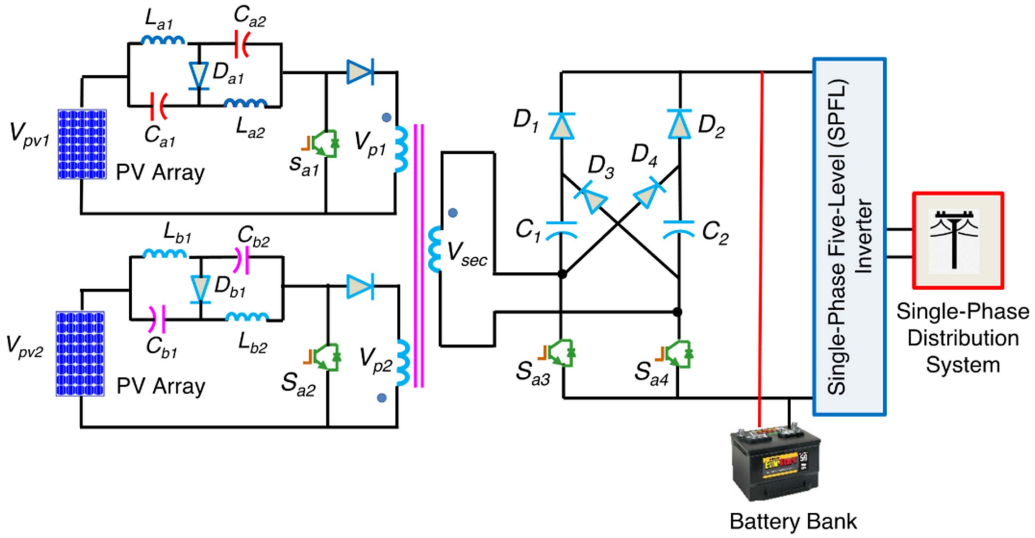


FIGURE 3. Proposed multi-port *Z*-network converter.

impedance network charge the capacitors, and S_{a2}, S_2 and S_6 are activated. The primary voltage of the transformer (V_{p1}) is equal to the input voltage (V_{pv1}) plus voltage across inductors (L_{a1} and L_{a2}).

At this point, the voltage across the transformer, V_{p2}, is zero, therefore the capacitor C_2 gets charged by the secondary side of the transformer via diode D_4. Capacitor C_5 drain slope is defined by the inverter's output voltage, V_{inv}. One way to express the capacitor voltage of the network is as follows.

$$V_{Ca1} = V_{La1} = V_{Ca2} = V_{La2} \tag{1}$$

$$V_{Ca1} = V_{Ca2} = \frac{d_{sa1}}{1 - 2d_{sa1}} V_{pv1} \tag{2}$$

This is the way that the inductors' voltage can be expressed:

$$V_{Lb1} = V_{Cb2} + V_{pv2} \tag{3}$$

$$V_{Lb2} = V_{Cb1} + V_{pv2} \tag{4}$$

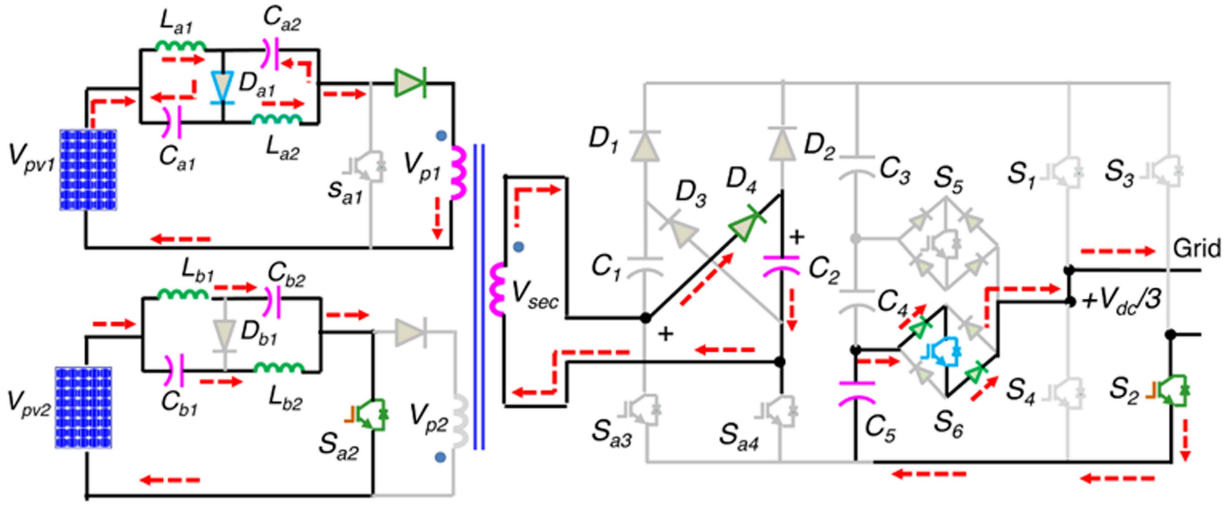
Also, the transformer and inverter's voltages are written as

$$V_{p1} = V_{pv1} + V_{La1} + V_{La2} \tag{5}$$

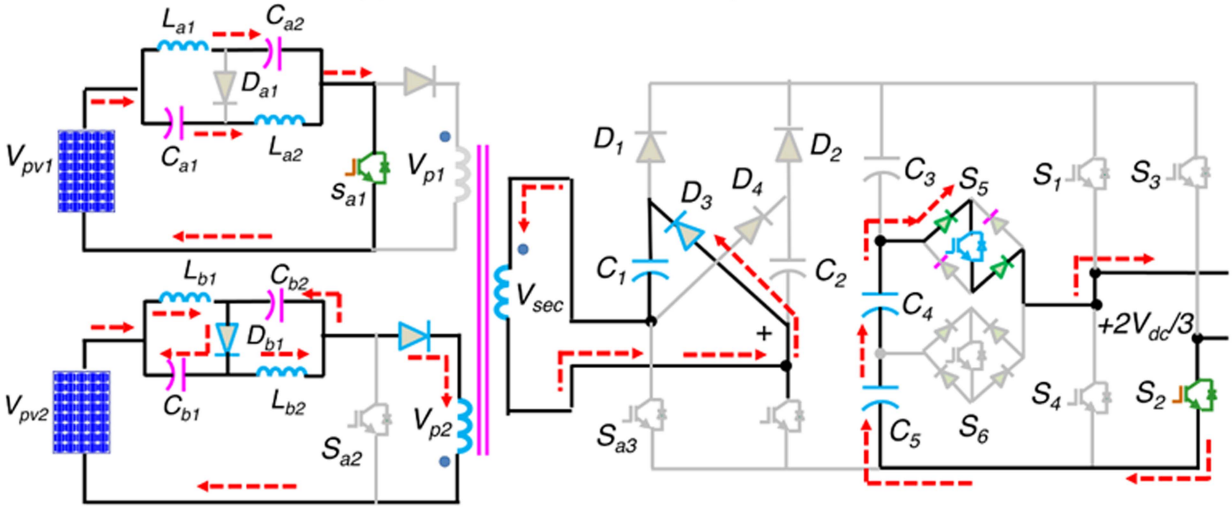
$$V_{\text{sec}} = V_{c2} = \left(V_{pv1} + V_{La1} + V_{La2}\right) n = nV_{p1} \tag{6}$$

$$V_{inv} = +\frac{V_{dc}}{3} \tag{7}$$

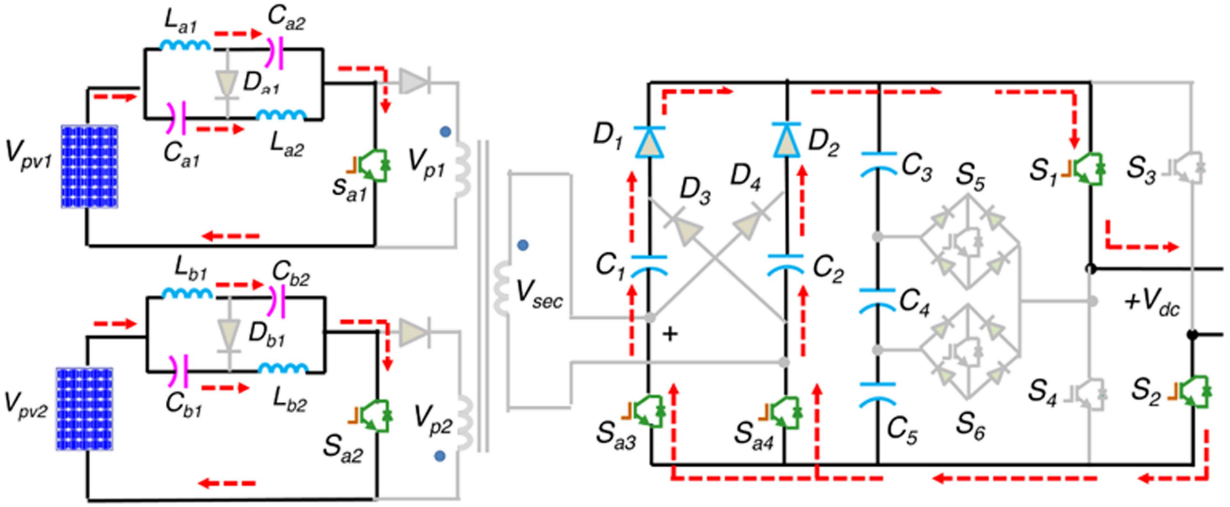
In Fig. 4(b), the second subinterval, shown by the time interval [t_1–t_2], shows that switches S_{a1}, S_2, and S_5 are all conducting at the same moment. This results in the current charging of inductor L_{a1} and inductor L_{a2} and the discharge of inductor L_{b1} and inductor L_{b2}, respectively. So, the input voltage of primary 2 plus the total of V_{Lb1} and V_{pv2} is $n(V_{pv2}+V_{Lb1})$, which is a multiple of n and charges C_1. Fig. 4(b) shows that the secondary current flowing through the



(a) 1st interval of a +ve half cycle

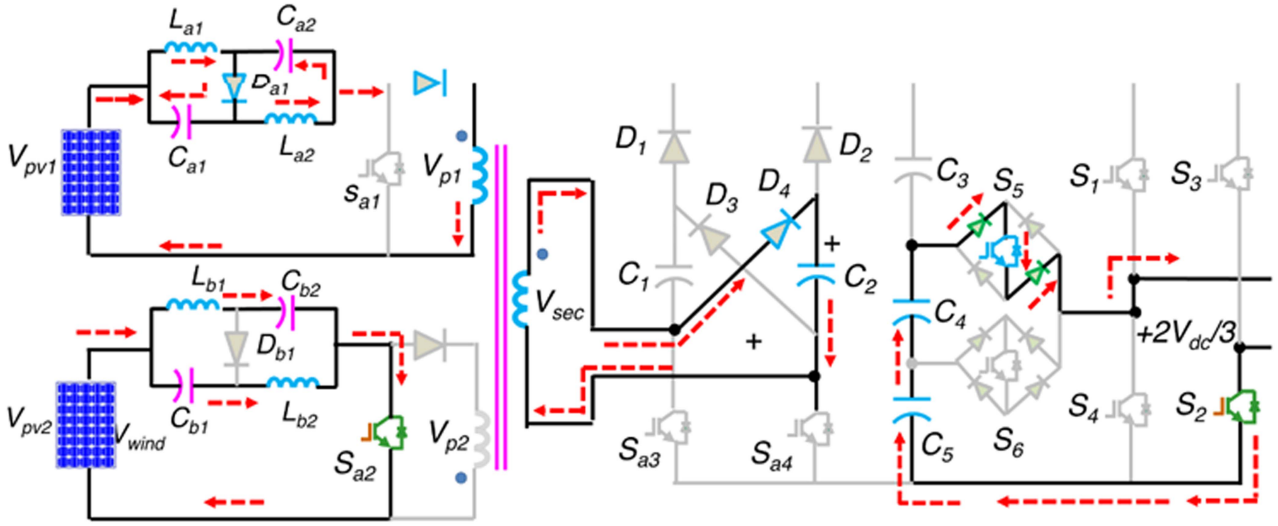


(b) 2nd interval of a +ve half cycle

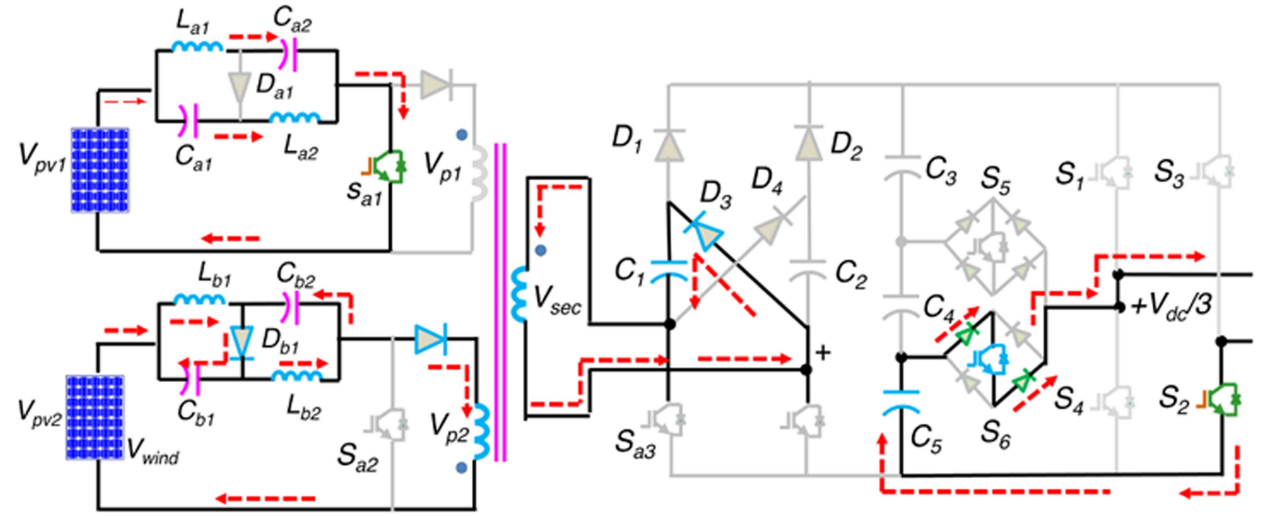


(c) 3rd interval of a +ve half cycle

FIGURE 4. Proposed TPZNC fed SPFL inverter operation under positive half cycle.



(d) 4th interval of a +ve half cycle



(e) 5th interval of a +ve half cycle

FIGURE 4. ***CONTINUE***

transformer is negative. The slope utilized to drain capacitors C_4 and C_5 is determined by the voltage present at the output of the SPFL inverter. The voltage output across the inverter circuit's terminals is set to $+2V_{dc}/2$. The following expression represents the capacitors' voltage of the network:

$$V_{Cb1} = V_{Lb1} = V_{Cb2} = V_{Lb2} \tag{8}$$

$$V_{Cb1} = V_{Cb2} = \frac{d_{sa2}}{1 - 2d_{sa2}} V_{pv2} \tag{9}$$

Similarly, the inductors' voltage is expressed:

$$V_{La1} = V_{Ca2} + V_{pv1} \tag{10}$$

$$V_{La2} = V_{Ca1} + V_{pv1} \tag{11}$$

Also, the transformer voltage and inverter are expressed as

$$V_{p2} = V_{pv1} + V_{Lb1} + V_{Lb2} \tag{12}$$

$$V_{\text{sec}} = V_{c1} = (V_{pv2} + V_{Lb1} + V_{Lb2})n = nV_{p2} \tag{13}$$

$$V_{inv} = +\frac{2V_{dc}}{3} \tag{14}$$

In the subinterval $[t_2–t_3]$, the inductors L_{a1}, L_{a2}, L_{b1}, and L_{b2} will keep being charged, as shown in Fig. 4(c), until the switches S_{a1} and S_{a2} are off at t_3. Simultaneously, all magnetic fields are removed from capacitors C_1 and C_2. Capacitors C_1 and C_2 supply power to the AC load/grid by charging capacitors C_3, C_4, and C_5 on the dc bus. A reading of $+V_{dc}$ is produced by the inverter's output terminals due to

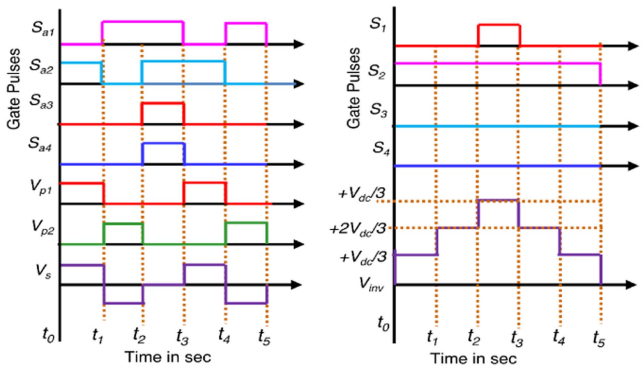


FIGURE 5. Switching patterns and output of MPZNC and SPFL inverter during +ve half cycle.

TABLE 1 Positive Half-Cycle Switching Pattern

Switches										V_{inv}
S_{a1}	S_{a2}	S_{a3}	S_{a4}	S_1	S_2	S_3	S_4	S_5	S_6	
OFF	ON	OFF	OFF	OFF	ON	OFF	OFF	OFF	ON	$+V_{dc}/3$
ON	OFF	OFF	OFF	OFF	ON	OFF	OFF	ON	OFF	$+2V_{dc}/3$
ON	ON	ON	ON	ON	ON	OFF	OFF	OFF	OFF	$+V_{dc}$
ON	OFF	OFF	OFF	OFF	ON	OFF	OFF	ON	OFF	$+2V_{dc}/3$
OFF	ON	OFF	OFF	OFF	ON	OFF	OFF	OFF	ON	$+V_{dc}/3$

the circuitry's design. The inductors' voltage are expressed as follows:

$$V_{La1} = V_{Ca2} + V_{pv1} \tag{15}$$

$$V_{La2} = V_{Ca1} + V_{pv1} \tag{16}$$

$$V_{Lb1} = V_{Cb2} + V_{pv2} \tag{17}$$

$$V_{Lb2} = V_{Cb1} + V_{pv2} \tag{18}$$

$$V_{inv} = +V_{dc} \tag{19}$$

Figs. 4 and 5 demonstrate the positive half-cycle basic operating waveforms and similar circuits, respectively. Except for the SPFL inverter, the TPZNC operation during subintervals 4 and 5 are identical to the subintervals 1 and 2. To provide an output of $+2V_{dc}/3$, the switches S_5 and S_2 are energized during the subinterval $[t_3–t_4]$. An output of $+V_{dc}/3$ is produced when the switches S_2 and S_6 are turned on during the subinterval that spans t_4 and t_5. The gate pulses and SPFL output for the first five periods are illustrated in Fig. 5. Table 1 displays the switching table that is by the positive half cycle of the SPFL inverter output. The output voltage of the SPFL inverters for different subintervals is listed in Table 1.

B. TPZNC UNDER NEGATIVE HALF CYCLE

The capacitors C_{a1} and C_{a2} are charged by the input source V_{pv} at t_0, and the inductors L_{a1} and L_{a2} charge them as well. From Fig. 6(a) when the switches S_{a2}, S_3, and S_5 are activated, the inductors L_{a1} and L_{a2}, get the primary voltage of the transformer. V_{p2}, the voltage across the transformer, remains at 0 V during this period. Capacitor C_2 may be charged to a voltage of nV_{sec} by the transformer secondary winding, thanks to diode D_4. The output voltage V_{inv} of the SPFL inverter determines how much current flows into capacitor C_3. Comparable to subinterval 1 in Section II-A, an expression for the voltage across the TPZNC elements is given in this section.

$$V_{inv} = -\frac{V_{dc}}{3} \tag{20}$$

The time when all three switches S_{a1}, S_3, and S_6 are conducted is included by the second subinterval, $[t_1–t_2]$ in Fig. 6(b). Loaded into L_{a1} and L_{a2} are thus the resulting energy transmitters and receivers. The charge on capacitor C_1 is $n(V_{wind}+V_{Lb1}+ V_{Lb2})$. A negative current passes via the transformer's secondary winding, as shown in Fig. 6(b). The output voltage of the SPFL inverter is used to determine the discharge slope of capacitors C_2 and C_3. The voltage produced by the SPFL inverter circuit's output terminal layout is shown in (21).

$$V_{inv} = -\frac{2V_{dc}}{3} \tag{21}$$

From Fig. 6(c), the impedance network's inductors L_{a1}, L_{a2}, L_{b1}, and L_{b2} are continuously charged during $[t_2–t_3]$ subinterval until the t_3 shutoff of S_{a1} and S_{a2}. Further, the electrostatic charges in capacitors C_1 and C_2 are eliminated. Two capacitors, C_1 and C_2, charge capacitors C_3, C_4, and C_5, which then supply power to the grid and AC load. Given the configuration of the SPFL inverter's circuit, it is feasible to read $-V_{dc}$ from the terminals while the device is operating. A graphical depiction of the grid voltage may be generated by employing the following notation.

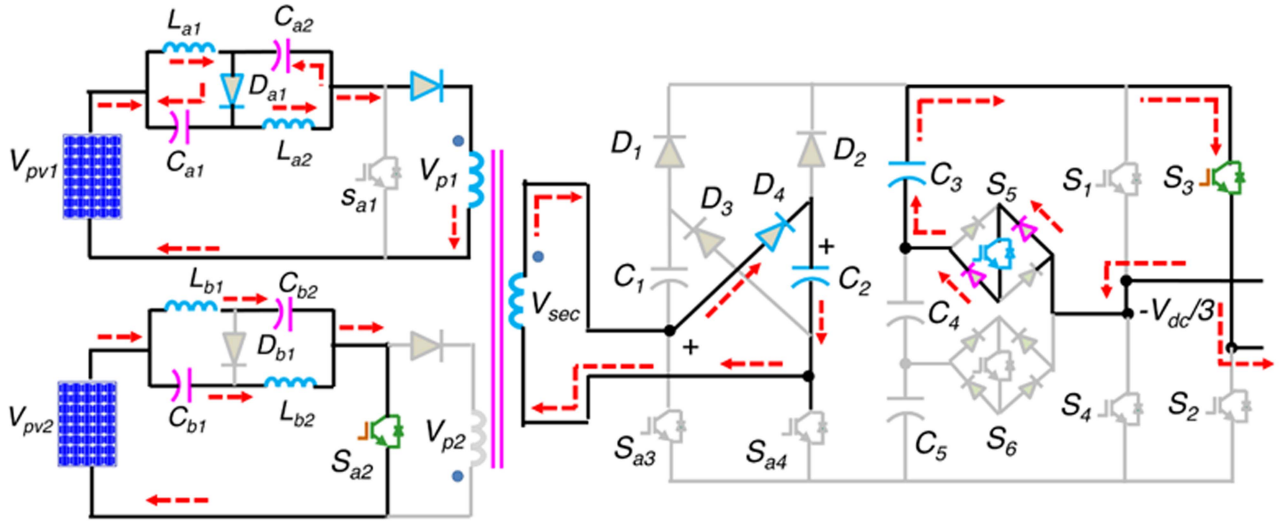
$$V_{inv} = -V_{dc} \tag{22}$$

Figs. 6 and 7 show the same circuits and the related waveforms involved during the negative half cycle. Except the SPFL inverter, the TPZNC's operation in subintervals 4 and 5 is quite comparable to that in subintervals 1 and 2. Between time intervals t_3 and t_4, the switches S_3 and S_6 are turned on to permit an output adjustment to $-2V_{dc}/3$. During the subinterval that spans from t_4 to t_5, the switches S_3 and are turned on, leading to an output of $-V_{dc}/3$. The output of the SPFL, waveforms of the transformer, and gate pulses from the second five periods of the experiment are shown in Fig. 7. The current waveform and the inductors' voltage are also depicted in Fig. 8.

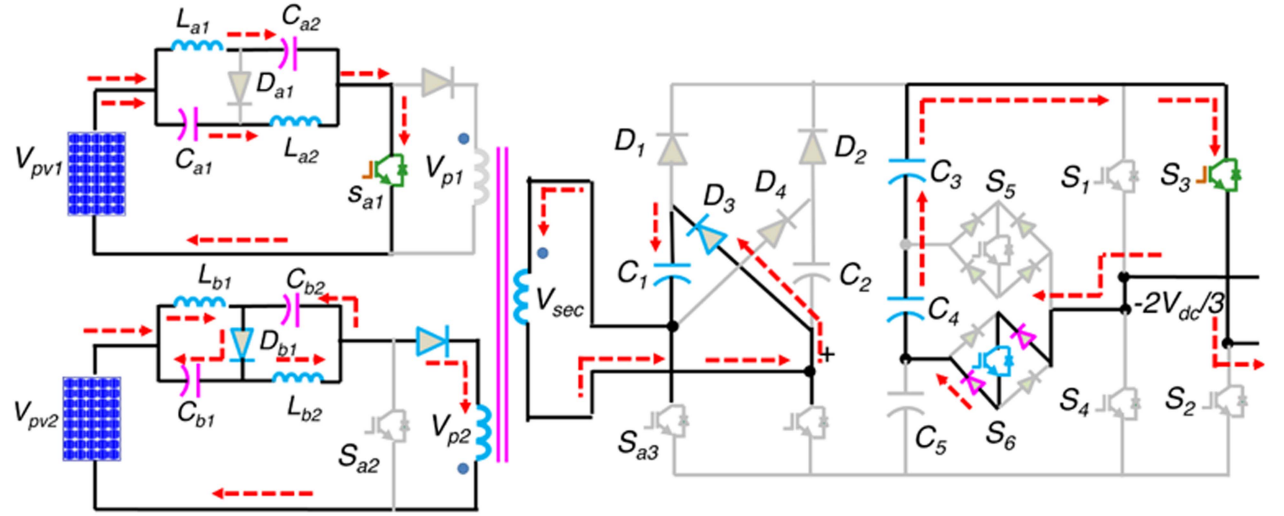
For the negative half cycle, the switching table is shown in Table 2. As can be seen from the table, the SPFL inverter's output voltage is divided into several subintervals.

C. SMALL-SIGNAL MODEL OF MPZNC

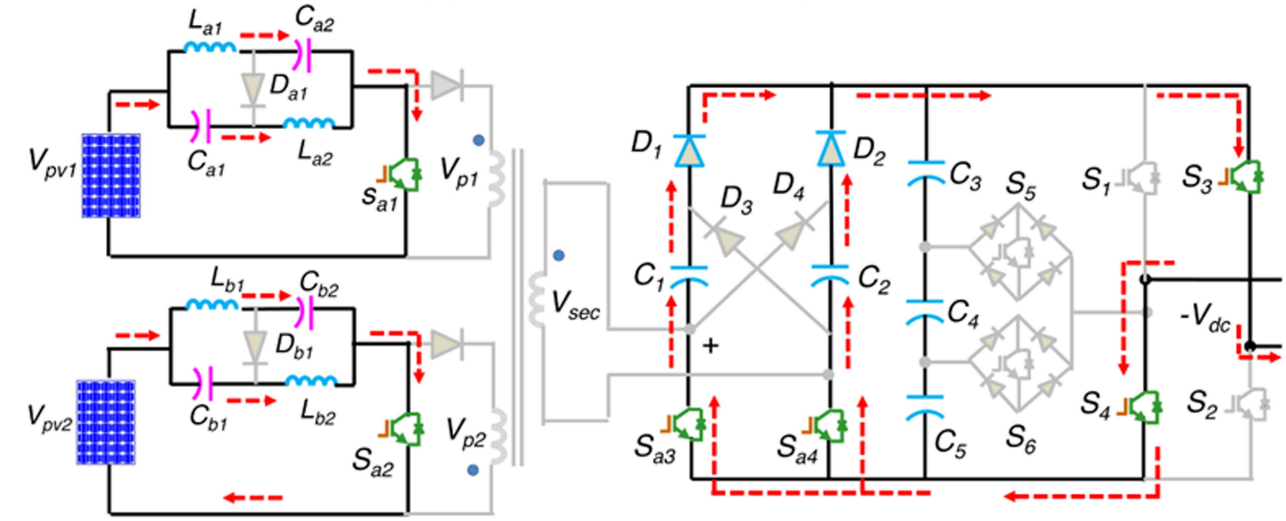
For the derivation of the small signal model, it is assumed that the diodes and switches of the proposed multi-port Z-network converter are ideal or lossless and that each inductor and capacitor have an equivalent series resistance. The



(a) 1st interval of a -ve half cycle

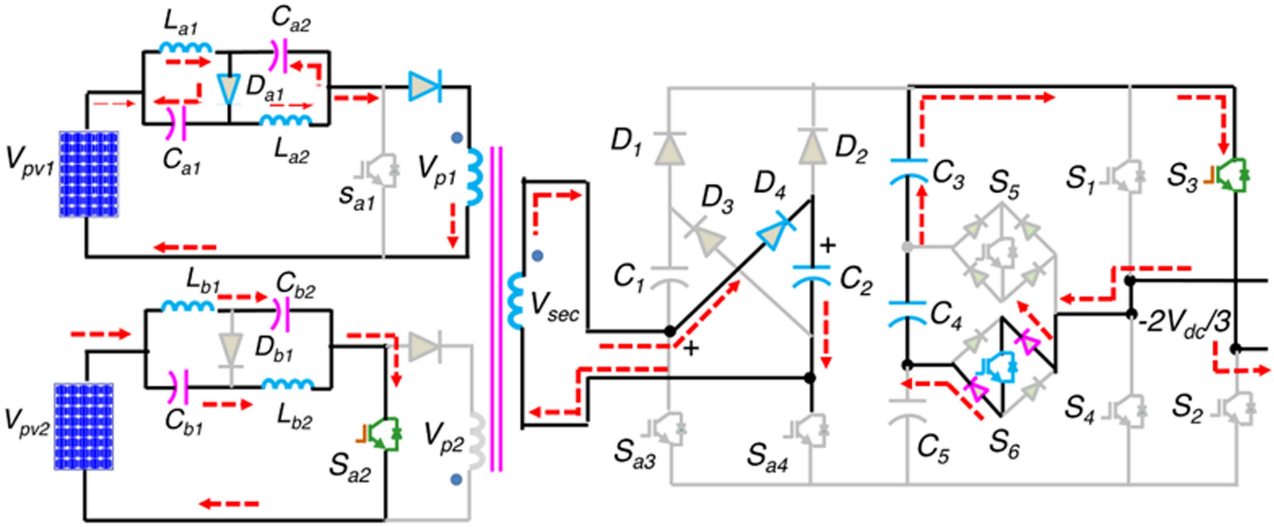


(b) 2nd interval of a -ve half cycle

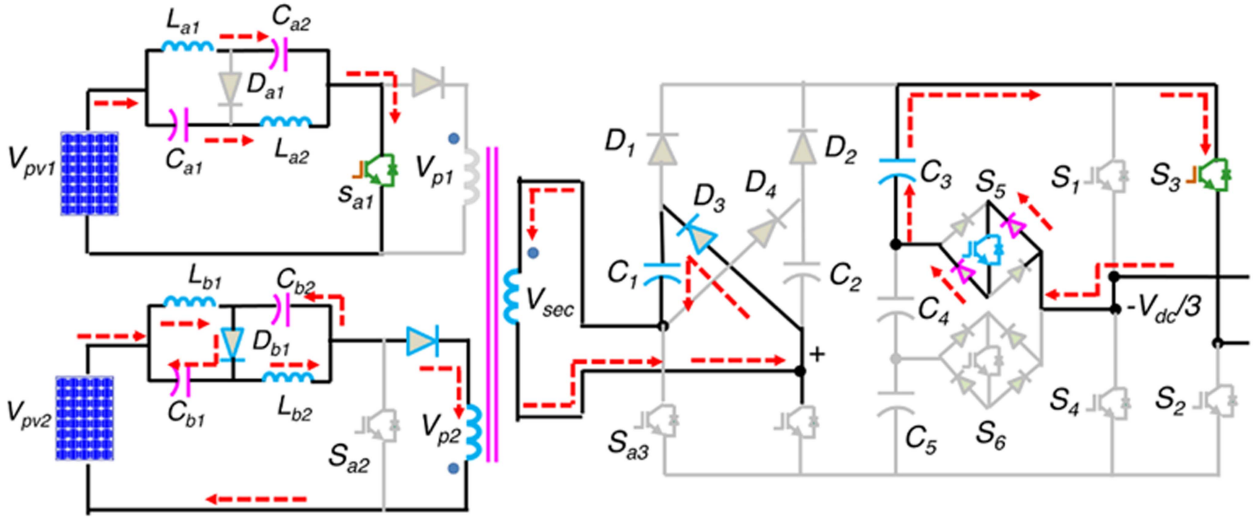


(c) 3rd interval of a -ve half cycle

FIGURE 6. **Proposed TPZNC fed SPFL inverter operation under negative half cycle.**



(d) 4th interval of a -ve half cycle



(e) 5th interval of a -ve half cycle

FIGURE 6. *CONTINUE*

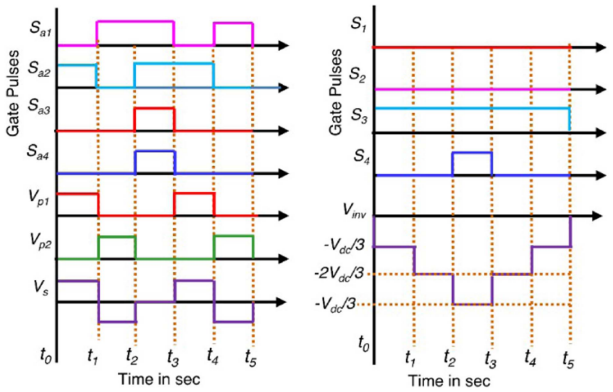


FIGURE 7. **Switching patterns and output of TPZNC and SPFL inverter during a -ve half cycle.**

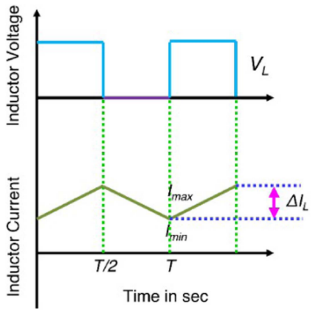


FIGURE 8. **Voltage and current waveform of inductor.**

concept of circuit averaging is used in the development of the small signal model of the proposed MPZNC. The small

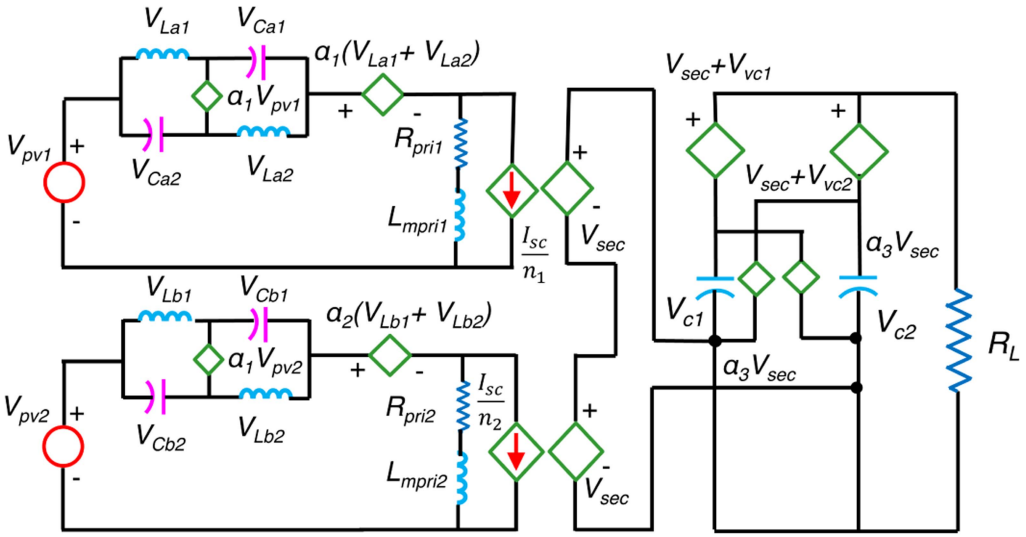


FIGURE 9. Small signal model of the proposed Multi-Port Z-Network Converter (MPZNC) showing DC and AC small-signal components.

TABLE 2 Negative Half-Cycle Switching Pattern

S_{a1}	S_{a2}	S_{a3}	S_{a4}	S_1	S_2	S_3	S_4	S_5	S_6	V_{inv}
OFF	ON	OFF	OFF	OFF	OFF	ON	OFF	ON	OFF	$-V_{dc}/3$
ON	OFF	OFF	OFF	OFF	OFF	ON	OFF	OFF	ON	$-2V_{dc}/3$
ON	ON	ON	ON	OFF	OFF	ON	ON	OFF	OFF	$-V_{dc}$
ON	OFF	OFF	OFF	OFF	OFF	ON	OFF	OFF	ON	$-2V_{dc}/3$
OFF	ON	OFF	OFF	OFF	OFF	ON	OFF	ON	OFF	$-V_{dc}/3$

signal model of the MPZNC consists of Direct Current (DC) and high-frequency alternating current (AC) versions of the MPZNC as illustrated in Fig. 9. Expressions for the average switching voltage and the primary currents of the transformer are provided in (23) to (26), respectively.

It is clear that the averaged switch current, denoted by I_{Sa1} and I_{Sa2} is the function of the input currents, denoted by I_{pv1} and I_{pv2}, but the averaged diode voltage, denoted by V_{Da1} and V_{Db1} are defined in terms of the input voltage, denoted by V_{pv1} and V_{pv2}. Because of this, the three-port switching network that consists of the IGBT and the diode may be substituted by sources of regulated current and voltage, respectively. In line with (26) and (28), respectively, the IGBT is substituted with a current-controlled current source, and the diode is substituted with a voltage-controlled voltage source. The subsequent study that is pertinent to the creation of the small-signal model assumes the following assumptions at various points in time:

1) Continuous Conduction Mode (CCM) is the mode in which the converter works.
2) The high-frequency transformer is ideal; that is, its magnetizing inductance is limitless, its leakage inductances are zero, and the stray capacitances are not taken into consideration.
3) The transformer has an unlimited magnetizing inductance, and it does not store any energy but uses it to generate electricity. As a result, the magnetizing inductance does not play a role in determining the order of the transfer functions.

By adding small-signal perturbations that are overlaid on the DC currents, voltages, and duty cycle, the averaged model is disrupted. The terms d_1, d_2, V_{pv1}, V_{pv1}, i_{pv1}, and i_{pv2} refer to the perturbations that occur in the duty cycle of S_{a1} and S_{a2}, input voltage and input current, accordingly respectively.

$$V_{Sa1} = V_{La1} + \alpha_1 V_{pv1} + V_{La2} + \alpha_1(V_{La1} + V_{La2}) \quad (23)$$

$$V_{Sa2} = V_{Lb1} + \alpha_2 V_{pv2} + V_{Lb2} + \alpha_2(V_{Lb1} + V_{Lb2}) \quad (24)$$

The primary 1 current of the transformer referred to as the secondary can be expressed as

$$I_{pri1} = \frac{I_{sc}}{n_1} \quad (25)$$

The primary 2 currents of the transformer referred to as the secondary can be expressed as

$$I_{pri2} = \frac{I_{sc}}{n_2} \quad (26)$$

By applying KVL to the output loop comprising of the secondary winding, voltage doubler, and the load are expressed as

$$V_L = V_{\text{sec}} + V_{c1} = V_{\text{sec}} + V_{c2} \quad (27)$$

where the coefficients α_1 and α_2 are expressed as

$$\alpha_1 = \frac{n_1 V_{pv1}}{[1-(1+n_1)d_{a1}]^2} \quad (28)$$

$$\alpha_2 = \frac{n_2 V_{pv2}}{[1-(1+n_2)d_{a2}]^2} \quad (29)$$

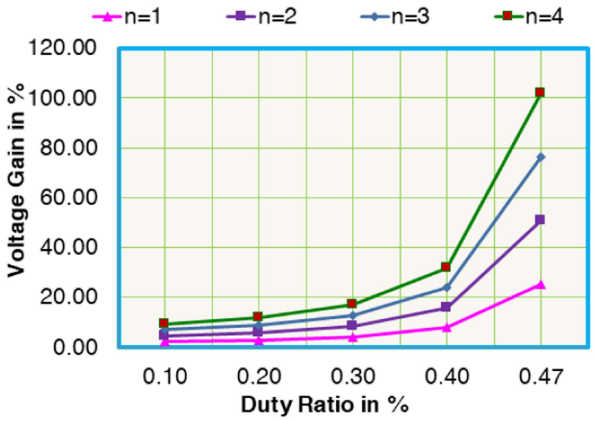


FIGURE 10. Voltage gains of the TPZNC.

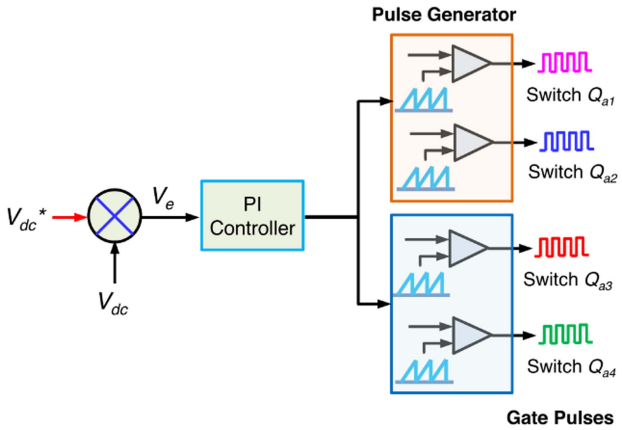


FIGURE 11. TPZNC voltage control scheme.

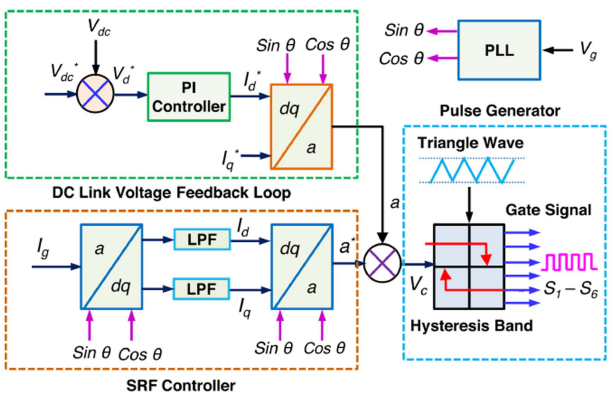


FIGURE 12. Hysteresis band-based SRF control scheme for SPFL inverter.

D. RELATION BETWEEN VOLTAGE GAIN AND DUTY RATIO

At steady state, the proposed converter to facilitate better comprehension of the function, $L_{a1} = L_{a2} = L_{b1} = L_{b2}$ and $C_{a1} = C_{a2} = C_{a3} = C_{a4}$ are examples of when the Z- network treats the inductance and capacitor values as being identical. During continuous conduction mode, the TPZNC operation is

TABLE 3 Experimental Model Design Parameters

Element	Value	Element	Value
L_{a1}, L_{a2}, L_{b1} and L_{b2}	40 µH	Grid Voltage	230 V
C_{a1}, C_{a2}, C_{b1} and C_{b2}	100 µF	Supply Frequency	50 HZ
Transformer	1.5 kVA	Maximum Power	150 W
V_{p1}, V_{p2}	200 V	Open Circuit Voltage	22.5 V
V_{sec}	400 V	Short Circuit Current	8.81 A
Turns Ratio	1:2	Voltage at maximum power	17.96 V
C_1 and C_2	100 µF	Load Resistance	230 Ω
C_3, C_4 and C_5	0.114 µF	Load Inductance	0.114 mH

demonstrated with Figs. 4 and 6. As seen in analogous circuits of two different modes, turning on S_{a1} and S_{a2} switches activates D_{a1}, D_{a2}, D_{a3}, and D_{a4} diodes when the capacitors are connected in reverse parallel. While V_{pv} and C_{a2} at the input charge L_{a1}, they charge L_{a2} at the output. Concurrently, the load is being supplied by V_{pv} via D_{a2}. At steady-state, the equations $V_{La1} = V_{pv} + V_{Ca2}$, $V_{La2} = V_{pv} + V_{Ca1}$, and $V_p = V_{pv} + V_{La1} + V_{La2}$ are constructed using Kirchhoff's law. *Sa1* deactivated, D_{a1} and D_{b1} take over as active, D_{a2} and D_{b2} switch to reverse blocker, L_{a1} charges C_{a2}, L_{a2} charges C_{a1}, $V_{pv,}$ and L_{a1} are linked in series with L_{a2} to supply the charges to primary 1 of the transformer, as shown in Fig. 6. Capacitors C_1 and C_2 receive their power from the secondary. Hence, the following are some relevant equations:

$$V_{Ca1} = V_{Ca2} = \frac{V_{pv1} D_{sa1}}{1 - D_{sa1}} \tag{30}$$

$$V_{Cb1} = V_{Cb2} = \frac{V_{pv2} D_{sa2}}{1 - D_{sa2}} \tag{31}$$

To determine the input voltage of the transformer's primary, one can use (32) and (33).

$$V_{p1} = V_{pv} + V_{La1} + V_{La2} = \frac{2 - D_{sa1}}{1 - D_{sa1}} V_{pv1} \tag{32}$$

$$V_{p2} = V_{wind} + V_{Lb1} + V_{Lb2} = \frac{2 - D_{sa2}}{1 - D_{sa2}} V_{pv2} \tag{33}$$

$$V_{\text{sec}} = \left(\frac{2 - D_{sa1}}{1 - D_{sa1}} V_{pv1}\right) 2 = \left(\frac{2 - D_{sa2}}{1 - D_{sa2}} V_{pv2}\right) 2 \tag{34}$$

Equation (28) provides an expression for the output voltage of the proposed TPZNC.

$$V_o = \left(\frac{4 - 2D_{sax}}{1 - D_{sax}} V_{in}\right) \tag{35}$$

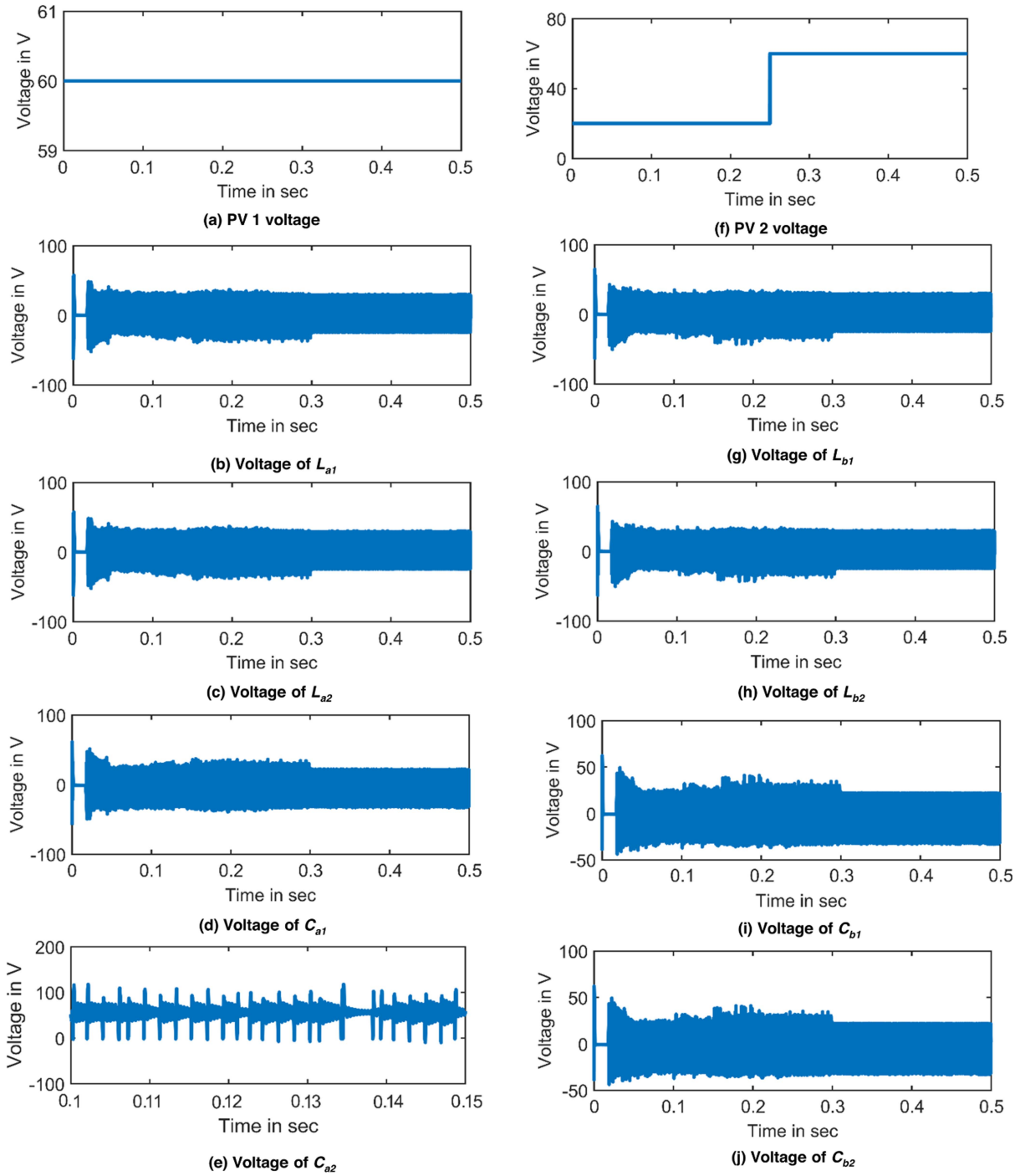


FIGURE 13. Results of active and passive elements of impedance network obtained through simulation study.

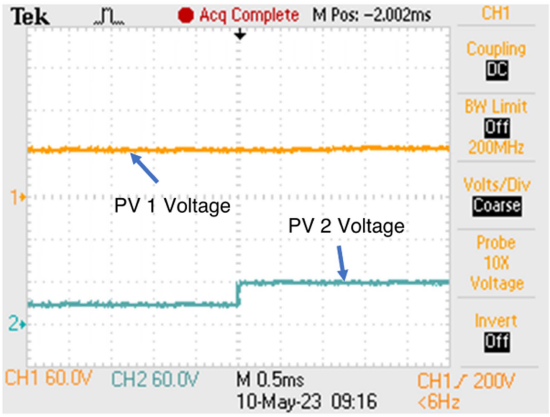
Here is an equation that represents the voltage gain (V_{gain}) of the proposed TPZNC.

$$V_{gain} = \frac{V_o}{V_{in}} = \left(\frac{4 - 2D_{sax}}{1 - D_{sax}}\right) \tag{36}$$

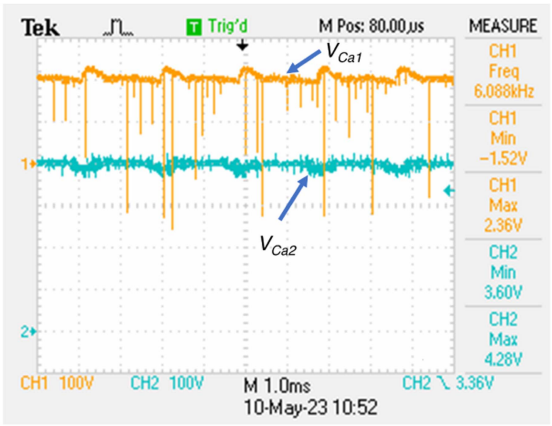
Fig. 10 shows the voltage gain of the converter for various duty ratios and turns ratios.

III. PROPOSED CONTROL SCHEME

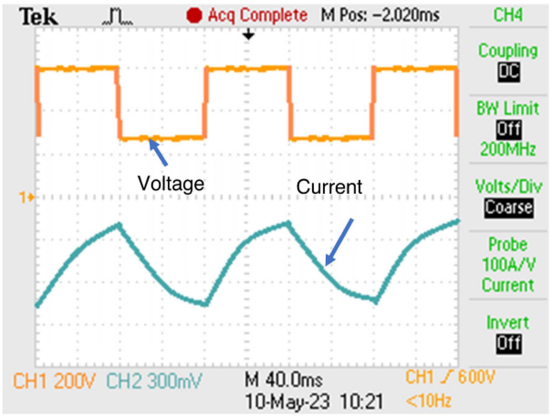
An SPFL inverter's function when connected to the utility grid is to supply the grid with a regulated and controlled AC voltage. Not only that, but it also has the responsibility of keeping the grid and the SPFL inverter in unison. A total of two control loops were built to accomplish the task of controlling the flow of electricity. The regulation of the DC bus voltage and the synchronization of the inverter with the grid were the intended



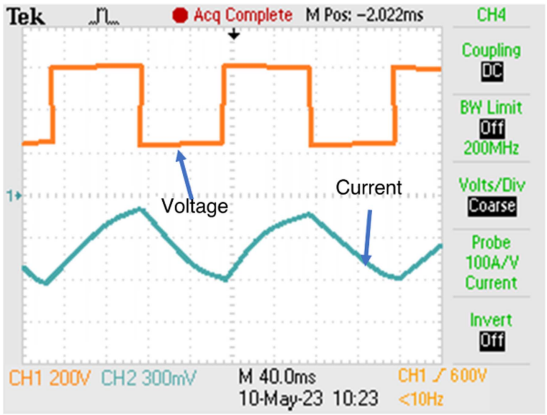
(a) PV 1 and PV 2 Voltage



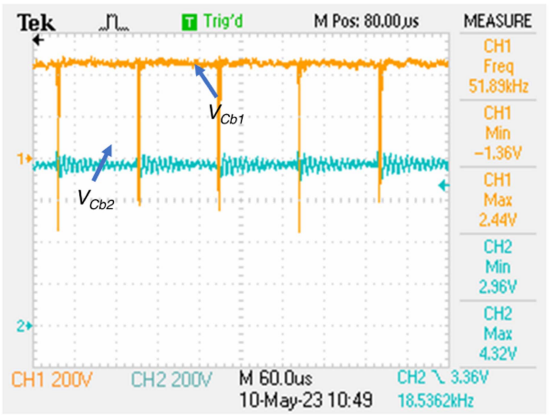
(c) Voltage of C_{a1} and C_{a2}



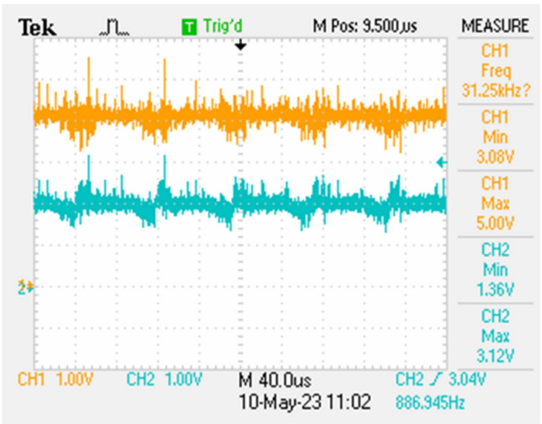
(b) Voltage and Current of L_{a1} and L_{a2}



(d) Voltage and Current of L_{b1} and L_{b2}



(e) Voltage of C_{b1} and C_{b2}



(f) Current of C_{b1} and C_{b2}

FIGURE 14. Results of active and passive elements of impedance network obtained through experimental study.

purposes of these loops. One uses an internal voltage control loop, while the other uses a hysteresis band pulse generator based on a Synchronous Reference Frame (SRF) theory that uses PI controllers. They are both seen as crucial components of the whole.

A. CONTROL STRATEGY OF TPZNC

The voltage variations in the DC-bus of a grid-connected inverter cause associated loads to malfunction. To keep the DC-link voltage constant, this problem is solved by using a more traditional type of controller called the inner voltage

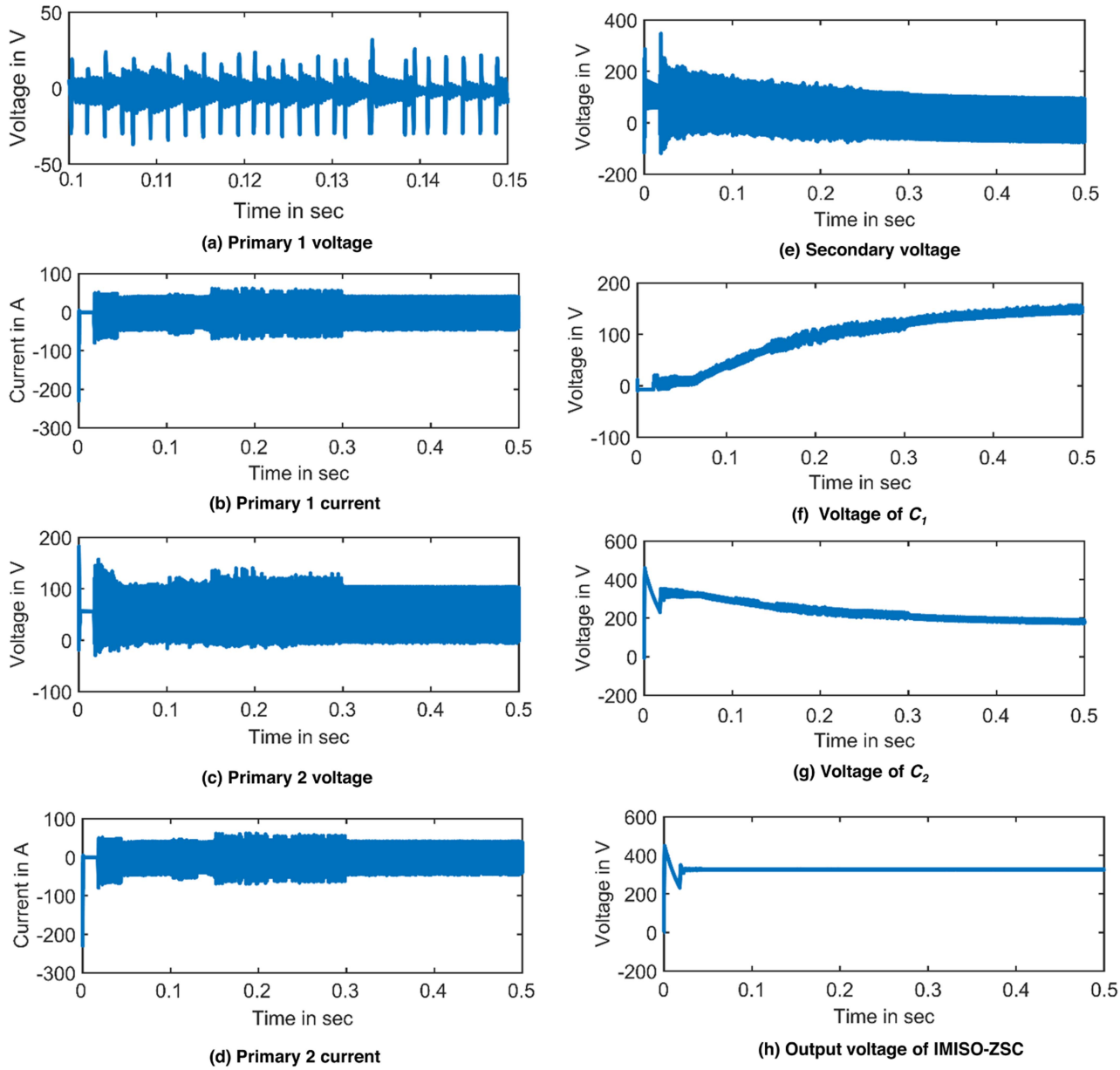


FIGURE 15. Results of transformer and output terminal by simulation study.

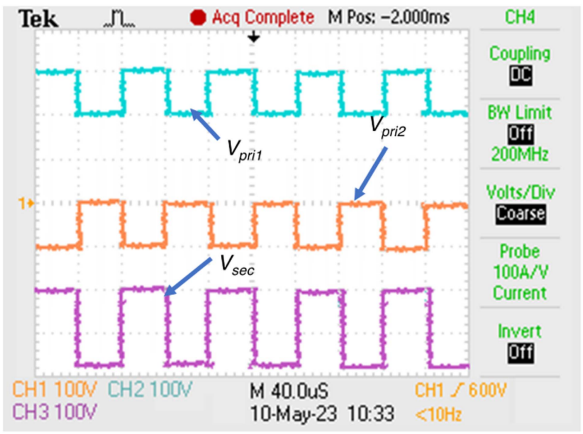
control loop with a PI controller. The PI controller gains are determined based on the step responsiveness of the transfer function.

The PI controller shown in Fig. 11, generates gate pulses for the TPZNC. An error voltage, V_e, is generated when the reference circuit's voltage, $V_{dc}*$, is compared to the DC-link feedback circuit's value, V_{dc}. The PI controller is then instructed to rectify the incorrect signal using that error voltage. The gate pulse generator receives a duty cycle instruction from the PI controller and then pulses the Q_{a1}, Q_{a2}, Q_{a3}, and Q_{a4} switches.

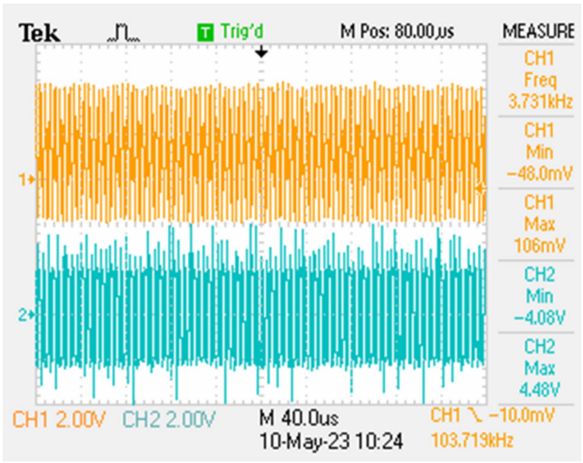
$$V_c(t) = k_p V_e(t) + k_i \int_0^t V_e(t)dt \tag{37}$$

B. CONTROL STRATEGY OF SPFL INVERTER

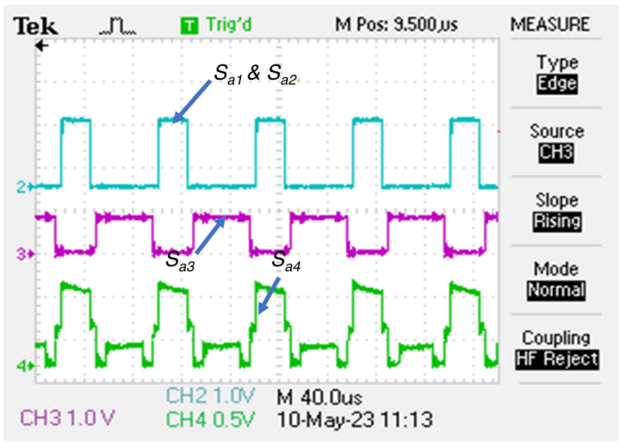
This section proposes a grid-side controller for PV system-grid power flow management based on the hysteresis band and the SRF theory. It also keeps the single-phase SPFL inverter's output voltage in step with the grid voltage. The method by which the controller located on the grid exerts its control is shown in Fig. 12. It is critical to consider the grid's phase sequence, frequency, and voltage while attempting to synchronize an inverter with an existing grid. The voltage output by the SPFL inverter is in sync with the grid supply. The inverter's output voltage is defined by its modulation index. The output frequency of the single-phase alternating current voltage is dependent on the switching frequency.



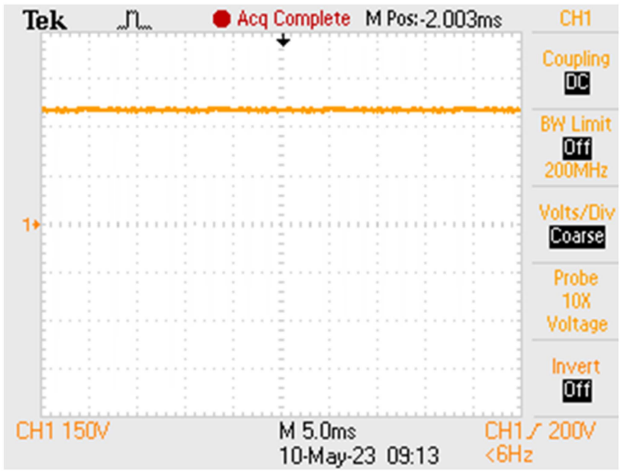
(a) Primary and Secondary Voltage



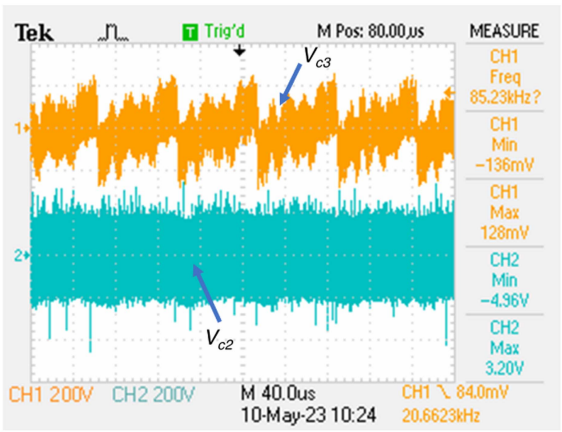
(b) Primary and Secondary Current



(c) Gate Pulses of S_{a1}, S_{a2}, S_{a3}



(d) DC link voltage



(e) Voltage of C_{b1} and C_{b2}

FIGURE 16. Experimental results of TPZNC.

The comparison of the DC-link voltage V_{dc} with the reference voltage V_{dc*} produces an error voltage V_d*. After that, the PI controller receives the error voltage V_d* and uses it to compensate for the erroneous signal, resulting in I_d*. The V_d* and V_q* are transformed into a by use of the dq to a conversion block. A product block is used to process the reference wave $a*$, which is received from the grid current I_g, to create the V_c. Time-locked gate pulses for the SPFL inverter are generated by a hysteresis band pulse generator. The following expression represents the formula for transforming I_g into I_d and I_q.

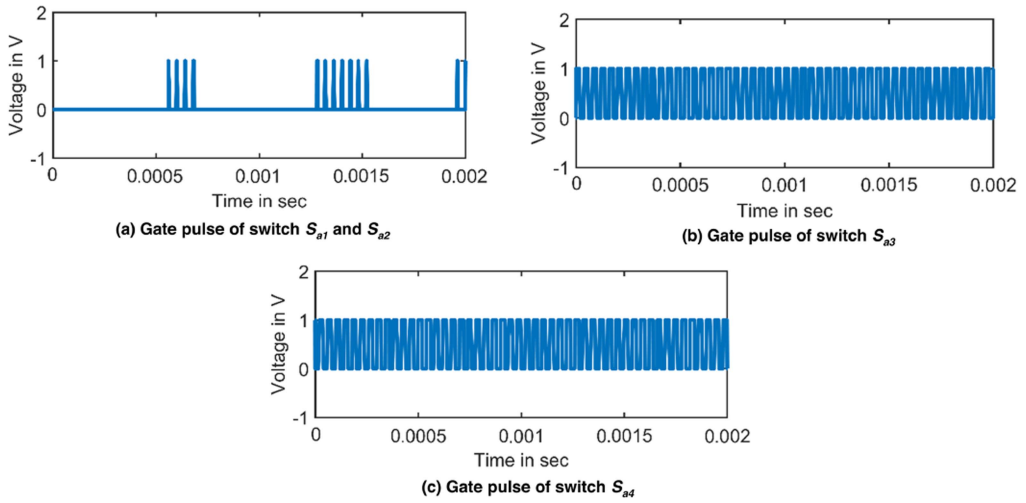


FIGURE 17. Gating signal of active switches.

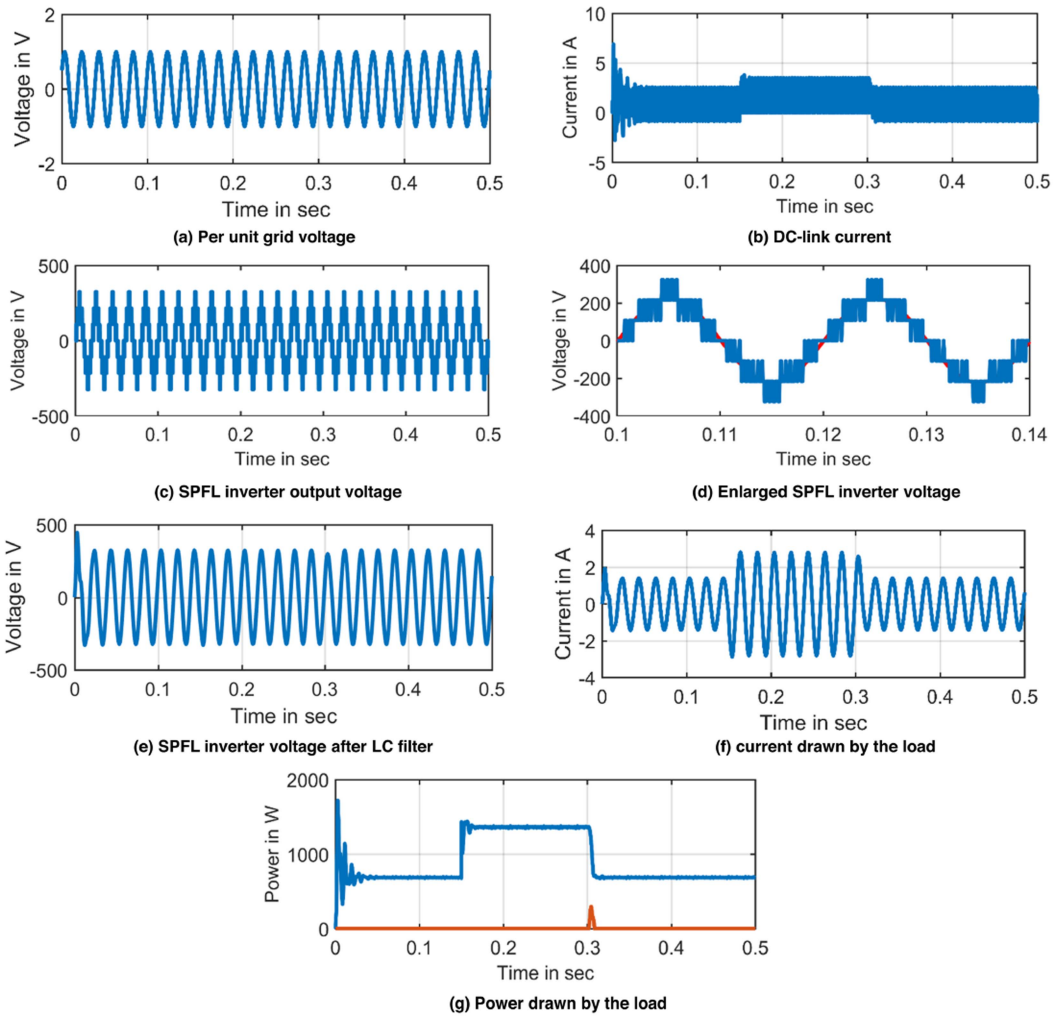
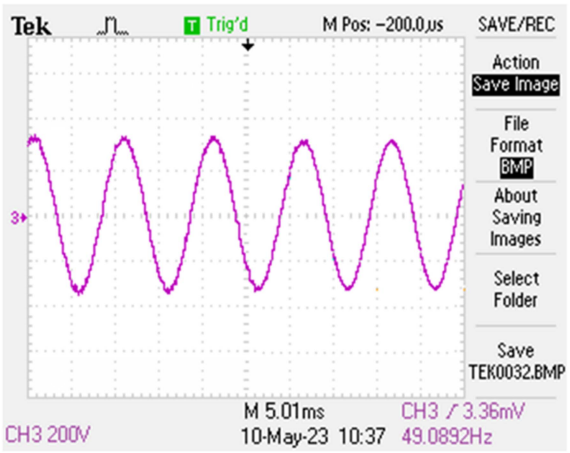
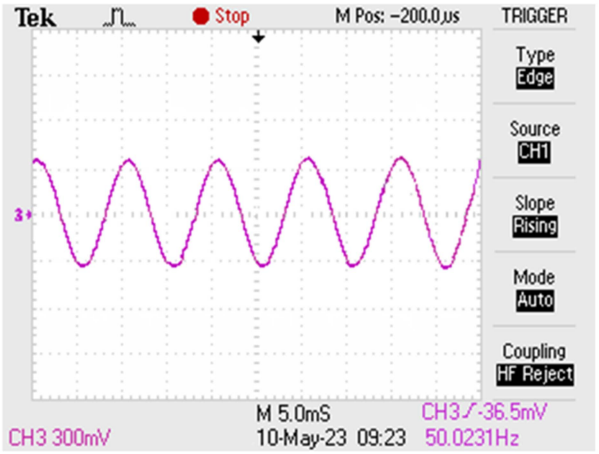


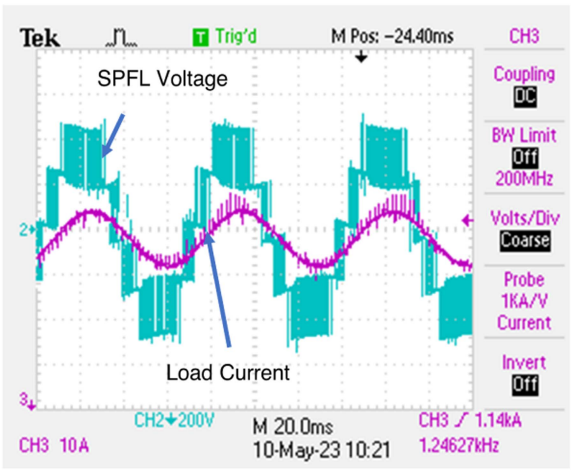
FIGURE 18. Simulation results of SPFL inverter and load.



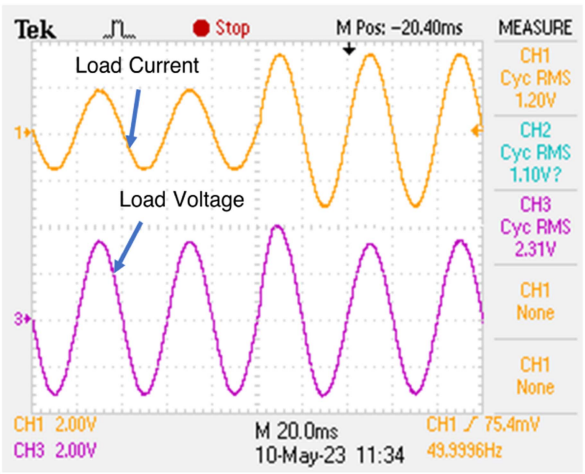
(a) Load voltage



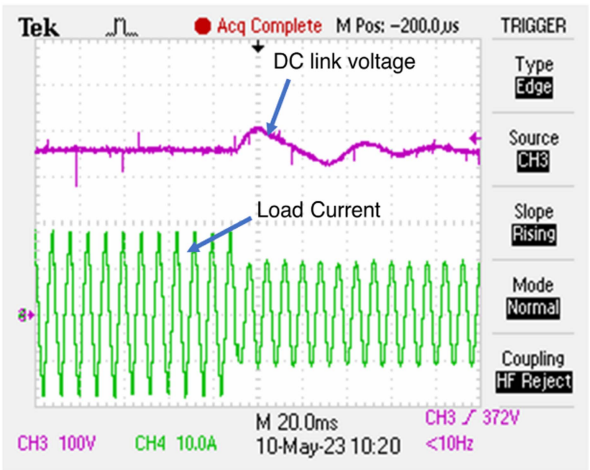
(c) Constant load current



(b) SPFL voltage and load current



(d) Load voltage and dynamic load current



(e) DC link voltage and dynamic load current

FIGURE 19. Results of SPFL inverter and load by experimental study.

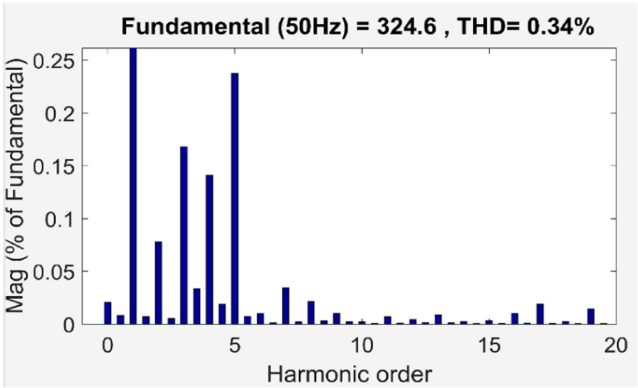


FIGURE 20. Voltage THD analysis by simulation study.

$$\begin{bmatrix} I_d \\ I_q \end{bmatrix} = \begin{bmatrix} \sin(\theta) & -\cos(\theta) \\ \cos(\theta) & \sin(\theta) \end{bmatrix} \begin{bmatrix} I_{real} \\ I_{image} \end{bmatrix} \tag{38}$$

The real and imaginary parts of the grid current can be represented by (39) and (40), respectively.

$$I_{real}(t) = I_m \sin\theta \tag{39}$$

$$I_{image}(t) = -I_m \cos\theta \tag{40}$$

A method to convert dq variables into a and $a*$ is given by (41), which is displayed below.

$$\begin{bmatrix} I_{real} \\ I_{image} \end{bmatrix} = \begin{bmatrix} \sin(\theta) & \cos(\theta) \\ -\cos(\theta) & \sin(\theta) \end{bmatrix} \begin{bmatrix} I_d \\ I_q \end{bmatrix} \tag{41}$$

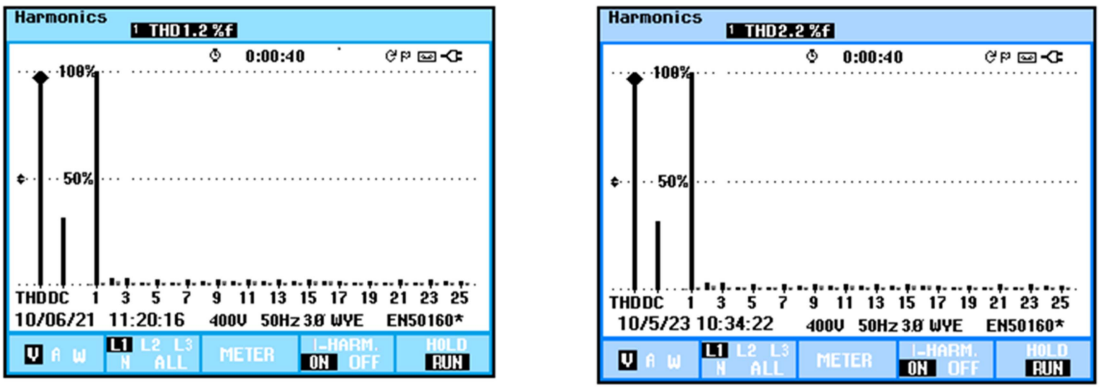
IV RESULTS ANALYSIS AND DISCUSSION

The simulation and experimental prototype model were made using a 1.5 kW, 230 V (RMS), 50 Hz scale-down model to examine the potential advantages and disadvantages of the proposed TPZNC-fed SPFL inverter. To do the evaluation, The boost factor, its capability to deliver regulated DC output, and its power transmission capacity are taken into consideration. To ensure a fair assessment of the TPZNC, this is carried out. A hardware implementation is used to examine the operation of a single-phase grid-connected SPFL inverter that receives its input from a reduced TPZNC. To evaluate the virtual model, the virtual system's discrete sample time has been configured at 50 µs. The suggested TPZNC's input ports are supplied with electricity by 750 W, 60 V PV arrays, each with a rating of 60 V. For the design parameters listed in Table 3, the proposed system was verified.

A 750 W, 60 V PV array was subjected to a steady 1000 W/m^2 of light from the start of the run. An illumination that varies concerning the time is applied to the PV array 2. Increasing the solar illumination from 500 W/m^2 to 1000 W/m^2 produces a voltage that may be adjusted. Also, a dynamic load with 230 Ω/460 Ω resistance and 0.114 mH/0.228 mH inductance was attached to the terminals of the SPFL inverter. The purpose of this experiment is to evaluate the operational efficiency of the proposed model under dynamic load conditions. The PV array's photovoltaic cells can generate 750 W of power when operated at 60 V. The output is 750 W at 60 V, as shown in Fig. 13(a) when 1000 W/m^2 solar light is applied. Even with the switches S_{a1} and S_{a2} closed, the inductors L_{a1} and L_{a2} will get PV voltages. This procedure will be carried out until the input voltage reaches its maximum. Inductors L_{a1}, L_{a2}, L_{a3}, and L_{a4} are linked in a way that permits the PV and wind sources to release their stored energy in series with each other. The impedance network inductors are primarily grounded at 50 V. Fig. 13 shows the waveforms that were generated by the simulations. In the range of 0–0.25 seconds, the PV array 2 generates 30 V, and in the range of 0.25–0.5 seconds, 60 V, as shown in Fig. 13(f). A transformer's input inductors and primaries are powered by the on-time/off-time ratio of its primary chopping switches, S_{a1} and S_{a2}. The primary switches' duty ratio determines the voltage across inductors L_{a1}, L_{a2}, L_{a3}, and L_{a4}. The input voltage of the primary may be increased by a factor of 1:2 with the help of this transformer. The TPZNC prototype model results obtained through the three-phase digital storage oscilloscope are illustrated in Fig. 14. It shows the similar results presented in Fig. 13.

Fig. 14 shows that the result of the experimental model coincides with the simulation results presented in Fig. 13. A similar performance is obtained in both the simulation and experimental model. Figs. 15 and 16 show the output voltage MPZNC, the voltage across the transformer's primary and secondary, and the capacitors C_1 and C_2. One hundred volts is the voltage reading from the transformer's primary winding. Capacitors C_1 and C_2 received twice as much voltage from the transformer's secondary as they did from the main. To assess the feasibility of implementing the proposed MPZNC-fed SPFL inverter, the six-phase power analyzer experimental findings are showcased.

Exhibited in Fig. 15 is the voltage between the IMSO-passive and active components. Fig. 16(a) shows the voltage output from the PV array 1 and 2. The TPZNC input ports are powered during prototype development by two separate sources of electricity. To test the converter's capacity to regulate voltage, the source 2 output voltage is raised to 60 V from 30 V. L_{a1}, L_{a2}, L_{a3}, and L_{a4} are impedance network inductors, and their voltage and current are shown in Figs. 13 and 14. A look at the current waveform reveals the inductor's charging and discharging curves. The primary windings of the transformer have a voltage of about 100 V apiece. There is a secondary voltage of about 200 V as of Figs. 15(e) and 16(a). The voltage and current of the various passive components are illustrated in Fig. 16. These exactly match the simulation results shown in Fig. 15. Fig. 16(c) and Fig. 17 displays the gate pulses of the power switches S_{a1}, S_{a2}, S_{a3}, and S_{a4}. To achieve the necessary boost factor and regulate the DC bus voltage, the switching pulses are produced. Figs. 18 and 19 display the utility per unit value, as well as the current flow in the DC bus of the SPFL inverter, the voltage waveform of



(a) Voltage THD under constant load

(b) Voltage THD under dynamic load

FIGURE 21. Voltage THD analysis by experimental study.

TABLE 4 Numerical Comparison Between the Interleaved Boost Converters

Duty Ratio	LBC [18]		η in %	ITPIFBC [13]		η in %	ZSC [16]		η in %	Proposed TPZNC		η in %	V_{in}
	n=2	Gain		n=2	Gain		n=2	Gain		n=2	Gain		
0.10	67	1.11	94	133	2.22	91	143	2.38	93	285	4.75	92	60
0.20	75	1.25	94	150	2.50	91	180	3.00	94	360	6.00	93	60
0.30	86	1.43	95	171	2.86	92	255	4.25	93	510	8.50	92	60
0.40	100	1.67	94	200	3.33	90	480	8.00	92	960	16.00	91	60
0.47	113	1.89	94	226	3.77	91	1530	25.50	92	3060	51.00	91	60

	Number of Components			
Inductors	1	2	2	4
Capacitors	1	3	2	6
Switches	1	4	1	4
Diodes	1	4	2	8
Transformer	-	2	-	1

five-level, the voltage waveform of expanded mode, the power and the related current taken by the load. The simulation and experimental results of the SPFL inverter part have proved the ability of the proposed system to transport the power generated by the PV arrays to the local load and single-phase distribution network.

By manipulating the input voltage and load, the simulation validation evaluated the overall system performance. The extra load has been accounted for by modifying the experimental model. An additional 1.5 A brings the total AC load on the system up to 3 A as shown in Fig. 18(f). The prototype continues to supply 3 A of current at 230 V. The same case is carried out in the prototype model, the current measured during the dynamic load change is illustrated in Fig. 19(d). The DC link voltage during the removal of a portion of the load is presented in Fig. 19(e). A small disturbance is observed during the disconnection of the load.

The inverter introduces Total Harmonic Distortion (THD) into the grid voltage, which may be measured using the Fourier transform (FFT) analysis. Fig. 20 displays the SPFL inverter voltage THD content as a consequence of the simulation. After the connection of the SPFL inverter to the utility, the THD of the output voltage was tested using power quality equipment to find the percentage of THD. As seen in Figs. 20 and 21, the load voltage THD, as determined by the power quality monitoring instrument is within 2.2%. It is within the allowable limit of 5% as specified by the IEEE Standard IEEE 519.

Table 4 compares the performance of the suggested TPZNC and the traditional converters mentioned in references [13], [16], and [18], to highlight the advantages of the former. The suggested TPZNC outperforms the other traditional converters considered in the comparison table concerning gain. The approximate efficiency for the converter under consideration is 93%. The picture of the experimental setup is illustrated in Fig. 22. In the picture, the names of the various components of the proposed system are mentioned.

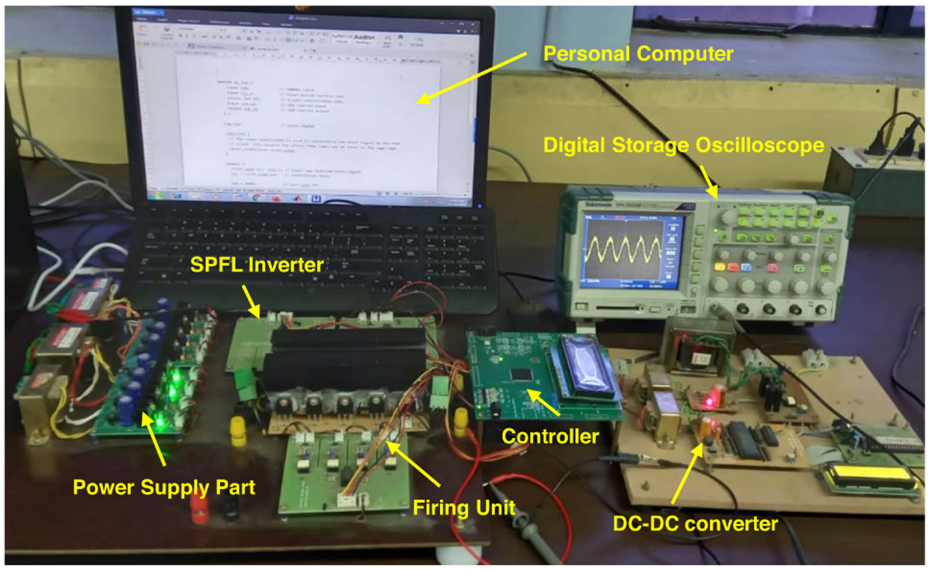


FIGURE 22. Picture of the experimental study.

V CONCLUSION

This research proposes a new type of dc-dc converter that uses a switched impedance network and features a high step-up isolation of the Z-Netwok. Thoroughly covered topics include analyzing the operating principle, choosing the settings, and comparing it to other existing high step-up dc-dc converters. Finally, to back up the recommended converter's potential benefits, the results of the experiments and simulations that were conducted are presented. With less voltage stress and lower current stress across the switches, the suggested TPZNC outperforms previously established high step-up dc-dc converters in terms of output voltage gain. The voltage gain of the suggested converter is double that of the standard ZSC. Because of this, the converter can handle a wider range of input voltages and use fewer cascading boost stages. The upgraded design of the converter is responsible for all these advantages. Around 93% of the time, the converter is efficient. Hence, the suggested converter is now more reliable and has a higher boost factor, making it a good choice for applications requiring a high step-up voltage. Systems that connect renewable energy sources to the grid are one example of this type of application; others include wind systems, solar PV systems, and hybrid wind-solar systems.

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