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A Survey of Hybrid Circuit Breakers: Component-Level Insights to System-Wide Integration

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ABSTRACT This survey provides a comprehensive review of hybrid circuit breakers and their applications in 1 kV to 800 kV, both alternating current and direct current systems. The paper introduces the research motivation and key applications of hybrid circuit breakers, followed by a detailed analysis on the generic structure and operation principles of four core components: the mechanical switch, the semiconductor devices, the energy absorbers, and the commutation switch. Critical challenges on the optimization of each component are identified and potential solutions are suggested. Moreover, the paper innovatively summarizes the system-level considerations that are critical for the holistic development of hybrid circuit breakers, such as current sensing, control latency, hardware in the loop validation, and integration of multiple HCBs for multi-terminal DC system protections. This review seeks to provide design considerations and streamline the prototyping process of hybrid circuit breakers from the component, topology and system integration perspectives, which will benefit the advanced protection equipment in emerging systems such as renewable energy integration, electrified transportation, and multi-port power systems.

INDEX TERMS Direct current circuit breakers, hybrid circuit breakers, control, medium voltage direct current, high voltage direct current, power system protection, and multi-terminal DC switchgear systems.

NOMENCLATURE

AC	Alternating current.
ACC	Auxiliary commutation circuit.
BDPS	Bi-directional power switches.
CB	Circuit breaker.
CHIL	Controller hardware-in-the-loop.
DC	Direct current.
DCCBs	Direct current circuit breakers.
DER	Distributed energy resources.
DS	Disconnect switch.
DSP	Digital signal processor.
FPGA	Field-programmable gate array.
GaN	Gallium nitride.
HCBs	Hybrid circuit breakers.
HIL	Hardware-in-the-loop.
HVDC	High voltage direct current.
IEGT	Injection Enhanced Gate transistors.
IGBT	Insulated-gate bipolar transistor.
IGCT	Integrated gate-commutated thyristor.
LVDC	Low voltage direct current.
MBD	Monolithic bi-directional.
MCBs	Mechanical circuit breakers.
MOSFET	Metal-oxide-semiconductor field-effect transistor.
MOV	Metal oxide varistor.
MVDC	Medium voltage direct current.
PA	Piezoelectric actuator.
PBD	Point-based design.
SBD	Set-based design.
SiC	Silicon carbide.
SSCBs	Solid-state circuit breakers.
TCA	Thomson coil actuator.
TIV	Transient Interruption Voltage.
WBG	Wide bandgap.

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I. INTRODUCTION

A. BACKGROUND

DC systems are becoming increasingly popular due to their superior attributes compared to AC networks, such as reduced power losses and enhanced flexibility devoid of synchronization requirements [1], [2], [3]. Nonetheless, the lack of protection mechanisms, specifically DCCBs, during electrical faults impedes the expansion of DC systems [4], [5]. This is partly due to the inherent difference between AC and DC systems, where the former naturally possess current zero-crossing points, a feature absent in the latter, rendering traditional CBs ineffective in fault scenarios [6], [7], [8], [9], [10], [11]. Consequently, attention turns to the three main categories of DCCBs: MCBs, SSCBs, and HCBs (combining mechanical and solid-state switches). MCBs, despite their low on-state resistance, suffer from prolonged opening time in naturally commutated HCBs with both contact-separation time and arcing commutation time, failing to meet the swift interrupt requirements for contemporary DC grid protection [12]. Additionally, these switches' interruption processes tend to produce arcs, significantly compromising their durability and reliability [9], [10]. Intriguingly, specific techniques such as current injections may facilitate openings at considerably lower currents and thus minimal arcing, thereby enhancing the scalability of MCBs in different voltage and current levels [13], [14]. However, this paper categorizes such techniques under HCBs' technologies, considering the prevalent use of solid-state switches in these techniques for controlling the current injections. Turning to SSCBs, they are deemed faster but suffer from considerable on-state power losses especially when applied in MVDC and HVDC systems [15]. In situations where voltage levels range from tens to several hundreds of kilovolts, even state-of-the-art WBG devices require the usage of multiple devices in series to withstand DC voltages, and/or in parallel to distribute considerable DC nominal currents [16]. Consequently, HCBs, which amalgamate the benefits of both MCBs and SSCBs, emerge as a more promising solution in these applications. This has led the focus of this paper towards HCBs.

B. STANDARDS AND LITERATURE REVIEW

The standards for DC grid protection are diverse, each tailored to specific applications and system configurations. For instance, IEC 62040 is developed for uninterruptible power systems (UPS) [17], while IEEE P2030.10 is designed for rural and remote electricity protections [18]. Despite the different fault behaviors across various applications, the need for efficient fault clearing, isolation, and recovery is a universal aspect addressed by circuit breakers. However, the specific standards for DC circuit breakers are still notably lacking.

In the area of DC circuit breakers standards, the focus has largely been on low-voltage applications, particularly those below 3200 V. The standard IEEE C37.14-2015 [19], applicable to these applications, requires circuit breakers to handle 1.65 times the nominal current within 8 ms. As the field of HCB evolves, APAR-E has introduced proposed protection requirements [20], though comprehensive standardization is still in development. The established technical metrics by APAR-E, targeting parameters such as a minimum rated power of 1 MW and an efficiency greater than 99.97%, a response time under 500 μs, and a lifespan exceeding 30,000 cycles or 30 years. These criteria are essential for advancing standardized, effective MVDC circuit breaker solutions. For example, with a 12 kA current, the highest standard, the rise rate signifies a fault condition of approximately 0.975 A/μs.

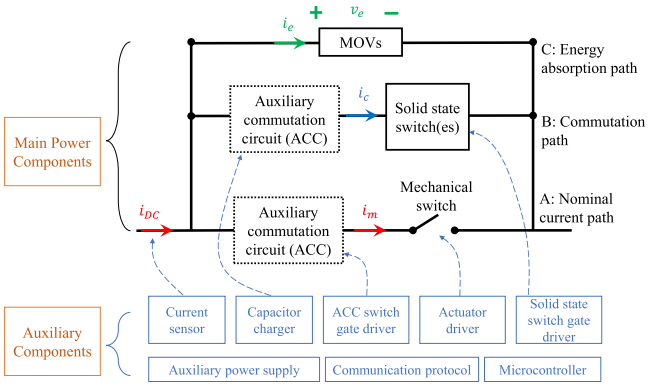

FIGURE 1. Generic structure of a HCB.

In the HVDC circuit breaker sector, TIV and protection system delay, are of paramount importance. HVDC breakers must comply with DC insulation coordination standards, maintaining a TIV no greater than 1.5 to 1.6 per unit (p.u.) to ensure the secure interruption of fault currents [21]. This helps in safeguarding against insulation failure, with a TIV around 1.5 p.u. being particularly effective for rapid current interruption. Moreover, the protection system delay needs to be as short as possible, ideally below 2 ms, to guarantee system responsiveness. This underscores the need for integrated system-level design and accurate controller configuration.

Conversely, existing literature predominantly focuses on summarizing different HCB topologies. Studies categorize these topologies based on the position of the commutation circuit (ACC) relative to mechanical switches, or by the current commutation mechanisms employed, such as zero current or zero voltage switching. Despite these classifications, there is a lack of in-depth analysis comparing the advantages and disadvantages of these topologies.

In conclusion, while some standards and metrics are in place, significant gaps remain, especially in terms of comprehensive guidelines and in-depth analyses of circuit breaker topologies. Our paper aims to bridge these gaps, offering a much-needed perspective that contributes to the advancement of efficient and reliable HCB. Moreover, this paper takes a unique perspective of system-intergration. Here the system does not refer to the overall DC system, but rather the HCB system that integrates mechanical switches, semiconductors, and MOVs as illustrated in Fig. 1.

C. CONTRIBUTION OF THIS PAPER

Achieving fault protection objectives in MVDC and HVDC systems may necessitate more than just HCB topological enhancements; innovations at breaker components and system integration levels are also critical. For instance, advancements at the HCB system level, particularly the integration of the control law accelerator–a peripheral function of the DSP, can contribute to a minimized fault clearing time, thereby satisfying the stringent MVDC protection requirements [22]. Furthermore, the energy absorption devices are perceived as the most susceptible components that heavily influence the lifespan and reliability of HCBs [23]. The selection of energy absorption devices has often been overlooked in most literature, but it has recently garnered substantial attention. More importantly, novel system-level integration techniques, like reduced latency control, could facilitate fault clearing time within the sub-millisecond range–an achievement that was once thought to be extremely challenging for HCBs due to the requisite coordination control between mechanical and solid-state switches [22]. Last but not least, system integration goes beyond just integrating components into a single HCB. This paper takes a step further by reviewing how multiple HCBs are topologically combined into a HCB-based switchgear for multi-terminal DC system protection.

In summary, this paper embarks on a comprehensive review of HCB components and system integration techniques, which all are indispensable for designers in the process of HCB prototype development. This paper will not only serve as a valuable guideline for HCBs design from component to system level but also ignite innovative ideas for future development across diverse applications including but not limited to renewable energy resource integration, electrified transportation, and multi-port power systems.

The structure of this paper unfolds as follows: Section II offers an overview of the development status and operation principles of HCB. Component selection is delved into in Section III, spotlighting mechanical switches, solid-state switches, and MOVs, while also exploring topology with insights into the merits and challenges of representative topologies in each category. The highlight of this review lies in Section IV, which delves into system-level considerations. This section not only elucidates the critical aspects of integrating HCB components discussed earlier but also the topological integration of multiple HCBs in switchgear tailored for multi-terminal DC system protection. We conclude the discussion with conclusions and a glance towards the future in Section V.

II. DEVELOPMENT STATUS AND OPERATION PRINCIPLES OF HCB

A. GENERAL STRUCTURE OF HCB

Fig. 1 presents a generic structure of the HCBs, which consists of four essential components, namely, the mechanical switch, solid-state switch(es), ACC, and energy absorption devices. In this manuscript, considering the prevalent use of MOVs as the energy absorption devices, we adopt "MOVs" as a representative term for all such energy absorption devices. This notation is consistently applied in the subsequent sections for uniformity and ease of understanding.

Mechanical switches are indispensable component of HCBs which carries a nominal current at a remarkably low on-state resistance, often less than one milliohm, leading to virtually negligible on-state power losses [24], [25], [26], [27], [28]. On the other hand, the slow motion of contacts in mechanical switches may significantly delay the fault interruption, considering the MOVs cannot establish the switching overvoltage until a sufficient insulation strength is established between contacts [29]. Therefore, an ultrafast actuation mechanism is the key to innovations in two types of mechanical switches for HCBs: the breaker type with an arcing capability and the disconnector type without an arcing capability [30]. An arcing mechanical breaker, while capable of negating the need for an ACC, does have its limitations – primarily, its intrinsic arcing phase that extends over several milliseconds [31]. This characteristic renders it more suitable for LVDC applications, where the implications of arcing are more readily manageable [31], [32]. However, within the LVDC domain, HCBs typically lag behind SSCBs in terms of operational speed and economic viability [10]. Conversely, the non-arcing mechanical disconnector excels in fast achieving contact separation, often within a sub-millisecond duration [29]. This advantage, though, comes with the caveat of necessitating an ACC to address any arising fault currents [33]. Such configurations are notably prevalent in MVDC and HVDC HCB systems, especially in systems where the arcing can pose significant challenges

The inheritance of mechanical switches has facilitated the early adoptions of HCBs in conventional AC systems. For example, a hybrid fault limiting circuit breaker has been operational as a bus coupler to interconnect 11 kV AC distribution systems in U.K. [34]. On the low-voltage level, the HCB concept has been applied to a commercial 600 V AC, 250 A thermal-magnetic molded case circuit breaker and demonstrates a 8.4 kA fault interruption [31]. In above application scenarios, both HCB concepts aim to reduce arcing hazards of AC breakers by adding power semiconductors and energy absorption devices. Although replacing an AC breaker with a HCB that possesses enhanced non-zero current interruption features in legacy AC systems seems advantageous, the economic rationale for such AC HCBs becomes less compelling when considering the additional investment required for power semiconductors.

The auxiliary commutation circuit or ACC is a unique component of HCBs that does not exist in MCBs or SSCBs. An ACC is unnecessary for arc-commutated HCB topologies with an arcing mechanical breaker. If a HCB uses an ultrafast disconnector to target sub-millisecond interruption time, an ACC is added to facilitate the current commutation from the mechanical switch branch to the solid-state switch branch in a HCB while the fault is still developing. It is critical to trigger the ACC as soon as the fault is detected before the fault

becomes exceedingly high to be commutated. In the upcoming commutation mechanisms section, the load commutation switch type of ACC, for example, typically has a peak fault current threshold. On the other hand, the current injection type of ACC in the solid-state switch path is marked by the fastest rate at which its fault current can rise.

Ideally, placing the ACC in the bypass solid-state switch path is preferred as it avoids on-state losses during normal operation and various current-injecting topologies have been proposed and summarized in existing review papers, such as [4], [8]. However, a bypass-branch ACC requires precharged capacitors and associated chargers, which further increases the complexity of system integration and the cost of auxiliary circuits in HCBs. Due to these issues, the early installations of HCBs such as [35], [36] and [37] utilize arc commutation or load commutation switch to slightly simplify the auxiliary circuits and boost the reliability of overall breaker.

Solid-state switches in HCBs take the commutated fault current from the mechanical switch and initiate the fault interruption by further transferring the current into MOVs. In essence, the solid-state switches in current-injection type of HCBs take on the role of the 'current switching' that was traditionally done by a switching arc in conventional breakers. They achieve this by transitioning from a conducting state to a non-conducting state in just a few microseconds. Yet this microsecond-level semiconductor interruption time is negligible as compared to the millisecond-level contact separation time in a mechanical switch. It is rather the surge current turn-off capability that becomes the most important parameter for selecting solid-state switches in HCBs, especially in MVDC system whose DC fault ramp rate gets very high. A recent HCB development named EDISON has targets for a high rate of rise in fault current of 40 A/us so that its solid-state switches need to interrupt 3 kA peak fault current after a 250us delay [22].

While recent advancements have seen the commercialization of SSCBs based on silicon devices such as ABB's recent IGCT-based solution [38] and Astrolkwx silicon IGBT-based solution [39] for 1 kV, 1 kA DC systems, and the potential of cascading 1.2 kV to 10 kV WBG semiconductors like SiC MOSFETs in MVDC systems [10], HCBs still posses unique advantages. For example, HCBs maintain superior conduction efficiency, especially in kA-level transimission network and large distribution grids. Economically, HCBs are also more favorable as they require fewer surge-handling semiconductors like IGBTs (5x to 7x rated current) in the commutation path, as opposed to placing them in the nominal conduction path as seen in SSCBs. This translates to HCBs offering a more cost-effective semiconductor solution than SSCBs for MVDC and HVDC protection.

Finally, metal-oxide varistors, also known as MOVs, operate as voltage clamping and energy dissipating devices. [40], [41]. In a sense, the MOVs in HCBs substitute the "current interruption" functionality from a switching arc in conventional breakers by attenuating the fault current down to zero. It is the existence of MOVs in HCBs, SSCBs, and MOV-assisted MCBs that endows a breaker with non-zero, DC current interruption capability. Without MOVs in these advanced breakers, either the arcing chamber or semiconductors will be burnt during the fault interruption process. Therefore, the MOVs are "consumables" in HCBs whose lifetime expectancy defines how many times a HCB can interrupt short-circuit faults.

The difficulty of lifetime analyses on MOVs come from the ceramic-sintered, amorphous microstructure that may easily deviate V-I characteristics of an MOV from its datasheet values. The common practice of parallel MOVs in HCBs to boost a higher energy absorption capability is also problematic when MOVs are not from the same batch and thus cause unequal current sharing. As nonlinear resistors, MOVs often exhibit fast-front overvoltage spikes whose magnitude depends on the semiconductor-to-MOV loop inductance and semiconductor turn-off speed, both values are difficult to be estimated during the HCB design stage. In short, given that MOVs are the most "passive" component in a HCB, they tend to bring the largest uncertainty in performance as compared to other HCB components according to real-world prototyping and installation practice [23].

In addition to the mechanical switches, ACC, solid-state devices, and energy absorption elements that constitute the power circuits, auxiliary components in the control circuits also play a critical role to ensure the integrity of HCBs, as Fig. 1 depicts. The auxiliary circuits include but not limited to the fault current detection circuit, the driving circuit of mechanical switch actuator, gate drivers of solid-state switches, gate driver of ACC switches, capacitor chargers in ACC, auxiliary power supplies for all above semiconductor gate drivers, and the digital microcontroller circuit to coordinate the time sequence of HCB power components.

Comparatively, HCBs have much more auxiliary circuits to coordinate than an MCB or SSCB, which has potentially impacted the reliability of HCB. If any of auxiliary circuits become malfunctional or lost coordination with other parts, the performance of overall HCB gets compromised. To tackle this system-level integration challenge, an effective solution is to perform hardware-in-the-loop validations early in the development. More details about system-level topics of HCB will be given in Section IV.

B. TYPICAL OPERATION PRINCIPLE OF HCB

The operation of a generic HCB can be conceptualized as a five-stage process, which encompasses: 1) normal operation, 2) fault detection, 3) current commutation, 4) current-holding period, 5) energy absorption. The circuit configurations in each stages are represented in Fig. 2. Concurrently, key current and voltage waveforms associated with these stages are delineated in Fig. 3 [42]. The following section provides a comprehensive discussion on the principles underpinning each of these stages.

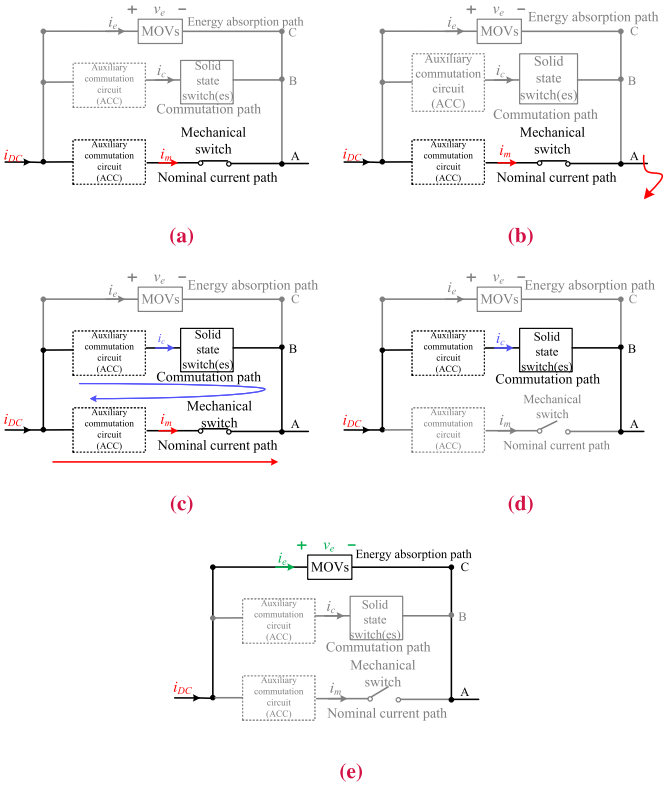

FIGURE 2. Operation stages of a generic HCB. (a) Normal operation ($0 - t_0$). (b) Fault detected ($t_0 - t_1$). (c) Commutation process ($t_1 - t_2$). (d) Current-holding period ($t_2 - t_4$). (e) Energy absorption ($t_4 - t_5$).

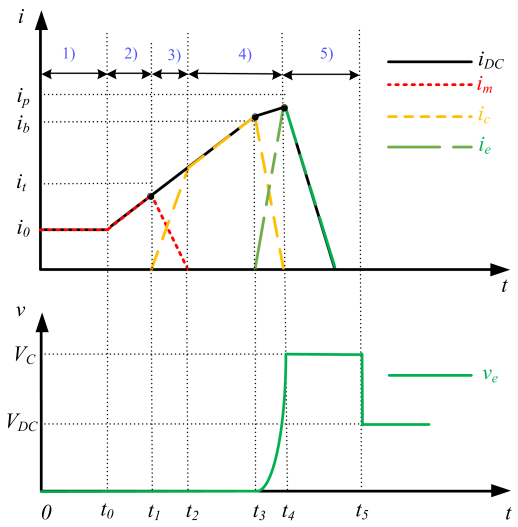

FIGURE 3. Typical current and voltage waveforms of HCB.

1) NORMAL OPERATION ($0 - t_0$)

Fig. 2(a) depicts the path of current flow during normal operation, while the corresponding current and voltage waveforms are presented in Fig. 3 with the time span labeled as 1). The DC current flows along the nominal current path with a rated current of i_0, and the mechanical switch current, i_m represented by the red dotted line, is equal to the DC current, i_{DC} shown by the black line (i.e., $i_m = i_{DC} = i_0$).

2) FAULT DETECTION ($t_0 - t_1$)

Fig. 2(b) depicts the path of current flow during the fault detected, while the corresponding current and voltage waveforms are presented in Fig. 3 with the time span labeled as 2). A fault occurs at t_0, causing the nominal current to increase at a specific rate until it reaches the threshold value, i_t. This fault current rate relies on factors such as source and line inductance [43], [44], DC-link voltage [45], and the nature of the fault (e.g., bolted fault).

3) COMMUTATION PROCESS ($t_1 - t_2$)

Fig. 2(c) depicts the path of current flow during the commutation process, while the corresponding current and voltage waveforms are presented in Fig. 3 with the time span labeled as 3). Upon reaching i_t at t_1, the commutation process commences, directing the nominal current (i.e., the fault current) to the commutation path by the means of ACC. Consequently, the nominal current i_m declines while commutation path current i_c rises, as shown in the yellow dashed line. The process concludes at t_2, with the fault current fully diverted to the commutation path, causing i_m to become zero, or a relatively small value that allows the mechanical switch to open under a zero-current condition. As a result, i_c to equal the fault current, indicating a completion of current commutation.

4) CURRENT-HOLDING PERIOD ($t_2 - t_4$)

Fig. 2(d) depicts the path of current flow during the current-holding period, while the corresponding current and voltage waveforms are presented in Fig. 3 with the time span labeled as 4). The fault current continues to increase to i_b until t_3, when it is commutated to the energy absorption path and the MOV voltage starts to increase. Within this period, the mechanical switch initiates opening, but it is crucial to keep the current near zero in the nominal path. If not, opening the mechanical switch under a high current condition could pose significant risks, particularly for DS types that have minimal or no arcing capabilities. Various strategies can be implemented to regulate the nominal path current near zero, a topic that will be further explored in the topology section. Nonetheless, by t_4, the fault current flows solely through the MOVs clamping the voltage at, V_c, higher than the DC voltage, V_{DC}, facilitating fault current clearance. As solid-state switches enable rapid commutation from t_3 to t_4, the fault current experiences a slightly reduced fault di/dt and a minor peak increase to, i_p, during the entire circuit breaker operation. It's worth mentioning that the MOVs' transient voltage is anticipated to surpass the clamping voltage V_c. However, this is expected to stabilize near V_c when the system reaches a steady state.

5) ENERGY ABSORPTION ($t_4 - t_5$)

Fig. 2(e) depicts the path of current flow during the energy absorption, while the corresponding current and voltage waveforms are presented in Fig. 3 with the time span labeled as 5). Finally, at t_5, the fault current is entirely extinguished by the MOVs. At this point, the voltage across MOVs v_e is equal to the DC source voltage V_{DC}. It should be noted that in instances where an isolated switch is inseries with the HCB, upon complete fault clearance, the isolated switch is turned off, resulting in a zero voltage (v_e) across MOVs.

Fig. 3 presents a fundamental depiction of HCBs' operation with sequential timing. However, it is worth noting that the actual waveforms may exhibit slight variations depending on the specific topology employed. For instance, in topologies utilizing an LC circuit as the ACC, the fault current during t_1 and t_2 may display an exponential decline as part of the resonance waveform. Thanks to the necessity for fast commutation, the commutation time could be much smaller than that of the resonant cycle, and therefore, the current decrease can be approximated as a straight line rather than an exponential one [46]. Additionally, there may be some overshoot and undershoot resulting from the resonance of parasitic inductance and capacitance. Nevertheless, such non-ideal circumstances do not detract from the fundamental principles underlying HCB operation [46], [47].

Consequently, the subsequent section of this paper will embark on a detailed examination of each individual components of HCBs, specifically with respect to cutting-edge mechanical switches, solid-state switches and MOV selections. Subsequently, the paper will outline the various topologies based on distinct commutation techniques via different ACC.

III. COMPONENT ADVANCEMENT

A. MECHANICAL SWITCH

1) OVERVIEW

Although mechanical switches are indispensable components and key enablers of early adoption of HCBs in AC systems, they impose several difficulties and bottlenecks while adopting hybrid configurations to achieve ultrafast DC facult protection. There remains several critical problems in mechanical switches of DC HCBs. Firstly, mechanical switches take a much longer time to open due to the mechanical inertia of metal contacts. A brief discussion on contact materials will follow below. Secondly, mechanical switches need a powerful actuation system to separate metal contacts in few ms. Two common mechanical switch actuators, TCA and PA, are summarized in this section. Thirdly, mechanical switches need extra arcing time on top of contact-separating time during interruptions, which further delays the current commutation to the semiconductor branch and the MOV branch. Several arcing considerations are generalized in later discussion.

As previously outlined in the section on the general structure of HCBs, there are two primary categories of mechanical switches used in HCBs, depending on their arcing capabilities: DS and MCBs, as illustrated in Fig. 4 [30]. For

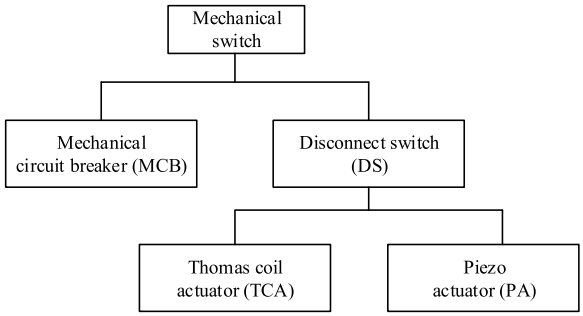

FIGURE 4. Classification of the mechanical switches.

clarity, DS switches, despite having comparatively reduced arcing capabilities, are renowned for their swift disconnecting speed enabled by innovations in the driving mechanism [48]. Various ultrafast actuators such as Thomson coil acutators (TCA) [49] and piezoelectric actuators (PA) [50] are utilized in DS to minimize its contact separation time. Given these limitations, they are most suitable in scenarios where artificial current zero-crossing points are necessitated through current commutations, a process particularly critical or even mandatory in MVDC and HVDC systems [7]. Alternatively, MCBs, which can function independently or as a component within HCBs, are often equipped with robust arcing chambers such as vacuum interrupters, allowing them the ability to withstand arcs during the current commutation process [34]. When utilized in HCBs, these MCBs fall into the arc-based commutation category.

While both DS and MCBs can utilize additional circuits for zero voltage and/or current turn off, DS switches are generally favored due to their superior speed brought by the ultrafast actuators and a smaller size brought by the elimination of arching chamber compared to MCB counterparts [30]. For medium-voltage and high-voltage installations, the fault current will keep rising during the current commutation from the mechanical switch branch to the semiconductor branch, considering neither the arc or the ACC is designed to establish a sufficiently high voltage to override the system voltage (i.e., 10 kV and above) [51]. Consequently, the fault current might surpass the peak turn-off capability of solid-state switches. This scenario is more probable in low impedance systems where the fault rate is exorbitantly high. Therefore, given the expeditious interrupt attributes of DS, their utilization and investigation for HCBs are of significant interest.

DS switches utilize advanced actuation mechanisms such as TCA and PA to achieve ultrafast contact separation [30]. TCA utilizes electromagnetic repulsion force to move a coil or a disc, which is generated by pulsating currents from precharged capacitors [52]. Piezoelectric actuators, on the other hand, capitalize on the inverse piezoelectric effect, wherein an applied electric field provokes mechanical strain in a stack of crystalline material, culminating in actuation force and displacement output [53], [54].

The challenges associated with PAs often stem from the assumption that insulation strength increases linearly in

conjunction with a critically damped contact travel curve [55], [56]; however, actual behavior displays significant oscillations, leading to potential insulation failures. Real-world PAs can experience up to 48% overshoot and 60% undershoot in contact separation due to underdamped actuation systems [50], which necessitates careful voltage regulation to prevent dielectric breakdown. To address these issues, three mitigation strategies are proposed: improving insulation per contact distance, using MOVs after contact establishment, or implementing closed-loop control for critical damping–with the latter showing the most promise. Accurate PA modeling is crucial for effective control, balancing precision against complexity. Additionally, to enhance PA performance, reducing the effective mass of the contacts can increase resonance frequency, and mechanical amplification can extend actuator stroke within compact sizes, enabling their use in small electronic devices [29], [50].

In some applications of mechanical switches, particularly where the voltage and current demands are moderate, arc quenching may not be a critical requirement, allowing for simpler contact designs. However, in scenarios that require exceedingly high-speed interruption and swift reinstatement of dielectric strength, the implementation of specialized arc quenching mediums becomes a topic worthy of detailed exploration. Sulfur hexafluoride (SF6) stands out for its non-toxic, non-flammable properties and excellent thermal conductivity, yet it is environmentally detrimental due to its significant global warming potential and the toxic by-products formed when it reacts with water [51]. On the other hand, vacuum arc quenching is highly valued for its ability to rapidly extinguish arcs and restore dielectric strength, ensuring minimal electrical system downtime. Air blast methods are notable for their suitability in high-frequency operations, low maintenance, and compact design, while also enhancing safety by reducing fire risks [57]. Although oil provides robust insulation, it carries environmental risks and fire hazards that necessitate rigorous control measures [58]. Carbon dioxide (CO2), in contrast, offers a safer and more environmentally friendly alternative, with reduced toxicity and flammability compared to SF6 and oil, presenting itself as a viable option in safety-critical applications [59].

Last but not least, effective contact materials are essential for efficient circuit interruption. These materials should ideally have excellent electrical and thermal conductivity, which aids in minimizing losses and facilitating heat dissipation, respectively [60]. Additionally, strong dielectric properties are necessary for quick recovery after interruption. A critical aspect is their low weld strength, ensuring smooth contact separation, particularly vital under high fault currents. Pure elements often do not satisfy these requirements comprehensively, leading to a preference for alloys [61]. Alloys, particularly those incorporating elements like aluminum, silver, and copper, are favored due to their balance of low resistance and high conductivity. However, they pose increased risks of erosion and welding. The optimization of these alloys involves meticulous adjustments in particle size, careful selection of additives, and precise control of furnace conditions, all of which fine-tune their final properties [62].

To evaluate DS switches for HCBs, following key parameters must be considered.

- On-state resistance. When DS is typically closed to conduct nominal current, the on-state resistance ascertains the conduction losses, which influences the thermal designs. Generally, the on-state resistance of DS is correlated with the applied contact force. In essence, if the contact force is excessively substantial, the on-state resistance can be exceedingly minuscule (several microhms), and vice versa.
- Voltage withstanding capabilities. When DS are opened to insulate the fault, they are anticipated to endure at least twice the DC voltage [63]. Consequently, the contact stroke distance is a paramount parameter governing the voltage withstanding capabilities.
- Turn-off speed. The dynamic merit for evaluating DS is its opening velocity to isolate the fault (closing speed is of lesser concern regarding overall protection). For TCA, the opening speed is directly proportional to the driving energy. Thus, a tradeoff exists between reduced driving energy and accelerated opening speed, which necessitates designing according to specific applications. The driving energy frequently incurs elevated costs due to higher pre-charged voltages of the driving circuit and increased capacitance [64], [65].
- Efficiency. The DS are predicated on energy transitioning from electrical to mechanical contact repulsions. This energy transition efficiency in TCA is significantly inferior compared to PA.
- Power density. In specific applications, such as in the context of electric aircraft, this metric can hold significant importance.

In a recent 500 kV HVDC project commissioned in China, it has been reported that when a TCA is incorporated in an HCB, it can be actuated to open within a brisk 3 ms duration, as noted in [66]. Concurrently, ABB, which also deploys TCA as the mechanical switch within its HCBs, has indicated in its review paper that the TCA's opening time falls within the range of a few milliseconds, although a specific duration is not provided [67]. Conversely, the use of PAs in HCBs, particularly for MVDC and HVDC applications, is currently within the research and development stage. Thus far, only laboratory tests have been reported. These tests indicate that a PA with a 15 kV rating takes approximately 0.5 ms to open. Although there are few commercially available PAs on the market, such as those by CEDRAT TECHNOLOGIES (CTEC) [68], their application for HCBs in MVDC or HVDC contexts necessitates custom amplification techniques. These techniques are essential to extend the stroke distance, thereby establishing sufficient voltage withstand capabilities.

B. SOLID-STATE SWITCHES

The progress in solid-state technology has enabled the application of HCBs in high-power scenarios. However, the

suitability and efficiency of these devices vary across different applications and design requirements. For instance, the commericially available 600 V GaN devices may not be ideal for HVDC systems that necessitate a large number of GaN devices to maintain voltage and current.

The surge current turn-off limit is the most important parameter for solid-state switches in HCBs [69]. The inrush conduction loss and the hard-switching loss while turning off a fault current may trigger thermal runaways and ultimately failures in semiconductor dies [70]. While most power MOSFETs suggest a safe surge current turnoff capability at about twice the rated current, power IGBTs in HCB applications have reported a higher turn-off capability around 5 to 7 times the rated current [69], [71]. This high turn-off current has consolidated the prevalence of IGBTs in HCBs. Other thyristor-alike devices like IGCTs and GTOs with a kA-level turn-off current are also promising candidates for MVDC and HVDC HCBs [72], [73]. Power transistors, either silicon or WBG-based, are not the first choice for HCBs due to their limited surge capabilities. Although SiC MOSFETs are known for their low on-state conduction losses, this trait doesn't inherently make them preferable for HCBs, especially considering their position in the commutation path where no nominal current flows.

Moreover, while SiC MOSFETs are also perceived to support higher voltage and current ratings, the prevalent commercial ratings remain below 3.3 kV and 1 kA [10]. Even as 10 kV MOSFET modules gradually emerge, ongoing research work on aspects like short-circuit protections and device reliability prevent their widespread commercial use or preference among designers [74]. As a result, today's MOSFETs (Si and SiC) are primarily apt for HCBs used in LVDC systems, ACCs, or downscaled prototypes. This voltage limitation extends to GaN devices that also have limited surge turn-off ratings [75]. The strategy of reaching high voltage and high current by arranging numerous devices in series and parallel configurations may not be ideal either, as it intensifies design complexity and total cost.

GTOs and SCRs once held a dominant position in HVDC HCB applications due to their high voltage ratings exceeding 6.5 kV and high current ratings falling within the 3 to 6 kA range [8]. However, they have several disadvantages when compared to other high power rating devices, such as IGBTs. IGBTs exhibit a significant advantage in switching speeds, outperforming GTOs and SCRs by a factor of ten or more. Additionally, the turn-off process for IGBTs is less complex. In contrast, SCR turn-off relies entirely on external circuits, as SCRs cannot actively interrupt a non-zero current. This necessitates a resonant circuit to artificially create zero-crossings in configurations such as Z-source [76]. For GTOs, the turn-off process demands a substantial negative gate current, proportional to the on-state current. Typically, the ratio of on-state current to the required negative gate current for GTO turn-off ranges between 2:1 and 5:1, suggesting that deactivating a GTO conducting 1000 A may require several hundred amperes of negative gate current [77].

Si-IGBTs are expected to be the most suitable devices nowadays for MVDC and HVDC HCBs, considering their power ratings, commercial availability, and long-term operational testing, among other factors. For example, the commercially available ABB's HCB includes four solid-state switch stacks, each containing 20 IGBTs rated at 4.5 kV connected in series [35]. This design targets HVDC applications at 320-kV/9-kA. At the MVDC level, Yuchen et al. have described the EDISON circuit breaker, which uses six 6.5 kV press pack IGBTs in series for a 12-kV/3-kA DC system in shipboard applications [22]. These instances illustrate the feasibility of providing MVDC to HVDC protections using a reasonable quantity of IGBTs. However, the question of how to select the appropriate IGBTs concerning the voltage level, current level, and packaging, among other factors, remains. Jian Liu has provided a comprehensive procedure for selecting IGBTs [78]. Apart from voltage and current ratings, several significant considerations, including power density (especially current density) and maximum junction temperatures, have been taken into account. It has been observed that discrete IGBTs tend to have higher current densities and lower junction temperature increases compared to their module counterparts, due to lower thermal capacitance during HCB operation. Nonetheless, it is still advisable to calculate the IGBT's turn-off energy, which can lead to device failure, and to include an RC snubber in the design.

Alongside IGBTs, IGCTs, IEGTs, and ETOs also hold promise for HCB applications. Both IGBTs and IEGTs are similar in terms of structure, and the voltage and current ratings they can attain, as well as the drive power required [66]. A subtle distinction between the two is that IEGTs have a slightly lower on-state voltage drop compared to IGBTs. In most circumstances, IEGTs and IGBTs are interchangeable, provided they are both commercially available and the vendor prices are similar. On the other hand, IGCTs are current-controlled devices. The driving power for IGCTs is considerably higher, reaching up to 100 W; however, the driving power is only around 5 W - comparable to that of IGBTs and IEGTs - when maintaining IGCTs in their off-state [66]. An instance of IEGTs in application can be observed in the Zhangbei 500 kV DC grid, which comprises 320 submodules, each incorporating two parallel IEGTs with a rating of 4.5-kV/3-kA [66]. A recent example of IGCTs being utilized in HCBs can be seen in [72], where a prototype with a rating of 10-kV/20-kA was developed using 4500-V/4000-A IGCTs provided by CRRC. This project also shows the potential for IGCTs to be employed in future developments, including those involving 160 or 500 kV HVDC systems.

Monolithic bidirectional switches offer enhanced per-chip-area on-state resistance compared to discrete solutions. Currently, numerous MBDS switches are commercially available, including the GaN-based switch from Panasonic [79] and Btran [80], among others. Moreover, additional laboratory demonstrations continue to emerge. While the advantages of MBDS are more pronounced in solid-state circuit breakers, the prospect of a compact design remains an appealing feature

for bidirectional HCBs. However, the surge turn-off capability of monolithic bidirectional transistors remains a question [81].

C. MOV

MOVs, which are commonly utilized in HCBs, are exposed to impulse stresses that significantly reduce their lifespan and degrade their reliability [82], [83], [84]. These impulse pulses are distinct from the overvoltage found in traditional power systems for which MOVs are originally designed [85]. Thus, it is imperative to meticulously select MOVs that are specifically designed for HCB applications, considering their lifespan and reliability [86]. The conventional method for selecting MOVs typically considers factors such as their continuous voltage rating, required clamping voltage, peak current, and energy absorption requirements. However, this approach often assumes nominal operating conditions and overlooks worst-case scenarios, such as those involving bolted faults where the fault current rate increases and peak current rises. Additionally, the lifespan aspect is frequently omitted. Consequently, there has been a growing interest in MOV selection based on lifespan. This approach ensures that the MOVs selected are well-suited to withstand impulse stresses and other demanding high-current conditions, resulting in enhanced reliability and durability [23].

As such, selecting the appropriate MOV entails a sophisticated multi-objective design challenge that can be tackled using either a SBD approach or PBD approach [86]. Numerous design factors, including pulse current duration and longevity, might span a broad spectrum of values and warrant meticulous consideration. For example, the surge current that MOVs can handle fluctuates based on numerous factors including system specifications and MOV configurations. Moreover, the duration of the surge current - from the moment current enters the MOVs until it's completely cleared - isn't fixed either. Both the magnitude and duration of the current can impact the lifespan of MOVs. Therefore, these factors should be comprehensively considered during the selection of MOVs. This principle applies to other parameters as well, with their combinations delineating a design space in which only a limited set of combinations fulfill all design constraints, thereby narrowing the range of viable solutions. To pinpoint a feasible solution, MOV selection ought to take into account multiple aspects capable of further constraining the set of viable solutions such as cost and volume.

In contrast, the PBD approach contemplates the most extreme scenario, establishing the confines of the solution set. In general, the outcomes derived from the PBD method should represent a subset of the SBD results, given that the latter encompasses a more extensive design space as opposed to the singular worst-case scenario examined in the point-based technique. A myriad of alternative approaches or algorithms can address this multi-objective function problem. The core of MOV selection lies in integrating longevity and resolving this multi-objective function.

A potential drawback of this design methodology is the underlying assumption that the available data on the MOV is universally valid. Although this assumption does not impact the MOV selection process, it may compromise the accuracy of the conclusions drawn from the SBD and/or PBD approaches. It is worth noting that this data is typically supplied by the manufacturer. Therefore, it is crucial to not only call for additional research on the accessibility of DCCB varistor lifetime data but also for researchers to develop a MOV testing methodology to acquire more reliable data for their individual applications.

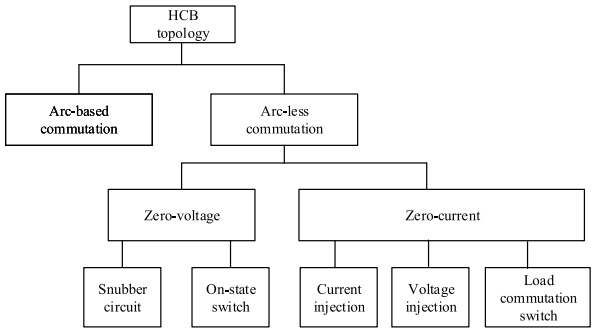

FIGURE 5. Classification of HCB topology based on different commutation mechanisms.

D. COMMUTATION MECHANISM

As shown in Fig. 5, this subsection presents a comprehensive summary of three major commutation mechanisms in various HCBs topologies:commutation with arc, commutation under zero-voltage, and commutation under zero-current. It is worth noting that the latter two are classified as controlled commutation with minimal or no arcing.

1) COMMUTATION WITH ARCS

The arc-based or natural commutation is characterized by a simple structure with a mechanical switch along the nominal path and parallel solid-state switches without an ACC. Upon fault detection, the mechanical switch is opened under fault current conditions, leading to arc formation. The ensuing arc voltage forces the fault current to the semiconductor switch in parallel, due to its lower resistive path. This semiconductor switch then conducts the fault current for a certain period of time until the mechanical breaker recovers its full dielectric strength. Calibrating the dielectric recovery time is challenging, there are thus multiple studies like [87], [88], [89] investigating the recovery behaviors of arcing chambers during arc commutation processes. Subsequently, the semiconductor switch is turned off, triggering the MOV to clamp the transient voltage surge. According to the principles of arc commutation described above, it's clear that meticulous design or selection of the mechanical switch is critical. The mechanical switch necessitates not only a swift contact separation speed but also a significantly high arc voltage that has to exceed the solid-state conduction voltage drop, thereby ensuring the successful commutation of fault current away from the mechanical switch. However, the mechanical switch

does not need to quench the arc. Depending on the used contacts and the voltage demand of the semiconductor bypass, a slightest contact gap might be sufficient. If one gap is not enough to provide a voltage that's high to achieve a complete commutation, a double contact systems with a second pair of dedicated arcing contacts can be used. This allows natural commutation to be used in MV applications. A contemporary instance of an arc-based HCB design is the joint venture between ABB and U.K. Power Networks that ran from 2017 to 2022, referred to as the PowerFul CB project [34]. The designed circuit breaker is tailored for a 12 kV system with a steady current of 2 kA, and a constrained peak current of 13 kA.

The arc-based commutation has some inherent limitations. Arc occurrence requires the mechanical switch to have arcing capabilities, which necessitates the use of peripheral devices. As a consequence, the arcing capabilities of the mechanical switch serve as a limiting factor for the attainable voltage and current ratings of the HCB. Furthermore, an arc can cause degradation of the insulating material and release harmful gases and particles, posing a significant safety hazard to people and equipment in the vicinity. This issue is further compounded when high power density such as in aircraft, is required [90], [91], [92].

2) COMMUTATION UNDER ZERO-VOLTAGE

The concept of zero-voltage aims to restrict the voltage across the mechanical switch while it is being turned off. To accomplish this objective, a snubber circuit can be incorporated across the mechanical switch. One simple approach is to use only a capacitor, but this results in the energy stored in the capacitor flowing to the mechanical switch during the reclosing process. Consequently, the RCD snubber circuits are more frequently employed to address this issue [93]. Let V_M represent the maximum permissible voltage across the mechanical switch, i_p denote the threshold current at which the mechanical switch is turned off, and $\Delta t_{M,off}$ signify the mechanical switch's turn-off time. In this context, the necessary snubber capacitance can be determined as

$$C = \frac{i_{\mathrm{p}} \Delta t_{\mathrm{M,off}}}{V_{\mathrm{M}}} \tag{1}$$

Consider a typical MVDC circuit breaker as an example. With a maximum current of 2 kA, a turn-off time of approximately 1 ms, and a maximum allowable voltage of 20 V when no arc is present, the required capacitance in this scenario is 0.1 F. From this calculation, it is evident that the capacitance is directly proportional to both the current rating and the mechanical switch's turn-off speed. Consequently, in high voltage and high current applications, the capacitance must be significantly larger, as the high current necessitates a larger capacitance while the mechanical switch's maximum voltage remains relatively low. Moreover, it is possible to parallel a low voltage rating MOV using other methods, although this may come at a certain cost [94].

An alternative strategy is to parallel a semiconductor component, which could be a MOSFET, IGBT, or a similar device, depending on the specific voltage and current requirements [95].

Furthermore, [96] introduces a topology that integrates a coupled inductor in series with the mechanical switch. This design activates during fault conditions, where an increased current in the primary winding induces an electromotive force (EMF) across the secondary winding, with a certain coupling coefficient. Concurrently, if semiconductor switches in the parallel path are engaged, this emf compels a current transfer from the mechanical switch. A critical aspect of this topology is the close coupling of primary and secondary windings, ideally approaching unity in the coupling coefficient to maximize mutual inductance, essential for rapid current commutation. However, this necessitates that the mechanical switch be rated to handle normal steady-state load currents, especially under rapid current changes. Contrasting this approach, coupled inductor-based current injections will also be introduced in the zero-current sections in detail.

3) COMMUTATION UNDER ZERO-CURRENT

The principle of zero-current commutation revolves around engendering a zero-current state, enabling the mechanical switch to turn off either entirely without arcs or with minimal arcing. Zero-current commutation techniques can be further divided into three distinct strategies: current injection, voltage injection, and in-line load commutation switch.

The current injection employs the ACC to infuse a counteracting current into the fault current, leading to the nullification of the fault current to a net zero value. Upon realization of this state, the mechanical switch can be disengaged under the zero-current condition. Based on the relative positioning of the ACC, HCBs can be further categorized into three subtypes, illustrated in Fig. 6. Specifically, Fig. 6(a) depicts the ACC positioned within the commutation path, Fig. 6(b) shows the ACC situated along the nominal current path, and Fig. 6(c) represents configurations with the ACC present in both the commutation and nominal current paths.

The current injection strategy has the following crucial equations to demonstrate the current regulation, which is expressed

$$\frac{di_c}{dt} = \frac{1}{L_{loop}} \left(v_{ACC} - v_{on,drop} \right), \tag{2}$$

$$\frac{di_m}{dt} = \frac{di_{DC}}{dt} - \frac{di_c}{dt}, \tag{3}$$

where i_c is the discharge current that has the opposite direction to the fault current. v_{ACC} is the voltage across ACC.

In the case of Fig. 6(a), different ACC configurations can be used. The simplest form is the *LC* circuit where the voltage is the pre-charged capacitor voltage, as depicted in Fig. 6(a) Structure a. $v_{on,drop}$ represents the on-drop voltage of the semi-conductor switches. Since the fault current is mainly determined by the source inductance, and the fault types. As (3)

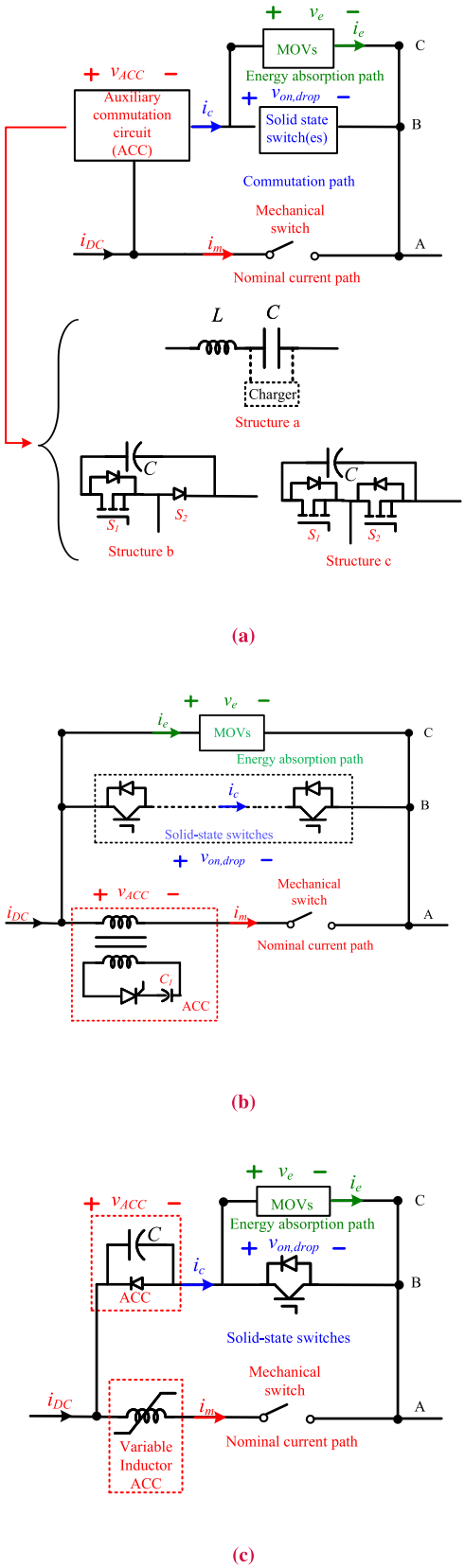

FIGURE 6. Current injection-based with different ACC positions. (a) ACC in the commutation path [97], [98], [99]. (b) ACC in the nominal current path [51]. (c) ACC in both paths [22].

shows, to regulate the main current is essentially to regulate i_c. From (2), it can be seen that different variables can be controlled as a handle to control the current i_c.

Fig. 6(b) illustrates that, under normal operational conditions, with both the SCR in the ACC and the solid-state switches turned off, the current is conducted via the mechanical switch and primary windings of the coupled inductors. The resistance along this path is in the magnitude of tens of micro-ohm, leading to operational losses of only tens of watt at rated currents in the range of several kiloamperes. In the event of a short-circuit fault detection, an opening command is sent to the mechanical switch, while a closing command is sent to the solid-state switches. Following this, at a predetermined moment, the SCR is turned on, creating a voltage across the primary windings of the coupled inductors which, in turn, initiate a loop current that flows through the mechanical switch, coupled inductors, and the Solid-State Switches. This mechanism ultimately reduces the fault current within the mechanical switch to zero. The ensuing overvoltage at the mechanical switch during the current's zero-crossing juncture is confined to a range of several tens to hundreds of volt. This restriction effectively obviates the possibility of the mechanical switch arcing, thus ensuring that the current is efficaciously shifted to the solid-state switch circuit.

In Fig. 6(c) with two ACCs, the voltage is the combined sum of both ACC voltages. In this specific scenario involving a variable inductor, it becomes saturated during either nominal or fault conditions, effectively behaving as a short circuit. For consistency with the other figures, v_{ACC} of Fig. 6(c) is shown solely to represent the voltage across the ACC in the commutation path.

The subsequent discussion outlines three strategies to regulate the current near zero, which are based on the control variables presented in (2), and represented by Fig. 6(c), and (a) structure b, and c respectively. Firstly, for example, the current can be regulated by managing the voltage of v_{ACC}. In this scenario, it is necessary to control the capacitor voltage using an external circuit. The governing principle for managing the capacitor voltage is to maintain it slightly above the sum of the voltage drop across the solid-state switches while keeping the difference between these two voltages minimal to enable effective current control. This method's drawbacks include the requirement of an external circuit for capacitor voltage control and the problematic delay when the current commutation rate is high, necessitating an exceedingly rapid response from current sensing to capacitor voltage adjustment.

The second approach involves controlling the loop inductance [22], as depicted in Fig. 6(c). This can be accomplished by employing a variable inductor. The inductor becomes saturated under nominal DC current conditions, exhibiting negligible inductance. When the current is commutated to the commutation branch, the inductor becomes desaturated, resulting in an inductance several orders of magnitude larger than that of the saturated state. As the inductance increases, the rate of change of the main current is constrained, allowing

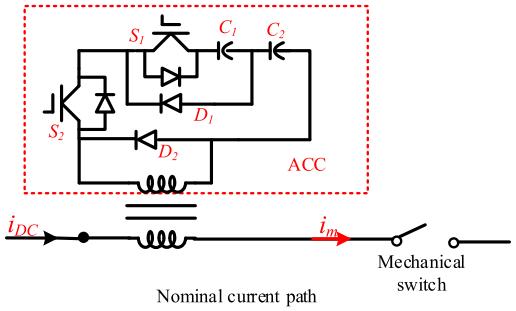

FIGURE 7. Voltage injection HCB with coupled inductors [101].

the mechanical switch to be turned off. The challenges associated with this method include: First off, the necessity for the inductor to transition abruptly from desaturation to saturation, meaning that the inductor's inductance must change rapidly to effectively limit the current, which demands a high permeability material inductor such as a nanocrystal, and the highly nonlinear nature of the inductor due to its BH curve, making it difficult to accurately model the commutation process analytically and leading to a somewhat empirical parameter design.

The third approach emphasizes controlling the dt or duty cycle, necessitating an external circuit such as a half-bridge or MOSFET and diode [98], [99]. This method involves using the ACC's PWM to decrease the main path current when the pre-charged capacitor is engaged and increase when it is disconnected. The pre-charged capacitor's insertion or disconnection is controlled through the PWM operation of the external circuit. This can be executed using a synchronous half-bridge, where switches S_1 and S_2 are alternately turned on, connecting and disconnecting the pre-charged capacitor C, respectively. When C is connected, it discharges negative current into the main current path to neutralize the fault current, while disconnection allows the fault current to rise, keeping the current within a narrow range. This setup can be simplified using a MOSFET and diode combination, or extended to a full-bridge for bi-directional capabilities. However, this method's constraint is the extremely high switching frequency; for instance, regulating the main path current at 10 A (a plausible assumption for an MVDC system with a rated current exceeding 1 kA) requires switching on and off within 0.3 μs with a 60 A/μs commutation rate, which is highly challenging [22]. To lower the switching frequency, one can either accept a reduced commutation rate–an undesirable outcome–or use multilevel structures with WBG devices [63], [100]. Although this may increase equivalent frequencies, control complexities also grow significantly.

A dual approach of the current injection, suggested in the literature [101], entails injecting a negative voltage instead of a negative current shown in Fig. 7. Pre-charged capacitors C_1 and C_2 can be connected by turning on S_1 and S_2 and disconnected by turning off S_1 and S_2. The core idea is to introduce a voltage with negative polarity to the DC bus voltage, which results in a decrease in current. This can be accomplished through direct voltage injection in low voltage DC systems where the pre-charged capacitor's voltage may exceed the DC bus voltage. However, for MVDC or HVDC systems with DC bus voltages spanning from several kV to hundreds of kilovolt, a high turns ratio transformer is required.

As suggested in the literature, a pulse transformer or coupled inductors with high coupling coefficients has been designed to accomplish this objective. [102] proposes a coupled inductor topology reliant on current reflection from an auxiliary resonant circuit in the primary winding. This design incorporates a current-fed high-gain converter, akin to a boost converter, to charge the capacitors effectively. In a similar vein, CCDC (Current Commutated DC breaker) proposed in [66] employs an air-core transformer, conceptualized as a mutual inductance component. This system diverges by utilizing a pre-charged capacitor that, upon activation of thyristors, discharges through the transformer's winding, creating a voltage across the opposite winding. During this operation, the mechanical switch enters an arcing state, with the semiconductor switch engaged. The CCDC thus generates an oscillating current between the mechanical and semiconductor switches, facilitating efficient current transfer. A notable limitation, however, is the requirement for a high-voltage isolated power supply for both the CCDC and other HCB components.

Further extending this concept, [103] adapts the coupled inductance model to various CCDC configurations, including the NPC type. [104] development also follows a similar trajectory, employing a thyristor in a full-bridge configuration to introduce bidirectional capabilities. Summarizing these diverse approaches, a key determinant in achieving rapid commutation rates is the coupling coefficient. Designing high-coupled inductors in high-power settings often involves a trade-off, balancing the need for efficient current transfer against practical constraints in switch ratings and system complexity. Also, further research is required to address the insulation requirements for MVDC or HVDC with such transformers/coupled inductors.

The load commutation switch is a solid-state device that operates considerably faster than a mechanical switch. During a fault interruption, the load commutation switch is turned off first, compelling the current to commutate to the solid-state switch branch. Diverse load commutation switch, or ACC, structures have been proposed, encompassing configurations like a single low-voltage, high-current rating switch as depicted in Fig. 8 Structure d, or designs inspired by full-bridge frameworks as seen in Structures e and f. The solid-state switches can also adopt different structures, ranging from series and/or parallel configurations in Structure I, to GTO-based in Structure II, or full-bridge configurations integrating fully controllable IGBTs and diodes in Structure III and IV, respectively. Notably, these configurations have been documented in operational HVDC projects as cited in [35], [36], [37], [73].

A comprehensive comparison of various commutation strategies can be seen in Table 1 and detailed important

TABLE 1. Comparison of Different Topologies Based on Different Commutation Mechanisms for HCBs

Category	Type	Advantages	Disadvantages	Exemplified references
Arc Commutation		Simple topology Easy operation	Arc quenching issues Reduced mechanical switch's reliability	[34]
Zero Voltage Commutation		No pre-charged circuit Minimal arc	Requires snubber design Needs fully controllable device	[95]
Zero Current Commutation	Current Injection	Fast commutation Minimal arc	Extra control for zero current Pre-charged circuit often required	[22]
	Voltage Injection	Similar to current injection	Needs full DC voltage	[101]
	Load Commutation Switch	Fast commutation Sustained zero current	Power losses	[35]

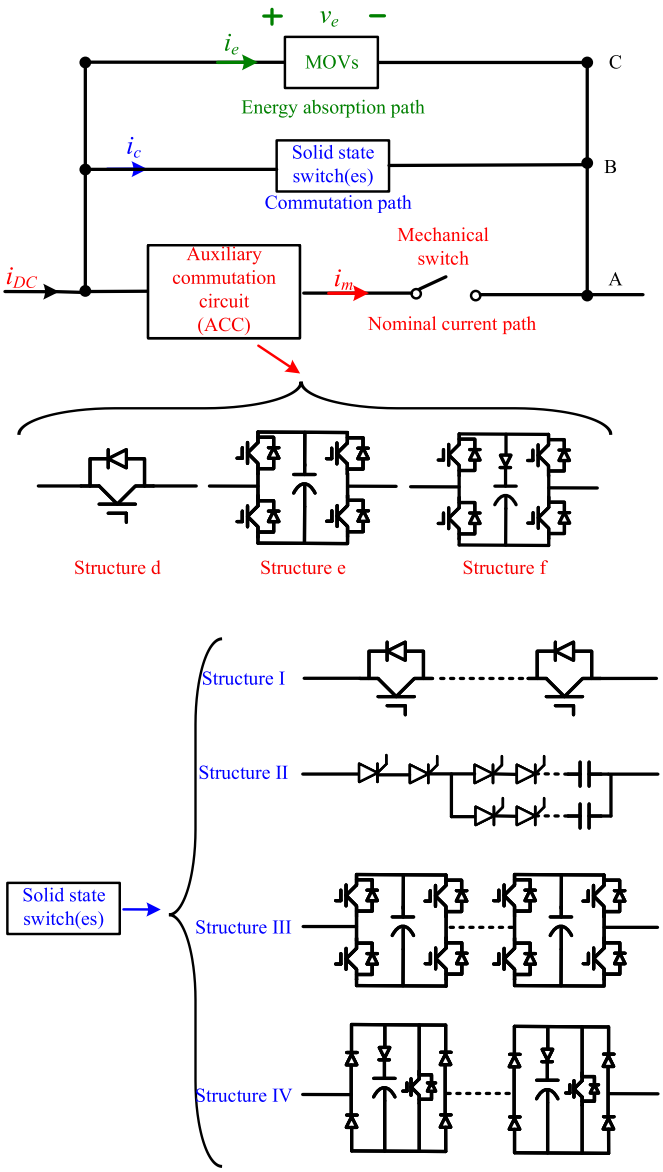

FIGURE 8. Load commutation switch-based zero current commutation. [35], [36], [37], [73].

metrics comparisons can be found in Table 2. The table illuminates how different commutation mechanisms lead to diverse topologies, each possessing unique advantages and disadvantages. The challenge often lies in balancing between simplicity of design and more degrees of freedom in control. For instance, while arc-based commutation systems are simple in structure, they struggle with current control. Zero current commutation, on the other hand, has gained considerable popularity in this regard. Current and voltage injection strategies are often limited by the energy storage capacity of their associated capacitors or inductors, which are used to counteract fault currents. On the contrary, the load commutation switch, through its design, commutates the current to the commutation path during its turn-off phase, bypassing this limitation. However, this comes at the expense of power losses during normal operation.

IV. SYSTEM INTEGRATION ISSUES IN HCBS

The preceding sections have focused on addressing critical challenges at the component level of HCBs. In this section, we will discuss various system-level issues, including current sensor selection and control delay minimization, both of which are crucial for high-speed current interruption. Besides, we will examine the pipeline design procedure from hardware in the loop to mitigate risks during prototype development and outline the requirements for test beds. Last but not least, system integration extends beyond the mere incorporation of components into a single HCB. It also involves the topological arrangement of several HCBs into an HCB-based switchgear intended for multi-terminal DC system protection. This aspect will also be discussed in the review.

A. CURRENT SENSOR SELECTION

CBs necessitate the utilization of current sensors capable of measuring the rapid current commutation process, which can reach several hundreds of amperes per microsecond. These sensors should minimally interfere with normal operation while maintaining a compact size if power density is a concern for the breaker.

TABLE 2. Comparison of the Exemplified HCB Circuits in Important Metrics

References	Voltage rating	Nominal Current	Peak current	Fault clearing speed	Current commutation rate	Submodule switch counts
[34]	12 kV	2000 A	25 kA	<1 ms	11 kA/ms	N/A
[95]	600 V	100 kA	N/A	N/A	N/A	2 SCR+3 mechanical switches+1 diode
[98]	12 kV	2 kA	8 kA	<500 us	400 A/us	2+6 IGBTs+1 Mechanical
[22]	12 kV	2 kA	8 kA	<500 us	100 A/us	1 diode+6 IGBTs+1 Mechanical
[101]	600 V	Start from 0	30 A	10 us	3 A/us	4 SiC JFET+4 IGBTs
[35]	320 kV	2 kA	9 kA	2 ms	3.5A/us	20 IGBTs+1 SF6 mechanical switch+Low rating switches for commutations
[36]	200 kV	2 kA	15 kA	3 ms	N/A	Full bridges
[37]	535 kV	3 kA	25 kA	3 ms	10 kA/ms	4 diodes+2 IGBTs
[73]	120 kV	1.5 kA	7.5 kA	4.3 ms	2.9 A/us	2 main thyristor+2*submodule thyristors+ 2 main IGBTs

Current sensors can be broadly divided into several categories, one of which is based on the flux measurement approach. This category can be further segmented into open-loop and closed-loop configurations. Closed-loop Hall sensors are utilized to measure current, as exemplified in [22], [105]. Alternatively, an open-loop Hall sensor, specifically the LEM HAS 400-S, is deployed to measure current, as depicted in [106]. These sensor types exhibit contrasting characteristics, with open-loop configurations being cost-effective but offering lower resolution. Conversely, closed-loop sensors deliver higher resolution at an elevated cost.

Another prevalent method involves using a shunt resistor, exemplified in [107]. The major drawback with this approach lies in the power losses resulting from resistor usage, which poses problems for MVDC or HVDC systems. Current sensors based on alternative technologies, such as Giant Magneto Resistance [108], have also been explored. However, commercially available options for diverse current ratings and voltages are less numerous compared to the previously mentioned sensor types.

In addition to DC current sensors, maintaining current for the opening of the mechanical switch in HCBs presents unique challenges, especially when PWM is employed for instance in Fig. 6(a) Structure b and c. Specifically, during the turn-off phase of the mechanical switch, the current must be tightly regulated to a near-zero level. There are alternative strategies for controlling the current as noted in the zero-current commutation section, such as using variable inductors or load-commutation switches to direct the current towards the commutation branch. Nevertheless, these approaches come with their own set of complications. For instance, the design of the variable inductor can be complex, and introducing load commutation switches into the main current pathway can result in increased losses and costs.

If the PWM method is used, the near-zero current has to be measured. This current measurement can be resolved by the additional sensor that is only meant to measure this small current. For measuring this small current, several requirements have to be met: first, it will not saturate during the DC nominal current as this additional sensor has to be co-located with the DC current sensor; second, this should not have excessive power loss or preferably no power-loss; last but not least, the current sensor should have enough bandwidth so that it can capature the dynamics during the current-holding period. Summarizing these key requirements, a non-intrusive PCB-based Rogoskwi coil is placed for the current measurment [109], [110]. The rogoswki coil's measuring principle is based on the rate change of the current and no saturation would occur for it. Hence, this Rogoswil coil can be served as additional sensor for measuring the small current during the current holding period.

B. CONTROL DELAY MINIMIZATION

To achieve precise and rapid control for HCB with extremely high current commutation rate, the following requirements must be satisfied:

1) Accurate control sequence: Any erroneous triggering of the mechanical switch or IGBTs in an incorrect sequence could produce a massive, uncontrollable arc, leading to the failure of current commutation and the destruction of the breaker.
2) Swift fault response and minimized control delay: As the targeted current commutation time is very short, the controller must respond quickly to the current slew rate. Any additional delay caused by the controller or measurements would defer the current commutation process and increase the peak value of a fault current, potentially resulting in an inability to interrupt the fault current.

The control latency can be attributed to two factors: hardware latency and software latency. Hardware latency is primarily limited by the bandwidth of specific components, such as the current sensor, which introduces certain delays. Although employing a higher bandwidth sensor can reduce this delay, it often results in increased costs. In contrast, software delay is a more universal issue, independent of topologies, as each topology involves certain sequential control.

As reported in [22], using a control-law-accelerator can reduce the time delay by 33%. This reduction is crucial in high commutation rate scenarios, as a 33% delay reduction (0.8 μs) corresponds to an 80 A difference when a 100 A/μs commutation rate occurs. Another approach is implementing a dual-core structure. The dual-core structure can assign tasks with different sampling frequencies to independent cores, increasing computation efficiency. This feature is particularly beneficial in HCBs, as most HCBs operate in a monitoring mode that communicates with other system elements, such as relays, at a slow rate, typically in the millisecond timeframe. However, when a fault event occurs, the entire fault clearing process must be completed within 1 ms for MVDC systems, requiring switches to be controlled within a microsecond

timeframe. As a result, the monitoring tasks can be assigned to one core, while the time-critical control tasks can be delegated to the other core. The two cores can communicate via an internal bus within the DSP, which features negligible delay. Due to this dual-core structure, there is a 25% delay reduction compared to a single-core structure [22]. Furthermore, since the HCBs' monitoring mode occupies most of the operation time, the two-core configuration in the monitoring mode is equivalent to the single-core case without increasing computation burden.

Similarly, in a project commissioned for Zhangbei as reported by [111], a DSP TMS320C6657 with a core speed of 1.25 GHz, together with a Xilinx XC7K325 FPGA structure, were employed to minimize delay from the hardware standpoint. From the software's perspective, a finite state machine control architecture was incorporated to manage events such as turn on, turn off, and reclosing, among others. For data transmission, a Serial Rapid IO interface was utilized, supporting a data volume of 2000 bytes with a transmission speed of 10 Gbps.

A timely control is also critical for a new HCB control method which turns off semiconductor submodules one after another to establish breaker voltage while the switch contacts are still separating in an ultrafast DS [112], [113], [114]. The benefit is the acceleration of voltage build-up and fault current attenuation at an earlier moment. However, if the semiconductors are turned off too early and the MOV voltage goes higher than the insulation withstand limit of contact gap, there could be breakdown failures in the DS [115], [116]. In this manner, it is critical to ensure a low-latency, closed-loop control of HCB to maximize the benefits of this novel HCB control method [22].

C. MOV ENERGY BALANCING

In HCB systems, fault current redirection into the energy absorption pathway, comprising MOVs, is achieved by turning off IGBTs in solid-state switches. A critical limitation of this conventional HCB tripping method is its reliance on mechanical switches attaining sufficient voltage tolerance to withstand the counter-voltage from parallel MOVs prior to commutating the fault current into the MOV paths.

The 'sequential tripping' strategy, also termed 'progressive switching,' addresses this by sequentially turning off semiconductor switches. This approach mitigates the simultaneous turn-off challenge but introduces several complications: 1) The need for multiple switching actions to either insert or bypass MOVs, which may induce overvoltages damaging both the FMS and semiconductor switches. 2) An unbalanced energy distribution among the MOVs, potentially compromising HCB reliability and performance.

Open-loop control systems, proposed in [115], rely on pre-set tripping sequences and timings, yet their effectiveness diminishes under variable system conditions. Alternative strategies, such as rotating the MOV insertion order ([117], [78]), fail to guarantee long-term energy equilibrium. Adjusting MOV sizes ([113]) negatively impacts HCB modularity and scalability. In contrast, closed-loop systems ([55]), resembling MMC capacitor voltage balancing methods, offer greater adaptability but risk excessive switching and voltage overshoot, especially in non-continuous applications like DC-CBs.

A novel approach outlined in [112] suggests enhancing gate turn-off resistance. This strategy circumvents the need for additional components like RCD snubbers to address the overvoltage issue. Furthermore, an MOV energy balancing algorithm that merges pre-defined tripping sequences with real-time energy absorption-based timings is posited. This method aims to minimize switching actions and ensure consistent energy balance under varying conditions. However, its efficacy is contingent on the precision and stability of MOV characteristics.

D. HARDWARE IN THE LOOP PROTOTYPING AND TESTBED BUILTUP

Designing HCBs presents a formidable challenge, especially in the realm of precision control. Rapid commutation rates, reaching into hundreds of amperes per microsecond, necessitate impeccable timing control; any latency, however minuscule, could result in considerable control errors. Parasitic parameters add another layer of complexity by influencing the commutation rate. Experimental testing, in the absence of precise models, poses undue safety risks and is often a less optimal approach.

In order to circumnavigate these obstacles, HIL has shown promise as a practical tool for refining control algorithms and detecting potential latencies under various testing conditions [118], [119]. By mitigating risks associated with physical trials, HIL enhances the safety and reliability of experimentation. Additionally, HIL modeling proves useful in studying HCBs' behavior within a system. By treating the HCB as a "black box" within MVDC or HVDC systems, we can explore system-level control.

Nevertheless, replicating HCBs in an HIL environment poses its own set of challenges. HCBs comprise mechanical switches, solid-state components, and often MOVs for energy absorption. Accurately modeling the behavior of mechanical switches–particularly their turn on and turn off characteristics–poses a significant hurdle due to the dearth of available models. The case for solid-state parts is a balancing act between modeling complexity and fidelity, especially when multiple HCBs are employed in MVDC or HVDC systems. If heat dissipation becomes a concern, a thermal model for the solid-state components is required. MOVs, similar to mechanical switches, lack readily available components in the HIL library and their highly nonlinear behavior further complicates their representation.

One approach to model solid-state switches is to utilize a truth table to represent the on and off binary states, a strategy used in [120]. While useful for studying the functioning of HCBs in a system, this model doesn't offer adequate insights into HCB design. [121] took a similar route, deriving HCB's

equivalent circuit for each operational stage and finding the respective analytical solutions. Nonetheless, the solutions may be imprecise due to the non-linear traits of MOVs, mechanical switches, and snubber circuits. Both of these methods offer system level models, relatively simple to deploy in HIL settings but lack detailed insights for HCB design. Alternatively, device level models can be used for HIL. For instance, [122] developed an IGBT device model for FPGA HIL based on pre-measured experimental data, incorporating switching losses and detailed switching characteristics. This model aids in HCB design. [123] extended this methodology, developing three distinct models apt for different applications: a two-state model, a curve fitting model, and a nonlinear behavior model. A comparison of device-level and system-level performance between HIL emulation and commercial offline simulation tools validated the models' accuracy.

For mechanical switch modeling, a common method is a two-state model representing on and off resistors [123], [124]. However, [22] modeled the mechanical switch according to a derived transfer function and represented it in an equivalent circuit model. Since mechanical switches vary significantly, their characteristics do as well. Therefore, it's advisable to start with a two-state model and, if necessary, derive a detailed model following individual switch testing, and represent it in a curve-fitting or equivalent circuit manner.

MOVs models usually fall into two types. The first, exemplified in [123], is a nonlinear resistor model. However, transient stage computations often require over 20 iterations, significantly extending computational time. Hence, the nonlinear function must be piecewise linearized into ten sections to reduce iteration times. A simpler strategy is represented by [22], utilizing a diode and snubber circuit.

In addition to modeling, verification of HCBs constitutes another significant hurdle, especially on the laboratory scale. As summarized by [125], existing test benches for circuit breakers, with regards to voltage and current ratings, unfortunately, fall short of replicating real-world conditions. To navigate this shortcoming, dual-circuits have been proposed to separately test the HCB's maximum current interruption and voltage withstanding capabilities [126]. However, despite the relative simplicity of this circuit's implementation, it presents issues such as limited current controllability and non-smooth transitions between tests. [127] provides a comprehensive summary of current test circuits used for HCB verification. Ranging in complexity, the simplest of these circuits involves a capacitor discharging to an HCB to assess its current interruption abilities. However, this approach fails to evaluate voltage withstand capabilities and may necessitate the inclusion of additional passive elements like thyristors as backup protective devices in the event of a test circuit failure. A slightly more complex dual-circuit is depicted in [126] with the aforementioned disadvantages. A third testing approach utilizes a low-frequency AC short-circuit-generator-based test bench. Despite its low frequency, the AC voltage produced by this circuit differs from DC voltages, meaning that maximum voltage withstanding capabilities for AC and DC can vary.

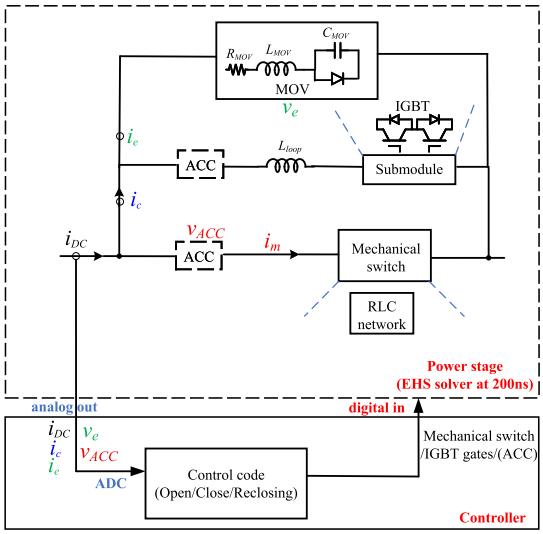

FIGURE 9. Showcase of a CHIL implementation of a typical HCB.

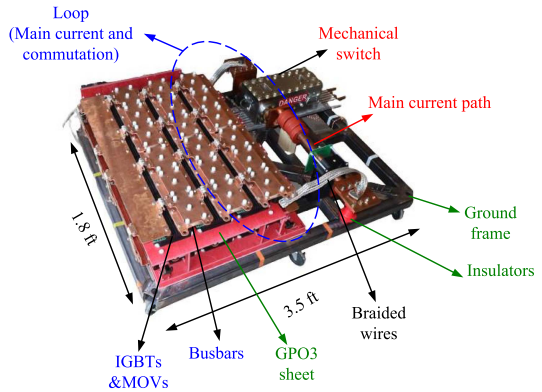

FIGURE 10. 12 kV and 2 kA HCB breaker prototype prototype [22].

Thus, the results obtained from this test circuit may not accurately reflect real-world DC applications. The most complex approach, offering the best controllability, employs converters to simulate all fault test waveforms, a strategy similar to Power Hardware-in-the-Loop [118] or grid emulators [128] used for converter testing. By utilizing the extensive controllability of converters, the output current and voltage can be directly generated by the converter. The primary disadvantage is that the test capabilities heavily depend on the converters or power amplifiers required for circuit testing.

Fig. 9 showcases a CHIL implementation of a typical hybrid circuit breaker. The CHIL connection entails the controller receiving analog outputs from the CHIL simulator and sending digital inputs to the mechanical switches and solid-state switches or ACCs if necessary. CHIL simulation serves as an excellent method for verifying the entire control sequence discussed earlier, determining time delays, and providing guidelines for selecting appropriate phase margins for the hardware, as increased delays could amplify current or voltage magnitudes.

Fig. 10 illustrates a MVDC circuit breaker with a rating of 12 kV and 2 kA. This prototype serves as a reference for the general layout and design of HCB [22]. Several important features must be highlighted. Firstly, it is crucial to maintain a small loop between the main current path and the commutation path to minimize loop inductance. To accomplish this, not only is the physical size of the mechanical switches and solid-state circuits taken into account, but also braided wires are employed to conduct sufficient current. These wires establish flexible connections over short distances to minimize resistance. Furthermore, bus bars span the entire commutation path to reduce inductance. The second critical aspect is achieving appropriate insulation. A ground frame is advised to connect the high power circuit's chassis. Insulators are used to prevent any discharge from high to low voltage potential. A GPO3 sheet is employed to ensure solid insulation. Along with the HIL control and the test circuit for the HCB as discussed, this outlines a general design process for an HCB circuit.

E. HCB-BASED MULTI-TERMINAL DC SWITCHGEAR SYSTEM

In this subsection, the integration of multiple HCBs will be discussed to accommodate the need to protect multi-terminal DC grids. A seemingly straightforward approach would be to deploy HCBs at every connection. This implies that for a DC bus connected to (n-1) lines, each line should be equipped with an HCB for protections. However, this strategy presents considerable challenges, including elevated costs and substantial space requirements.

A more feasible solution leans towards the utilization of HCB-based multi-terminal DC switchgear system, especially favored for multi-terminal DC power grids at MVDC or HVDC levels. The essence of this switchgear is grounded in the notion that multiple lines can share pivotal components like MOVs or solid-state switches, thus reducing system expenses substantially. It's imperative to underline, though, that this approach mandates the addition of selector switches for each line, sometimes referred to as residual current breakers [129], or auxiliary switches [130]. Nevertheless, the costs associated with these selector switches are markedly lower than those of solid-state switches and MOVs, accounting for only a sliver of the overall expenditure.

The operation of this HCB-based multi-terminal DC switchgear system mirrors the principles of two-port HCBs, with the main difference lying in the communal usage of components across diverse lines. A study by S. Zhang et al [131] segregates these setups into three categories: ground bridge, half bridge, and full bridge. Within this framework, it's important to highlight that half bridge and full bridge allude to the selector switch configurations, not the solid-state switch modules. In terms of each line's circuit breaker, they are delineated based on commutation principles into forced current commutation, termed as load commutation switch herein, and artificial current zero crossings, dubbed as current injection in this paper. Hence, the merits and shortcomings of these HCB-based multi-terminal DC switchgear systems follow those of load commutation switch-based and current injection-based alternatives. Concurrently, similar work has proposed diverse topologies and cohesive structures for this switchgear. For instance, C. Zhang et al. [132] proposed the merger of the switchgears with a current flow controller, while N. Han et al. [133] championed its amalgamation with a fault current limiter. Broader comparisons and fiscal evaluations are elaborated in [131].

To amplify our grasp and deployment of these switchgears, ongoing evolution and enhancement of models, such as state-space models for half-bridge types as spotlighted in [130], are required. This modeling paradigm is equally relevant for other circuit breakers. Furthermore, a graph theory-driven perspective on diverse prospective topologies for the switchgear was introduced in [134]. In short, despite the assorted configurations within the HCB-based multi-terminal DC system switchgear, their operational principles and architecture remain deeply rooted in two-port HCBs. At present, while this switchgear represents a promising solution for multi-terminal DC protections, a more in-depth exploration into their dependability and failure scrutiny is needed.

V. CONCLUSION AND FUTURE WORK

This paper offers an extensive review of HCBs. The progress in HCB technology can be attributed to advancements at the component, topology and system integration levels. This paper surveys the state-of-the-art mechanical and solid-state switches, as well as MOVs, which together form the basic structure of an HCB. Additionally, the paper categorizes HCB topologies by proposing a unified HCB structure, with the ACC serving as the differentiating factor for distinguishing each topology. System-level issues, such as control and pipeline design of HCBs, are also discussed to provide valuable resources for researchers and designers, facilitating a more streamlined design process.

Future work in the field of HCBs can be envisioned in the following areas:

- (1) Component level: The mechanical switch, which serves as the speed bottleneck for HCBs, has significant potential for improvement through the use of different switching technologies, such as PAs. For PAs themselves, the issues discussed in this paper need to be addressed through the development of new materials and control schemes. Furthermore, with the availability of solid-state switches featuring higher power density and power ratings, there are opportunities to enhance the compactness of HCBs and increase their switching counts.
- (2) System level: The system-level sequential control must keep pace with speed requirements. As a result, faster controllers with optimized software code are necessary. Additionally, accurate loop inductance estimation and thermal design are crucial and require iterative processes and precise software predictions and more versatile CHIL elements.

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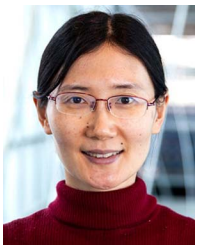

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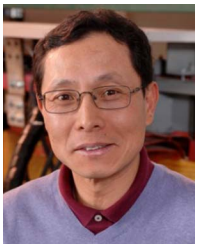

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