Wear-Out Analysis of a Grid-Forming Two-Phase Three-Wire Converter Under Unbalanced Load

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ABSTRACT The grid-forming converter that supplies voltage magnitude and frequency is a key element for isolated remote communities, and then wear-out analysis is an essential figure of merit. Therefore, this paper proposes the two-phase three-wire (2Φ3 W) grid forming converter applied in a case study of isolated riverside communities in the Brazilian Amazon region. The proposed *xyn*-converter displaces the voltage line angle in 180°, differing from $\alpha\beta n$-converter and *abn*-converter that displace voltage line angle in 90° and 120° respectively. First, the authors have also proposed a semiconductor current stress evaluation for 2Φ3 W converters comparing the RMS current. Then, the lifetime evaluation of the three evaluated grid-forming converters is conducted. The results show that the converter operating in the *xyn*-converter presents the highest reliability among the three converters. Finally, the thermal stress analysis is validated by means of a 2Φ3 W converter prototype with an open semiconductor module. For the evaluated converters, the *xyn*-converter has the least thermal stress for balanced and unbalanced load conditions and therefore the longest lifespan. The experimental validation shows that the average temperature of the *xyn*-converter is 19.4% and 23.3% lower than both the *abn*-converter and the $\alpha\beta n$-converter under balanced load conditions.

INDEX TERMS Grid-forming converter, isolated AC power grids, lifetime consumption, wear-out.

I. INTRODUCTION

Different configurations for ac power grids are proposed in the literature, such as single phase, two-phase two-wire, two-phase three-wire, three-phase three-wire and three-phase four-wire. This paper focuses on the two-phase three-wire (2Φ3 W) isolated power system, with two phases and neutral. In real applications, the 2Φ3 W grid is a common practice in some regions of South America, especially in Brazil, for rural areas using single-phase transformers with tapped secondary and neutral [1]. In addition, isolated grids are found in some parts of Africa, Central America, Asia, and Europe [2].

Reference [3] shows the reliability of 2Φ3 W PV inverters considering three different configurations of the grid structure in terms of the displacement of the line voltage angle: 90° ($\alpha\beta n$); 120° (*abn*) and 180° (*xyn*). Since thermal loading directly affects the lifetime of power converters, phase angle

displacement plays an important role. The authors in [4] have compared the *abn*, $\alpha\beta n$ and *xyn* systems for active power oscillation and the magnitude of the neutral current.

Other references have investigated the control of 2Φ3 W power converters. The authors in [5] present the results of an active power filter to compensate harmonics and exchange reactive power with the 2Φ3 W grid. Reference [6] shows a flexible control strategy based on the Conservative Power Theory capable of adequately synthesizing control references for a photovoltaic-based multifunctional inverter operating in a 2Φ3 W grid. The authors of [7] formulated alternative methods through the p-q theory focusing on the control of 2Φ3 W converters driven with the overlap of two simultaneous operation modes to further mitigate neutral currents. The authors of [8] propose active power conditioning in 2Φ3 W circuits based on the exchange of powers between existing

phases, using the DC link of multilevel converters. All of these works use an angle displacement of 120° between the line voltages. The main advantage of this grid configuration is the direct connection with the distribution power system, which is usually set as a three-phase grid.

The authors in [9] and [10] have proposed the quadrature line voltages for the 2Φ3 W electrical power system (i.e., displaced by 90°). In this grid configuration, the instantaneous active power is constant, which reduces the inherent voltage oscillation on the DC-bus of the power electronics converters.

It is possible to find some works concerning reliability of power electronic converters in the literature. The reliability of an isolated buck-boost DC-DC converter (IBBC), designed with a series resonant converter (SRC) configuration, is investigated in [11]. Reference [12] proposes a new method to assess the reliability of fault-tolerant power converters, considering wear-out failure. In [13], the overall system reliability of a single-phase two-stage PV inverter involved in reactive power compensation is evaluated, considering three different mission profiles (Aalborg, Goiânia, and Izaña).

Different studies have looked into how the chosen mission profile can influence the system or converter lifetime consumption. Reference [14] suggests a strategy to correct errors in the estimation of the lifetime consumption of a single-phase grid-connected photovoltaic inverter when the resolution of the mission profile decreases. In [15], a design tool is introduced to explore how mission profiles can impact the reliability of SiC-based PV inverter devices. Reference [16] examines the reliability of PV inverters, specifically focusing on the effects of varying the resolutions of the mission profile.

However, a notable gap in the literature lies in the discussion of current stresses and wear-out experienced by 2Φ3 W power converters. Reference [17] mainly compares the wear-out between the three grid-forming converters (GFC) (*xyn*, *αβn* and *abn*) under balanced load conditions and unit power factor. Hence, this paper aims at fulfilling such a gap by providing the following contributions:

- Comparison of analytical expressions for semiconductor current stress under realistic current unbalances between phases, considering amplitude current unbalance, and angular displacement between voltage and current in each phase;
- Employs a lifetime prediction methodology to demonstrate the performance of the *xyn*-GFC when compared to *abn* and *αβn* converters;
- Additionally, experimental tests are conducted to measure thermal stress, establishing that the *xyn*-GFC experiences the lowest thermal stress among the three evaluated 2Φ3 W converters.

The organization of this paper is as follows: Section II presents the proposed analytical evaluation of semiconductor current stresses for various load conditions. Section III outlines the wear-out prediction method and thermal measurement experiments. The simulation and experimental results are detailed in Section IV, and the conclusions are summarized in Section V.

II. PROPOSED SEMICONDUCTORS CURRENT STRESS EVALUATION FOR GENERAL LOAD CONDITION

The GFC structure evaluated in this paper is shown in Fig. 1. Analytical expressions are obtained for the average (I_{AVG}) and RMS (I_{RMS}) current values through the power devices (S_1-S_6 and d_1-d_6). The computation of average and RMS currents is inspired on the approach derived in [18], which has calculated the current stress for a three-phase converter, and has been adapted for the 2Φ3 W converter. The analytical model neglects the current ripple in the output of the converter and considers perfect sinusoidal signal modulation for sinusoidal pulse width modulation (SPWM) as shown Fig. 2, without loss of generality. The duty cycle δ of the voltage pulses is obtained by comparing the modulation signal with the carrier signal ($v_{(j,k,n),n}$) given by:

$$\delta = \frac{1}{2}\left[1 + Mv_{(j,k,n),n}\right]. \tag{1}$$

where the subscripts j, k and n represent the phases of the converter, and M is the modulation index given by:

$$M = \frac{2V_L}{v_{dc}}, \tag{2}$$

where V_L is the line-to-neutral peak voltage, and v_{dc} is the DC-link voltage. The voltage and current values in the output of the converter are as follows:

$$v(t)_{j,k} = V_{j,k}\sin\left(\omega t + \theta\right), \tag{3}$$

$$i(t)_{j,k} = I_{j,k}\sin\left(\omega t + \theta + \phi_{j,k}\right), \tag{4}$$

where $V_{j,k}$ and $I_{j,k}$ are the peak values of voltage and current in each phase respectively, θ is the angle displacement between the phase voltages (in this paper $\theta = 90°$, $120°$ or $180°$ in phase k, $\theta = 0$ in phase j), and $\phi_{j,k}$ is the angle displacement between voltage and current in each phase.

The current flows through the IGBTs during the switching period T_s, as shown in Fig. 3. The average and RMS currents values are given by:

$$I_{AVG} = \frac{1}{T}\int_t^{T+t} \delta i_t.dt, \tag{5}$$

$$I_{RMS}^2 = \frac{1}{T}\int_t^{T+t} \delta i_t^2.dt. \tag{6}$$

where T is half of the fundamental period of the current.

For the $\alpha\beta n$-converter configuration, $\theta = \frac{\pi}{2}$. The average current trough the phase leg semiconductor S_1 at the $\alpha\beta n$ converter consider the duty cycle as:

$$\delta_{S_1} = \frac{1}{2}\left[1 + Mv_{jn}\right] = \frac{1}{2}\left[1 + M\sin(\omega t)\right]. \tag{7}$$

Using (5), (6), and (7) the average and RMS currents through switch S_1 are:

$$I_{AVG,S_1} = \frac{1}{\pi}\int_0^\pi \frac{1}{2}\left[1 + M\sin(\omega t)\right]I_j\sin\left(\omega t + \phi_j\right)d\omega t, \tag{8}$$
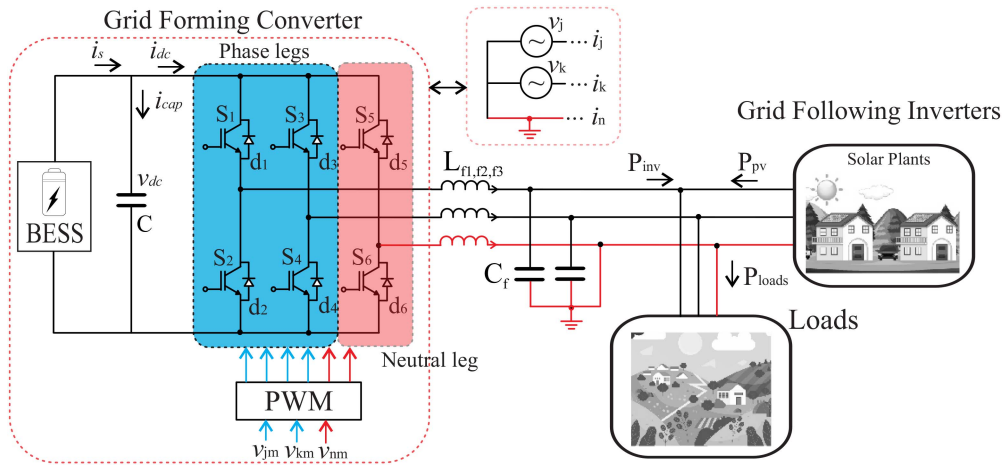
FIGURE 1. Structure of a grid-forming converter for 2Φ3 W isolated ac power grid.
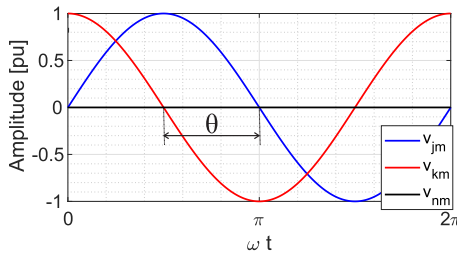

FIGURE 2. 2Φ3 W reference signals for SPWM. θ is the displacement angle of the voltage references, which can assume 90°, 120° or 180°.
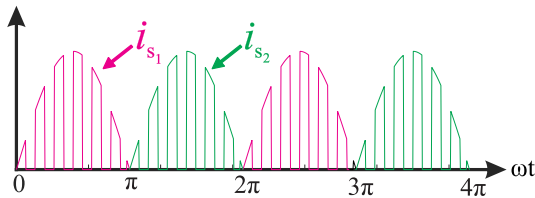

FIGURE 3. Collector currents of IGBTs S_1 and S_2.

$$I_{AVG,S_1} = \frac{I_j}{\pi} + \frac{MI_j}{4}\cos(\phi_j). \qquad (9)$$

$$I^2_{RMS,S_1} = \frac{1}{\pi}\int_0^\pi \frac{1}{2}\left[1 + M\sin(\omega t)\right] I_j^2 \sin^2\left(\omega t + \phi_j\right) d\omega t, \qquad (10)$$

$$I_{RMS,S_1} = I_j\sqrt{\frac{1}{4} + \frac{2M\cos(\phi_j)}{3\pi}}. \qquad (11)$$

The average and RMS currents stress for S_2 is similar to S_1 presented in this section, regardless of the adopted converter configuration. The procedure for switches S_3 and S_4 differs in the peak current, which is I_k instead of I_j, and ϕ_k instead ϕ_j.

The procedure for the current stress evaluation of diodes is identical to that of IGBTs. The difference is the duty cycle. As an example, the duty cycle for diode d_1 is given by:

$$\delta_{d_1} = 1 - \frac{1}{2}[1 + Mv_{jn}] = 1 - \frac{1}{2}\left[1 + M\sin(\omega t)\right]. \qquad (12)$$

Thus, the average and RMS current stress for the diode d_1 are:

$$I_{AVG,d_1} = \frac{I_j}{\pi} - \frac{MI_j}{4}\cos(\phi_j). \qquad (13)$$

$$I_{RMS,d_1} = I_j\sqrt{\frac{1}{4} - \frac{2M\cos(\phi_j)}{3\pi}}. \qquad (14)$$

The average and RMS currents for the diode d_2 is similar to the diode d_1 regardless of the adopted converter configuration. For diodes d_3 and d_4, the difference is the peak current which is I_k instead of I_j, and ϕ_k instead of ϕ_j.

The modulation signal to compare with the carrier signal for neutral IGBTs is a constant signal ($v_{nm} = 0$). Thus, the duty cycle for neutral leg semiconductors does not depend on the modulation index and shows a constant value ($\delta = \frac{1}{2}$). Fig. 4 shows the currents at the output of each converter topology, considering balanced load conditions, highlighting the period when the switch S_5 conducts during the positive half-cycle of the neutral current. The integration interval to calculate the average and RMS current of the neutral leg switches is affected by load unbalances. In this paper, two types of unbalance are considered separately for the analysis of current stress in neutral semiconductor devices: current amplitude and angular phase displacement between voltage and current in the phases.

The average and RMS current stresses on switch S_5 are as follows:

$$I_{AVG,S_5} = \frac{1}{\pi}\int_{t_i}^{t_f} \frac{1}{2}\left[-I_j\sin\left(\omega t + \phi_j\right)\right.$$
$$\left. - I_k\sin\left(\omega t + \phi_k + \theta\right)\right] d\omega t, \qquad (15)$$

$$I^2_{RMS,S_5} = \frac{1}{\pi}\int_{t_i}^{t_f} \frac{1}{2}\left[-I_j\sin\left(\omega t + \phi_j\right)\right.$$
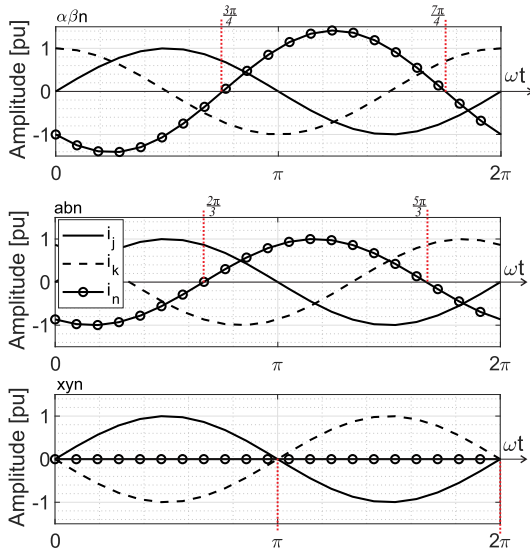$$\left. - I_k\sin\left(\omega t + \phi_k + \theta\right)\right]^2 d\omega t, \qquad (16)$$

FIGURE 4. Phase current of the 2Φ3 W converters: $\alpha\beta n$, *abn*, and *xyn*. Balanced load conditions.

where t_i and t_f are the start and end of the integration period.

Note that for neutral semiconductors, the duty cycle is identical for IGBTs and diodes. Therefore, the current stress is the same on IGBTs and diodes.

A. STRESS CURRENT FOR AMPLITUDE CURRENT UNBALANCE

For this analysis, $I_j \neq I_k$, $\phi_j = \phi_k = \phi$. In this case, the integration interval to obtain the current stress occurs when the neutral current is equal to zero, thus:

$$-I_j \sin(t_i) - I_k \sin(t_i + \theta) = 0. \tag{17}$$

Thus, for each converter, it is possible to find the integration interval by finding the roots of (17) for each θ value. Therefore, the integration intervals for each system are as follows:

$$
\begin{cases}
t_{i,\alpha\beta n, AU} = \arctan\left(-\frac{I_k}{I_j}\right), \\
t_{i,abn, AU} = \arctan\left(\frac{\frac{\sqrt{3}}{2}}{\frac{1}{2} - \frac{I_j}{I_k}}\right), \\
t_{i,xyn, AU} = \pi, \\
t_{f,alpha\beta n, AU} = \arctan\left(-\frac{I_k}{I_j}\right) + \pi, \\
t_{f,abn, AU} = \arctan\left(\frac{\frac{\sqrt{3}}{2}}{\frac{1}{2} - \frac{I_j}{I_k}}\right) + \pi, \\
t_{f,xyn, AU} = 2\pi.
\end{cases}
\tag{18}
$$

where the subscript *AU* represents the current amplitude unbalance analysis. Using (15), (16) and (18) the average and RMS current for the semiconductor devices of the neutral leg are calculated for unbalanced current amplitude. Table 1 summarizes the expressions proposed for semiconductors, considering a generic system.
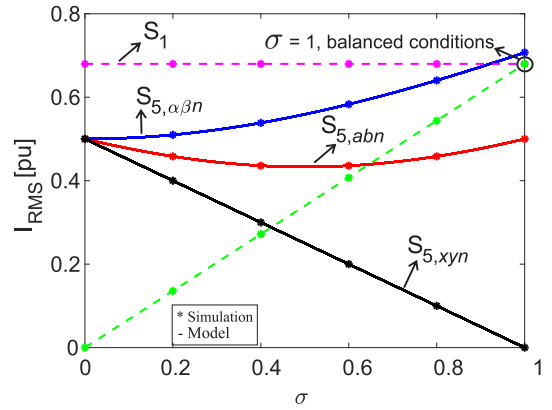

FIGURE 5. RMS current through the IGBTs for different unbalanced factor. *Remark:* The RMS current in the phase legs is the same for all the considered converters. The main differences are observed in the neutral leg devices.

B. STRESS CURRENT FOR DIFFERENT ANGLE DISPLACEMENTS UNBALANCE

For this analysis, $I_j = I_k$, $\phi_j \neq \phi_k$. As explained in the previous subsection, the integration interval to obtain the current stress occurs when the neutral current is equal to zero. The integration interval is then defined by:

$$
\begin{cases}
t_{i,\phi U} = -\frac{\phi_j + \phi_k + \theta}{2}, \\
t_{f,\phi U} = -\frac{\phi_j + \phi_k + \theta}{2} + \pi.
\end{cases}
\tag{19}
$$

where the subscript ϕU represents the different angle displacements unbalance analysis. Using (15), (16) and (19) the average and RMS current for the semiconductor devices of the neutral leg are calculated for different angle displacements unbalance, and are found in Table 1.

C. EFFECT OF CURRENT AMPLITUDE UNBALANCE ($I_j \neq I_k$, $\phi_j = \phi_k$)

The unbalanced load is taken into account in the current stress evaluation assuming the following relation in the phase currents amplitudes:

$$I_k = \sigma I_j, \tag{20}$$

where σ is the unbalance factor, the ratio between the peak currents of phase k and phase j. The system is current balanced when $\sigma = 1$, and $\phi_j = \phi_k$.

Fig. 5 shows the currents through the switches S_1, S_3, and S_5 under current unbalance in the phase legs of 2Φ3 W converters, considering $\phi_j = \phi_k = \phi = 0$. The RMS values of the current stress, obtained by means of Table 1, are plotted in per unit (pu) values of the rated current. Due to the SPWM modulation, the current stress differs only on the neutral leg. When the converter is under balanced load condition, the current through the switches S_1 and S_3 is the same. However, when $\sigma \neq 1$, the current through the switch S_3 increases with an increase of σ. Regardless of the value of the unbalance factor, the RMS current through switch S_5 is always lower in

TABLE 1. Proposed Analytical Expressions of Current Stresses on the Power Semiconductor Devices of 2Φ3 W Converter

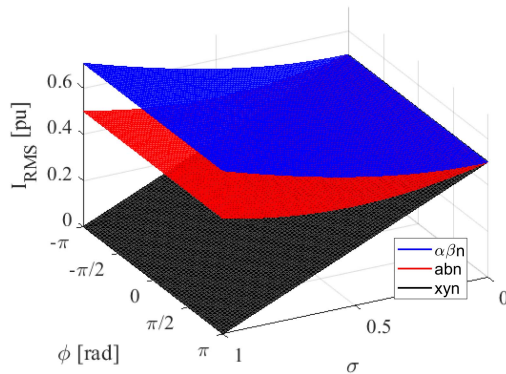|	S_1-S_4	
System	I_{AVG}	I_{RMS}
All systems	$\dfrac{I_{j,k}}{\pi} + \dfrac{M I_{j,k} \cos\phi_{j,k}}{4}$	$I_{j,k}\sqrt{\dfrac{1}{4} + \dfrac{2M\cos\phi_{j,k}}{3\pi}}$
	d_1-d_4	
All systems	$\dfrac{I_{j,k}}{\pi} - \dfrac{M I_{j,k} \cos\phi_{j,k}}{4}$	$I_{j,k}\sqrt{\dfrac{1}{4} - \dfrac{2M\cos\phi_{j,k}}{3\pi}}$
	S_5-S_6, d_5-d_6	
	Amplitude unbalance	
$\alpha\beta n$	$\dfrac{\sqrt{I_j^2 + I_k^2}\cos(\phi)}{\pi}$	$\sqrt{\dfrac{I_j^2 + I_k^2}{4}}$
abn	$\dfrac{(I_k - 2I_j)\sqrt{\dfrac{I_j^2 - I_j I_k + I_k^2}{(I_k - 2I_j)^2}}\cos(\phi)}{\pi}$	$\sqrt{\dfrac{I_j^2 - I_j I_k + I_k^2}{4}}$
xyn	$\dfrac{(I_j - I_k)\cos(\phi)}{\pi}$	$\sqrt{\dfrac{(I_j - I_k)^2}{4}}$
	Angle displacement unbalance	
$\alpha\beta n$, abn, xyn	$\dfrac{(I_j + I_k)\cos(\frac{1}{2}(\theta + \phi_k - \phi_j))}{\pi}$	$\sqrt{\dfrac{I_j^2 + 2I_j I_k \cos(\theta + \phi_k - \phi_j) + I_k^2}{4}}$

FIGURE 6. RMS current through the IGBTs of the neutral leg (S_5 and S_6) considering different unbalance factor and $\phi_j = \phi_k$.
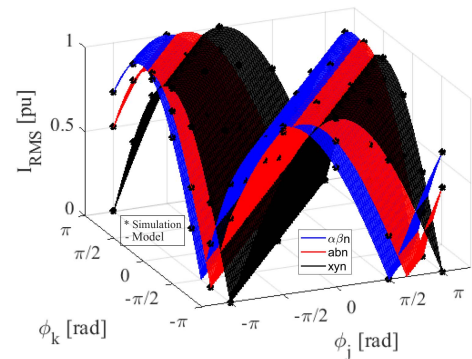

FIGURE 7. RMS current through the IGBTs of the neutral leg (S_5 and S_6) considering $I_j = I_k$, and $\phi_j \neq \phi_k$.

the *xyn*-GFC than in the other two converters, leading to a lower loss. The $\alpha\beta n$-GFC shows the highest loss value in neutral switches, regardless of the current unbalance between the phases. The values of the analytical equations were compared with simulations conducted in PLECS for several operating points, as shown in Fig. 5. The maximum error obtained between the simulation and the equations is 0.1%.

In the literature, it is recommended to consumers that loads should be distributed in the system equally between phases, and the maximum value adopted for the difference in the maximum current from one phase to another should be 10% [19]. Fig. 6 shows the effect of current unbalance on neutral switches for each converter for a different angle displacement between voltage and current. Regardless of the value of σ, the *xyn*-GFC shows the lowest stress value under unbalanced load conditions.

D. EFFECT OF DIFFERENT ANGULAR DISPLACEMENTS ($I_j = I_k$, $\phi_j \neq \phi_k$)

For this analysis, identical current amplitudes in phases are considered ($I_j = I_k$=1 pu), and the effects of different angular displacements between voltage and current in each phase (i.e., $\phi_j \neq \phi_k$) on semiconductor current stress are investigated. Fig. 7 illustrates the current stress for different values of angular displacement between voltage and current in the phases. It is evident that there are regions where each converter shows the highest stress. The values of the analytical equations were compared with simulations conducted in PLECS for several operating points, as shown in Fig. 7. The maximum error obtained between the simulation and the equations is 0.1%.

Fig. 8 provides a top view of Fig. 7, considering only the angular displacement values of each phase. This result shows that all three converters have regions where they are the most
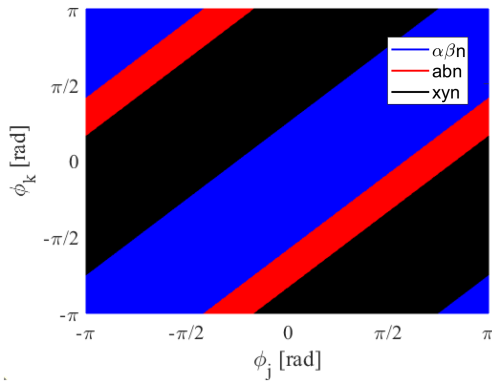
FIGURE 8. Top view of the RMS current through the active switches of the neutral leg (S_5 and S_6) considering $I_j = I_k$, and $\phi_j \neq \phi_k$.
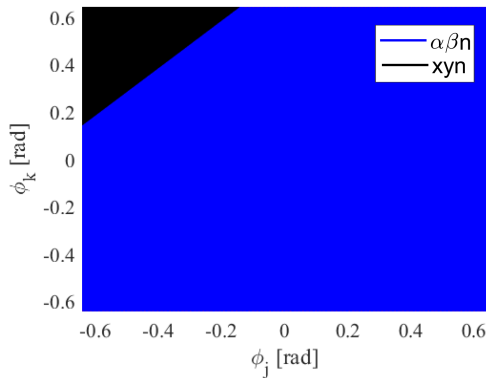

FIGURE 9. Top view of the RMS current through the active switches of the neutral leg (S_5 and S_6) considering $I_j = I_k$, and $-0.6435 < \phi < 0.6435$ rd.

stressed. It should be noted that the *abn*-converter exhibits smaller stressed regions compared to the other converters.

Following the Brazilian Regulatory Energy Agency (ANEEL), responsible for standardizing all electricity consumption, the power factor value is limited to 0.92 for industrial consumers connected to the grid. These parameters do not apply to isolated systems but provide a good operating standard for loads. Considering that isolated areas typically have loads with a lower power factor (such as electric motors), the analysis focuses on current stress in regions where these loads typically operate. In this study, the angle displacement values between voltage and current representing power factors ranging from 0.8 to 1 (that is, $-0.6435 < \phi < 0.6435$ rd) were examined.

Fig. 9 shows the top view of Fig. 7, considering the angular displacement values corresponding to the angles at which loads operate in isolated systems. It is evident that within this load threshold, the blue region consistently dominates, meaning that for the majority of operating points considered in this analysis, the $\alpha\beta n$-GFC exhibits higher levels of current stress.

III. WEAR-OUT PREDICTION METHOD AND THERMAL MEASUREMENT

The reliability of the components of the power electronics converter is significantly influenced by temperature [20]. To
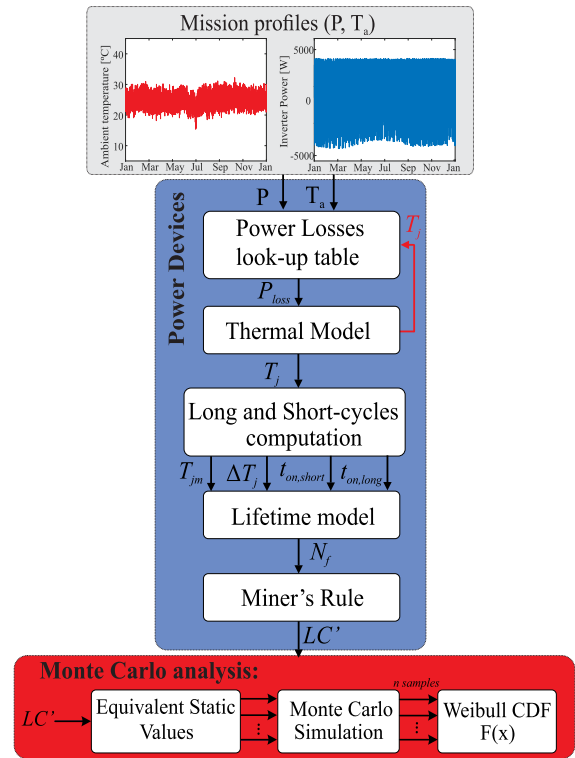

FIGURE 10. Flowchart for the lifetime evaluation of semiconductor power devices.

assess the reliability of the GFC, a one-year mission profile is used, taking into account power and ambient temperature (T_a), following the approach described in Fig. 10 [3]. These profiles are customized for the Amazon region of Brazil, where variations in temperature and irradiation patterns are considered.

Losses in power semiconductor devices are classified into conduction and switching losses, with their estimation relying on lookup tables developed from manufacturer-provided data. The calculation of power losses incorporates considerations of temperature and blocking voltage dependencies [21]. These semiconductor losses are then integrated into a thermal model to determine the junction temperature, following a methodology similar to that described in [22].

For the evaluation of wear-out failure due to bond wire lift-off, the Bayerer model introduced in [23] is employed. Subsequently, a Monte Carlo simulation is used for a statistical analysis of damage values calculated according to the Miner's rule, in the methodology presented in [24]. This simulation allows for variation of parameters within lifetime models and facilitates the observation of junction temperature behavior in different operational scenarios, ultimately yielding a histogram of accumulated damage for each device. The resulting histogram is approximated using a Weibull distribution $u(x)$. Then, the cumulative density function (CDF) or unreliability is computed, given by:

$$F_m(x) = \int_0^x u(x)dx, \qquad (21)$$

TABLE 2. Parameters of the Isolated Power GFC

PLECS	
Parameter	Value
Converter rated power	4.5 kW
Phase-to-neutral voltage	127 V$_{RMS}$
Line frequency	60 Hz
Switching frequency	12 kHz
DC-link capacitor (C)	5x470 μF
DC-link voltage	390 V
Output filter capacitor (C$_f$)	40 μF
Output filter inductors (L$_{f1}$, L$_{f2}$, L$_{f3}$)	1 mH,
Output filter X/R ratio	20
Damping resistor	4 Ω
Voltage controller	K_i = 123.37,
	K_p = 0.1359,
	K_{res} = 200
Current controller	K_p = 18.541,
	K_{res} = 2000
Heatsink-to-ambient thermal resistance	0.13 K/W

Experimental setup	
Parameter	Value
DC-link voltage	120 V
Switching frequency	24 kHz
Line frequency	60 Hz
Load inductance	1.2 mH
Load resistance	8 Ω
Output filter capacitor	40 μF

FIGURE 11. Communities load profile: (a) Marabá. (b) Monte Sinai. (c) Pagodão. (d) São Thomé. (e) Três Unidos. (f) Mission profile created using the 5 communities.

where x is the operation time. This unreliability function reflects the failure rates at the component level, with a primary focus on failure mechanisms. To establish system-level unreliability, it is necessary to build a reliability block diagram that incorporates the associations of component-level functions [25]. Several methodologies are available in the literature, including part-count models, combinatorial models, and state-space models. This paper uses the model found in [20]. The part-count model relies on the following assumptions: Any fault that occurs to each of the components or subsystems will cause the overall system to fail; at components level, the failure rates of the same components are assumed equal during useful lifetime; the system is treated as a series structure of all components or subsystems. Finally, the system-level lifetime of the GFC is approximated as follows:

$$F_{sys}(x) = 1 - \prod_{m=1}^{H}(1 - F_m(x)) \tag{22}$$

where H is the number of components (only power devices in this paper) in the converter. The wear out is typically used to quantify lifetime consumption and is based on a well-validated methodology in the literature [26], [27].

Table 2 shows the parameters used in the PLECS simulations for lifetime evaluation to extract module loss information. Infineon's module has been chosen for the simulations and experiment test bench, FP25R12KE3 module.

The power load profile is created considering five Brazilian riverside communities in Amazon Region (Marabá, Monte Sinai, Pagodão, São Tomé, and Três Unidos) found in [28]. Fig. 11(a)–(e) shows the five load profiles for each community. These power profiles were used to create a standard profile for a riverside community. Each community is considered as a day of consumption in a generic riverside community, where the peak consumption is 5 kW. The final result is shown in Fig. 11(f). This 5-day pattern is repeated to obtain a one-year mission profile with a 10-minute sampling rate, shown in Fig. 12(a).

One-year PV generation mission profile is created using data collected in [29], shown in Fig. 12(b). Global horizontal irradiance and temperature data in the Brazilian Amazon (2°58'48.0"S 64°52'12.0"W) are considered in this work. The power mission profile (P_{inv}) shown in Fig. 12(c) and used in the grid-forming 2Φ3 W converter is the difference between load (P_{load}) and PV generation (P_{pv}). The grid-forming mission profile presents only active power.

The experimental results are obtained by means of a 2Φ3 W GFC prototype, described in Table 2. The converter assembly allows access to the semiconductor module for thermal images, as shown in Fig. 13(a). The silica gel layer was removed from the power module and the module was painted in black to improve measurement accuracy. The FLIR i60 thermal camera captured the thermal images. Because of the alteration of the dielectric properties caused by removing the gel layer, precautionary action was taken during the tests. The maximum voltage applied to the DC bus was limited to 150 V for safety reasons. Furthermore, the value of the switching frequency was twice that of the simulation to achieve higher thermal stress at lower power levels.
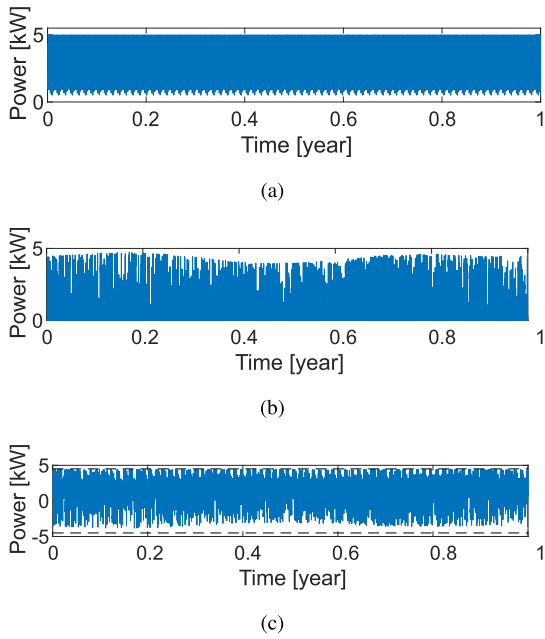
FIGURE 12. Power profiles: (a) One year load of a riverside community. (b) One year PV plant generation. (c) One year 2Φ3 W GFC power.
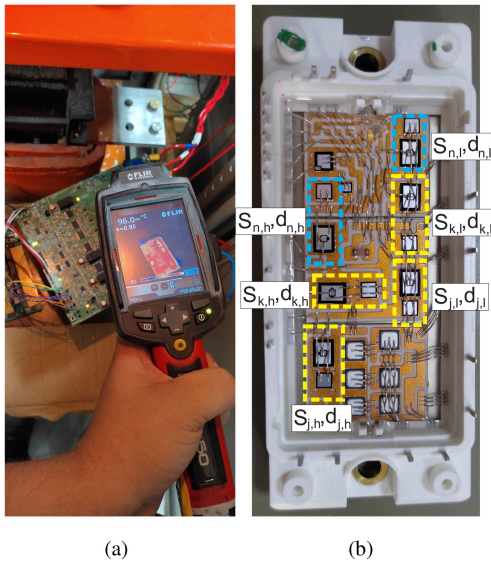

FIGURE 13. (a) Thermal measurement of the prototype semiconductors. (b) Top view of the open semiconductor module FP25R12KE3 by Infineon. In yellow are highlighted the phase semiconductors and in blue the neutral semiconductors.

The position of the IGBTs and diodes is shown in Fig. 13(b). The subscripts j, k, and n refer to the phase of the converter, and the subscript h refers to the high-side semiconductors (positioned on the right side of the image) and l stands for the low-side semiconductors (positioned on the left side of the image).

A cascade control is employed for the isolated grid-forming inverter in this study, as illustrated in Fig. 14. The outer loop
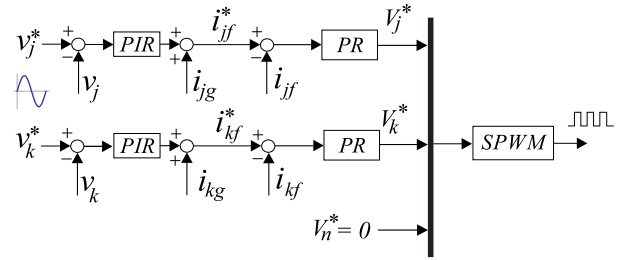
FIGURE 14. Control of the isolated 2Φ3 W grid-forming converter.
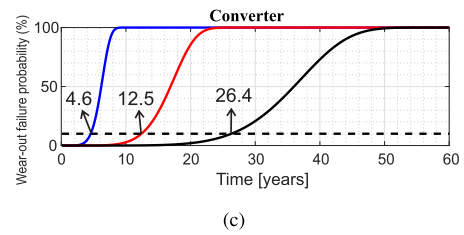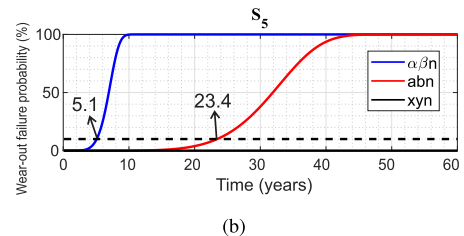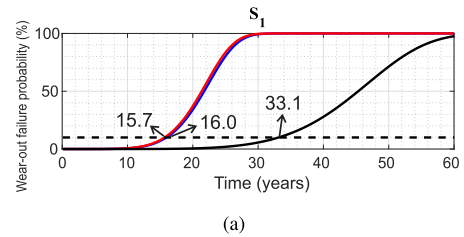
FIGURE 15. (a) IGBT S_1 unreliability function. (b) IGBT S_5 unreliability function. (c) Overall converter level unreliability function considering all semiconductors.

regulates the line voltage through a resonant proportional-integral controller. The inner control loop is based on a resonant proportional controller. The reference voltage is sent to a PWM modulator [30]. The current control loop is tuned using the methodology described in [31]. The discretization of resonant controllers is based on the Tustin method. The voltage control loop is tuned using the pole placement method, with a phase margin and crossover frequency of 54.4° and 532 Hz. The controller gains are shown in Table 2.

IV. SIMULATION AND EXPERIMENTAL RESULTS
A. UNRELIABILITY RESULTS
In Section II, it is noted that the xyn-GFC has the lowest current stress in most cases among the converters presented in this paper. Fig. 15(a) shows the unreliability function for the IGBT S_1 of the GFC. The value in B_{10}, which indicates the time when 10% of the samples have failed, is similar for

the *abn*-GFC and $\alpha\beta n$-GFC. However, the *xyn*-GFC reaches the B_{10} in 33.1 years, showing higher reliability. Fig. 15(b) shows the unreliability function for the IGBT S_5 of the GFC. The $\alpha\beta n$-GFC shows the highest thermal stress in the neutral leg, resulting in a low unreliability value in B_{10} for the IGBT S_5 (5.1 years). For these results, the converter under balanced load is considered, in which the current through the neutral leg of the *xyn*-GFC is zero. Thus, the only loss in this IGBT is the switching one, which statistically implies a low probability of failure, with its value at B_{10} estimated at 3500 years.

The unreliability of the system considering all IGBTs and diodes for the three converters studied in this paper is shown in Fig. 15(c). The *xyn*-GFC has the highest reliability, with a B_{10} value of 26.4 years. As expected, the $\alpha\beta n$-GFC exhibits a highest probability of failure due to the more significant thermal stress imposed on the semiconductors (4.6 years). The *xyn*-GFC presents 111.2% higher value in B_{10} than the *abn*-GFC, and 473.9% higher value in B_{10} compared to the $\alpha\beta n$-GFC.

B. THERMAL RESULTS

1) BALANCED LOAD CONDITIONS

The converter running under balanced load is considered in the first test, and a long-term test is conducted to allow the converter to reach steady-state temperature. The results display thermal images of the converter with flowing 585 W of output power. For each case, the converter had been in operation for one hour before capturing the images.

Fig. 16 shows the module semiconductors thermal images for the $\alpha\beta n$, *abn*, and *xyn* converters. Fig. 16(a) shows the temperature for the $\alpha\beta n$-GFC. Note that neutral IGBTs and diodes experience higher stress levels than phase ones, resulting in higher temperatures reaching 115 °C. The semiconductor temperature for the *abn*-converter is shown in Fig. 16(b). Generally, the module temperature is lower than observed in the $\alpha\beta n$-GFC. Furthermore, it seems that the IGBTs exhibit similar temperatures since the current passing through the phase and the neutral components are equal.

The *xyn*-GFC shows the lowest thermal stress, as seen in Fig. 16(c). The module temperature difference is barely discernible on the temperature scale used for the other two converters. Fig. 16(d) shows the temperature on different scales for visualization. The temperature of the neutral IGBTs is significantly lower, and they do not exhibit hotspots like phase semiconductors. In particular, all semiconductors are mounted on the same heatsink, implying that the thermal impedance remains consistent throughout the power semiconductor module. However, even under identical operational conditions, different temperatures are observed for the phase semiconductors and, consequently, different unreliability values. Also, the current flowing through the neutral leg contributes to vary in the temperatures of the adjacent semiconductors.

Fig. 17 shows histograms of the temperature distribution across pixels in Fig. 16(a), (b), and (d). The images are
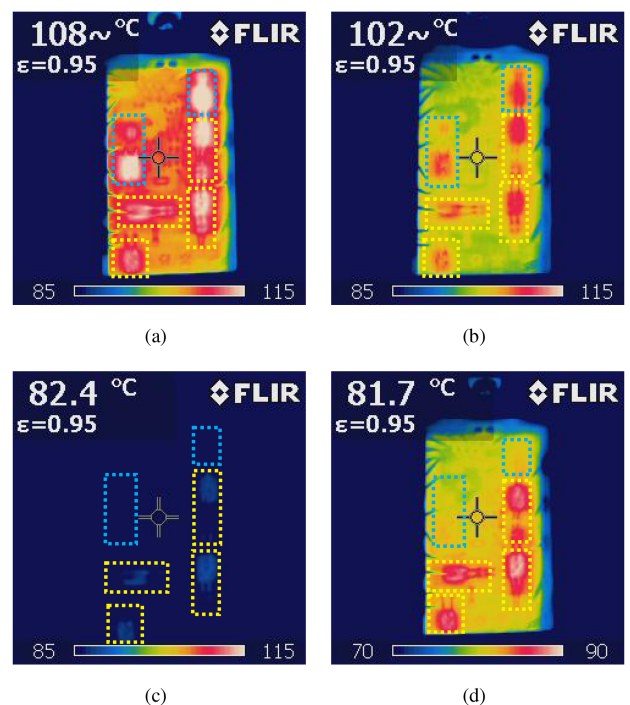

FIGURE 16. Thermal images of the semiconductors of the GFC operating on: (a) $\alpha\beta n$-GFC; (b) *abn*-GFC; (c) *xyn*-GFC; (d) *xyn*-GFC with different temperature scale.
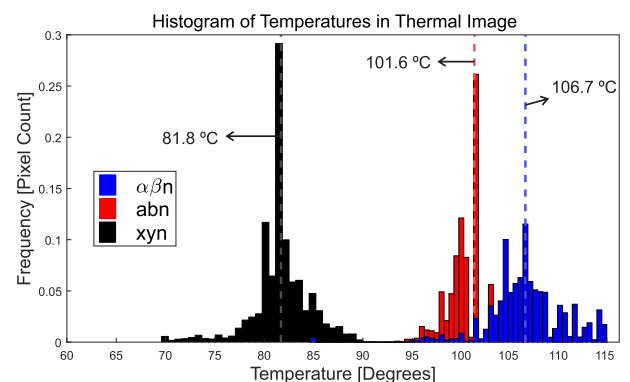

FIGURE 17. Histogram of temperatures in thermal images for balanced load conditions.

cropped to focus on the interior of the semiconductor module. The *xyn*-GFC has the lowest average temperature at 81.8 °C. This makes the *xyn*-GFC average temperature 19.4% cooler than the *abn*-GFC and 23.3% cooler than the $\alpha\beta n$-GFC.

2) UNBALANCED LOAD CONDITIONS

The test comprises operating the converter for one hour until it reaches steady state with 500 W of output power evenly distributed between the two phases. Once steady state is achieved, a load unbalance is introduced in which one phase carries 250 W of power while the other carries 75 W. The same test is conducted for the three converters. The converter runs in an open-loop control configuration, meaning that the decrease
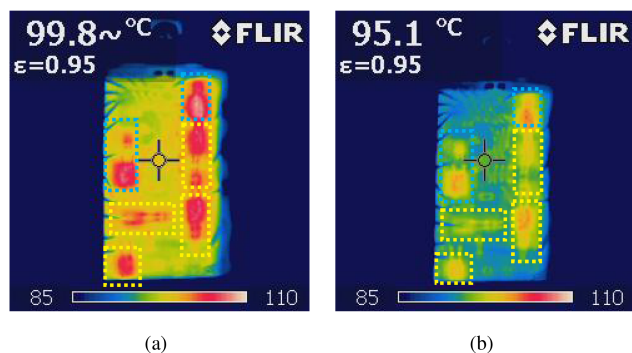
FIGURE 18. $\alpha\beta n$-converter operating under: (a) balanced load conditions, flowing 250 W in each phase; (b) unbalanced load conditions, flowing 250 W in phase *j* and 75 W in phase *k*.
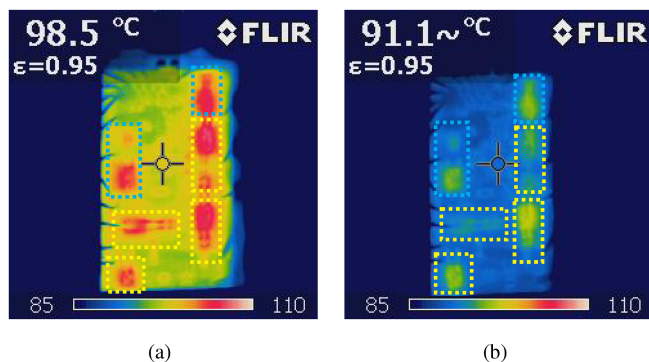

FIGURE 20. *xyn*-converter operating under: (a) balanced load conditions, flowing 250 W in each phase; (b) unbalanced load conditions, flowing 250 W in phase *j* and 75 W in phase *k*.

FIGURE 19. *abn*-converter operating under: (a) balanced load conditions, flowing 250 W in each phase; (b) unbalanced load conditions, flowing 250 W in phase *j* and 75 W in phase *k*.

when operating as $\alpha\beta n$-GFC while consistently exhibits lower temperatures when operating as *xyn*-GFC.

V. SUMMARY OF WEAR-OUT ANALYSIS OF A GRID-FORMING 2Φ3 W CONVERTER

Regardless of the electrical power system used, the reliability of power converters in an isolated ac power grid is a key issue. Depending on the geographical location of the system, maintenance costs become considerably high. In such circumstances, the design of reliability and condition monitoring is a key concept to reduce maintenance and replacement costs in isolated remote grids.

Table 3 shows a comparison of several papers in the literature, evaluating the type of grid configuration, the type of result in the paper (simulations, hardware-in-the-loop, experimental results), if there is any analytical analysis of semiconductors current stress, and if there is any reliability evaluation method. The proposed work addresses an existing gap in 2Φ3 W systems, as they currently lack a more detailed analysis of reliability studies for the converters, in addition to proposing equations to measure current stress under unbalanced load conditions, which has not yet been presented in the literature. To elucidate this issue, the authors proposed a semiconductor current stress evaluation for 2Φ3 W converters comparing the RMS current for three 2Φ3 W grid-forming converters: $\alpha\beta n$-GFC, *abn*-GFC, and *xyn*-GFC.

Considering the current amplitude unbalance, the proposed equations show that the $\alpha\beta n$-GFC is always the most stressed, regardless of the unbalance between phase currents. The *xyn*-GFC always shows lower stress regardless of the unbalance. Taking into account the effect of different angular displacements between current and voltage in the phases, the $\alpha\beta n$-GFC and *xyn*-GFC have more operating points where they are more stressed.

The reliability results demonstrate that the behavior of the neutral current greatly influences the converter lifespan. Under balanced conditions, the *xyn*-GFC exhibits a null neutral current, significantly reducing the thermal stress of the converter and increasing its reliability. The thermal results indicate that the *xyn*-GFC shows better thermal performance than the $\alpha\beta n$-GFC and *abn*-GFC, regardless of whether they

in current in one phase leads to a lower line-to-neutral voltage than in the other phase.

Fig. 18 shows the thermal images for the $\alpha\beta n$-converter operating under load balanced and unbalanced conditions. As Fig. 5 illustrates, regardless of the unbalance, the neutral current in the converter is greater than the phase current. The module temperature is lower because the converter processes less power. However, it is still noticeable that the temperature in the neutral semiconductors is higher than that in the unbalanced phase semiconductors.

The thermal images for the *abn*-converter operating under balanced and unbalanced loads conditions are shown in Fig. 19. Fig. 5 shows that for a value σ of 0.5, the RMS current through the switch S_5 is higher than through the switch S_3. Additionally, Fig. 19(b) shows that the temperature through the neutral IGBTs is slightly higher than the unbalanced phase IGBTs. In the case of the *abn*-GFC, for values σ below 0.674, the RMS current through the neutral IGBTs is higher, resulting in increased power losses and, consequently, higher temperatures in the neutral IGBTs.

Finally, Fig. 20 shows the thermal images for the *xyn*-converter operating under balanced and unbalanced loads conditions. Note that the introduction of the unbalance leads to current flow through the neutral leg, resulting in a temperature hotspot in the neutral semiconductors. Irrespective of the unbalance, the converter shows higher thermal stress
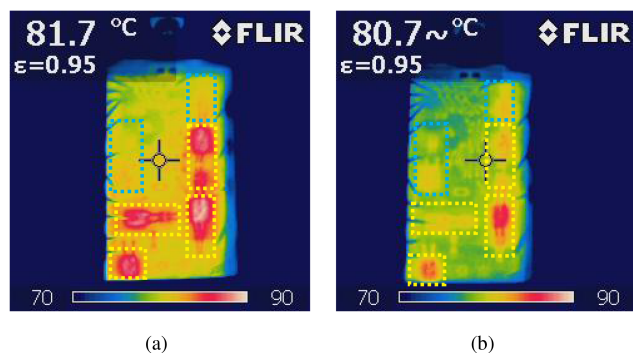
TABLE 3. Comparison of Correlate Papers in Literature: Grid Configuration, Result Types, Analytical Current Stress and Reliability Method

Reference	Grid configuration	Isolated system	Results	Analytical current stress	Reliability
[4]	*abn* 2Φ3W	No	Simulations	No	No
[5]	*abn* 2Φ3W	No	Simulations	No	No
[6]	*abn* 2Φ3W	No	Hardware-in-the-loop	No	No
[7]	*abn* 2Φ3W	No	Simulations	No	No
[8]	*abn* 2Φ3W	No	Simulations	No	No
[10]	$\alpha\beta n$ 2Φ3W	No	Simulations	No	No
[11]	dc grid	No	Simulations, Experiment	No	*Mission-profile based*
[12]	Three-phase	No	Simulations, Experiment	No	*Mission-profile based*
[13]	Single-phase	No	Simulations	No	*Mission-profile based*
This paper	$\alpha\beta n$, *abn* and *xyn* **2Φ3W**	**Yes**	**Simulations, Experiment**	**Yes**	***Mission-profile based***

operate under balanced or unbalanced load conditions. These findings highlight the superior thermal and reliability performance of the *xyn*-GFC in 2Φ3 W grids.

VI. CONCLUSION

This paper proposed general analytical expressions to evaluate current stresses in the grid-forming converter operating in three different configurations in terms of line voltage displacement angles (i.e., 90°, 120° and 180°). It also compares the wear-out prediction of the IGBTs and performs tests to show the thermal behavior of semiconductors.

In terms of lifetime, the *xyn*-GFC demonstrates superior results by exhibiting the highest reliability compared to the other two converters. Specifically, when considering IGBTs and diodes, the *xyn*-GFC achieves a value of B_{10} of 26.4 years. The *xyn*-GFC presents 111.2% higher value in B_{10} than the *abn*-GFC, and 473.9% higher value in B_{10} compared to the $\alpha\beta n$-GFC.

Thermal images demonstrated that the *xyn*-converter experiences lower thermal stress. Regardless of whether the converter supplies balanced or unbalanced loads, the temperatures recorded in the *xyn*-GFC are consistently lower compared to the other converters when considering the same power level. Conversely, $\alpha\beta n$-GFC exhibits greater thermal stress in all cases, indicating higher temperatures. Under balanced load conditions, the *xyn* converter shows 19.4% lower average temperature than *abn*-converter, and 23.3% lower average temperature than $\alpha\beta n$ converter. The results validate the proposed analytical expressions.

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