IEEE Open Journal of
Power Electronics

Received 8 January 2024; revised 19 February 2024; accepted 13 March 2024. Date of publication 19 March 2024;
date of current version 16 April 2024. The review of this article was arranged by Associate Editor Xiong Du.

Digital Object Identifier 10.1109/OJPEL.2024.3379294

A Comprehensive Overview of Reliability Assessment Strategies and Testing of Power Electronics Converters

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This work was supported in part by HiEFFICIENT Project, in part by ECSEL Joint Undertaking (JU) under Grant 101007281 through European Union's Horizon 2020 Research and Innovation Programme and Austria, Germany, Slovenia, The Netherlands, Belgium, Slovakia, France, Italy, and Türkiye.

ABSTRACT Power electronics converters (PECs) are responsible for efficiently converting electrical energy between power generators, storage systems and power consumers/loads. The PECs are subjected to complicated power loading factors throughout their operations and, thus, are proven to have issues regarding lifetime. Therefore, according to the original equipment manufacturers and suppliers, the reliability of the PECs is a key priority in order to be widely used and accepted in the industries. In this context, this review article aims to provide a comprehensive overview of reliability assessment strategies and testing protocols for ensuring the lifetime requirements of PECs. In addition, the paper conducts a thorough investigation of various strategies that are employed to enhance reliability during the design and useful life phase, including the analysis of different types of failure mechanisms, identification of factors contributing to failures, and assessment of techniques for estimating and regulating junction temperatures to prolong the lifetime of the system under real-life operating conditions. Furthermore, the article highlights the challenges encountered in monitoring and predicting component degradation and outlines the crucial steps for conducting a functional safety analysis. Particular emphasis is provided on summarizing the different accelerated aging tests for power electronics converters used in automotive applications, as these tests have yet to be fully covered in previous literature. This study provides an overview and guidelines for understanding the reliability of PECs and identifying potential areas for future research. Finally, the paper concludes most of the ongoing research and innovations in this area and provides insights into the future trends and challenges in enhancing the reliability of power electronics converters.

INDEX TERMS Power electronics converters, prognosis, reliability, condition monitoring, temperature-sensitive electrical parameter (TSEP), remaining useful lifetime (RUL), functional safety (FuSa) and lifetime models.

I. INTRODUCTION

Nowadays, the incredible growth in the use of IT systems, renewable energy generation, electrical vehicles (EVs) and aerospace applications has resulted in employing more and more power electronics converters (PECs) [1]. PECs are commonly used in various applications to effectively transfer electrical energy between sources, storage systems, and users. In order to be widely adopted and utilized in competitive markets, PECs must demonstrate high efficiency and reliability and adhere to established standards. As multiple industries rely on PECs to create energy-efficient interfaces, the reliability of these converters is a critical factor in developing new interfaces and improving existing ones [2].

Moreover, the increasing use of PECs in specific applications and scenarios, such as continuous power delivery, low-frequency maintenance (e.g., offshore wind turbines), and applications with high safety requirements (e.g., aerospace), has brought attention to the reliability challenges faced by these converters. Many PECs do not have redundant systems in place, so any fault in a device, component, or subsystem can cause the entire system to fail, leading to safety issues and higher operation and maintenance costs [3].

In order to enhance the reliability of PECs in these applications, it is necessary to adopt practical approaches during the design stage, manufacturing process, and real-world operation. This requires researchers to understand state-of-the-art design techniques thoroughly, identify failure mechanisms and indicators, comprehend the operating environment, including mission profiles, and implement innovative methods for increasing the lifetime of PECs [3], [4]. Ref. [5], [6] provide a thorough examination of failure mechanisms, causes, failure sites, and stress variables. Furthermore, ref. [3], [5], [7], [8], [9] offer a comprehensive introduction to various lifetime estimation methods, encompassing both physics-based and empirical approaches. These methodologies are employed to calculate the ultimate end of life during the design stage. Additionally, other models referred to as data-driven models, have been introduced in [10], [11]. These models utilize past data, including real field data and accelerated aging tests, to predict reliability, rather than relying solely on physical properties and formulas.

Furthermore, in real-world operation, there is still a chance to improve the lifetime of PECs through techniques such as manipulating output load, cooling system effort, and PWM pattern, which can be classified as an active thermal management method. However, these approaches have their advantages and disadvantages that must be carefully considered, and their selection should take into account the specific application and other factors such as efficiency and cost [12], [13].

Additionally, it is crucial to incorporate accelerated aging tests into reliability checklists. These tests offer valuable insights into the system- and device-level parameter changes and weaknesses throughout the aging process. Conducting accelerated aging tests is essential for gathering data to prepare both data-driven models and physics-based models, as well as for conducting advanced failure mechanism analyses during the design stage [14], [15]. This information can then be utilized to identify key signals indicating impending failures. Additionally, it can aid in the development of appropriate sensor technology and techniques aimed at enhancing the health of PECs through condition monitoring programs [15], [16], [17], [18]. In a condition monitoring program, specific electrical and mechanical signals are continuously monitored and compared with a health baseline to estimate the health status of PECs. Besides, in ref. [3], prognostics and health management approaches are discussed. These methods provide further insight into predicting and managing potential failures in PECs, complementing the condition monitoring efforts. In the event of an emergency detected through condition monitoring, such as a significant deviation from the health baseline, active thermal control methods or other strategies may be implemented to improve the health status.

To focus more specifically on reliability analysis for specific semiconductor devices, ref. [9], [19], [20] have concentrated on assessing the reliability of insulated gate bipolar transistors (IGBTs). These studies delve into various aspects such as failure mechanisms, failure precursors, accelerated aging tests, and analytic cumulative degradation models developed for IGBT models. Conversely, in articles [4], [8], the emphasis lies on reviewing aging mechanisms and accelerated aging tests specifically intended for SiC-based applications which provide detailed information on the reliability challenges associated with SiC MOSFET. In ref. [21], an overview of the failure mechanism in GaN HEMTs has been presented.

Furthermore, in addition to semiconductors, capacitors play considerably essential roles in improving the reliability of PECs which are responsible for 19% of failures [22]. In ref. [23], failure modes, failure mechanisms, and lifetime models of Aluminum Electrolytic Capacitors, Metallized Polypropylene Film Capacitors, and high capacitance Multi-Layer Ceramic Capacitors are discussed.

Despite the aforementioned efforts, a comprehensive review paper to assess reliability strategies, encompassing both offline and online methods, is needed to be covered. In addition, according to the best search of authors, a detailed list of required reliability tests for wideband gap-based semiconductors (e.g., SiC and GaN) is still missing in the existing literature. Therefore, this paper aims to narrow this research gap as follows. This paper presents the failure mechanisms of chips and packages at the device level in Section II, reviews prognostics frameworks and models for estimating the lifetime of PECs in Section III, and presents approaches and definitions for assessing the reliability of PECs during the design phase in offline mode in Section IV. A detailed use case for assessing the lifetime of a PEC in an automotive application is also provided. Section V provides a comprehensive analysis of control methods that could enhance the longevity of power electronics components and systems during operational scenarios, including a thorough investigation of using junction temperature and temperature-sensitive electrical signals as inputs. Additionally, an accurate junction temperature measurement technique in a real application is also presented. Furthermore, functional safety is thoroughly analyzed to identify potential faults or malfunctions of the PEC and its components throughout its operational lifetime. Section VI describes methods and test setups for conducting power cycling tests, while Section VII describes detailed testing requirements, conditions, and methods for reliability testing of SiC and GaN devices. Finally, Section VIII discusses emerging trends in PEC reliability and offers guidance for future lifetime-related research activities. Fig. 1 provides an overview of the topics covered in this review paper.

FIGURE 1. General overview and interconnection of covered reliability-related topics in this paper.

II. FAILURE MECHANISMS OF POWER ELECTRONICS DEVICES

With the proliferation of power electronics devices in a wide range of applications, it is critical to identify the root causes of failure to ensure optimal performance and longevity. Power electronics device failures can arise from various mechanisms, including thermal, mechanical, electrical, and environmental stresses, and require comprehensive investigation to determine the underlying factors and develop appropriate mitigation strategies. According to previous research on reliability, there are two types of failures in semiconductor power modules: "chip-level failures" and "package-level failures," both of which are caused by electrical overstress, repetitive thermomechanical loading, and wear-out mechanisms [5], [24]. The wear-out mechanism in semiconductor power modules leads to the degradation of the chip and package over time, which is manifested in changes in characteristics such as thermal impedance, leakage current, vibration, and noise level. In Section V, the parameters referred to as failure precursors or failure identifiers will be clarified. This section will present a detailed analysis of failures occurring at the chip/package level in semiconductors based on Si and SiC.

A. CHIP-LEVEL FAILURE MECHANISMS

There are several categories of mechanisms that can cause degradation at the chip level. These types of degradation occur as a result of the chip being subjected to electrical and thermal stress during operation, as well as other factors such as electrostatic discharge, lightning surge, and external radiation (e.g., radiation in avionic applications). These phenomena can all contribute to the acceleration of the chip degradation process [25], [26]. In the following sections, various mechanisms that can lead to chip failures are investigated.

1) GATE OXIDE

A notable area of concern for chip-level failures in semiconductor devices, especially in SiC MOSFETs, is linked to the reliability of the gate oxide structure. This vulnerability

is attributable to various degradation mechanisms, including Time-Dependent Dielectric Breakdown (TDDB), Hot Carrier Injection (HCI), and Bias Temperature Instability (BTI) [27]. When a MOSFET is continuously subjected to electrical or thermal stress, electrons can become trapped in the gate oxide layer and build up over time. The gate oxide is the dielectric layer between the gate terminal and drain and source terminals in MOSFETs [28], [29]. The accumulation of electrons trapped in the gate oxide layer can lead to the formation of a conduction path through the dielectric from the gate to the adjacent substrate, resulting in a gradual reduction in the thickness of the gate oxide layer. Eventually, the oxide will fail, leading to a breakdown of the MOSFET. This process is referred to as TDDB. The time-dependent breakdown can manifest as an increase in gate leakage current, a shift in gate threshold voltage, and a decrease in drain current [30], [31]. This type of failure has also been observed in IGBTs [9]. Hot carriers are generated by electrical stress. When a strong electrical field is applied, holes or electrons may acquire sufficient kinetic energy to overcome the barrier and inject into the substrate layers and gate oxide layer, initiating the degradation process in the semiconductor [29], [32]. This failure mechanism is thought to be the primary cause of TDDB [11]. Similar to the two aforementioned degradation mechanisms, BTI is initiated by the trapping of carriers in the gate-oxide layer, resulting in parameter shifts. Unlike immediate failures, BTI may not lead to instantaneous breakdown but contributes to a gradual decline in device performance over time.

2) LATCH-UP

Latch-up can occur when a high $\frac{dv}{dt}$ is applied to the switch during the turn-OFF transition [38], [39], [40]. This failure mechanism can affect both IGBTs and MOSFETs, as it involves the activation of parasitic bipolar junction transistors (BJTs) in MOSFETs and thyristors in IGBTs, which results in a loss of control over the drain/collector current via the gate voltage [41].

3) METAL MIGRATION

This failure mechanism is caused by high current density and the formation of metal voids, which increases interconnect resistance. While this mechanism has not been observed in power semiconductors because of their large size, it has been observed in Schottky diodes and microprocessors that require high current densities [42], [43], [44].

B. PACKAGE-LEVEL FAILURE MECHANISMS

Package-related failures often result from mismatches in the thermal properties of different adjacent substrates in power modules, which can impact the cooling and heating rates of the module. A coefficient of thermal expansion (CTE) is the rate at which the size of a material changes with respect to temperature change. Size considerations can be made by changes in length, area or volume, and therefore, there are coefficients derivable for linear, area and volume expansions.

When the modules are subjected to repetitive thermomechanical stress, cracks may develop due to the presence of different CTE and resulting shear stress along the contact area. The severity of this failure is highly dependent on the packaging technology used. Bond wire and solder fatigue are primary failure mechanisms associated with package degradation [45], [46], [47]. Fig. 2 illustrates the internal structure of a SiC power module, as well as common failure mechanisms. According to the power cycling tests in [48], on over 40 IGBT modules of 400A/1200V, bond wire failure accounts for nearly 70% of total failures. Additionally, a survey on failure analysis studies conducted between 1993 and 2014, covering 70 publications [49], indicates that die attachment is the primary concern in 30% of cases, followed by wire bonds at 28%. However, failures at the chip level are less than 5%, suggesting they are less critical. Therefore, more attention should be given to die attachment and wire bond failure. It's worth noting that this data applies to Si MOSFETs and IGBTs, as reliable sources for SiC MOSFETs are currently unavailable.

1) BOND WIRE FATIGUE

Bond wire fatigue can be classified into three types: bond wire lift-off, bond wire heel-crack, and bond wire-body damage [22], [50]. Bond wire lift-off failure is typically caused by the mismatch in CTE and strain between bond wires (typically made of aluminum) and the die (made of silicon), which leads to shear stress [51], [52]. This stress can cause a crack to form at the edge of the interconnection and propagate towards the center, reducing the contact area and increasing the electric resistance. The increase in resistance leads to an increase in conduction losses, which in turn exacerbates the growth of the crack in the bond wire [13], [53]. Ultimately, the bond wire may lift off and the semiconductor will cease to function. Bond wire heel-crack and body damage failures, on the other hand, occur when cracks form at the bond wire heel and body due to repeated flexure during temperature cycling [54].

2) SOLDER FATIGUE

Solder fatigue is characterized by the formation of cracks and voids in the solder interconnection between layers. In power module semiconductors, the solder layers are typically found between the die, baseplate, and insulating layer known as direct bonded copper (DBC). As previously mentioned, the different CTE between adjacent layers can lead to the formation of shear stress. The resulting cracks and voids can impede proper heat dissipation between the die and baseplate, increasing thermal impedance [55], [56], [57]. Thermal impedance increases as the chip solder degrades within the package, leading to hotspots on the die and elevated temperatures [58]. It is noteworthy to say that while solder fatigue initiates the degradation process of the semiconductor, bond wire damage is typically the primary cause of failure in the device.

To explore further into the fatigue failure of wire bonds and solder, Paris' law is commonly employed to calculate

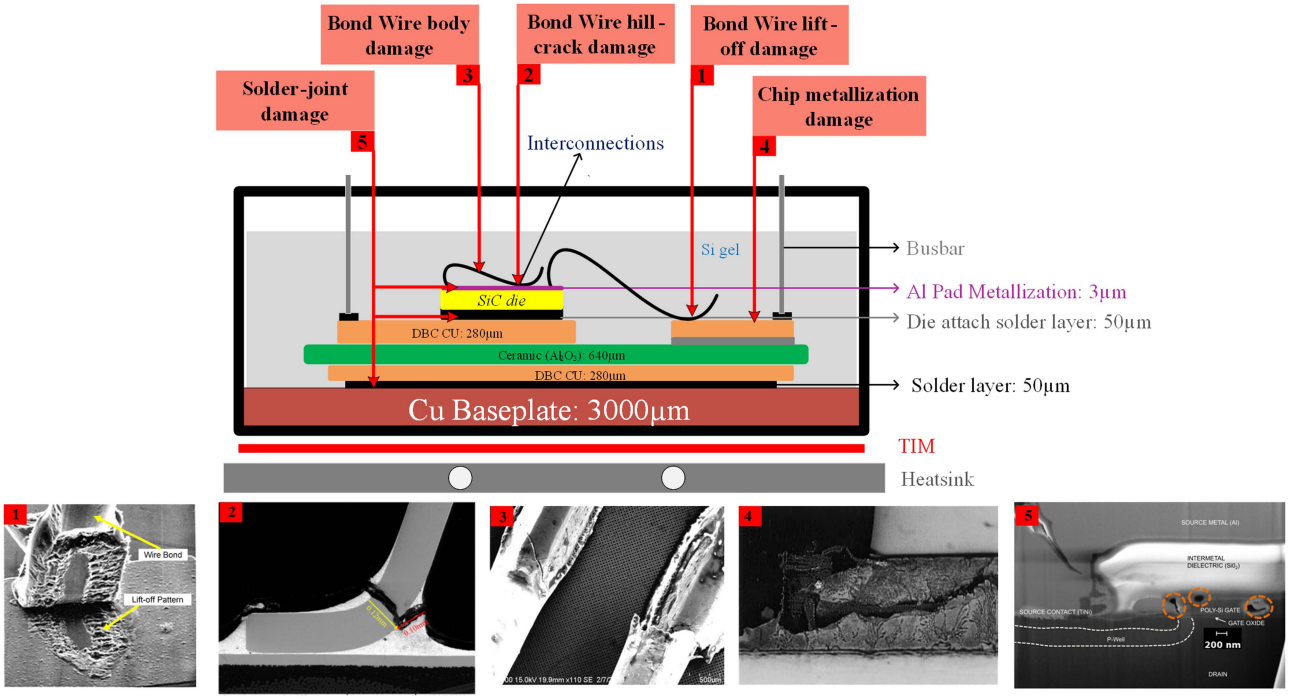

FIGURE 2. Multilayer structure of power module, here scanning electron microscopy (SEM) images of the following failure mechanisms are illustrated: (1) bond wire lift-off damage [33], (2) bond wire heel-crack damage [34], (3) bond wire body damage [35] , (4) solder-joint damage [36], (5) gate oxide degradation [37]. The potential failure sites in the SiC MOSFET power modules are shown through the red arrow.

the growth of degradation, represented as (dA) per cycle (dN), or the crack growth rate, utilizing the plastic strain deformation-induced per cycle ($\Delta\varepsilon_{pl}$) as a damage indicator. This relationship is shown in (1), where C_1 and C_2 are material constants [59].

$$\frac{dA}{dN} = C_1\left(\Delta\varepsilon_{pl}\right)^{-C_2} \tag{1}$$

Equation (1) highlights that as plastic strain increases, the crack growth rate also increases, resulting in a shorter lifetime. Additionally, solder and wire bond interconnectors experience temperature fluctuations due to harsh external environments. Moreover, thermomechanical stresses typically emerge from mismatched CTE between layers. The resulting thermal stress and equivalent strain can also be expressed as a function of temperature swing (ΔT), as depicted in (2) [50].

$$N_f = C_3(\Delta T)^{-C_4} \tag{2}$$

III. LIFETIME ASSESSMENT APPROACHES

With the increasing complexity of products and the need for enhanced performance and efficiency, lifetime assessment approaches are becoming increasingly crucial for original equipment manufacturers and suppliers seeking to develop highly efficient and long-lasting products. Lifetime assessment approaches provide a systematic means of identifying potential failure mechanisms and assessing the reliability of products over their expected lifetime. Prognostic approaches are a type of lifetime assessment approach, as they aim to estimate the remaining useful life of a product and/or system through the analysis of various forms of data and modeling techniques. These approaches are particularly useful for providing early warning of potential failures and/or degradation in both the design stage and real-field operations and informing decisions about maintenance, repair or replacement. Although prognosis approaches employ different methodologies than other lifetime assessment approaches, they share a common objective of maximizing the reliability and performance of products over their expected useful lifetime. It is important to note that prognosis differs from diagnosis. Diagnosis involves identifying the current health status of the device under test (DUT) and determining the nature, progression, and severity of any faults. In contrast, prognosis involves assessing and predicting the health status and remaining useful lifetime (RUL) of the DUT. The prognosis also aims to identify any undesirable performance and predict any potential future failures as early as possible. This approach can generally be divided into four categories, which are discussed in this section.

A. CANARY APPROACH

Historically, miners would keep canaries in mines as an early warning system for hazardous gases, as the birds are sensitive to these gases and would die in their presence. Similarly, a canary device or prognostic cell in electronic circuits is subjected to the same operating conditions as the target electronic device. While the canary device degrades through the same mechanisms as the target device, it will fail before the target device and can therefore predict its failure earlier [60]. In a

study published in [61], a canary method was introduced to detect solder interconnect failures. The prognostic cell comprises a resistance path which is formed by a near-zero ohm ceramic chip resistor soldered to the pad to fail earlier than the target device which is the standard pad resistor. The temperature cycling test was performed to examine the canary method. 16 standard resistors with a standard pad width and 24 canary resistors with a pad width of around 20% of the one for standard resistor were soldered to test board. The results showed a 78% increase in the strain range in the canary resistors in comparison with the standard resistors. Furthermore, in [62], the authors proposed a circuit for monitoring the TDDB of an integrated circuit (IC) that could provide an early warning of failure. The prognostic cell included a feedback loop that would remove power from the stressing circuit when the prognostic cell triggered. This help to prevent further current drain and rising power dissipation in the event of oxide failure.

B. PHYSICS-BASED APPROACH

This method relies heavily on a thorough understanding of the performance and behavior of physical systems under real-field loading conditions. It can generally be divided into two models: the Physics of Failure (PoF)-based model and the Empirical-based model. The PoF-based method utilizes life cycle loading information, geometry, material properties, failure mechanisms, and failure modes of power electronic (PE) devices to implement prognostics and assess reliability [61], [72]. Basically, the PoF model is based on the mathematical analysis of semiconductors, which can also be done using Finite Element Method (FEM) software. On the other hand, the empirical model is based on parameters and variables related to the experiments and is developed by statistical analysis, curve fitting, and studying data gathered from accelerated lifetime tests. It is important to note that the empirical model is only valid for load conditions similar to the experiment conditions from which data was gathered to develop the empirical model [5].

Table 1 presents physics-based models for estimating the lifetime of semiconductor materials, focusing on degradation in bond wire and solder joints. These models were developed for Si-based semiconductors, but they are also used for SiC semiconductors [8]. To improve the accuracy of predicting the lifetime of SiC semiconductors, it would be beneficial to create models that specifically consider the dominant failure mechanisms in these materials. One such failure mechanism is gate oxide degradation [16].

In addition to fatigue, various factors can contribute to degradation in semiconductor materials, such as corrosion, creep, fouling, and time-dependent dielectric breakdown [73]. To analyze different types of degradation processes in semiconductors, various modeling approaches have been developed. For instance, the Howard model is used to study corrosion, the Black model is used to analyze Electromigration, the Rudra model is used to investigate Stress driven diffusion voiding, the E and $\frac{1}{E}$ models are employed to study TDDB and the Okabayashi model is used to examine stress-driven diffusion voiding [74], [75].

In the context of cycling fatigue models, the Coffin-Manson model is a relatively simple lifetime model that takes into account the temperature swing at the bond wire. The model is deficient in that it overlooks the mean value of junction temperature and is exclusively applicable to junction temperatures below 120 °C, as described in sources [5], [50], [63], [76].

The plastic strain-based model, derived from the Coffin-Manson model, suggests that bond wire failure is primarily attributed to plastic strain, thereby overlooking the influence of elastic strain. In the lifetime equation for this model, C_1, C_2 are material-dependent parameters and ε_p is the plastic strain [5], [50], [77], [78].

The solder plastic strain lifetime model is specifically designed to estimate failure in solder interconnections, and takes into account the length of the solder interconnect (L), plastic strain (ε_p), and material-dependent parameters a and b [64], [79], [80].

The Coffin-Manson model is suitable for low cycle fatigue, whereas the Basquin lifetime model, as referenced in [65], [81], [82], is applicable to high cycle fatigue. It is utilized for predicting the number of cycles to failure through stress calculations. This model is suitable for low ΔT_j values, and uses stress range ($\Delta\sigma$) as damage metric instead of plastic strain.

The Coffin-Manson-Arrhenius model is an improved version of the Coffin-Manson model and takes into account the mean junction temperature as well as temperature swings between 30 K and 80 K [51], [83]. However, it still lacks crucial parameters such as heating time.

Another model that was derived from the Coffin-Manson model is the Norris-Landzberg model, which also considers the temperature cycling frequency parameters in addition to the parameters considered by the Coffin-Manson model, as described in refs. [5], [24], [66]. This model fails to capture solder joint deformation behavior completely and can consequently result in misleading reliability estimations [84].

The large solder joint model is used to estimate the long-term reliability of solder joints, taking into account several extrinsic factors such as the lateral size of the solder joint (L), the thickness of the solder layer (x), the CTE mismatch between the lower and upper plates ($\Delta\alpha$), the fatigue exponent (c), the ductility factor of the solder (γ), and the temperature swing (ΔT) [63].

Furthermore, in 2008, Bayerer et al. developed a promising lifetime model called CIPS 2008, which takes into account various parameters of power module characteristics and cycling data. The parameters considered by this model are shown in Table 1, including the heating time (t_{on}), junction temperature (T_j), DC current applied per wire (I), bond wire diameter (D), blocking voltage (V), and coefficients K and B, which are calculated based on experiments and statistical data, as described in [68]. However, this model neglects to assign greater importance to low temperature swings, where

TABLE 1. State-of-the-Art Lifetime Models of the Semiconductor

Failure model	Failure position	Equation	Variables	References
Coffin–Manson[1]	*Bond wire*	$N_f = a \times (\Delta T)^{-n}$	ΔT	[63]
Plastic Strain Model[2]	*Bond wire*	$N_f = C_1 \times (\Delta\varepsilon_p)^{-C_2}$	$\Delta\varepsilon_p$	[5], [59]
Plastic Strain Model[3]	*Solder interconnect*	$N_f = \frac{L}{\alpha \times (\Delta\varepsilon_p)^b}$	$\Delta\varepsilon_p$	[64]
Basquin[4]	*Bond wire*	$N_f = C_1 \times (\Delta\sigma)^{-C_2}$	$\Delta\sigma$	[65]
Coffin–Manson–Arrhenius (LESIT)[5]	*Bond wire*	$N_f = a \times (\Delta T_j)^{-n} \times e^{\frac{E_a}{kT_m}}$	ΔT_j, T_m	[51]
Norris–Landzberg[6]	*Solder interconnect*	$N_f = A \times f^{n_2} \times (\Delta T_j)^{-n1} \times e^{\frac{E_a}{kT_m}}$	ΔT_j, T_m, f	[66], [67]
Large Solder Joint[7]	*Solder interconnect*	$N_f = 0.5 \times [(L \times \Delta\alpha \times \Delta T)/(\gamma \times x)]^{\frac{1}{C}}$	ΔT	[63]
Bayerer (CIPS 2008)[8]	*Bond wire*	$N_f = k \times (\Delta T_j)^{B1} \times e^{\frac{B2}{T_{J,max}}} \times t_{on}^{B3} \times I^{B4} \times V^{B5} \times D^{B6}$	ΔT_j $T_{J\,max}$, t_{on}, I, V, D	[68]
Scheuermann[9]	*Bond wire*	$N_f = A \times (\Delta T_j)^{a} \times (a_r)^{B1 \times \Delta T_j + B0} \times [\frac{C + (t_{on})^{\gamma}}{C + 2^{\gamma}}] \times e^{\frac{E_a}{kT_m}} \times f_{diode}$	ΔT_j t_{on} T_m	[69]
SEMIKRON[10] (new version)	*Bond wire*	$N_f = A_0 \times A_1^{B} \times (\Delta T_j)^{-B} \times (\Delta T_j)^{a} \times [\frac{C + (t_{on})^{\gamma}}{C + 2^{\gamma}}] \times e^{\frac{E_a}{kT_m}} \times K_{thickness}$	ΔT_j t_{on} T_m	[70]
GaN Lifetime Model[11]	*Solder interconnect*	$\Delta\gamma = \frac{(\Delta a \times \Delta T_s \times L)}{h}$ $C = 0{,}442 - (6 \times 10^{-4} \times T_s) + 1{,}74 \times 10^{-2} \ln(1 + f)$ $N_f = \frac{1}{2}(\frac{\Delta\gamma}{2\varepsilon_f})^{\frac{1}{C}}$	f T_s ΔT_s	[71]

[1] a, n: material-dependent parameters, ΔT: temperature swing. [2] C_1, C_2: material-dependent parameters, $\Delta\varepsilon_p$: plastic strain. [3] α, b: material-dependent parameters, L: solder interconnect length. [4] C_1, C_2: material-dependent parameters, $\Delta\sigma$: stress range. [5] a, n: material-dependent parameters, E_a: activation energy, k: Boltzmann constant, ΔT_j: junction temperature swing, T_m: junction temperature mean value. [6] A, n_1, n_2: material-dependent parameters ,E_a: activation energy, k: Boltzmann constant, f: temperature cycling frequency parameters, ΔT_j: junction temperature swing, T_m: junction temperature mean value. [7] L: solder joint lateral size, x: solder joint thickness, $\Delta\alpha$: CTE mismatch, C: fatigue exponent, γ: solder ductility factor, ΔT: temperature swing. [8] $B1 \sim B6$: material-dependent parameters , k: Boltzmann constant, ΔT_j: junction temperature swing, T_{max}: junction temperature max value, E_a: activation energy, t_{on}: heating time, I: DC current applied per wire, V: blocking voltage, D: bond wire diameter. [9] A, a, $B0$, $B1$, C, γ: material-dependent parameters , ΔT_j: junction temperature swing, T_m: junction temperature mean value, E_a: activation energy, k: Boltzmann constant, t_{on}: heating time, f_{diode}: diode impact factor. [10] B, a, A_0, A_1, C, γ: material-dependent parameters , ΔT_j: junction temperature swing, T_m: junction temperature mean value, E_a: activation energy, k: Boltzmann constant, t_{on}: heating time, $K_{thickness}$: thickness factor. [12] $\Delta\gamma$: shear strain range, Δa: CTE mismatch, ΔT_s: temperature range, L: equivalent half length of device, h: solder joint standoff height, f: cyclic frequency, T_s: mean cyclic solder joint temperature, C: fatigue ductility exponent, $\Delta\gamma$: cyclic shear strain energy, ε_f: fatigue ductility coefficient.

the lifetime would be significantly longer due to the lower temperature.

The Scheuermann's lifetime model is used to evaluate the lifetime of a device based on the field experience of the device under test operating for cycles at low frequencies. This model takes into account several parameters, including the body diode impact factor (f_{diode}), junction temperature swing (ΔT_j), mean junction temperature (T_m), and heating time or pulse duration (t_{on}) of the semiconductor. Other parameters considered by the model include the bond wire aspect ratio (a_r), technology factor (A), material-dependent parameters α, β_0, β_1, γ, and C, the Boltzman constant (k), and the activation energy (E_a) [85]. Similarly to the Bayerer model, this model overlooks the significance of low temperature swings. Additionally, it fails to consider the impact of high blocking voltage on the ultimate lifetime.

In the updated version of Scheuermann lifetime model, as reported in reference [70] and modified by Semikron, the chip thickness factor ($k_{thickness}$) is employed to influence the impact of higher blocking voltage on the device's lifetime. The model posits that under higher voltages, the chip thickens, resulting in increased stiffness and consequently higher stress on interconnections and lower lifetime.

However, authors in [86] have claimed that the semiconductor chip with a higher blocking voltage capability, characterized by a wider surface, allows for an increased number of wire bonds. This, in turn, reduces the applied current to each wire bond, leading to an increased lifetime.

In the context of SiC MOSFETs, the updated Semikron models are applicable for SiC, as they account for this by incorporating the $k_{thickness}$ factor. It should be noted that the Young's modulus in SiC (501 GPa) is nearly three times higher than that of Si (162 GPa), resulting in higher stiffness [14].

Another crucial consideration is the pulse duration (t_{on}). In the updated version, t_{on} varies from 70 ms to 60 s for DC power cycling tests (as discussed in Section VI), and it ranges from 40 ms to 500 ms for AC power cycling tests. Results from [87] suggest that for pulse durations below 40 ms, there is minimal difference compared to those at 40 ms. Conversely, for longer cycles exceeding 60 s, it may be considered that deformation saturates for $t_{on} > 60$ s [88].

However, while the aforementioned lifetime models are suitable for Si and SiC devices, they are not applicable to semiconductors where thermal activation energy does not influence their reliability. For example, GaN HEMTs are not affected by thermal activation energy at temperatures below 300 °C. Additionally, a majority of these models were developed to describe wire bond fatigue in Si and SiC, which is less relevant for GaN HEMTs due to the development of new packaging techniques such as GaNpx and clip-bond packaging [89]. In GaNpx packaging, laser technology is employed to create vias that connect the copper foil to the die without the use of conventional bond wire or in clip-bond packaging technology, solid copper-clip is utilized instead of internal bond wire.

However, the degradation of solder between the chip and copper layer of Aluminum PCB can be a factor in the reliability assessment of the GaN device. This degradation is caused by the combination of electro-thermal stress and the difference in the CTE between the materials, which leads to the formation of cracks in the device due to thermal cycling [90], [91], [92]. To consider this in the forecasting of the lifetime of GaN HEMTs, the Coffin-Manson lifetime model has been modified to incorporate a term for shear strain, as illustrated in Table 1. In this model, the shear strain, denoted as $\Delta\gamma$, represents the amount of stress that causes the crack in the solder joint to propagate, and it can accumulate over time as the device is used. The fatigue ductility factor, denoted as C, is dependent on the mean cyclic temperature of the solder joint (T_s). Other parameters that are relevant to the lifetime model are the temperature swing (ΔT_s), the cyclic frequency (f), and the mean number of cycles to failure (N_f) [92], [93], [94]. The limitation of this model arises from its invalidity when subjected to temperature cycles exceeding 1000 per day.

Several examples are presented below to gain insight into the prediction of the lifetime of electronic components using physics-based models in specific applications. In ref. [95], a PoF-based model was presented for the RUL estimation of electronics components soldered on a PCB that is subjected to vibration loads. The authors modified a strain model using finite element analysis software, and then used strain gauges mounted on the back side of the PCB to measure the strain and calculate the RUL. The crucial aspect is the comparison between predicted results and experimental findings, revealing differences ranging from 1.4% to 70.77%. In articles [96], [97], a real-time electro-thermal model for the lifetime estimation of power modules was proposed based on the failure of bond wire joints and solder layers using Coffin-Manson and plastic strain models. In ref. [80], a compact thermal model and a PoF-based model were proposed to calculate the temperature in the solder interconnection and the accumulated plastic strain in the solder material under different load conditions, respectively.

The authors in [98] proposed a prognostic method for an inverter that utilizes IGBTs as the main switches. In this study, the focus was on the die-attach solder fatigue, which was analyzed using a plastic strain-based model. The authors also modified the damage accumulation method (i.e., Miner's rule) by updating the thermal resistance value, which increases due to damage, and incorporating this updated value into the electro-thermal model and the semiconductor characteristics. Additionally, the analysis indicates that crack initiation is highly dependent on stress levels, whereas crack propagation does not exhibit such a dependency on stress level. In ref. [99], four different failure sites were analyzed: chip mount-down solder joints, substrate mount-down solder joints, busbar solder joints, and aluminum bond wire. Also, a strain-based model was used to determine the lifetime of a semiconductor power module. To analyze lifetime, thermal cycling loading consisting of -40°C and 125°C temperatures, with 15 minute ramps and dwell times, was employed. Ultimately, the analysis revealed that the busbar solder joint was the primary failure site significantly impacting the lifetime of the entire module, with a total of 946 cycles. The paper [55], focuses on predicting the lifetime of a MOSFET utilized in an automotive anti-lock braking system, which requires a substantial number of operational cycles. Specifically, it examines the impact of degradation on the drain aluminum surface resulting from spikes in the gate oxide, leading to elevated device heating. The output results demonstrate that occurrences of this gate voltage spike can decrease the lifetime by a factor of 150. Finally, in articles [85], [100], the operating lifetime of SiC MOSFET and IGBT modules in electric vehicle and photovoltaic inverter systems, respectively, were predicted using Scheuermann's lifetime model.

C. DATA-DRIVEN APPROACH

Data-driven approaches for predicting the reliability of electronic systems and devices often utilize techniques such as data analytics, machine learning (ML), and Markov models. These approaches use past data, such as experiments and aging tests, to predict reliability rather than relying on physical properties and formulas [101], [102]. ML algorithms are mathematical model mapping methods used to learn or uncover underlying patterns embedded in the data, meaning they can perform recognition, classification, and prediction on data by learning from existing data (training set). Based on past data behavior, typically, a model is built that can then be used to accurately predict the state of health (SOH) of the devices

TABLE 2. Data-Driven Models

Method	Failure site	Failure indicator	Refs.
Gaussian	Die attach	MOSFET/ ON-state resistance	[101]
Relevance Vector Machine	-	MOSFET/ON-state resistance	[103]
Markov Chain	-	MOSFET/Gate leakage current	[104]
Kalman filter	Die attach	MOSFET/ON-state resistance	[105]
Kalman filter	Electrolytic Capacitors	Capacitance value	[106]
Gaussian process regression biased with Bayesian inference	-	IGBT/ON-state collector–emitter voltage	[107]
Particle filter	-	IGBT/Collector-emitter current	[108]
Exponential Empirical	-	MOSFET/ON-state resistance	[109]
Bayesian Inference Estimator	Gate-oxide degradation	MOSFET-IGBT/ Gate threshold voltage	[110]
Unsupervised machine-learning	-	MOSFET/ON-state resistance	[111]
Gaussian process regression, Kalman and Particle filter	Die attach	MOSFET/ON-state resistance	[112]

in question. The lifetime of a device is determined based on when its condition-monitored data reach a failure threshold level, which is defined based on standards and experience. As discussed in ref. [29], this approach requires a large amount of data to accurately cover all expected variations and provide reliable estimates. It is important to mention that additional requirements besides having enough data need to be fulfilled in order to provide accurate estimates, for instance, adequate data-preprocessing and hyperparameter tuning. Table 2 lists some examples of data-driven methods.

D. FUSION (HYBRID) APPROACH

Hybrid-based approaches for predicting the RUL of a device combine PoF-based models with data-driven approaches. This method reduces the reliance on past data and can handle previously unseen failure modes. Generally, data-driven models are used to detect anomalies in measured data, and a combination of PoF-based and data-driven models can be used to estimate the RUL [113]. Article [114] provides a review of hybrid approaches for RUL prediction in various fields. In ref. [89], a PoF-based model for the degradation of solder interconnect between GaN HEMT and PCB was initially calculated based on variations in drain-source resistance. Also, during testing, the coefficients of the PoF-based model were updated using sensor data and a data-driven method (i.e., a neural network). In article [115], a fusion prognostics method was used to estimate the RUL of multi-layer ceramic capacitors. First, a failure mode, mechanism, and effect analysis (FMMEA) was used to identify potential failure mechanisms and a failure model. In this case, data from history and standards were used to define failure rather than using a failure model. Then, using this failure definition and a data-driven method to track the behavior of parameters, the lifetime was calculated.

IV. OFFLINE RELIABILITY ASSESSMENT METHODOLOGY

The assessment of the reliability of PE components and subsequently whole systems without actively operating them is known as offline reliability assessment. This evaluation can be conducted through a range of techniques including testing, analysis, and simulation. Offline reliability assessment is often utilized to forecast the reliability of a system prior to its implementation, or to evaluate the reliability of a system that is no longer in service. Additionally, it can be used to identify potential reliability problems and devise strategies for improving the system's reliability. In this paper, the focus of offline reliability assessment is on forecasting reliability prior to implementation, particularly during the early design stage.

A. DESIGN FOR RELIABILITY (DFR)

In order to improve the reliability of power electronic converters, it is beneficial to address reliability issues during the early design stage. Physics- based models can serve as a baseline for a design for reliability (DFR) methodology. Results from multi-physics-based models and optimizing components, topology, and control systems can be used in the design stage to improve the performance of the device or system [85], [116], [117], [118]. Additionally, using PoF/empirical lifetime models in the DfR methodology can provide valuable insights into material selection. Such models help estimate the lifetime of active and passive elements subjected to various stressors like thermal cycling, vibrations, and mechanical shock. A comprehensive DfR process includes defining a lifetime model, identifying real-life mission profiles, and measuring thermomechanical stress. The previous section addressed the first requirement, while the following section will elaborate on the remaining two. By implementing the DfR approach, design engineers can identify potential reliability issues and devise strategies to improve the reliability of the device or system.

1) MISSION PROFILE-DEFINITION

A mission profile is a comprehensive list of all the scenarios and conditions that a DUT is expected to encounter during its intended use and over its entire lifetime. It describes the stress factors that the DUT will experience from the time of production until failure occurs. Additionally, mission profiles are specific to different applications. As such, the same DUT may encounter different mission profiles depending on the specific application for which it is used. For example, mission profiles related to automotive applications differ from those related to photovoltaic/wind applications, even if the same PECs are utilized as the DUT.

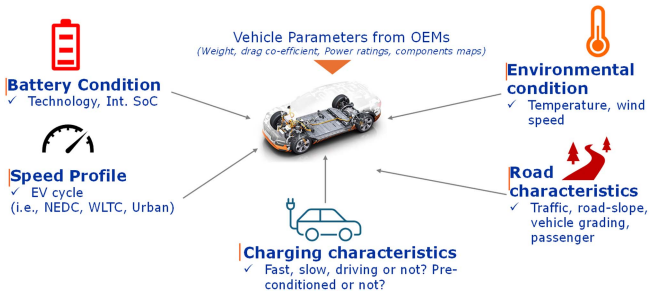

FIGURE 3. **Overview of mission profile for automotive applications [22].**

For instance, in ref. [119], a mission profile based on solar radiation was defined for a converter used in photovoltaic systems. Meanwhile, ref. [120] defined a wind profile, and ref. [121] defined a sea elevation profile for wind power and wave energy applications, respectively. For EVs applications, mission profiles have been defined based on factors such as the battery state of charge (SoC), coolant temperature, power train thermal system, driving cycle, and requested torque of the electric motor [22], [122], [123]. It should be noted that the mission profiles can be categorized as environmental, application-specific, and user-specific. Environmental mission profiles include ambient temperature, road characteristics, altitude, irradiance, wind speed, and humidity. Application-specific mission profiles include battery technology, initial SoC (i.e., battery condition), and charging characteristics, which depend on the brand of the vehicle. In contrast, vehicle speed profiles and vehicle payload due to passengers can be considered user-specific mission profiles. An example of an overall mission profile for EV applications is illustrated in Fig. 3.

2) MULTI-FIDELITY MULTI-PHYSICS MODELING

Once a suitable mission profile has been identified, the next step is to evaluate the behavior of PECs under subjected working conditions. To achieve this, the use of Multi-fidelity multi-physics modeling (MFMPM) has become an increasingly powerful method for estimating the behavioral performance of PECs. This technique involves a combination of different modeling methods that operate at varying levels of detail, allowing for the simulation of a PEC's behavior under different operational conditions and stressors. By integrating multiple physical phenomena and stress factors, such as thermal, electrical and mechanical stress, MFMPM can provide a more precise assessment of the PEC's reliability. In the context of improving the design and reliability of PECs used in EV applications, two distinct modeling techniques are employed to facilitate fault diagnosis, prognosis, and predict the reliability and lifetime of the PECs under various mission profiles. Specifically, the high-fidelity (HiFi) model is used to analyze the semiconductor module and thermal model of the optimized PEC, while the medium-fidelity (MFi) model focuses on mission-profile oriented temperature profiles of all devices to assess ageing stress and lifetime [124]. By adopting these modeling techniques, the design for reliability of the PECs can be represented and evaluated more accurately, and reliable benchmarks can be predicted. To speed up the process of optimization and simulation, less accurate fast models are utilized to simulate different EV driving scenarios. For instance, a detailed HiFi simulation model may slow down the EV simulation process as it requires a small simulation step size (1 μs or 0.1 μs) for accurate results of the HiFi PE component's simulation. In contrast, the standard step size for an entire EV simulation is typically 0.01s. Using a 1 μs step size for a HiFi model of an EV, it can take up to 15 minutes to complete 1 ms of simulation on a PC with Intel Core i7 Processors. Therefore, it would take approximately 52 years for this PC to simulate a single complete Worldwide Harmonized Light Vehicle Test Procedure (WLTP) driving cycle [125], [126].

3) COUNTING ALGORITHM

In order to accurately estimate the End of Life (EoL) of semiconductors under cyclic thermal load conditions, it is necessary to extract key features from the temperature profiles that the device under test experiences during the relevant mission profile [127]. These features, such as the temperature mean value and dwell time, can then be input into lifetime models in order to assess the reliability of the semiconductor. One method for extracting these features is the cycle counting algorithm, which can be implemented using various techniques such as the simple range counting algorithm, the level crossing counting algorithm, the peak counting algorithm, the range counting method, and the rainflow cycle counting (RCC) algorithm. These algorithms allow for the identification of functional parameters that are necessary for accurate EoL predictions [98], [128], [129]. On the other hand, these counting methods do not have universally accepted definition of a temperature cycling methods [130]. Previous research has demonstrated the differences in output results obtained using various counting algorithms when applied to the same mission profile [128]. The rainflow cycle counting algorithm, developed by Endo and Matsuish, is a well-known method for extracting features from temperature profiles that is able to handle both small and large cycles. It is commonly used in applications where real-time processing of data is not necessary, as it need large amounts of data that require significant processing time and storage space. However, there have been efforts to improve the efficiency of the RCC algorithm, such as reducing the data size by processing data in short time intervals or using the ordered overall range method (OOR), which only saves the minima and maxima of temperature profiles. These approaches can help to improve the performance of the RCC algorithm in terms of processing time and storage requirements [13], [131]. In [79], [132], an online version of the RCC algorithm was implemented. This means that the algorithm was designed to process data in real-time, rather than being applied to a dataset after it has been collected. This can be useful in situations where it is necessary to perform

TABLE 3. Analytic Cumulative Degradation Models

Characteristics	Miner	DLDR	NLDR
Linear damage evaluation	✓	✓	×
Load level dependence	×	✓	✓
Load sequence consideration	×	✓	✓
Complexity	Simple	Simple	Complex
Model equation	$D = \sum \frac{n}{N_f} = 1$	$D_l = \sum \frac{n}{N_l} = 1$ $D_{ll} = \sum \frac{n}{N_{ll}} = 1$ $N_l = f(N_f)$ $N_{ll} = N_f - N_{ll}$	$(\frac{n}{N_f})^{q(\Delta T_j)} = 1$

feature extraction and analysis on temperature data as it is being collected, rather than after the fact. In addition, it is worth noting that the application of the classical rainflow counting algorithm may not be evident in lifetime models such as Semikron or Bayerer. This discrepancy arises because the rainflow counting algorithm does not differentiate between ON pulse time and OFF time, whereas the lifetime models exclusively consider the heating time. Moreover, in order to accurately predict the EoL of a DUT that experiences cyclic stress of varying amplitude, it is necessary to take into account the accumulated damage caused by the stress. One method for doing this is the Palmgren-Miner linear accumulation rule, which states that the DUT will fail when the accumulated damage (D), calculated using (3), reaches a value of 1. In this equation, n_j is the number of cycles experienced by the DUT at stress level j, and N_j is the number of cycles to failure at the same stress level, as calculated using a PoF or empirical lifetime model [118], [133], [134].

$$D = \sum_{j=1}^{k} \frac{n_j}{N_j} \tag{3}$$

In addition to the Palmgren-Miner linear accumulation rule, there are several other methods for accumulating damage in order to predict the EoL of a device under test. Some examples of these methods include the Double Linear Damage Rule (DLDR), and the Non-linear Damage Rule (NLDR). These models take into account factors such as the level of load, the interaction between different load levels, and the sequence of load levels in order to predict the EoL of the DUT. Table 3 demonstrates a comparison between these rules. Miner's rule fails to anticipate the impact of loading sequence, resulting in inaccurate predictions [9], [135]. Consequently, DLDR is introduced to enhance accuracy with only a modest increase in computational effort, without necessitating additional material data or mission details. It should be noted that the in applications that involve severe high-cycle and low-cycle loading, Miner's rule leads to unacceptable, nonconservative results [136]. Additionally, NLDR addresses loading sequence effects and modifies material properties and stress levels through a parameter "q", recognizing that material mechanisms during fatigue are not linear and become particularly so high in the pre-fracture stage [137].

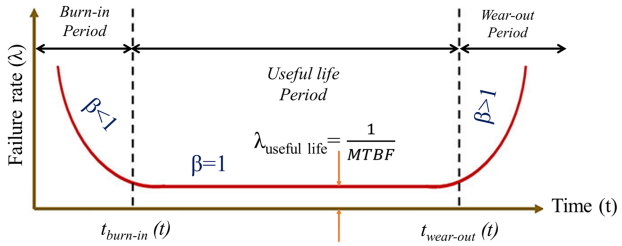

FIGURE 4. Failure rate curve (bathtub) as a function of time.

Although these models can be useful in certain situations, the Palmgren-Miner linear accumulation rule, LDR, is still the most widely used method for estimating the lifetime of semiconductors [135].

4) RELIABILITY METRICS AND PREDICTION APPROACH

In order to enhance the performance of PECs, it is essential to carefully select both the converter topology and the control system. These design choices can have a significant impact on the overall performance, efficiency, and reliability of the PEC. The assessment of environmental conditions and load profiles, as well as the implementation of scheduled maintenance programs, can also contribute to improved system performance when undertaken as part of a reliability assessment program. However, certain metrics and measures are needed to evaluate lifetime improvements in PECs.

A number of metrics for reliability assessment have been introduced that are intended to satisfy customer and application requirements. These metrics, commonly used for reliability assessment, include the reliability (R(t)), failure rate (λ_i), mean time to failure (MTTF), and mean time between failure (MTBF). The reliability (R(t)) is defined as the probability that a system/subsystem/component will function as intended under specified operational conditions for a given time interval [0, t]. It should be noted that the reliability may decrease over time, and warranties and guarantees should be established for commercial products to account for this decline [138], [139]. The failure rate, denoted by λ_i, conveys "an indication of the proneness to failure of the item after time t has elapsed" [138]. The lifetime of an object can be divided into three distinct phases, as depicted in Fig. 4. In the initial

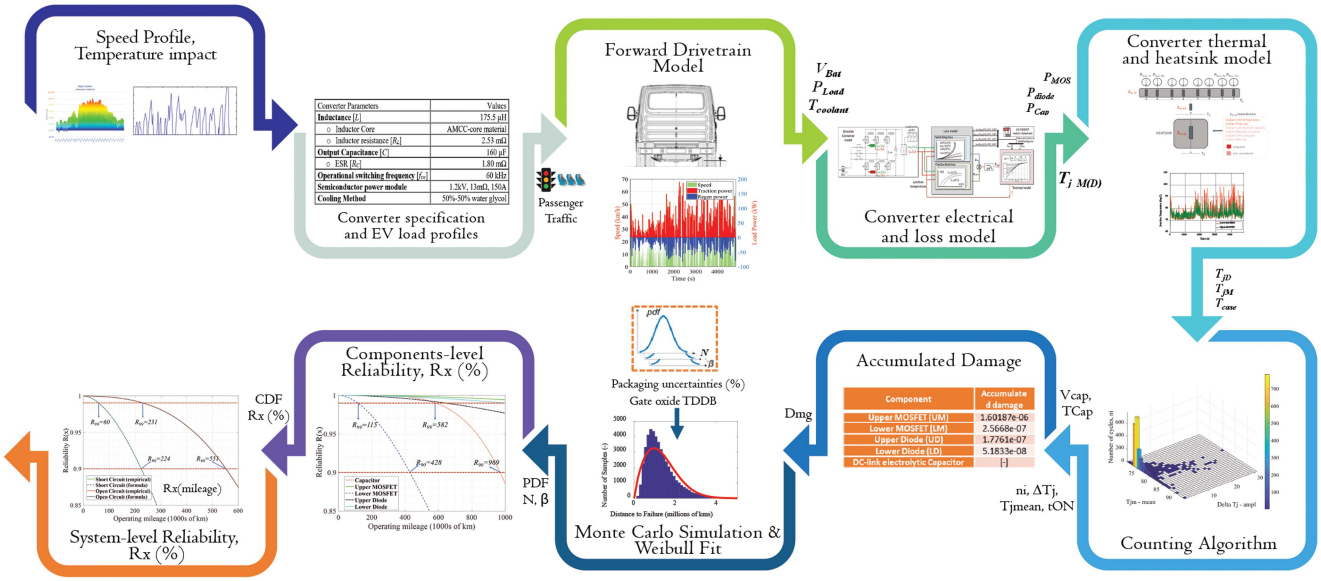

FIGURE 5. Stepwise real-life mission profile-oriented lifetime estimation method.

phase, failure may occur due to weaknesses in the material, variations in quality, or errors made during the production process. While a range of quality tests may be conducted to identify and remove defective products before they are sold to consumers, some defects may go undetected, leading to a high failure rate in this stage. In the second phase, sudden failure occurs at a constant rate. The MTBF and the useful lifetime are also defined within this phase. The final phase is characterized by gradual failure resulting from wear-out on the product [138], [140], [141].

The MTBF is a measure of the amount of time that a given population of units will operate without experiencing failure, assuming a constant failure rate. MTBF can be calculated using various standards such as MIL-HDBK-217F, Siemens SN29500, Telcordia SR-322, and RDF-2000, which utilize historical data to estimate the lifetime of electronic components. Also, in 2017, the IEC 61709 standard was published, which takes into account factors such as temperature cycling, various operating conditions, and mission profiles in the calculation of MTBF for electronic elements. The MIL-HDBK-217F standard defines MTBF as follows [142], [143]:

$$MTBF = \frac{1}{\lambda_i} \tag{4}$$

$$\lambda_i = \lambda_b \pi_T \pi_A \pi_S \pi_Q \pi_E \tag{5}$$

In (5), λ_b is defined as the base component failure rate, π_T is a scaling factor, π_A represents the type of application and takes into account power rating, π_S represents voltage stress, and π_Q and π_E represent part quality and the operating environment, respectively.

Last but not least, in order to calculate the MTTF, a stress-strength analysis that takes into account non-constant failure rates and wear-out processes is necessary. This is equivalent to operating in the third phase of the bathtub curve. To calculate

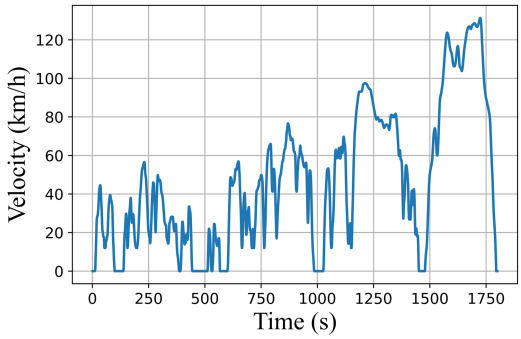

FIGURE 6. Speed profile of an EV during WLTC.

the failure rate, it is necessary to determine the probability that the stress applied to passive/active components exceeds their strength. In order to determine the failure distribution, Monte Carlo simulation may be used to simulate the effects of uncertainty in device parameters on lifetime estimation. It is worth noting that this uncertainty is often the result of manufacturing or modeling procedures [144], [145].

a) DFR approach. use-case for automotive applications: Fig. 5 illustrates a stepwise method for estimating the lifetime of automotive PECs based on real-life mission profiles. In this paper, the impact of driving cycles on the lifetime of SiC-based inverter is demonstrated as a case study. Therefore, the Worldwide Harmonized Light Vehicles Test Procedure (WLTP) is selected as driving cycle, which consists of a distance of 23.3 km, a duration of 1801 seconds, and an average speed of 46.5 km/h, as shown in Fig. 6.

The first step in this lifetime estimation process involves establishing the EV load profile and converter specifications. These are then utilized to generate a forward drivetrain model that converts speed and torque into electrical parameters. The converter model is subsequently implemented in a simulation,

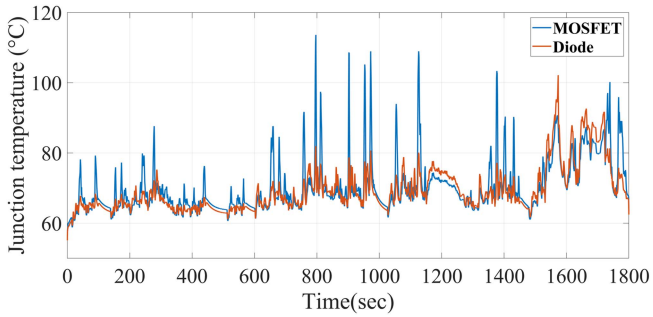

FIGURE 7. Thermal stress loading during WLTP.

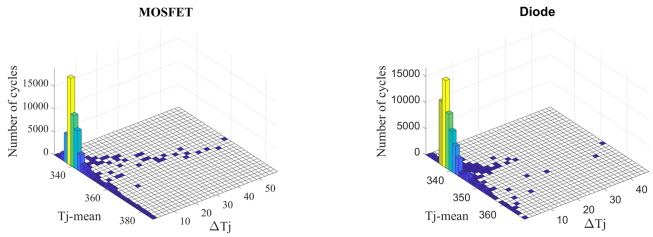

FIGURE 8. Number of cycle ni, mean junction temperature Tj-mean (k), temperature swing ΔTj (K).

along with a model for estimating power losses. Physics-based lifetime models transform stress values into the number of cycles required by the accumulated damage model. It is worth noting that the converter electrical model may be updated after a certain amount of damage has been incurred, for example by modifying the drain-source resistance or thermal impedance in the electro-thermal model. The thermal model and cooling system specification are then employed to determine the junction temperature profile concerning the load profile and power losses, which translates the mission profile into thermal stress.

In this paper, the junction temperature of the one SiC-MOSFET switch and its body diode is estimated using a high-fidelity electro-thermal model [125], as depicted in Fig. 7. For simplification, it is assumed that the other MOSFETs and body diodes have the same thermal response throughout the driving cycle. Afterward, the thermal stress profiles transfer through a cycle counting algorithm (CCA). The CCA is utilized to classify strains, temperature cycles and their combinations for fatigue analysis. In this paper, a modified rainflow cycle counting algorithm (RCCA) is used, according to [22], [85]. The RCCA provides the number of cycles N and determines the amplitude of the junction temperature swing ΔT_j, the mean junction temperature T_{jm} and the pulse duration of the MOSFETs ton, as shown in Fig. 8. Physics-based lifetime models transform stress values into the number of cycles required by the accumulated damage model. It is worth noting that the converter electrical model may be updated after a certain amount of damage has been incurred, for example by modifying the drain-source resistance or thermal impedance in the electro-thermal model. Afterward, once the junction temperature profile has been determined, the lifetime of the semiconductor can be estimated by taking into account other

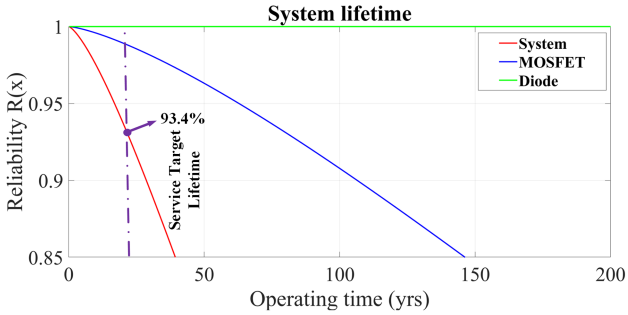

FIGURE 9. System and component level lifetime estimation result for WLTC speed profile.

failure mechanisms such as gate oxide failure. It is worth noting that the specifications of the semiconductor may not be identical to other semiconductors produced by the same company, and the environmental conditions and application may not be the same as those during power cycling tests. As a result, a certain degree of uncertainty needs to be considered in the lifetime parameters, and Monte Carlo simulation is employed to consider the uncertainty impacts. To apply statistical analysis to the output of the Monte Carlo simulation, a suitable function (e.g., Weibull) is chosen for curve fitting, allowing for the estimation of statistical-based information such as reliability and failure rate.

Finally, by calculating failure rates, ultimate failure, reliability probability, and the MTTF, actions can be taken to improve the lifetime of the device by modifying topologies and control systems, combining active and passive elements in series or parallel, etc. In this paper, the reliability of the inverter is calculated based on the failure association of the MOSFET and diode. Only the six SiC MOSFETs and six anti-parallel body diodes are considered in this study. Because the inverters in EVs lack redundancy, the inverter system immediately fails if a failure occurs in any of these two components.

Besides, for the system-level lifetime calculation, it is considered that the inverter will be subjected to six Worldwide Harmonized Light Vehicles Test Cycle (WLTC)/day, which equals three hours of effective driving. The corresponding lifetime concerning the WLTP mission profile is displayed Fig. 9, and it can be seen that the targeted lifetime of the inverter is 20 years, and it is achievable with a reliability percentile of 93.4%. The lifetime parameters used in this paper are applied SEMIKRON lifetime model [22]. As a consequence, this offline reliability assessment method can be readily employed during the initial design phase, especially when the hardware representative of the DUT is not yet fully commercialized. This approach facilitates the acquisition of reliability-focused design optimization, contributing to the establishment of design guidelines.

b) DFR approach. use-case for charging applications: To showcase the applicability of the lifetime assessment method, a second case study is considered for off-board charger applications only considering the reliability factor of SiC MOSFETs. It applies all methodologies outlined in the

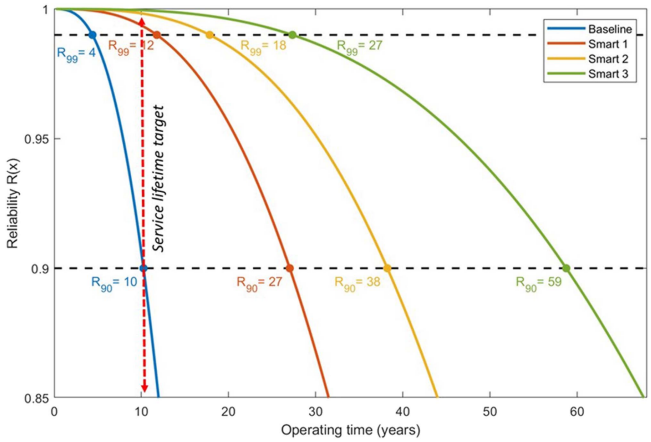

FIGURE 10. System-level lifetime estimation results for different current profiles [146].

previous case study, with the exception that in this particular application, the mission profiles are completely different. Consequently, analyses are conducted for four distinct mission profiles: "baseline," wherein no load variation occurs during charging, and three smart charging profiles derived from the optimal charging scheduling algorithm [146].

The overall system reliability of the charger is depicted in Fig. 10 as a function of operational time in years. Also, it can be seen from the figure that smart charging strategies can improve the lifetime of the charging system by at least a factor of 2.7 compared to conventional charging.

B. LIFETIME ESTIMATION OF CAPACITOR

Capacitors constitute a critical component in PECs, accounting for 19% of the observed failures according to field data [22]. As such, their integration into the design process is imperative. The selection of capacitors for use in power electronics converters is constrained by the need for cost and size reduction, the ability to function in harsh environments, and compatibility with high-power applications in industries such as aerospace, automotive, and renewable energy. The most commonly used capacitors for this purpose include aluminum electrolytic capacitors, multi-layer ceramic capacitors, and metalized polypropylene film capacitors. Furthermore, the main failure mechanisms for aluminum electrolytic capacitors are electrolyte vaporization and electromechanical reaction, for multi-layer ceramic capacitors it is moisture corrosion and dielectric loss, and for metalized polypropylene film capacitors it is insulation degradation and flex cracking [23], [147], [148], [149], [150]. More information about these types of capacitors can be found in [23]. It should be noted that the lifetime of DC-link capacitors depends on the operating voltage and hotspot temperature, and a model for predicting the lifetime based on empirical data is provided in (6).

$$L = L_0 \times \left(\frac{V}{V_0}\right)^{-n} \times e^{\frac{E_a}{K_B}\times\left(\frac{1}{T}-\frac{1}{T_0}\right)} \tag{6}$$

In this equation, L and L_0 represent the lifetime of the capacitor under actual and testing conditions, respectively. V and V_0 are the applied voltages under actual and testing conditions, respectively. T and T_0 are the temperatures (in Kelvin) of the capacitor under actual and testing conditions, respectively. K_B is Boltzmann's constant, and E_a is the activation energy. The exponent n reflects the dependency of the capacitor's lifetime on the applied voltage, which is dependent on the type of capacitor and the material used for the dielectric. Lowering the voltage will cause lower stress on the capacitor's dielectric during actual conditions, which can extend its lifetime [143]. Also, T is considered as the hotspot of the capacitor, which can be calculated using (7).

$$T = T_a + 1.5 \times Z_{th} \times \sum_{h=1}^{\infty} (I_{cap,h}^2 \times ESR_h + I_{leak}\left(V_{op}\right) \times V_{op}) \tag{7}$$

In (5), T_a represents the ambient temperature, Z_{th} denotes the thermal impedance, V_{op} signifies the operating voltage, I_{leak} (V_{op}) represents the leakage current which varies with the operating voltage, $I_{cap,h}$ denotes the capacitor current while h represents current harmonic, and ESR_h signifies the equivalent series resistance that varies with the current harmonic frequency. In addition, a coefficient of 1.5 is utilized to increase the effects of temperature rise caused by current in comparison to the ambient temperature [151], [152].

Furthermore, other lifetime models have been proposed for specific types of capacitors. For instance, (8), (9), and (10) proposed by Nichion, Rubycon, and Panasonic, respectively, are used for predicting the lifetime of aluminum electrolytic capacitors.

$$L = L_r \times 2^{\frac{T_r - T}{10}} \times 2^{1 - \frac{\Delta t_r \times \left(\frac{I_r}{I}\right)^2}{K}} \tag{8}$$

$$L = L_r \times 2^{\frac{T_r - T}{10}} \times 2^{\frac{\Delta t_r}{10} - \frac{\Delta t}{10}} \times \left(\frac{V_r}{V}\right)^{2.5} \tag{9}$$

$$L = L_r \times 2^{\frac{T_r - T_a}{10}} \tag{10}$$

In the case of film capacitors, the Cronell Dublier and Faratronic models, represented by (11) and (12) respectively, are utilized.

$$L = L_r \times 2^{\frac{T_r - T}{10}} \times \left(\frac{V_r \times F}{V}\right)^8 \tag{11}$$

$$L = L_r \times T_f \times \left(\frac{V_r}{V}\right)^9 \tag{12}$$

In the aforementioned equations, L_r denotes the rated lifetime, while L represents the actual lifetime. T represents the ambient temperature, T_r signifies the rated temperature, V_r denotes the rated voltage, and V signifies the actual voltage. Also, Δt_r represents the temperature rise, T_a denotes the core temperature, and F and K are coefficients.

V. ONLINE RELIABILITY ASSESSMENT METHODOLOGIES

In addition to performing a DfR analysis, the reliability of PECs can be further improved through a condition monitoring process. Condition monitoring involves evaluating the current health status and real-time measurement of parameters (e.g., junction temperature, drain-source resistance) in order to identify deviations from healthy baseline values and take appropriate actions. According to a survey conducted in the industry in 2011, 93% of participants considered reliability in power electronics to be a serious issue, and 50% of them agreed that implementing a condition monitoring program could help improve reliability [153]. By combining these active monitoring efforts with techniques to predict the future health of a system, known as prognosis, early maintenance can be carried out before faults occur. Furthermore, prognostic data can also be utilized for proactive control measures that aim to improve the lifetime of a system. For example, prognostic data can be used to implement load reduction strategies that help to control semiconductor temperature (T_j) and modify stress levels on the power switches. The combination of prognostic techniques and a proactive control approach is referred to as Prognostic and Health Management (PHM). The effective implementation of condition monitoring and PHM strategies requires a thorough examination of prior methods for detecting and predicting critical signals that indicate degradation in semiconductors, such as junction temperature and implementing measures to enhance the lifetime of these components. This can be achieved through the adoption of active thermal control policies. This section delves into a comprehensive analysis of the key factors that facilitate the successful implementation of condition monitoring and PHM.

A. INDICATOR FOR CONDITION MONITORING

As previously discussed, condition monitoring plays a crucial role in ensuring the reliable operation of power electronic systems, especially in demanding settings such as the automotive industry. Recently, several indicators have been proposed to evaluate the health of power electronic devices and systems during operation. These indicators are primarily based on the analysis of specific parameters, such as temperature, vibration, or electrical signals. By continuously monitoring these parameters, it is feasible to identify abnormal operating conditions, anticipate potential failures, and optimize maintenance and repair schedules to extend the system's lifetime [154]. Furthermore, these measurements are useful for PHM activities, which aim to predict the remaining useful life and overall health status of systems by detecting potential failures and determining the extent of degradation. This approach enables the scheduling of maintenance before any failures occur [6].

Table 4 presents the failure identifiers and their corresponding failure sites in SiC MOSFETs. It should be noted that in the sensitivity column, usually only one number is included, providing some insight into the failure identifier. These values vary based on loading conditions. Furthermore, the complicated structures of GaN HEMTs and the need for detailed analysis of failure mechanisms in this type of semiconductor make it beyond the scope of this paper to cover failure identifiers and corresponding sites. However, refs [90], [155], [156], [157], [158], [159], [160] can be used as references for the investigation of failure identifiers in GaN HEMTs.

TABLE 4. Failure Indicators for SiC

Failure site	Failure Identifier	Sensitivity	Linearity	Refs.
Gate Oxide	Threshold voltage shift	0.22mV~2V ↑, 0.15mV ↓	Good	[16], [31], [161], [162], [163], [164]
	On resistance	12mΩ ↑	Medium	[7], [16], [165], [166]
	Gate leakage current	5pA ↓	Low	[167]
	Miller Plateau Voltage	0.5mV~3.6V ↑, 4V ↓	Low	[18], [168], [169], [170]
	Drain leakage current	0.01μA ~ 40μA ↑	Medium	[171], [172]
	Transconductance	3S ↓	Good	[173]
	Turn-on Delay Time	5ns ↑	Good	[174], [175]
	Parasitic Capacitances	60pF~ 350pF↑	Good	[176]
	Switching transient turn on	0.19A/ns ↓	Medium	[17], [175], [177]
Body Diode	Drain leakage current	3.65μA ↑	Low	[178]
	Forward voltage	100mV ↑	Low	[179]
Bond Wires, Solder layers	Bond wire resistance	4mΩ ↑	Low	[180], [181], [182]
	Body diode forward voltage	80mV ↑	Low	[16], [165]
	Die-attached solder resistance	-	-	[182]

On the other hand, due to the rising need for power electronics to function at elevated power and temperature levels, there is an escalating importance for the precise and reliable determination of junction temperature as a fundamental aspect of reliability engineering and condition monitoring. As a result, the following section will focus on the significance of junction temperature measurement as a failure identification technique.

B. JUNCTION TEMPERATURE ESTIMATION

Based on the analysis presented in Section II, the primary factor that leads to the failure of SiC and Si semiconductors is typically attributed to the junction temperature, especially its fluctuations. Furthermore, in various accelerated aging tests, such as power cycling tests, it is imperative to regulate the junction temperature to ensure optimal performance.

Accurately measuring this parameter is also critical for the successful implementation of condition monitoring and health management strategies, including thermal management. This parameter can be utilized to estimate the ultimate lifetime of the semiconductor device, as outlined by standards such as

the Military Handbook 271. Moreover, in certain applications, where other failure indicators like drain-source resistances are used to predict the RUL, it is necessary to calibrate these failure precursors against the junction temperature [98], [183]. As a result, it is necessary to continuously measure the junction temperature to improve reliability analysis and health management. In real-world environments, it is not possible to directly measure the junction temperature using instruments such as optical fibers or thermal cameras due to the presence of package materials and dielectric gels [184]. There are several established methods for estimating temperature, one of which involves installing sensors within the power module package. These sensors have been implemented in some commercial power modules [185], [186], [187], [188]. One method for temperature measurement involves placing a negative temperature coefficient (NTC) sensor on the DBC within the module, which allows for direct temperature measurement [189]. Another approach is to incorporate a p-n diode into a semiconductor package, and use the instantaneous forward voltage of the diode for temperature estimation [190].

However, the use of NTC sensors or p-n diodes for temperature measurement may not be highly accurate or rapid due to the presence of thermal impedance resulting from physical distance [188]. In addition, a significant number of semiconductor modules do not have integrated temperature sensors, which can further decrease the feasibility of temperature measurement. Moreover, these devices may experience deterioration over time and require recalibration, which may restrict their utility in certain situations.

Another method for estimating junction temperature is to use temperature-sensitive electrical parameters (TSEPs), such as internal gate resistance, gate threshold voltage, and body diode voltage, which have gained attention in recent years. Currently, it is believed that this is the only approach for quickly measuring the temperature of packaged semiconductors in less than 100μs [184], [191]. However, the use of TSEPs is limited and, in most cases, they are only used in controlled laboratory environments [13], [192]. The different TSEPs are illustrated in Table 5. Generally, the use of TSEPs for junction temperature estimation can be divided into static and dynamic characteristics. In the first category, a common method for temperature estimation is to measure the current and voltage across the power device, as the static characteristics (I, V) of the power module are dependent on temperature.

In dynamic characteristics, dynamic parameters such as turn-OFF transition and turn-OFF delay time are considered. However, these require sensitive and accurate measurement equipment, which may not be easily available [193]. One disadvantage of TSEPs compared to physical and optical methods is that this approach estimates the average temperature across the chip and may not provide accurate insight into the temperature of solder interconnects and bond wires [147], [225]. For instance, the temperature at the center of the chip device is typically higher than at the edges, which can further complicate matters in large-dimension devices and potentially limit the use of this method to discrete and single-chip semiconductors. Additionally, in packages with multiple chips operating at different temperatures, there may be only one shared common access point between the chips. As a result, the mutual influences of all chips must be taken into consideration.

TABLE 5. Summary of Different TSEP

TSEP	Device	Sensitivity	Linearity	Ref.
Gate resistance	MOSFET/IGBT	0.9~2.8 mΩ/°C	Medium	[194], [195], [196], [197]
Threshold voltage	MOSFET/IGBT	-6 ~ -9 mV/°C	Good	[191], [198], [199], [200], [201]
Turn-ON/OFF delay	MOSFET/IGBT	2ns, 4 ns/ °C	Good	[202], [203], [204], [205], [206], [207], [208], [209]
Turn-ON $\frac{di}{dt}$	MOSFET-IGBT	0.047~4 A/(μs°C)	Medium	[204], [210], [211]
Turn-OFF $\frac{di}{dt}$	MOSFET	0.35 A/(μs°C)	Low	[212]
Gate drive peak current at turn ON instance	MOSFET	1 ~ 4 mA/ °C	Medium	[213]
ON-state resistance	MOSFET	0.54 mΩ/°C	Low	[214], [215], [216]
ON-state voltage	IGBT	1 ~ 5 mV/°C	Good	[217], [218], [219], [220]
Body diode voltage	MOSFET	-2.65 ~ -4.8 mV/°C	Good	[175]
Short circuit	IGBT	-2.85 A /°C	Good	[221]
Saturation current	MOSFET/IGBT	0.17 A /°C	Good	[222], [223], [224]

Furthermore, commissioning tests to identify the relationship between TSEPs and junction temperature are usually conducted in controlled situations where the self-heating of the device is not taken into account. As a result, there will inevitably be a discrepancy between the commissioning results and the actual junction temperature [192]. Moreover, the TSEP approach is currently facing the challenge of aging and the subsequent need for recalibration, which can create technical limitations for its use in real-world environments. During the operation of semiconductors, statistical and dynamic electrical parameters will vary based on the initial state, which can lead to a decrease in the accuracy of temperature estimation over time. Therefore, it is necessary to develop improved measurement methods and recalibrate TSEP to address this issue [98], [175]. Additionally, certain TSEPs, such as those that utilize gate threshold voltage, can disrupt the normal operation of converters by decreasing the switching frequency [203]. Also, in the short circuit method, it is necessary to add auxiliary switches to the system, disable protection circuits, and ensure that only the device under test is subjected to the short circuit test [221], [226]. Moreover, thorough preparation of test parameters is essential to avoid the generation of misleading results. For instance, in the study conducted by [227], it is demonstrated that the sensing current significantly influences the voltage transition immediately following the biasing of the body diode of a MOSFET. Additionally, sensitivity and

linearity regarding temperature need to be addressed. This is evident in SiC MOSFETs, where the On-state resistance shows non-linearity with low sensitivity to temperature variations [228]. It is worth noting that system-level methods, such as the identification of changes in low-order harmonics in the output of a voltage source inverter (VSI), are also utilized for junction temperature estimation [229].

Furthermore, with the advancement of the Internet of Things (IoT), digital twin applications in power electronic systems have emerged. Machine-learning-based digital twin concepts have been proposed to estimate or monitor parasitic parameters, electrical/thermal states, and health status of power devices and converters. Consequently, a data-driven digital twin methodology has been proposed to develop a real-time hardware-deployable edge model for estimating junction temperature [230].

Another method for calculating junction temperature involves utilizing an analytical model that integrates an electro-thermal model with datasheet parameters. However, this approach encounters challenges during real-world implementation, as estimating power losses online is computationally inefficient, leading to reduced accuracy. Additionally, datasheet parameters such as thermal resistance are often provided for worst-case scenarios [193].

Moreover, in offline mode, this methodology can be employed to compute the junction temperature profile corresponding to a particular mission profile, which can subsequently be integrated into lifetime models [231]. A straightforward method for implementing the thermal model is to use a resistor-capacitor-based model (RC model), which offers the benefit of ease of simulation [232], [233], [234]. One popular method of utilizing the RC thermal model is the 1-D RC model depicted in Fig. 11. While this model benefits from ease of implementation in simulation platforms and fast speed, its accuracy is limited due to the lack of consideration for thermal coupling between chips and layers and uneven temperature distribution [235].

The RC thermal model can be divided into two categories: the Cauer model and the Foster model. In the Cauer model, the R and C elements are replaced with the material properties of each layer, thus allowing each RC component to represent the internal temperature of the corresponding layer. In the Foster model, data obtained through experimentation and provided in the datasheet are used to calculate the thermal impedance between the chip and the case. This means that it is not possible to calculate the internal temperature within the package (e.g., solder joint) as there is no information available on the thermal impedance of each layer [236], however, this model requires less calculation effort in comparison with the one for the Cauer. To address the limitations of the 1-D electro-thermal model, a three dimensional (3-D) lumped thermal model has been proposed which can account for thermal coupling and calculate steady-state and transient temperatures at different layers and locations. However, this method is not a suitable choice for long-term mission profiles as it requires the use of Finite Element Method (FEM) or Finite Difference Method

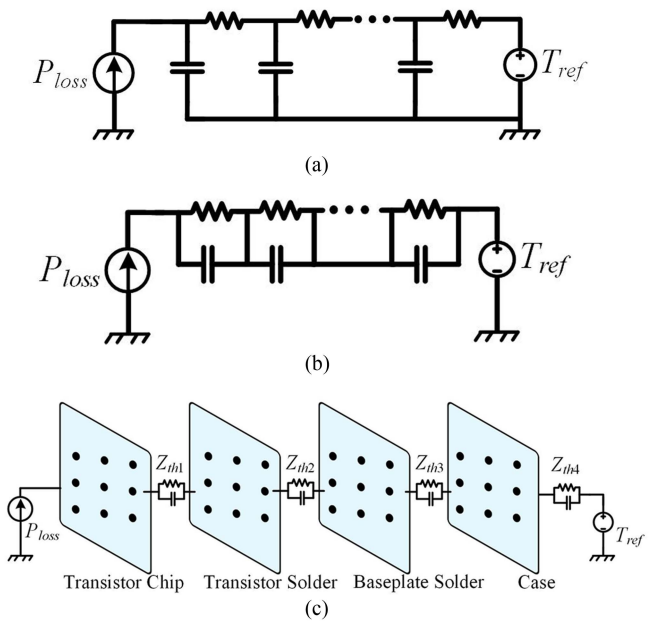

FIGURE 11. Electro-thermal model. (a) 1-D cauer model, (b) 1-D cauer model (c) 3-D model.

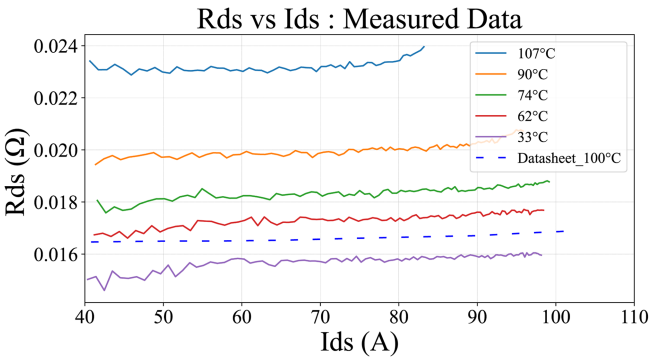

FIGURE 12. Collected data during the commissioning test.

(FDM) simulations to characterize the model results, which can be computationally intensive and may result in possible divergence for high thermal dynamics [237].

1) A USE-CASE ON JUNCTION TEMPERATURE ESTIMATION

In order to gain a deeper understanding of the feasibility of TSEPs for condition monitoring programs, it would be beneficial to implement one of the above approaches for junction temperature estimation in a real-world application. To this end, $R_{ds,on}$ measurement was chosen and carried out on a SiC Half-Bridge MOSFET Module (CAS120M12BM2) in a laboratory setting to evaluate the speed and accuracy of this TSEP in practice. In the initial stage of the process, a commissioning test was performed to generate a correlation map featuring $R_{ds,on}$, $i_{ds,on}$ at various T_j values [216]. As shown in Fig. 12, the commissioning test was conducted at the maximum drain-source current of 100A and the maximum junction temperature of 105˚C. Subsequently, in order to validate performance under real-world conditions, a boost converter

TABLE 6. FuSa Analysis Methodologies

Abbreviation	Explanation	References
ID	The objective of the **I**tem **D**efinition in the concept phase is to gather needed information about the item, its functionality, dependencies on, and interaction with the environment and other items.	[245]
HAZOP	The **Haz**ard and **Op**erability (HAZOP) is a team-based method for identifying potential safety and operational issues in system design, maintenance, or operation. It's formal, objective, ensuring a systematic, well-documented evaluation of potential problems/hazards.	[246], [247]
HARA	The **H**azard **A**nalysis and **R**isk **A**ssessment (HARA) in the automotive domain systematically determines potential risks in driving situations, introduces the Automotive Safety Integrity Level (ASIL), and sets Safety Goals.	[248]
FMEA	**F**ailure **M**odes and **E**ffects **A**nalysis (FMEA) systematically analyzes potential failure modes to prevent failures. It serves as a preventive process conducted before implementing new features or changes in products or processes.	[249], [250]
FSC	The **F**unctional **S**afety **C**oncept (FSC) defines necessary safety measures and requirements for system design to avoid residual risk.	[245], [251]
FMMEA	The **F**ailure **M**ode, **M**echanism, and **E**ffects **A**nalysis (FMMEA) methodology, derived from FMEA and Failure Mode Effect and Criticality Analysis (FMECA), focuses on understanding failure mechanisms rather than causes. It combines structured FMEA methods with "design for reliability" principles, considering operational conditions, duration of use, potential failure mechanisms, and active stressors.	[242], [243]

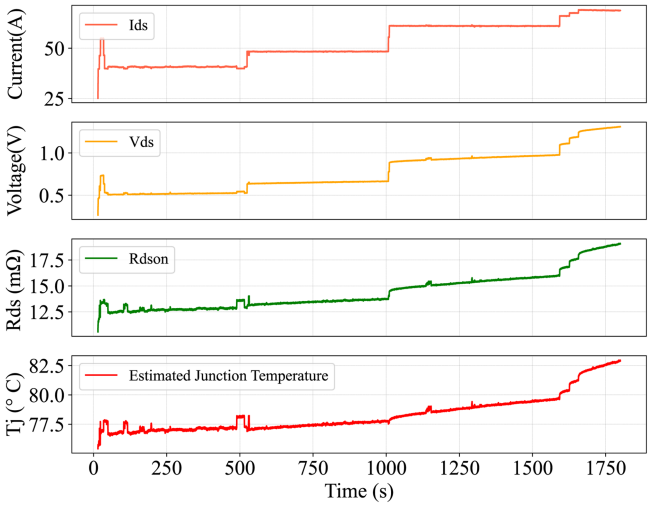

FIGURE 13. Online junction temperature estimation.

featuring the Half-Bridge Module as the main switch and output diode was employed, with the MicroLab Box responsible for generating gate PWM pulses and collecting data. It is important to note that gate PWM pulses were used to trigger data collection. In order to eliminate undesirable data, 100 samples were deliberately recorded, and after sorting and removing the upper and lower values, the average of the remaining samples was used as the final value. After completing a regression analysis of the commissioning test results in MATLAB, the corresponding mathematical function was implemented in MicroLabBox. Afterwards, a series of step loads were applied to the boost converter to observe the effects of changes in temperature. The Fig. 13 shows the variation in junction temperature with changes in load.

C. FUNCTIONAL SAFETY AND PHM

The use of condition monitoring and PHM techniques is fundamental to guaranteeing the functional safety (FuSa) of power electronics systems, particularly in safety-critical scenarios, where the failure of such systems can lead to severe consequences. Through the integration of these techniques in the design and operation of the system, faults can be effectively identified and isolated, and their impact can be mitigated. This, in turn, results in a more dependable and safer system. It is crucial to perform a PHM analysis and FuSa evaluation simultaneously with the development of a power electronics converter, as this enables the identification and resolution of potential faults or malfunctions of the system and its components over its lifetime, further enhancing the system's safety and reliability. Adherence to functional safety standards, such as IEC EN 61508 or industry-specific standards derived from it (e.g., ISO 13849 for simple systems, ISO 26262 for automotive, and ISO 25119 for agriculture), is mandatory. This section provides an example of a focus on the automotive domain, due to its stringent regulations and importance in the realm of electric mobility, where various types of PECs are employed. Table 6 provides a succinct summary of the required analysis methodologies.

In order to perform a functional safety analysis to identify potential faults over the item's lifetime, the following steps must be taken. The first stage in the concept phase involves defining the item, where relevant information about the item and its environment is gathered. Next, a HAZOP analysis must be performed. The output of this analysis is then used as input for the HARA. During the HARA, hazardous events at the item level are identified and classified in accordance with ISO 26262 and the Automotive Safety Integrity Levels (ASIL), where the risk of occurrence for a specific failure mode and its necessary level of avoidance is determined. The ASIL values range from ASIL D (most critical level) to ASIL A (low criticality). For each hazardous event, a safety goal is defined and the corresponding ASIL is assigned to each of the top-level safety requirements. The subsequent step is conducting the FMEA for each system level. A bottom-up approach is used to identify risks and potential failure modes of the PEC and its components, starting from the component level and

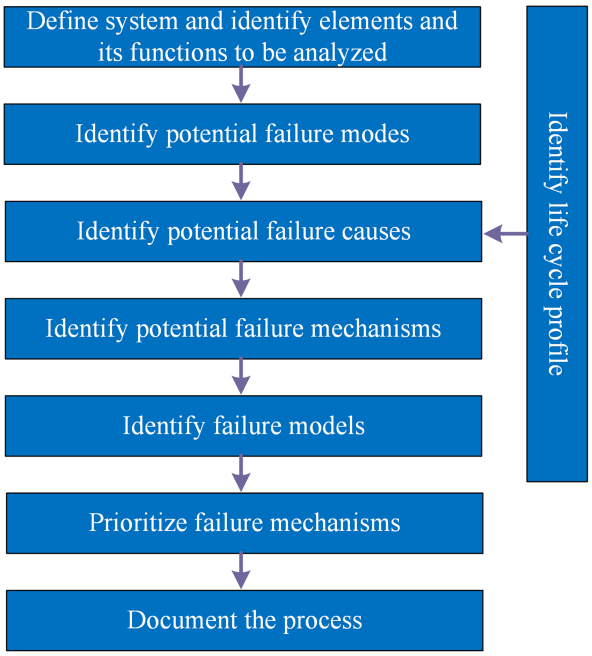

FIGURE 14. FMMEA methodology [244].

proceeding up to the system level of the PEC. For each level, a FMEA must be performed to determine the most critical risks. The final step in the concept phase is the formulation of the FSC. The FSC specifies the safety measures and requirements that must be met during the design and development of the system to eliminate an unacceptable residual risk.

While HARA and FMEA are widely utilized and acknowledged in various industries and for electronic products, as well as PECs [113], [238], [239], [240], [241], they fail to address the critical aspect of analyzing failure mechanisms for PHM. To address this shortfall, the FMMEA methodology has been developed. In order to react, comprehend, and forestall failures, it is necessary to identify the failure mechanisms in relation to the prevailing stresses (such as thermal stress, electrical stress, thermomechanical stress, and shear stress) that may induce these failures [242]. The objective is to properly choose the parameters of the failure mechanism to determine the actual precursors of failure for the health monitoring of the PEC system. A precursor refers to a change in a quantifiable variable that can be linked to subsequent failure (e.g., "temperature swing", "increase in resistance") [242], [243]. The procedures for conducting an FMMEA are depicted in Fig. 14 [244].

The superiority of the FMMEA approach compared to conventional reliability design methods lies in its integration of the concept of failure mechanisms into every aspect of the decision-making process [252]. This methodology utilizes failure mechanisms as the foundation of reliability evaluation, and has been acknowledged in the standards of prominent technical organizations, such as the IEEE 1413 [253], EIA/JEDEC [254], [255], [256], [257], [258], [259], and SEMATECH [260], [261], [262].

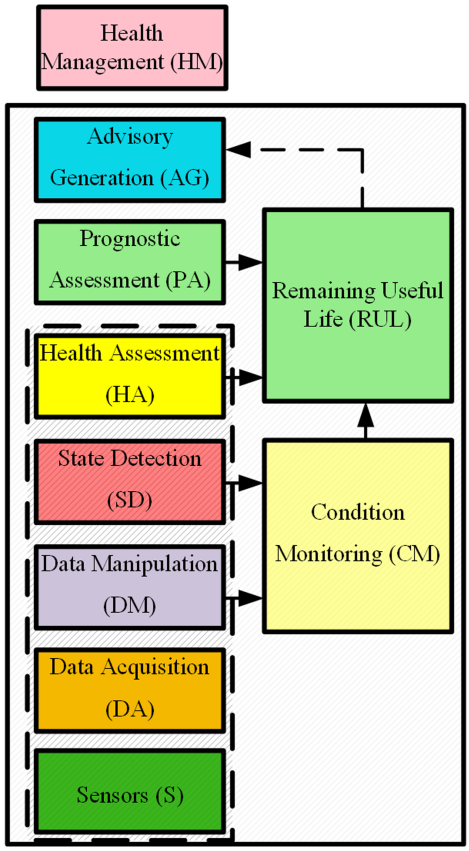

FIGURE 15. PHM functional structure [139].

On the other hand, it has been previously discussed that the integration of prognostic methods and a proactive control strategy constitutes the field of PHM. Through a PHM approach, faults can be detected in their early stages, and their progression can be monitored and predicted, which can significantly facilitate maintenance and asset management. By implementing such an approach, potential faults can be addressed before they escalate, thereby preventing more severe issues and reducing the overall costs of maintenance. There are varying interpretations of the term “prognostics” within the system health management community, including predictive analysis, reliability prediction, damage accumulation prediction, or condition-based prediction [139]. The functional architecture of a PHM system, in accordance with the IEEE std 1856-2017, is depicted in Fig. 15 and is comprised of the following components:

- Sensors (S),
- Data acquisition (DA),
- Data manipulation (DM),
- State detection (SD),
- Health assessment (HA),
- Prognostic assessment (PA),
- Advisory generation (AG),
- Health management (HM).

Sensors (S) are instrumental in converting physical quantities into data, which is then captured and recorded through the

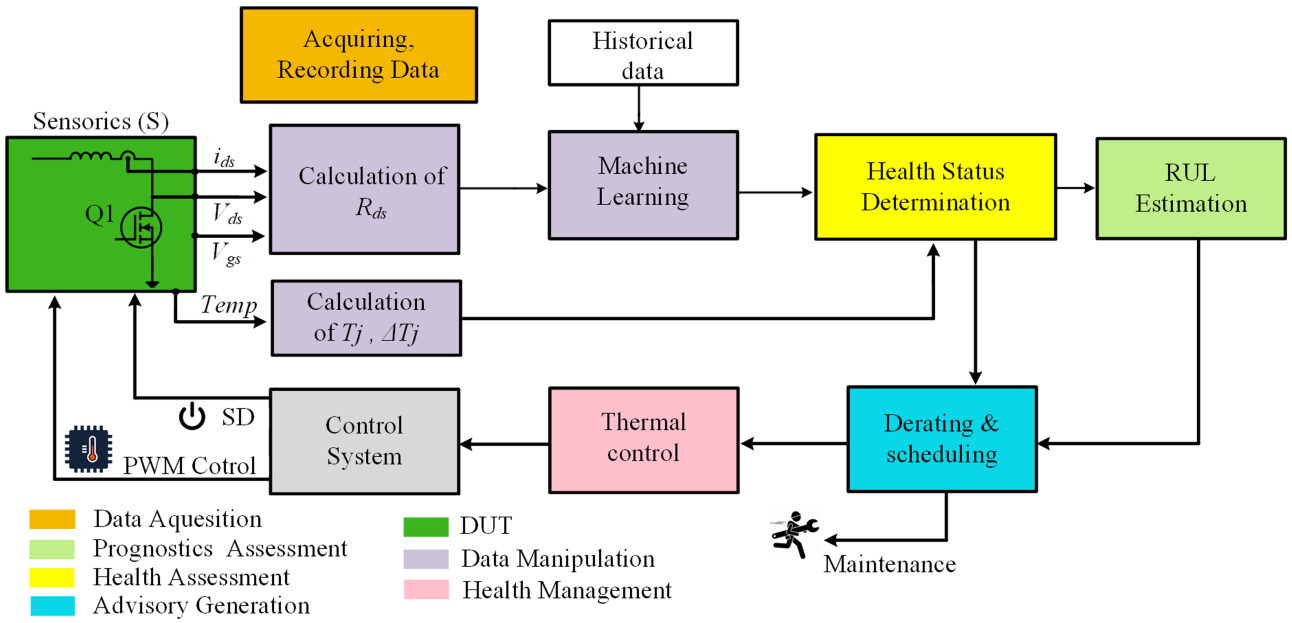

FIGURE 16. One approach for implementing PHM in power electronics converter.

process of data acquisition (DA). The subsequent step of data manipulation (DM) involves the processing of the obtained information by combining it with other sources and prior knowledge. The processed information is then further evaluated through state detection (SD), resulting in the inference of new information about the internal, non-observable state. Health assessment (HA) combines the information acquired from SD to formulate a health indicator state vector for further processing. Typically, functions up to this level comprise a Condition Monitoring (CM) system that provides valuable insights into the overall state of the system. Prognostic assessment (PA) offers a prediction of the future utilization and evolution of the system's health state and/or remaining useful life. Advisory generation (AG) provides action recommendations and information to external systems or operational personnel. Finally, the health management system, comprised of both automatic controls and human operators, provides a means to maintain the system in a healthy state or return it to a healthy state [139].

1) RELATIONS BETWEEN FUSA AND PHM

In order to acquire an accurate prediction of the time to failure of any given PEC or its component, it is important to understand what may cause the damage to it, what are the main stress factors and how this damage will be manifested in the system during its lifetime. To achieve this, right parameters, need to be selected for the monitoring, some parameters may be impossible to monitor directly, thus they need to be estimated. This means that good knowledge of the system and its critical failure mechanisms and modes is needed, in selection of the same. By conducting the functional safety analysis and the FMMEA a list of critical failure mechanism that effect on PEC and its component is obtained. This information may be used in conjunction with Data-driven, PoF, and Hybrid methods to obtain the failure prognosis through PHM program. As it is stated in [263], PHM requires participation from several sub-disciplines including signal processing, fault diagnosis and classification, feature extraction, condition-based maintenance, and fault prognosis. These sub-disciplines are in various stages of development, with some having been extensively researched even prior to the emergence of the PHM concept. Future advancements in the field hold great promise for improving the reliability and maintenance of PECs through both scientific research and standardization, such as the ongoing development of the technical report "ISO/AWI TR9839 Road vehicles- Application of predictive maintenance to hardware with ISO 26262-5."

2) PRACTICAL APPROACH FOR PHM IMPLEMENTATION

An example of PHM implementation for a PEC is shown in Fig. 16. The first step and most challenging step to implementing PHM is the selection of appropriate sensors and Data Acquisition systems (DAQ). The parameters of these systems, such as the sensor bandwidth, high voltage isolation, data transmission cost, and sampling rate, must be optimized to meet the requirements of the models that will use the collected data. The collected data is then processed, which may involve techniques such as filtering, reducing the size of the data set, or removing noise.

Based on the desired level of detail for failure analysis specific dataset is selected. Historical data from similar systems that have undergone ageing or accelerated ageing tests is also used.

A hybrid model between historical data and real-time data is used to estimate the degradation of the device over time. The Health Assessment unit of a PHM system seeks to understand

the degradation process of a device by analyzing degradation trends. Furthermore, as mentioned in Section II, one of the main causes of failure in Si/SiC devices is related to junction temperature and temperature fluctuations. Therefore, this parameter is also monitored in the Health Assessment unit. By trending electrical parameters (e.g., $R_{ds,on}$) and also defining failure criteria, the RUL of the device is forecasted.

This data, along with junction temperature information, is used by the Advisory Generation unit to take actions such as derating or scheduling early maintenance if the degradation process is accelerated. Afterwards, a new operating point voltage, current and temperature reference are generated and commanded to the control unit to reduce the aging of the PEC.

D. LIFETIME IMPROVEMENT METHODOLOGIES

The successful implementation of various emerging technologies, such as renewable energy systems and electric vehicles, depends heavily on the development of techniques that enable semiconductors to withstand the rigorous demands of daily operation while maintaining a consistent and reliable performance over an extended period of time. Controlling junction temperature and reducing thermal stress (i.e., reducing junction temperature swing) are crucial for improving the reliability of the device as it plays an important role in semiconductor degradation. Initially, junction temperature control can be achieved by using cooling systems. However, there are more effective methods for enhancing reliability through careful temperature control without incurring significant costs. These methods for reducing thermal stress can be divided into two categories: package-related approaches and active thermal management.

In terms of package-related approaches, utilizing pressure contact technology and *AlN*-substrate result in higher thermal conductivity, leading to an improvement in lifetime *by a factor of 2* compared to an Al_2O_3 substrate as discussed in [264].

In [265], the combination of pressure contact technology, spring contact, and silver diffusion technology, which eliminates the solder layer from the module architecture leads to enhancement in lifetime.

Another method for reducing thermal stress is active thermal control, which focuses on the concept of de-rating through the alteration and control of electrical parameters such as operating voltage, output power, and switching frequency. This method includes over temperature protection ($T_{j,max}$), decreasing the mean value of temperature ($T_{j,mean}$), and reducing junction temperature swings [12], [13]. However, this approach may affect the cost, control strategy, and efficiency of the converter. The concept of active thermal control can be further divided into various methodologies, as follows:

1) OUTPUT POWER CONTROL

In this methodology, load current is controlled if any undesired temperature fluctuations or temperature rises are detected by a temperature measurement system (e.g., TSEP). The maximum value of the reference current is only limited when the junction temperature or temperature swing exceeds its maximum values, allowing the power electronics converter to operate at its maximum limit without unnecessary performance degradation [93], [266]. Also, in [267], it was proposed that combining maximum power point tracking (MPPT) and absolute active power control could lead to an improvement in the lifetime of photovoltaic inverter systems by reducing thermal loading.

2) SWITCHING FREQUENCY

Another method for controlling T_j and smoothing its fluctuation (i.e., ΔT_j) is by controlling the switching frequency of the converter, as the switching losses are proportional to the switching frequency linearly. In order to control ΔT_j, it is necessary to increase the switching losses when the load decreases, which comes at the cost of efficiency. Power electronics converters are generally designed for high efficiency operation, so this approach has an impact on efficiency and thus there is a trade off between temperature swing control, and efficiency [93], [231], [268], [269], [270], [271]. In wide band gap (WBG) devices, the switching losses are lower than those of Si-based semiconductors, so the reduction in overall efficiency in WBG devices may be less significant [94]. Furthermore, to limit the mean value of T_j it is necessary to decrease the switching frequency [93], [266], [272], [273], [274], [275]. One disadvantage of this method is that the passive components must be designed for the worst-case scenario, leading to an increase in the volume of the converter. Also, in [273], a combination of current limit control and control of the switching frequency was employed to control the junction temperature.

3) TURN OFF TRAJECTORY

In this method, the turn-OFF trajectory is controlled in order to regulate the power losses during the turn-OFF transition and thus the junction temperature swing by using an auxiliary switch. However, this method results in an increase in the total volume and the temperature adjustment range is limited by the dc-link voltage, as this voltage has an impact on the turn-OFF losses [276].

4) GATE-DRIVE

Controlling gate-drive circuits is a prominent method for implementing active thermal control. The objective of this method is to modify conduction and switching power losses through the control of turn ON and turn OFF transitions and also the ON-state voltage of MOSFETs/IGBTs [277]. In [94], a two-step gate-drive circuit for GaN devices was proposed that can control the device slew rate, leading to the regulation of switching losses and conduction losses and the smoothing of thermal cycling. Also, in article [278], another three-level gate drive was proposed to operate the power module in the saturation region, resulting in increased power loss and limiting temperature swing. In [279], [280], [281], [282],

by controlling the gate-drive via adjustable gate voltage, the drain-source resistance can be controlled and the conduction losses profile shaped, which can improve the lifetime of the power MOSFET by a factor of two. However, thermal stability must be considered, which limits the maximum and minimum gate voltage values to prevent thermal runaway that may occur at low gate voltages. Also, in [283], the use of a variable voltage source allows for the manipulation of switching speed and thus the control of switching losses. In [284], a switchable gate resistor network is used to control the turn OFF and turn ON times through a closed-loop thermal control. In [285], Doncker et al. proposed a methodology based on an adaptive gate resistance, while in their other research paper [286], a combination of adaptive gate resistance and switching frequency methods were used to achieve dynamic loss manipulation, with the values chosen based on the average junction temperature estimated through a combination of thermal modeling and sensor data. In [287], the manipulation of both gate voltage and gate resistance is used to control switching losses. By measuring the junction temperature using a sensor and comparing it to a reference temperature, values for the gate voltage and gate resistance can be calculated. Additionally, to eliminate the use of variable voltage sources and resistance networks, a current-source gate drive can be utilized to regulate the gate current during the ON/OFF transition time [288], [289]. This approach requires feedback from a output reference current in order to control the gate current and, in turn, manipulate the switching rise/fall time.

5) MODULATION STRATEGY

In articles [290], [291], [292], series of new space vector modulation for three-level neutral-point-clamped converter were proposed that could relocate thermal loading between the power module used in the inverter in order to balance thermal distribution and control junction temperature. In [290], [291], the authors stated that their proposed methods could achieve uniform thermal distribution among devices, leading to a decrease in temperature swing by 8 K. Additionally, in reference [292], there was a significant reduction in overall loss in stressed devices by 12%. In article [293], a conditioning method was developed for a MOSFET-based interleaved converter through the proposal of active thermal control. In this approach, by measuring the ON-state drain-source resistance, the current reference is adjusted and the thermal stress can be controlled. The findings show that the temperature of the degraded switch can be reduced by 6 K, but at the cost of imposing additional stress on another switch, thereby increasing its temperature by up to 10 K. In [294], the introduction of duty cycle control combined with phase shift modulation is proposed to regulate the junction temperature in a dual active bridge converter, leading to a potential reduction in temperature fluctuation by 50%. During light load conditions, the duty cycle is decreased to boost peak current, whereas during normal operation, the converter operates with minimal losses. In [270], [295], [296], a discontinuous pulse modulation (DPWM) technique was employed to alleviate thermal stress by reducing switching losses, consequently lowering the junction temperature by up to 6 K and extending the lifetime by 56%. In article [297], carrier-based modulation approach was proposed which can reduce the stress of thermally stressed semiconductor devices through the selection of redundant switching states in each switching cycle and the optimization of power losses of the stressed device. In article [298], by changing the control strategy from space-vector-PWM (SVPWM) to DPWM and controlling the switching frequency, the switching losses can be decreased, leading to an increase in lifetime. The paper suggests that implementing the DPWM strategy can decrease junction temperature fluctuations by 11 K and double the lifetime. However, to further enhance lifetime, the switching frequency needs to be lowered, but at the expense of degrading the quality of the current waveform. The switching between these two controllers occurs when the failure precursor (i.e., ON-state drain-source resistance) exceeds the defined value. To regulate the temperature swing, the circulating reactive power between different paralleled power converters is controlled, potentially resulting in the manipulation of thermal distribution among power modules [299]. While temperature swings are reduced by 19 K, there remain questions regarding the applicability of circulating reactive power in meeting grid code requirements and accommodating various wind farm configurations. In ref. [300], the technique involves sensing the junction temperature of the power module and estimating its useful lifetime. Unequal power sharing among paralleled power converters is then implemented to extend the system's lifetime, utilizing a power routing algorithm with an optimization function. Monte Carlo analysis indicates that this strategy can increase the system's lifetime by three years.

6) COOLING SYSTEM

In this approach, temperature is controlled by increasing or decreasing cooling efforts [301], [302], [303], [304]. In ref. [301], a feed-forward open loop controller is utilized to monitor power losses and ambient temperature with enhanced dynamic response, while an additional closed-loop controller is used to control the baseplate temperature. In article [302], a PID compensator is tuned to the thermal impedance of the semiconductor and used to control the blower speed, allowing the generation of output based on power losses without the need for temperature feedback. In article [303], ambient temperature is also taken into account when controlling the cooling power in order to maintain a constant temperature.

VI. GENERIC ACCELERATED LIFETIME TEST

Ensuring the reliability of products and systems is essential for their successful operation and long-term performance. Reliability testing is a crucial process that enables manufacturers to evaluate the dependability and durability of their products through different approaches. One way to classify reliability testing is by considering the nature of the testing approach.

From this perspective, two main categories of testing methods emerge: quantitative and qualitative. Quantitative methods involve the calculation of metrics such as time-to-failure data and degradation curves, which can help demonstrate reliability. In contrast, qualitative methods focus on identifying the weakest points in a design or process by subjecting samples to stress close to their limits and determining destructive limits. Power cycling tests (PCTs) are a type of accelerated aging test that can be both quantitative and qualitative, depending on the specific testing approach used. These tests are performed to evaluate the reliability of semiconductors during operation, as they are capable of simulating long-term reliability in a laboratory setting over several days. These tests can also be used to identify failure mechanisms, modes, and indicators, as well as characterize lifetime models of semiconductors. During PCTs, power losses are controlled dynamically, leading to oscillation in junction temperature (T_j) and the onset of degradation. These tests are also known as active thermal cycling tests. In contrast, passive thermal cycling tests involve changing temperature swings (ΔT_j) to accelerate degradation of semiconductors, typically through the use of a thermal chamber or hot plate. It is important to note that by precisely controlling of $T_{j,mean}$, $T_{j,max}$, and $T_{j,min}$, different types of failure mechanisms can be excited.

Power cycling test methods involve different temperature cycling periods that can range from several seconds (fast cycling) to several minutes (slow cycling). Fast cycling can lead to failures in chip-near interconnections such as bond wires and die attach, while slow cycling can lead to failures in chip-remote interconnections such as DBCs. The former is referred to as PCsec, while the latter is referred to as PCmin [305], [306], [307]. For performing this test, first, it is important to identify the appropriate testbench based on the type of packaging, applications, and expected failure mechanisms. Generally, testbench can be classified as DC and AC power cycling circuits.

In the DC power cycling testbench, as shown in Fig. 17, a defined DC current profile is applied periodically to the DUT. The load current is cyclically varied between a minimum and maximum value, and the pulse ON time (t_{on}) and pulse OFF time (t_{off}) are adjusted, along with cooling system efforts to control the power losses that are primarily conduction losses in this case. This control strategy ultimately aims to adjust the upper and lower limits of the junction temperature. Furthermore, to estimate junction temperature, an auxiliary current source in the milliampere range is used to mitigate the effects of load current on the junction temperature.

It is noteworthy that using pulse current rather than switching DUT ON and OFF via PWM gate pulse may lead to unexpected failure mechanisms within the test time [9], [15], [35], [51], [308]. In addition, to increase the junction temperature, a higher current must be injected into the module, which may overload the bond wires. To address this issue, a new generation of DC power cycling has been proposed that drives the module in saturation mode as an adjustable current source, controlled by adjusting the gate voltage and

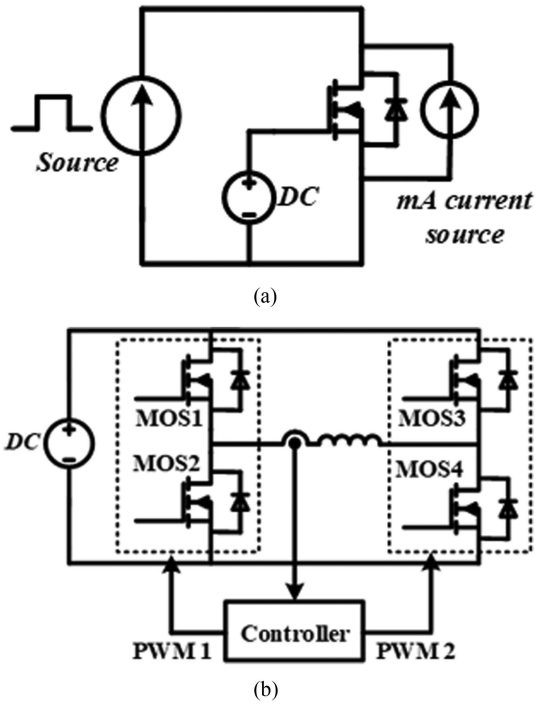

FIGURE 17. Power cycling test bench. (a) DC test set-up and (b) AC test set-up.

DC link voltage [308]. However, this method is not suitable for modules that utilize inner gate drive, and the measurement of failure precursors online is also challenging.

Another form of this test which involves turning the DUT ON and OFF, is the Avalanche test circuit, which considers both switching losses and conduction losses by using an inductive load [309]. Another challenge in DC power cycling is selecting suitable TSEPs to control junction temperature, as these parameters change during the degradation process, necessitating continuous calibration. Furthermore, hardware challenges such as ensuring signal integrity and selecting appropriate switch gate timing, as well as addressing measurement equipment requirements such as delays for voltage and current measurements due to limited sensor bandwidth and concerns related to common-mode noise, remain important considerations [310], [311].

In the AC power cycling test platform, the DUT is repeatedly switched by applying a PWM signal to its gate in a range of a few kilohertz under high voltage stress. The resulting conduction and switching losses elevate the junction temperature to a defined value, causing thermal stress. This test setup can more closely simulate actual operating conditions, but at the cost of increased complexity and expense. One example of a testbench for this test is a back-to-back inverter with an inductive load. This testbench is controlled to result in current circulation between inverters, which minimizes the required input power. However, the control strategy is complex and the body diode failure mechanism may impact the final results [15], [308], [312]. In articles [313], [314], accelerated tests were conducted on motor drives while the drives operated

under nominal load and 50% overload for 57 seconds and 3 seconds, respectively.

The results show that the time to failure depends on the frequency of load changes. Also, this method can rapidly age the DUT, within 15 days. However, due to the presence of highly inductive load (e.g., electrical machine), other factors such as voltage spike may also influence the output results.

A full-bridge inverter with an inductive load is another testbench that can accelerate the failure of semiconductors if the power module only has one leg as shown in Fig. 17 [35]. The PWM signals are used to create a sinusoidal current that circulates between legs, diodes and switches [15], [315]. References [316], [317] report on additional topologies for aging modules based on the required power. Furthermore, in response to the challenges surrounding the long-term reliability of GaN power devices, paper [318] introduced an AC power cycling test. This test has the capability to subject the Device Under Test (DUT) to both hard and soft switching modes, while also providing precise control over power loop inductance to manage overvoltage overshoot.

Notably, variations arise between AC power cycling and DC power cycling outcomes. In DC power cycling, elevating the current is necessary to achieve a specific junction temperature, while in AC power cycling, the contribution of switching losses becomes crucial in raising the junction temperature. The Bayerer model underscores the significance of the current per wire bond in determining the ultimate lifetime of the semiconductor.

Moreover, the control strategy for power cycling tests can be divided into four different methods: constant power ON-time and power OFF-time, constant power loss, constant case temperature swing, and constant junction temperature swing [2], [49], [319], [320]. It is important to note that all of these methods result in a different number of cycles to failure. A constant timing strategy involves the maintenance of a fixed ON-time and OFF-time, which leads to an increase in power loss and temperature oscillation within degradation procedure. The constant power approach involves maintaining a constant power loss, as well as a fixed ON-time and OFF-time, through the control of the current reference or gate voltage. This can compensate for variations in the ON-state voltage of the device under test. However, this approach is less applicable due to its reduction of acceleration influences and increase in the number of cycles to failure. The constant case temperature swing approach involves the maintenance of a constant maximum and minimum temperature of the case through the adjustment of ON-time and OFF-time. The final method, constant ΔT_j, involves the control of the maximum and minimum values of the junction temperature, ON-time, gate voltage, and load current in order to maintain a constant junction temperature swing.

The next step in conducting power cycling is the selection of proposed failure precursors, which can indicate an upcoming failure. The gate threshold voltage, drain-source resistance, collector-to-emitter ON-state voltage, thermal resistance, and gate current are common failure precursors in MOSFETs and IGBTs [235], [308]. Furthermore, aside from power cycling tests, there exist additional testing methods that target specific parts of semiconductors, including passivation layers and gate-oxides. The subsequent section offers a comprehensive examination of these testing approaches in the context of their application to the automotive industry.

VII. AUTOMOTIVE RELIABILITY TESTS

With the increasing complexity and sophistication of automotive systems, reliability testing has become a crucial process for manufacturers seeking to deliver high-performance, dependable products to their customers. While in the past, customers may have been content with warranty options or replacement products, today, the low risk of failure is a highly sought-after quality. As such, it is essential to subject automotive PECs to rigorous testing and stress testing before releasing them to customers, in order to validate their performance and ensure they meet specific requirements for high performance. To attain satisfactory performance of PECs, various reliability testing standards have been established, including the Joint Electron Device Engineering Council (JEDEC), International Electromechanical Commission (IEC), and MIL-HDBK-217F. In addition, the International Automotive Task Force (IATF) and Automotive Electronics Council (AEC) have published guidelines for automotive applications, with the former focusing on quality management system development and the latter aiming to ensure a certain level of reliability and quality. The European Center for Power Electronics (ECPE) has also released the Automotive Power Module Qualification (AQG 324) to cover power semiconductor module qualification.

The reliability tests aim to simulate the actual conditions in which the DUT is expected to operate in the future by applying controlled stress load profiles in a controlled environment. The performance of the DUT can be verified by monitoring key parameters such as thermal impedance, leakage currents, threshold voltages and temperature swings. Generally, the goals of these tests can be summarized as follows:

- Identifying the critical failure mechanisms and ultimate lifetime.
- Verifying product stability, quality, and reliability.
- Identifying the constraints and limits of devices/systems by altering reliability test conditions.

As the adoption of electric vehicles continues to expand, it is imperative to assess the criteria for ensuring the dependability of power electronics modules in the automotive sector. The present testing methodologies have predominantly targeted power electronics converters that are Si/SiC-based, as demonstrated in Table 7, which outlines the requirements specified in AQG324 [321]. On the other hand, to the best of authors knowledge, there are currently no qualification tests specifically for GaN-based power electronics converters in automotive application. Therefore, general tests for GaN HEMTs will be discussed, as shown in Table 8. The descriptions of these tests are provided below.

TABLE 7 Reliability Testing Standard and Detailed Test Condition Description for Si/SiC-Based Semiconductor Technology

Ref article	*Standard*	*Reliability Test*	*Test condition description*
[321], [322]	IEC 60747-15	Determining leakage inductance	Special test set up including two auxiliary switches are needed.
[321], [322]	IEC 60747-15	Determining Thermal Impedance	Junction and case temperature measurements are required. $R_{th} = \frac{T_j - T_c}{P}$.
-	AQG 324	Insulation tests (Insulation resistance)	Test duration (cycles)= 8*h*. Ambient temperature ($T_{ambient}$)=23±5 *°C*. Humidity=90%. Pressure=86-106*kPa*. Drain-source on voltage= 1.5 times of voltage stress in the circuit (at least 500*V*). Failure criteria: Decreasing insulation resistance to lower than 100*MΩ*.
[8], [321], [322]	IEC 60749-25	Thermal Shock	Test duration (cycles)= 1000*h*. -40ºC<$T_{storage\ temp}$<125 ºC. Temperature slope> 1 *K/min* & 6 *K/min*. dwell time > 15 *min*. Failure criteria: Thermal resistance (if the thermal resistance cannot be measured in test setup, DUT can be removed for specific time duration for measurement of the resistance).
[321], [322]	IEC 60068-2-6 IEC 60068-24	Vibration	(In accordance with point of use) Test duration= 22*h* per axis. Sinusoidal sweep. Acceleration= 100-200 $\frac{m}{s^2}$. Vibration frequency range is between 100 *Hz* and 440 *Hz*. It should show weak points in mechanical parts (e.g. case of module).
[321], [322]	IEC 60068-2-27	Mechanical Shock	Peak acceleration= 500 $\frac{m}{s^2}$. Shock duration= 6 *ms*. Shock form: half-sine.
[69], [167], [321], [322], [323]	IEC 60749-34	Power cycling (P_{Cmin} and P_{Csec})	P_{Csec}: On time (when the load is applied) is less than 15 second. Maximum and minimum of gate voltage is +15*V* and -5*V* respectively. P_{Cmin}: On time (when the load is applied) is between 1min and 15min. Maximum and minimum of gate voltage is +15*V* and -5*V* respectively. The target is calculating lifetime curve. Failure criteria: Increase in thermal resistance, on-state resistance, gate leakage current.
[8], [321], [322]	IEC 60749-6	High temperature storage	Test duration= 1000*h*. Ambient temperature ≥ 125 *ºC*. Note: The DUTs must be fully functional after the test.
[8], [321], [322]	JESD22-A119	Low temperature storage	Test duration= 1000*h*. Ambient temperature < -40 *ºC*. Note: The DUTs must be fully functional after the test.
[324], [325], [326], [327], [328], [329]	IEC 60747-8 IEC 60749-23	High-temperature Gate Bias / High Temperature Gate Switching	Test duration= 1000*h*. Drain-source on voltage= 0*V*. Maximum and Minimum of gate voltage= based on datasheet. Duty cycle and Frequency= Not defined explicitly. Ambient temperature= 150*ºC* / T_j maximum. Failure criteria: Gate-source leakage current, Threshold voltage.
[324], [325], [330]	IEC 60747-8 IEC 60749-23	High Temperature Reverse Bias	Test duration= 1000*h*. Ambient temperature =150*ºC* / *Tj* maximum. Drain-source ON voltage= 0.8-1 of $V_{ds,max.}$ Gate Voltage (V_{gs})= 0*V*. Failure criteria: Drain-source leakage current.
[331], [332], [333]	IEC 60068-2-67	High-humidity high-temperature reverse bias (H^3TRB)	Test duration= 1000*h*. Relative humidity= 85%. Drain-source on voltage = 0.8-1 of $V_{ds,max}$. Temperature= 85*ºC*. V_{gs}= 0*V*. Failure criteria: The drain-source leakage current.

TABLE 8 **Reliability Testing Standard and Detailed Test Condition Description for GaN-Based Semiconductor Technology**

Ref article	*Standard*	*Reliability Test*	*Test condition description*
[334], [335]	JEP180 JEP182	Switching accelerate lifetime test (SALT)	Test duration= 1000h. Voltage and Current= based on nominal power. In this test, lifetime wear-out model will be calculated. Test vehicle= boost converter (based on JEP182 and application, other topologies can be selected). Failure criteria: Change in efficiency, dynamic $R_{DS(ON)}$, $R_{DS(ON)}$, occurrence of short circuit, occurrence of open circuit, gate leakage current, drain leakage current.
[335]	JEP180 JEP182	Dynamic High-Temperature Operating-Life (DHTOL)	Test duration= 1000h. T_j= Maximum allowed temperature. Drain-source voltage= 0.8 of $V_{ds,max}$. Drain-source current= based on maximum power (mission profile). F_{sw}= Maximum allowable based on maximum allowed junction temperature.
[336], [337], [338]	JESD22A108	High-temperature reverse bias test (HTRB)	Test duration= 1000h. Ambient temperature ($T_{ambient}$)= 150^oC. Drain-source voltage= $V_{ds,max}$. V_{gs}= 0V. Failure criteria: leakage currents, $R_{ds,on}$, V_{th}.
[336], [337], [338]	JESD22A108	High-temperature gate bias test (HTGB)	Test duration= 1000h. Ambient temperature= 150^oC. Drain-source voltage= 0V. V_{gs}=6V. Failure criteria: leakage currents, V_{th}.
[157]	JEP122	Time Dependent Breakdown Failure Test (TDBF)	Test duration= 1000h. Ambient temperature= 25^oC. Drain=float, Source= GND. V_{gs}= 7~9V. Failure criteria: gate leakage current.
[339], [340]	JESD22A104 AEC – Q101	Temperature Cycling IOL	Test duration= 1000 cycles. 2 cycles/hour. -40^oC<$T_{storage\ temp}$<125^oC. Temperature slope> 6 K/min & 1 K/min. dwell time < 15min. Failure criteria: Thermal resistance, leakage currents, $R_{ds,on}$. Test duration= 15000 cycles. T_{cycle}= 4min (typical). ΔT_j =100^oC. Failure criteria: Thermal resistance, $R_{ds,on}$.

A. MODULE CHARACTERIZATION TESTING

To verify the parameters listed in the datasheet for semiconductors, it is necessary to characterize modules and conduct subsequent environmental and lifetime testing. This testing includes determining the parasitic inductance of semiconductors based on IEC 60747-15, determining the thermal resistance characteristics based on IEC 60747-15, evaluating the short circuit capability, and performing insulation tests.

B. ENVIRONMENTAL TESTING (THERMAL/MECHANICAL SHOCK AND VIBRATION TESTS)

From the perspective of environmental stress, there are both wear-out stresses and overstresses (shocks) caused by mechanical loads in addition to those caused by humidity, moisture, and contaminants. As power electronics converters in some applications, like electric vehicles, often encounter harsh environmental conditions, environmental stresses can have significant impacts on the overall health of the devices. This highlights the importance of considering the effects of these stresses. This test is designed to simulate the environmental and weather conditions that a vehicle is exposed to. Generally, this test is divided into three sub-tests. In the first test (i.e., the thermal shock test), the temperature is changed using a passive method such as a thermal chamber, in order to evaluate the resistance of the DUT to the stress caused by temperature changes between layers with different thermal expansion coefficients. In the vibration test, a vibration profile similar to what a vehicle experiences during driving is used to examine the functionality of the mechanical components of power electronics modules in automotive applications. Finally, in the mechanical shock test, a mechanical profile based on accidents or driving over curbs is applied.

C. SIC RELATED TESTING

The subsequent section is dedicated to specific tests aimed at obtaining a more profound understanding of the long-term reliability limitations of SiC MOSFETs. These tests subject the semiconductors to exaggerated temperature, voltage, and current stresses. The outcomes derived from these tests can subsequently be extrapolated to real-world conditions to estimate the device's operational lifetime. he parameters defined are centered around MOSFETs, but the tests could be relevant for other transistors like IGBTs. The most prevalent reliability tests include:

1) LIFETIME TESTING (PC_{MIN} AND PC_{SEC} FUNCTIONALITY)

This test aims to identify degradation of bond wire and solder joint within the package. This test method can be divided into two groups: AC power cycling test and DC power cycling test. In the former, both switching and conduction losses contribute to degradation, while in the latter only conduction losses lead to degradation. In other words, during these tests, the DUT is heated by passing current through its junction and cooled by turning OFF the current and activating an external cooling system. Power cycling standards generally distinguish between tests with short heating times (PC_{sec}), where the load current ON time is less than 15 seconds, and long heating times (PC_{min}). It is noteworthy that PC_{sec} applies thermo-mechanical stress to chip-near interconnections (e.g., die attach), while PC_{min} test applies stress to chip-remote interconnections (e.g., system soldering).

2) HIGH-LOW-TEMPERATURE STORAGE

Exposure to high or low temperatures can have significant effects on power modules. The purpose of this test, which subjects a semiconductor to extreme temperatures, is to evaluate or determine the effect of storage or transport at high or low temperatures on the semiconductor, which may result in cracks or fractures.

3) HIGH TEMPERATURE GATE BIAS (HTGB)/HIGH TEMPERATURE GATE SWITCHING (HTGS)

HTGB aims to evaluate how electrical and thermal loads impact MOSFETs, focusing on accelerating time-dependent dielectric breakdown, gate insulator degradation, and changes in Miller capacitance. The goal is to understand the degradation of gate oxide in MOSFETs under high-temperature conditions and maximum nominal gate voltage. Unlike HTGB testing, which applies a constant dc voltage to the gate, HTGS involves dynamic gate voltage switching. HTGS better simulates real-world conditions, resulting in less shift in gate threshold voltage compared to HTGB testing.

4) HIGH-TEMPERATURE REVERSE BIAS (HTRB)

This test aims to determine the long-term effectiveness of the package and chip passivation layer. This is significant because the manufacturing process for the module, as well as the varying thermal expansion coefficients of the utilized materials, may potentially affect the qualification of the passivation layer.

5) HIGH-HUMIDITY HIGH TEMPERATURE REVERSE BIAS (H^3TRB)

Many power electronics modules have chips that are embedded in silicone gel to provide dielectric insulation. These modules are not hermetically sealed, so moisture and contaminants can gradually reach the layers, which are especially harmful to plastic-packaged power devices. Thermo-mechanical stress and the different thermal expansion coefficients of the materials can reduce protection against external contaminants and lead to chemical corrosion. This test aims to investigate the effect of load on the passivation layer and the chip edge termination in the presence of humidity.

D. GAN-RELATED TESTING

Due to the unique materials and structures of GaN HEMTs compared to Si/SiC MOSFETs, traditional tests for Si or SiC reliability assessment are not applicable. For example, hot carrier injection and unclamped inductive switching tests rely on body contact and avalanche breakdown, but these are not possible or would damage the GaN switch because of the presence of an electrically blocking buffer. Therefore, it is necessary to identify new reliability tests specifically for GaN. One known failure mechanism in GaN HEMTs is hot carrier degradation that results in electron trapping and wear-out which is often attributed to hard-switching conditions. Thus, it is important to evaluate the reliability of GaN under switching conditions. The JEP180 and JEP180 standards suggest two methods for this purpose: the "Switching Accelerated Life Test" and the "Dynamic High-Temperature Operating-Life Test" [160]. Additionally, HTRB, H^3TRB and HTGB tests may be valid for GaN HEMTs, but the test conditions will need to be modified.

1) SWITCHING ACCELERATED LIFETIME TEST (SALT)

As mentioned previously, JEP180 and JEP182 provide methods for estimating the switching reliability of GaN devices. By extracting a switching lifetime model based on these methods, it is possible to calculate the MTTF of GaN devices. Achieving an appropriate MTTF through testing ensures that wear-out failure resulting from hard switching (e.g., hot electron injection) will not occur during normal operation and damage the semiconductors [334], [335].

2) DYNAMIC HIGH-TEMPERATURE OPERATING-LIFE (DHTOL)

This evaluation aims to gauge the durability of the GaN device when operating in conjunction with other dies in the package and other components in the power electronics converter. The objective is not to deliberately induce wear-out failures, but rather to identify any failures that may occur within the testing period and to assess the robustness of the device's interactions with other parts. Additionally, the efficiency of the device can

be calculated and checked for notable changes, and the test can offer insight into the reliable drain-source resistance and smooth switching transition without any shoot-through effects [335].

3) HTRB, HTGB,H³TRB, AND TDBF

The HTRB test, similar to the corresponding test for SiC devices, is designed to evaluate the effect of the maximum nominal drain-source voltage on the device. Also, the HTGB and H^3TRB tests have similar aims as those for SiC [336], [337], [338]. Additionally, the Time Dependent Breakdown Failure (TDBF) Test is another chip-level test that is less well known, but it focuses on evaluating gate insulation failure by applying a high gate-source voltage [157].

4) INTERMITTENT OPERATIONAL LIFE (IOL) AND THERMAL CYCLING

The power device in the IOL experiment is subjected to temperature fluctuations by turning the DC power supply ON and OFF to regulate the junction temperature. On the other hand, the thermal cycling test involves exposing the device to an external heat source to induce thermal cycling. The objectives of both tests are to evaluate the degree of thermal stress on the solder joints. Although the thermal cycling test subjects the solder joints to more significant stress than the IOL test, the degradation process speed is faster in the latter [339], [340].

VIII. FUTURE TRENDS

Although WBG (i.e., SiC, GaN and beyond) possess advantageous characteristics such as reduced size, higher efficiency and elevated thermal conductivity, their adoption in the power electronics market has been limited to a 1% share due to their less mature technology, robustness and long-term reliability issues compared to Si-based semiconductors [341]. Additionally, meeting customer expectations for low risk of failure, and market return rates in parts per million present ongoing challenges that require continuous improvement in the coming years. It is important to note that the advantageous characteristics of WBG make these devices suitable candidates for electro-mobility and renewable applications, provided that their defects can be adequately addressed. Therefore, in order to align reliability improvement efforts for WBG-based PECs with future demand, a comprehensive roadmap is necessary [342]. Table 9 summarizes the anticipated trends and requirements for addressing future reliability issues.

The first priority in this roadmap should be given to semiconductor packages, which are crucial for effective thermal management and improved electrical characteristics. Without new packaging techniques, it will be difficult to capitalize on the advancement in semiconductor materials and their properties. Hence, it is important to consider material improvements such as substances and substrate layers with higher thermal conductivity and new materials and bonding technologies that can withstand continuous power cycling. Additionally, WBG industries must establish a stable supply chain in wafer fabrication to meet the growing demand.

In order to decrease the size of converters through increased switching frequency, which is one of the advantages of using WBG devices, and to enhance the thermal stability of semiconductors, it is necessary to develop passive elements with new materials that can withstand high temperatures and switching frequencies. Carbon nanotube windings, ceramic capacitors with high-temperature stability, and improved dielectric and magnetic materials for storing more energy are potential candidates for future use.

As the switching frequency and power density of the PECs increase, there will be a greater need for more advanced control methods to achieve higher efficiencies, as more switching events create higher losses. Therefore, the low-level PWM controller must be carefully analyzed and reflected. The control systems need to focus on allowing performances and loads close to the boundary conditions and less oversizing will be required. The result is that both resources and power will be used more effectively. However, at the same time it is essential to maintain the performance and guarantee the safety over the system lifetime. Therefore, the control needs to be more accurate. The advanced control methods are expected to boost the drive system performance limits within maximum thermal constraints enabling maximum system efficiency. While new materials and packaging technologies are necessary for operation in high-temperature conditions, system-based active thermal management can be an effective means of cooling. Moreover, improved control software, with the potential for reduced hardware costs, is a crucial factor in distinguishing high-quality products. As WBGs are expected to operate at higher switching frequencies and powers, on one hand, a more adaptive and predictive low-level control system is required that will also enable rapid loss optimization (trade-offs for the inverter and motor losses). On the other hand, an advanced and powerful edge/cloud system is needed that will enable data analytics and machine-learning-based self-learning and self-calibration, allowing PECs to adapt the performance and thermal responses based on critical real-life mission profiles. Besides, sending all device-generated high-frequency data from a PEC to the cloud can cause bandwidth and latency issues. Edge computing brings enterprise applications closer to data sources such as IoT devices or local edge servers. Similar to generic edge computing, creating the trends is Cloud/Edge AI stack to improve efficiency, speed and latency, avoiding the need to send the high-volume and high-frequency data generated in the PEC to the cloud and rather do (pre-)processing in the edge node.

The implementation of PHM should be the next priority in this roadmap, as it is crucial for the development of future EV and renewable applications. While PHM is well-established in mechanical systems, it is still an emerging technology in PEC applications. PHM typically involves data acquisition and data wrangling through advanced sensorics and multi-core microprocessors, health and prognostic assessment, fault detection

TABLE 9 Road Map of PECs Reliability [342]

Challenges	Short-Term	Medium-Term	Long-Term
Packaging Technology	• Robust interconnect and joining technologies. Robust to wide and rapid temperature cycling via improving manufacturing process.	• Robust to temperature 250°C and wide and rapid temperature cycling via improving manufacturing process.	• Robust to temperature above 250°C and wide and rapid temperature cycling via improving manufacturing process.
Materials / Device	• NA	• WBG devices operate above 250°C • Integrated Multi-role sensors for health monitoring.	• Utilizing new materials with new features like enhanced thermal conductivity, electron velocity, etc.
Passive Components	• Temperature operation up to 200°C • Inductors with energy density above $0.01\frac{J}{cm^3}$ via improving thermal management. • Capacitors with higher frequency for temperature above 125°C.	• Robust dielectric and magnetic substance to temperature above 250°C.	• Temperature operation above 250°C.
Monitoring technology and thermal management	• Temperature within package estimation. • Active thermal management.	• Condition monitoring of electrical and mechanical changes (e.g., thermal resistance, displacement).	• Re-scalable cooling to achieve at least 10 times more cooling power than today's solution.
Control Software	• Managing temperature and power via adaptive modulation strategy.	• Control algorithms for changing operation conditions and load.	• Fault-tolerant predictive control algorithms to enables rapid losses optimization and fail-safe mode operation.
Reliability assessment and PHM implementation	• Gaining knowledge regarding failure mechanism, degradation process. • Condition monitoring of semiconductors and capacitors • Developing PoF models for WBG • Characterize degradation procedure in PEC. • Developing accelerated aging tests. • Design for reliability via lifetime prediction.	• Online lifetime estimation and health management. • Utilizing Machin learning approach for prognostics. • Fault tolerant mechanism. • Developing accelerated aging tests for new packages.. • Cloud based system level multi-physics models to enable faster collaboration across industry (and between organizations not co-located). • Multi-domain virtual prototyping environment (electrical, thermal, mechanical, reliability).	• Edge computing platform with AI based algorithm to improve data latency, efficiency and bandwidth. • Holistic, through-life predictive design tools with <1% margin of error. • Tools for multi-domain, multi-time-scale rapid design optimization.

and isolation, remaining useful life estimation, advisory generation, and health management [139], [343]. The first step to implementing PHM is to focus on identifying and analyzing the FMME, especially for the WBG devices, which are still under reliability investigation. The next step, after gaining an understanding of FMME, is to perform accurate multi-domain modeling of the PEC, which is a medium-term goal.

This modeling is linked to experimental results obtained from appropriate accelerated aging tests, including device and package aging tests. It is noteworthy that as new device and packaging technologies are introduced, these accelerated aging tests will continue to be developed. A key milestone in the roadmap is the online estimation of the lifetime and health status of PECs through the PHM program. While a significant number of research papers on prognosis in PECs have been published, important topics such as noise removal, data wrangling, the development of artificial intelligence (AI) models, Internet of Things (IoT) connectivity, edge and cloud connectivity, and cybersecurity still require further attention. Many industries are taking proactive steps to control degrading faults using predictive maintenance. Thus, it looks promising that the approaches will be considered in the next edition of ISO 26262. Finally, while fault tolerant systems are not currently a requirement for power electronics converters in EVs, like in aerospace applications, they are anticipated as critical factors for ensuring system health management and safety in the future. Furthermore, it is worth noting that sensors are identified as key components in these systems and need to be tolerant to temperature while maintaining accurate and precise outputs.

Based on the information gathered from reviewing papers and considering the vast scope of the reliability research area, this paper presents challenges and recommendations for future work as follows:

- The prognostics approach for lifetime calculation necessitates historical data from accelerated aging tests

or previous data from identical systems under similar conditions. However, it's important to note that accelerated aging tests exaggerate operating conditions and only account for limited failure mechanisms. On the other hand, real-world conditions involve multiple loads and failure mechanisms. Additionally, discrepancies between components, even if mass-produced by the same manufacturer, can invalidate old system data for new systems. Anomalies in the data can also impact the healthy baseline, potentially leading to overlooked upcoming failures.

- Many of the lifetime models used for SiC MOSFETs were originally developed for Si semiconductors. To obtain accurate lifetime estimation for SiC MOSFETs, it is essential to consider the dominant failure mechanisms specific to these devices and develop new lifetime models accordingly.
- Developing lifetime models for GaN HEMTs is crucial, as wire bond fatigue is not a significant issue for these devices, and existing Si-based models are not applicable. Additionally, the unique failure mechanisms of GaN HEMTs produced by different companies using different technologies cannot be considered.
- Most research papers measure failure indicators in controlled laboratory environments. Accurately measuring signals in noisy field conditions requires reliable and precise sensors. Additionally, measuring dynamic parameters during turn ON/OFF transitions necessitates high bandwidth (i.e., 100 MHz) equipment, exacerbating measurement challenges.
- An additional challenge is effectively processing and storing data generated by edge devices and the cloud. PECs, composed of transistors, diodes, inductors, and capacitors, often produce large volumes of data requiring resource-intensive data-driven approaches for analysis. Addressing these challenges requires ongoing research in areas such as data engineering, the Internet of Things, MLOps, cybersecurity threats and PEC's resilience against cyber-attacks.
- In the context of standardization, it is important to establish universal, interoperable, and semantic data models to assess and evaluate design for reliability, condition monitoring, and PHM in PECs. These standards should facilitate the coordinated operation of different systems from different vendors, enable comparative analysis by setting quality performance metrics, and drive continuous development in the field.

IX. CONCLUSION

While power electronics technologies have significant advances in recent years, reliability remains a critical concern. Despite the advancements in PE devices, their failure rates can still range from 1% to 10%, depending on the application and device type, and these failures can lead to costly downtime grid instability, and safety hazards, posing significant challenges to the reliable operation. Therefore, reliability has emerged as the main focus point within the power electronics community, drawing considerable attention from researchers, suppliers and manufacturers.

This literature review aims to provide a comprehensive summary of recent advancements in reliability research, encompassing methods for predicting and prolonging the lifetime of power electronics components. The review investigates various aspects including failure mechanisms, failure identifiers, and models for estimating the lifetime of semiconductors and different types of capacitors. Additionally, it clarifies fundamental reliability terms and metrics. To integrate reliability considerations into the design phase, the review discusses stepwise, mission profile-oriented lifetime estimation, and offers two different use cases for automotive and charging applications. Furthermore, effective implementation of condition and health monitoring in power electronic converters necessitates a thorough understanding of junction temperature estimation methods. Junction temperature variation, a primary contributor to semiconductor failures, has garnered significant research attention.

Furthermore, adopting active thermal management strategies is advised to enhance device/system longevity under real-world operating conditions. This paper provides a comprehensive overview of various thermal management techniques, despite their feasibility. In addition, conducting Prognostics Health Management analysis and Functional Safety assessments is essential for identifying potential faults or failures in PEC systems and their components over their lifetime. This article describes the necessary procedures for these evaluations, focusing particularly on the automotive sector, and includes a practical example.

A crucial section of this review paper delves into reliability tests of emerging wide band gap materials, i.e., SiC and GaN, encompassing both package-level and chip-level tests. Despite the promise of WBG materials, their reliability still lags behind that of Si-based devices. This highlights the pressing need to conduct standardized tests for both package-level and chip-level failure analysis. Package-level tests primarily focus on assessing reliability through power cycling and thermal cycling. On the other hand, chip-level tests encompass a range of methodologies such as HTGB, HTRB, and H^3TRB tests. These tests are essential for comprehensively evaluating the reliability and durability of WBG materials, paving the way for their wider adoption in various applications.

Lastly, the review sheds light on future reliability trends, serving as a guide for future research endeavors.

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