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Review of Active Thermal Control for Power Electronics: Potentials, Limitations, and Future Trends

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ABSTRACT The main factor that drives the aging of power semiconductor modules is the thermally induced stress caused by the maximum temperature and temperature swings. This thermally induced stress is usually counteracted in passive designs with oversizing of components, which brings additional cost to the system. This is a major limitation of future power electronic systems that are required to be more reliable with reasonable cost and for many applications to be lighter and smaller. Active thermal control (ATC) is a possibility to reduce the thermal stress of components during real-time operation without the need to modify the expensive converter power stage. Many studies have shown the potential of ATC to not only extend the lifetime of power converters because of the reduced stress, but also to increase the converter devices utilization by pushing them into their thermal limits with proper control. This makes ATC an appealing way to realize the contradicting reliability, cost, and power density requirements. This paper provides an overview of the benefits and objectives, structure, and implementation possibilities of ATC. It also provides and overview of the limitations and disadvantages of many ATC strategies. Based on this discussion, it highlights key issues that must be addressed by future research. Among them is minimizing the impact of different ATC strategies on the power losses, operational cost, and output voltage and current quality.

INDEX TERMS Active thermal control, junction temperature control, reliability enhancement, power electronics, semiconductor device lifetime.

I. INTRODUCTION

Power electronics are a key enabling technology in a wide range of applications including electric drives, electric vehicles, renewable energy, microgrids, and smart transformers. A common requirement for power electronics in these applications is that they should be as reliable as needed to the lowest cost, and for some applications the power density is also among the top priorities [1], [2].

Reliability is defined as the ability of a component or system to perform its intended function without failure over a given period of time. For power electronic systems, there are various components that are susceptible to different failure modes and failure mechanisms [2]. Identifying the weakest components, the dominant stressors, and understanding their failure mechanisms is the first step to address the reliability challenge in the above-mentioned applications. According to recent studies [1], [3] and industrial surveys [4], the power semiconductors were rated as one of the most component prone to failure in the power electronic system. Moreover, the temperature-related stressor comprising high temperature and temperature swing are identified as the main critical stressor for this component.

A typical structure of an IGBT power module is shown in Fig. 1 [5]. Apparently, it consists of different materials, were each is characterized by different coefficient of thermal expansion (CTE). When exposed to temperature swings, the power module experience thermal cycles which create mechanical stresses at different locations within the module.

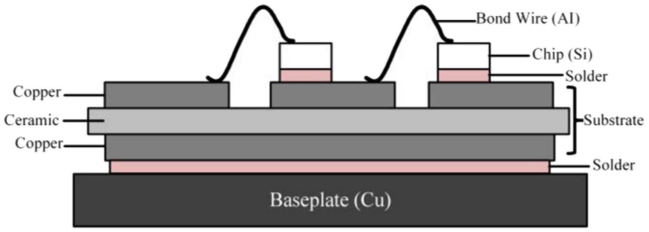

FIGURE 1. Typical IGBT power module structure [5].

This is especially true for the interfaces between dissimilar materials, i.e., bond wires and solder layers, due to the large CTE mismatch between the aluminum bond wire and the silicon chips, and between the substrate and the silicon chips. For frequent repetition of thermal cycles, the resulting stress causes fatigue and eventually the power module is destructed by bond wire lift-off or breaking of the solder joints, which are the main wear-out failure mechanisms. Unfortunately, the variable mission profile (i.e., operating conditions) in all the above mentioned applications is directly reflected by loading variations in the power converter, which result in complicated thermal cycling that can quickly trigger the failure of the modules [6], [7].

Common approaches for improving the reliability of power modules are an overrating of components (e.g., current rating or cooling system) or an improved design with increased packaging robustness. For instance, replacing the aluminum wire bonding with multiple copper posts and the common SnPb and SnAgCu solder alloys with silver sintering for chip attachment have shown better thermal conductivity and enhanced reliability [8]. However, these solutions usually accompanied with increased complexity and cost [9]. Hence, to mitigate overdesign and cost increase while still meeting the reliability targets, an enhancement approaches in the design and control domain are presented. In the design stage, a design for reliability (DFR) approach is proposed. In this approach, the lifetime of power electronic systems is estimated considering real mission profiles, and specific lifetime models for failure mechanisms induced by certain stressor (e.g., temperature-related stressor). Consequently, if the lifetime under specific design does not meet the application requirements, new component or packaging is considered. Then, the process is repeated until the targeted lifetime is achieved [10], [11]. However, the problem is that the actual mission profile is different from the mission profile used in the lifetime analysis. This is a challenge for the DFR approaches. Even for a specific application with anticipated mission profile (e.g., PV applications based on the local solar irradiance and ambient temperature), a design with minimum oversizing and minimum cost is difficult to be achieved. For example, a PV inverter designed for hot climate conditions (high average solar irradiance and high ambient temperature) is considered as overdesign for installation sites with cold climates, and vice versa. Moreover, considering a different inverter design for each site is impractical in terms of cost [12]. Therefore, a methodology to reduce the thermal stress during real time operation is of high importance to achieve the desired reliability without relying much on overdesign.

In recent years, active thermal control (ATC) strategies are proposed, which aims to influence the thermal stress of converter devices during real-time operation. As shown in (1), the junction temperature of the device depends on the power losses P_{Loss} and the cooling system temperature T_c. Therefore, by controlling either the loss related variables (e.g., the switching frequency [13], [14] and/ or current limit [15]) or the convection capability of the cooling medium [16], the junction temperature can be influenced. In ATC these control freedoms are exploited to realize different objectives, such as thermal cycling reduction and thermal overload prevention while pushing the device into higher current limits. A reduction of the power losses, for example, during high loading conditions implies a reduction in the peak junction temperature and consequently on the thermal cycle amplitude. Because the thermal stress is the life limiting factor for power modules and the main reason for oversizing of components, a realization of such objectives can improve the reliability or, alternatively, the power density without jeopardizing reliability.

$$T_j = T_c + (Z_{th}) * P_{Loss} \tag{1}$$

There are many control freedoms to manipulate the losses and loading of converters. For instance, on the device level, the gate resistance has almost linear relationship with the switching losses and thus can be used as a manipulated variable [17]. On the converter level, the switching frequency is one control possibility [14], while on the system level (e.g., between parallel connected converters) the real and reactive power reference among the converters can also be utilized [18], [19]. This wide variety of control freedoms, which can be utilized by ATC strategies with only software modifications or sometimes with only modifications to the control circuit (e.g., gate resistance control), makes ATC an appealing way to realize the contradicting reliability, cost, and power density requirements. However, despite all the benefits, ATC techniques still need to overcome several limitations in order to became visible in the future.

Remarkably, the determination of the junction temperature is the first step to realize an ATC. However, the junction temperature is normally hard to access and difficult to measure during real-time operation [7]. This calls for indirect temperature sensing methods, like temperature sensitive electrical parameter (TSEP) [20], thermal predictors [21] or thermal observers [22]. However, they still have to overcome their own limitations, which will be discussed throughout this article. In general, the extraction of junction temperature information with zero phase lag, high accuracy, and high bandwidth to track the fast dynamic behavior of the junction temperature is a big challenge, especially for those applications aiming to operate the devices near the thermal limits. Another challenge lies on mitigating the adverse impact of many ATC strategies on the system performance. For instance, employing an ATC that decreases the switching frequency during

high load conditions implies an increase of the current total harmonic distortion (THD) [13]. For many applications, like grid-connected applications, this could be seen as a great limitation considering the strict requirement on the THD at the point of common coupling (i.e., less than 5 % [23]). Therefore, ATC strategies shall address these limitations exclusively. The impact of different ATC strategies on the system performance will be the main challenge discussed in this article as it has not been comprehensively addressed by previous review articles on ATC [7], [24], [25], [26], [27].

This paper presents a comprehensive review of the state-of-the-art active thermal control for power semiconductors in power electronic systems. Its structure, and implementation possibilities on the device, converter, and system level is summarized. It also discusses the limitations and disadvantages of different ATC strategies. Accordingly, it identifies the different issues that must addressed by future research. Furthermore, the benefits of ATC for different converter structures are also discussed. The rest of this article is organized as follows. Section II provide an overview of the benefits and objectives of ATC in different applications and converter structures. In Section III, the general control structure of ATC and the thermal state variable extraction methods are presented. Section IV summarize the different implementation possibilities of ATC. Then, the challenges and the required future work in the field of ATC is given in Section V. Finally, Section VI concludes the paper.

II. BENEFITS AND OBJECTIVES OF ACTIVE THERMAL CONTROL

Active thermal control (ATC) strategy act during normal operation of the system. It uses temperature related variables to influence the junction temperature online [4]. The ATC has mainly four objectives. First, thermal cycling reduction. Second, maximizing thermal capacity of the power converters. Third, thermal stress balancing. Finally, thermal stress redistribution [28], [24]. The next subsections provide a brief description of how these objectives can meet different application requirements in terms of cost, power density, and reliability.

A. THERMAL CYCLING REDUCTION

The power devices have two types of losses, which are the switching and conduction losses. Both depends on the junction temperature of the device. If the converter operating conditions varies, the device losses will also vary leading to fluctuating temperature as shown in Fig. 2 [29]. Consequently, if the losses were reduced during high load operation, both the mean junction temperature and temperature peak value will be reduced leading to smoother junction temperature variation. Similarly, a smoother junction temperature can be obtained by increasing the losses during low load conditions [30]. Although, the mean junction temperature will be increased in this case, the lifetime of the power device will be improved because of the much higher effect of ΔT_j on the lifetime of the power devices [31].

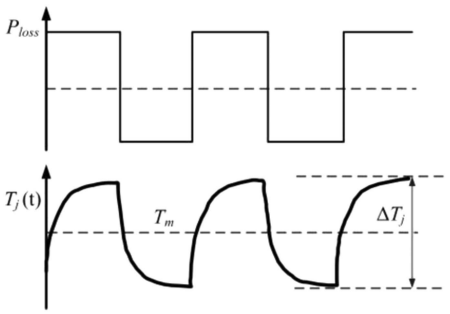

FIGURE 2. Typical junction temperature profile variation with load variation [29].

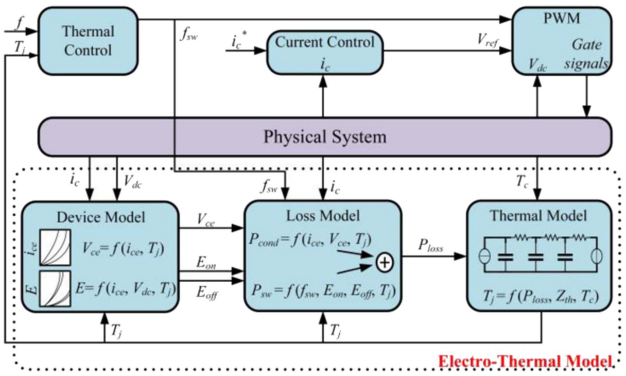

FIGURE 3. Possible structure of ATC using the switching frequency [21].

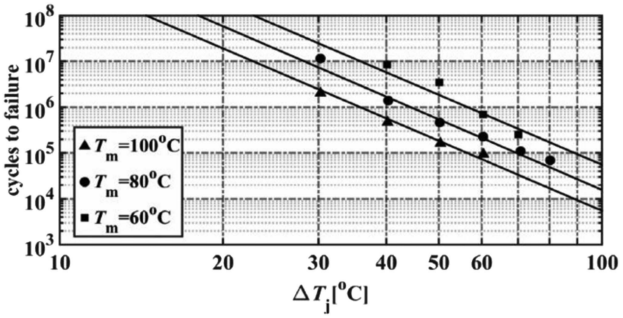

FIGURE 4. Number of cycles to failure of an IGBT module as a function of T_m and ΔT_j [33].

A possible structure of an ATC using the switching frequency as a loss related variable is shown in Fig. 3. The electro-thermal model, which links the device losses to the thermal behavior, is used to estimate the junction temperature. Afterwards, the junction temperature is given to the thermal controller which varies the switching frequency, and consequently the device switching loss, in order to achieve the desired control target [7].

The number of cycles to failure of an IGBT module as a function of the mean junction temperature T_m and junction temperature swing ΔT_j is shown in Fig. 4. This graph indicates clearly how a reduction of the temperature swing can improve the lifetime of the power module. The number of

cycles to failure nearly doubles for every 10 °C reduction of the temperature swing. Therefore, an ATC technique that can provide a large loss manipulation range within the system constraints is an effective mean to improve the lifetime of power modules. For instance, the switching loss accounts for the larger proportion of the total losses in high power IGBT modules [32]. Therefore, varying the switching frequency, for example, which has almost linear relationship with the switching loss can be useful. An ATC using the switching frequency has shown the capability to improve the lifetime of 1.2 MW two-level wind power converter in Malin Head, Ireland from 3.35 years to 9.77 years [33]. This implies a reduction in the maintenance cost, which is especially important, for example, in offshore wind power applications not only because of the high cost of wind power converters, but also because of the complex accessibility issues.

B. MAXIMIZING THERMAL CAPACITY AND OVERLOAD

ATC is an effective mean to increase the overload capability and to exploit the full thermal limits of power converters. It allows downsizing converters in size, cost, and weight without putting reliability at risk. This potential has been investigated for traction converters [34], motor drives [28], and renewable energy based voltage source converters (VSC) [15]. The later, for example, has been proposed to increase the overload capability during grid fault conditions. According to the grid operators, VSC should be transiently overloaded by a factor of 1.5–2 in a time range 80–500 ms to support the grid, mimicking the behavior of a synchronous generator (SG). However, unlike SG's, VSC power modules have very short thermal time constants and thus shall be rated for the maximum overload current. However, with ATC the same VSC can provide higher overload currents. Based on the fault current reference and junction temperature measurements, the ATC can adjust the current limit continuously, such that the VSC provide a transient current greater than 1 p.u without being destructed due to high junction temperature.

In [28], it has been shown that at high fundamental frequency ($f > 10$ Hz) a motor drive can operate safely for up to 200% of the rated torque compered to low frequency operation without reaching the maximum allowable junction temperature. This is because of the decaying thermal impedance (Z_{th} in (1)) frequency response at higher frequencies. The author exploited this property by employing an adjustable current limit based on the fundamental frequency and coolant temperature. It has been concluded that a smaller and more compact motor drive can be used for applications which do not require high torque at low speed.

C. THERMAL STRESS BALANCING

ATC strategies are also proposed to achieve loss and thermal balancing among the different devices in multilevel converters and multichip modules. In multilevel converters, the loss and stress distribution among the devices varies with the operating conditions, making some devices hot while others stay much cooler. The losses of the most stressed devices limit the output power and consequently, the power density of the converter. ATC uses advanced pulse width modulation (PWM) strategies and control structures to achieve more homogeneous temperature and loss distribution among the different devices. With ATC, not only the power density can be improved [35], but also the reliability of the whole converter [36].

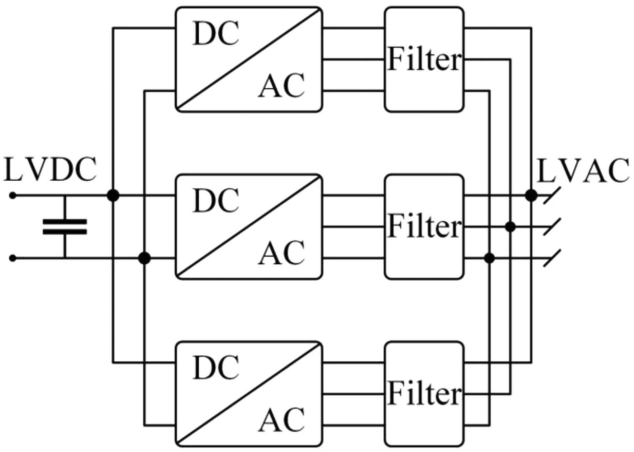

FIGURE 5. Modular converter structure for the LV side of a smart transformer [18].

D. THERMAL STRESS REDISTRIBUTION

ATC are also proposed to manipulate the load distribution among the different converters in a modular structure such as the one shown in Fig. 5, which is presented in [18] for the low voltage side of a smart transformer. In the contrary to the load balancing, the ATC in this case impose inequivalent load distribution among the different converters. This seems illogical at a first glance, as it will impose higher thermal stress on the most loaded converters. However, parameters of the power devices (e.g., on-state voltage drop) are subjected usually to device-to-device parameter mismatch. In addition, the heatsink temperature differ between the converters depending on the spatial configuration and the coolant flow. This result in a difference in the remaining useful lifetime (RUL). With equivalent load sharing some converters will fail earlier. Then, the damaged converters will be substituted during the maintenance procedure leading to higher mismatch in the converter's RUL [37], [38].

To this end, a thermal based power routing is proposed, which update the power of each converter actively based on the RUL. Under such control strategy, the stress on the most aged converters is partially transferred to the less aged once, and the reliability of the whole system is improved. Moreover, power routing can optimize the maintenance schedule and reduce the maintenance cost in power electronic-based power systems, such as in microgrids and smart transformer applications. For instance, predictive maintenance approaches based on the measurement of deteriorating variables, like the on-state voltage of IGBTs, are usually performed once the measured variables approach a certain threshold value [10]. In

this process, power converters that are close to failure before the next maintenance are also replaced resulting in a loss of lifetime for power converters which could potentially operate for longer period. With unequal power sharing however, a smart management of the different power converters loadings is performed in order to achieve the maximum operational profit [39].

III. ACTIVE THERMAL CONTROL STRUCTURE

This section briefly summarizes the thermal state variables extraction methods, RUL estimation procedure, and the control structures for ATC. The control structure will be introduced for the device and converter levels. For the system level (i.e., between multiple converters) the detail will be discussed in Section IV.

A. TEMPERATURE EXTRACTION AND LIFETIME ESTIMATION

1) TEMPERATURE EXTRACTION

Real-time junction temperature extraction is of interest for ATC strategies. Generally, the temperature extraction method for the implementation of ATC should have high accuracy, minimal phase lag, and high bandwidth to track the fast dynamic behavior of the junction temperature [22]. For this reason, the commonly used negative temperature coefficient thermistors (NTC) are not a viable solution. These are placed on the substrate often at a large distance from the location of the power semiconductors. As a result, the thermal capacitance that is established provide strong filtering and thus low bandwidth temperature information. Alternatively, an on-chip NTC can have an improved bandwidth. However, a special semiconductor chips with integrated sensing diodes are required for this approach. The sensing diodes occupy a space on the power module that can't be used as an active area, and thereby reduce the power density of the module [40]. Common temperature extraction methodologies for ATC are via temperature sensitive electrical parameter (TSEP) [37], [15], thermal predictors [34], [35], [41] and thermal observers [22].

The TSEPs are switching or conduction properties of power semiconductors, e.g., the on-state voltage or resistance [37], [15], [20], peak gate current [42], and turn-off and turn-on delay times [43], [44]. They occur because of electrical parameter variations with the device junction temperature, for example the threshold voltage, internal gate resistance, or the device capacitances. The TSEPs can be used to estimate the junction temperature with the help of an extraction circuit that is directly connected to the terminals of the device without the need for module integrated sensing. The extraction circuit can be integrated within the gate driver circuitry, which provides an excellent solution for compact power module [45].

An example of a TESP is the temperature sensitivity of the IGBT collector-emitter voltage. In this case, an extraction circuit is required to block the high dc-bus voltage while amplifying the small collector-emitter voltage when the device is conducting. Then, based on a lock-up table, the device current and the collector-emitter voltage are used to estimate the junction temperature [46].

The TSEPs can provide measurements of high bandwidth. However, TSEPs often inherently comes with short available extraction time, low temperature sensitivity at some operating points, and low signal to noise ratio. For instance, the temperature sensitivity of the on-state voltage is usually a function of the device current [47], making the determination of the junction temperature difficult at no or low current values. Alternatively, the temperature sensitivity of other TSEPs, like the threshold voltage, is shown to be constant over the entire operating range [48]. However, in this particular case, the extracted temperature is more susceptible to noise and electromagnetic interference. The high sensitivity to noise and the discontinuous capability to extract junction temperature (e.g., during the turn on/off delays) that comes almost with all high-bandwidth temperature extraction approaches, may require the implementation of a low pass filtering which strongly reduce the bandwidth and introduce phase lag in the transient temperature information [49].

Thermal predictors on the other hand can provide temperature information with zero phase lag. They exhibit an open loop structure and do not require special temperature-sensing data. A typical structure of a thermal predictor is shown in Fig. 3. The physical system provides electrical measurements, such as the current i_c and dc-bus voltage V_{dc}, which are used by the device model to determine the on-state voltage drop V_{ce} and the on and off switching energies (E_{on} & E_{off}). These information are utilized by the power loss model to determine the conduction and switching losses (P_{cond} & P_{sw}). Then, based on the thermal model and the cooling system temperature information T_c, the junction temperature can be determined. The thermal model can vary from simple models, such as foster [35] or cauer models (shown in Fig. 3) [34], to complex models that can even provide temperature information at different locations within the module, like matrix based thermal impedance models [50]. However, because of the open loop structure, they are strongly sensitive to model inaccuracies, which are very difficult to be avoided because of the difficulty in extracting an accurate switching loss energies [51] and the continuously progressing deviations in the electro-thermal model, for example, due to the thermal path degradation [49].

As a consequence, thermal observers are proposed which combine temperature measurements (e.g., via TSEP [47] or NTC [22]) with the electro-thermal model to estimate the junction temperature. This allows to compensate the modeling errors of the thermal predictor within a bandwidth specified in the observer design, which of course depend on the bandwidth of the junction temperature measurement technique. A structure of a thermal observer is shown in Fig. 6. It illustrates in principle how the deviation between the temperature measurement and the electro-thermal model output is compensated by regulating the power losses.

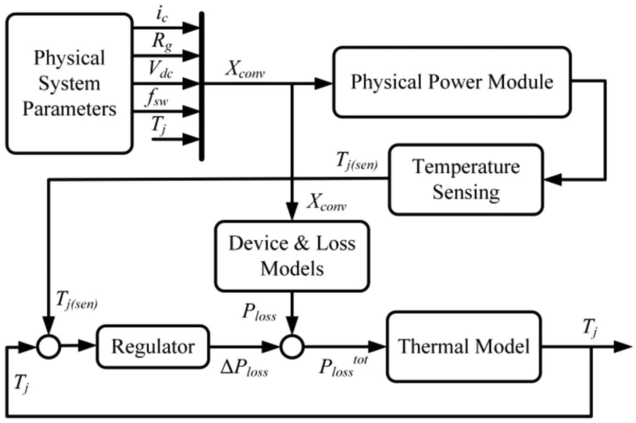

FIGURE 6. Structure of a thermal observer [46].

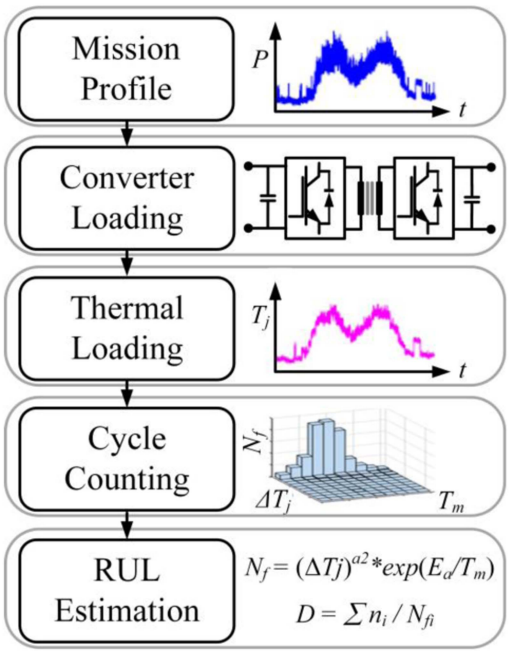

FIGURE 7. Lifetime estimation procedure [37].

2) LIFETIME ESTIMATION

The RUL estimation is a fundamental for many ATC strategies specially for those aiming to redistribute the loading among the converters in a modular structure. Most ATC strategies are employing the RUL prediction procedure shown in Fig. 7. First, the converter loading is extracted from the mission profile of the system (i.e., during a time period t). Then, the thermal loading (e.g., the junction temperature) is obtained using a temperature extraction method (e.g., thermal predictors). Afterwards, a lifetime model computes the damage resulting from every temperature cycle in the temperature profile. However, the junction temperature profile contains the mission profile dynamics, and thus have several temperature cycles of different magnitudes at different mean temperatures. Hence, a cycle counting algorithm is required to transfer the irregular profile into several regular cycles. The damage from all the cycles is then accumulated linearly, to calculate the total damage at that time period D [52], [53], [37], [18], [54].

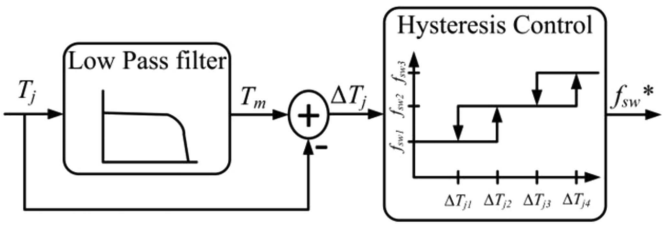

FIGURE 8. Open loop active thermal cycling reduction technique [21].

B. CONTROL STRUCTURE

A general structure of an ATC is shown in Fig. 3. It is worth to mention that the manipulated variable can be the switching frequency, modulation strategy, dc-bus voltage, and others which are going to be introduced in Section IV. Moreover, the thermal controller can be an open loop or closed loop controller. An example of an open loop controller for thermal cycling reduction using the switching frequency as a manipulated variable is shown in Fig. 8 [21]. It is obvious how positive values of ΔT_j (i.e., thermal cycles below the mean temperature) can be reduced by directly increasing the switching frequency. The relationship between ΔT_j and the manipulated variable can be set experimentally depending on the targeted thermal cycle amplitude and the allowable manipulation limit of the controlled variable.

Open loop control structures are very simple to implement and have shown the capability to achieve different ATC objectives, such as thermal cycling reduction [21], [55] and thermal balancing between devices [35], [56], [57]. However, this structure can't control the junction temperature accurately. Thereby, operating near the devices thermal limits is not possible [24]. In the contrary, closed loop control is an effective mean to realize all the control objectives of ATC. Closed loop controllers which are proposed in the literature include linear state feedback control [22], [15], [58], [59], [20] and model predictive control (MPC) [41], [60], [61].

A challenge for all closed loop active thermal cycle reduction techniques, however, is the determination of a stress relieving and minimally invasive junction temperature swing reference T_j*. Setting lower reference T_j* provide higher improvement on the device's lifetime. However, the controlled variables usually have negative impact on the system performance [13]. Hence, their variation range shall be restricted. Moreover, the capability to track the reference is confined by the loss manipulation limits. Therefore, closed loop ATC are required to operate within the loss manipulation range or implement an anti-wind up scheme to avoid instability [22]. This issue can be addressed with MPC by including the loss manipulation limits in the cost function of the primary control (e.g., current control). However, a proper derivation of the cost function and tuning of the weighting factors is necessary to

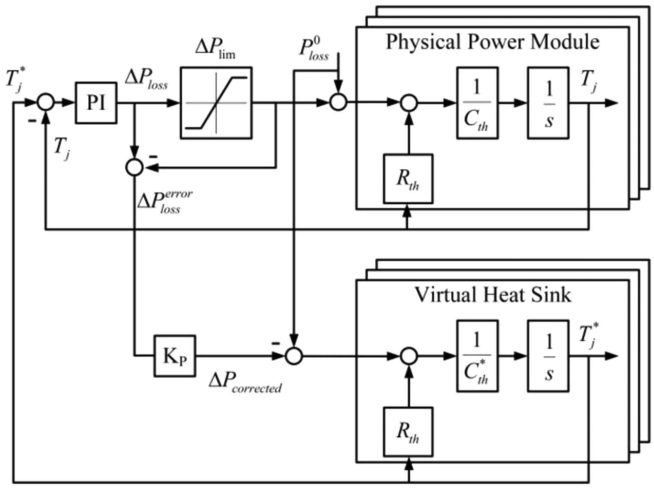

FIGURE 9. Virtual heat sink concept for junction temperature reference generation [46].

minimize the impact on the electrical, dynamics, and other system performance requirements [41], [60], [61].

Another interesting method to avoid an anti-wind-up and to generate a feasible reference for active thermal cycling reduction is the virtual heat sink concept, shown in Fig. 9. The virtual heat sink is a model of the physical power module, but with enlarged thermal capacitance. By more or less enhancement of the virtual capacitance, a feasible reference with reduced thermal cycles is created. The input to the virtual heat sink is the power losses at the original value of the manipulated input P^0_{loss}. Using the reference generated from the virtual heat sink as well as the temperature estimate (e.g., via TSEP), the thermal controller determines the required power losses that should be compensated by the manipulated variable ΔP_{loss}. If the loss command is partially feasible, the portion that could not be realized $\Delta P_{loss}{}^{error}$ is passed to the virtual heat sink via a feedback loop. In this case, the temperature reference of the virtual heat sink begins to follow the temperature in the physical power module until the system run out of limitation [17], [22].

IV. ACTIVE THERMAL CONTROL POSSIBILITIES

This section presents the different possibilities of ATC at different levels. Starting from the device level, where the stress on each device in the converter is regulated individually. Then, to the converter level, and finally to the system level where a converter in a system of multiple converters is treated as a single block. These levels can be further classified according to the control strategy as shown in Fig. 10. More details at each control level will be introduced in the following subsections.

Besides the control possibilities shown in Fig. 10, there is also the possibility to control the cooling system temperature (i.e., T_c in (1)). The control parameter can be the voltage applied to the fan in forced air cooling, or the voltage to a pump in a liquid cooling system. By controlling the cooling power, the thermal resistance of the heatsink can be

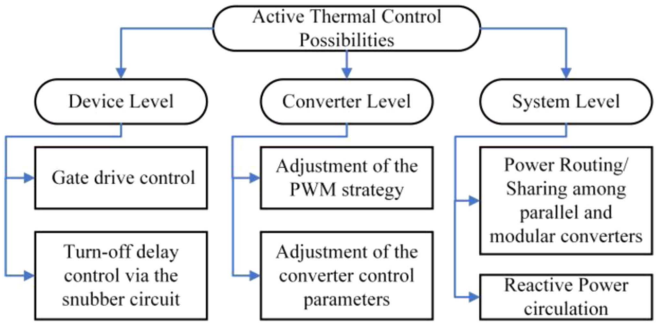

FIGURE 10. ATC possibilities at different levels.

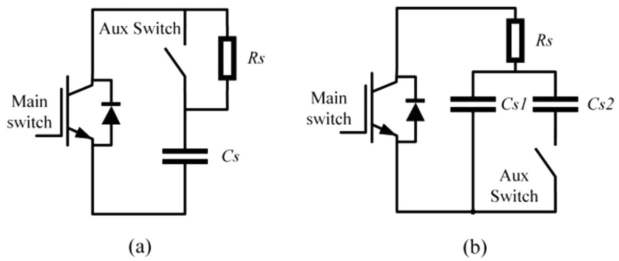

FIGURE 11. Turn of delay control via the (a) snubber resistance [32] and (b) capacitance [63].

adjusted leading to an adjustable heatsink temperature, and consequently junction temperature. Although, this technique can be implemented in all systems that features controllable cooling and it is shown to be effective in reducing thermal cycling [16], [62], especially the once with large duration, the focus of this section will be on the control methods that manipulates electrical parameters, and thus is not going to be further discussed.

A. DEVICE LEVEL

Turn of delay control via the snubber circuit is one possibility to realize an ATC on the device level. An IGBT connected in parallel to an RC snubber will work in the weak absorption trajectory with large turn off loss when the value of the resistance is very large. On the other hand, if the value of the resistance is very small and the capacitance is large enough, the IGBT will work in the strong absorption trajectory with a small turn off loss. With this in mind, two strategies were proposed to reduce the thermal cycling in [32] and [63] by the realization of variable resistance and variable capacitance, respectively. The two strategies were implemented by connecting an auxiliary switch in parallel to the snubber resistance and in series to an extra snubber capacitor as shown in Fig. 11(a) and 11(b), respectively. By controlling the switch delay time (i.e., time after the turn-off signal of the main IGBT), a controllable turn-off loss can be achieved. This means that a thermal cycling reduction is possible by manipulating the turn-off switching loss of the devices, for example by increasing the losses during light load conditions.

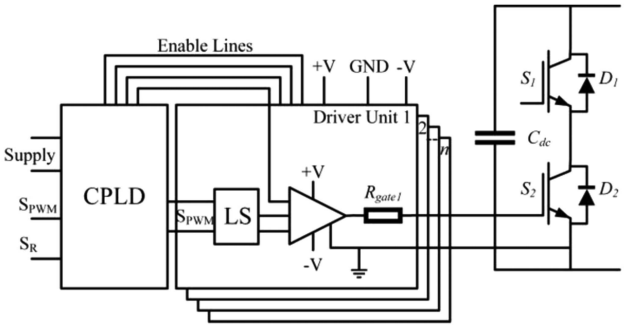

FIGURE 12. Schematic of an adaptive gate resistance [17].

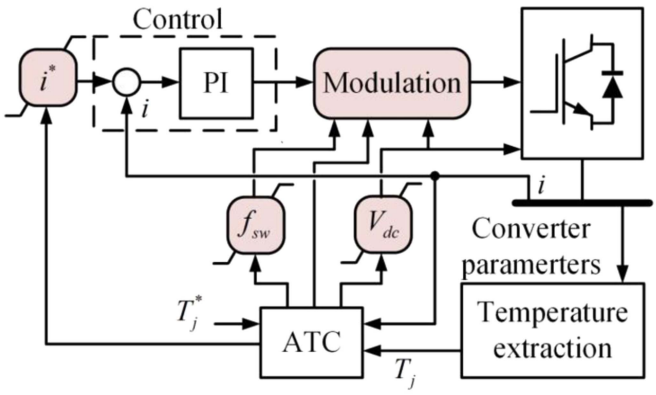

FIGURE 13. Basic scheme for the ATC at control and PWM level [7].

Another way to implement a device level ATC is by using an adaptive gate driver. A gate driver for balancing the thermal stress among parallel devices have been proposed using pulse shadowing strategy [56], turn-on delay control [64], and turn-off delay control [65]. In all the cases a modified structure with multiple gate-emitter connections is required to control each device (or group of devices) individually. In the pulse shadowing strategy, the devices with the highest thermal stress are removed at specific periods in order to reduce their total losses and thus the junction temperature. On the other hand, the other two control strategies manipulate the turn-on or off delay of the devices to manipulate their turn-on or turn-off switching loss, respectively. For instance, the device with the larger turn-on delay experience lower turn-on loss because of the reduced switching current during commutation and the switching is realized under lower voltage. This means that the most thermally stressed device can be switched at larger turn-on delay in order to balance its thermal stress with the other devices.

For thermal cycling reduction, an adaptive gate driver with variable gate voltage [66] and variable gate resistance [17], [67] are proposed. A possible structure of an adaptive gate resistance is shown in Fig. 12 [17]. It is composed of multiple parallel connected gate drivers were each receives one pulse width modulation (PWM) signal (S_{PWM}) and an enable signal from a Complex Programmable Logic Device (CPLD). In addition, the CPLD receives a control signal (S_R) that exhibits information about the required gate resistance to be applied. Accordingly, the CPLD match the required resistance by selecting a sequence from the multiple discrete values. The larger the gate resistance is the slower the charging of the gate leading to a reduction in the switching speed, and consequently an increase in the switching loss. This method can be applied to reduce thermal cycling by increasing the gate resistance above the typical values (e.g., around 6 Ω for Hybridpack2 IGBT module [17]) at light load conditions. A smaller gate resistance on the other hand is usually limited to avoid switching overvoltage at turn-off [17], [68]. Similarly, the gate voltage control can also reduce the thermal cycling by lowering the gate voltage at light load conditions. A lower gate voltage increases the on-state resistance and the switching time. Thus, increasing both the switching and conduction losses.

B. CONVERTER LEVEL

The converter controller generates a reference to a modulator, which in turn supply the gate signals to the converter as shown in Fig. 13. This means that at this level an ATC can be realized by modifying control variables, like the switching frequency, current reference, or dc-bus voltage, which has direct impact on the losses of the converter. In addition, different pulse width modulation (PWM) strategies have different impact on the converter devices loading, which means that they can used as a manipulation variable for ATC. The different possibilities at these two levels will be summarized in the following two subsections. In addition, the possibility of achieving an ATC with other control strategies, like finite control set model predictive control (FCS-MPC) will be described in a third subsection.

1) PULSE WIDTH MODULATION FOR ATC

The modulation strategy is an interesting way not only to achieve thermal cycling reduction, but also thermal and RUL balancing among different devices in the converter. In this section, different examples on different converter topologies will be given in order to illustrate how these objectives can be satisfied using PWM.

For three phase two level converters, the discontinuous PWM (DPWM) can be used. common DPWM methods, such as DPWM0, DPWM1, and DPWM2 clamps every phase for up to 60° duration to the positive and negative dc-bus in a fundamental cycle by adding a common mode clamping signal to the original sinusoidal modulation signals. The resulting DPWM modulation signals with a 60° clamping duration are shown for one of the three phases in Fig. 14. Compared to the conventional Sinusoidal pulse width modulation (SPWM), a 33% reduction in the average switching frequency and consequently in the switching loss is achieved when the clamping angle is set to 60° (i.e., no switching for 1/3 duration of the fundamental period). Moreover, if the clamping duration perfectly aligns the current peak, the switching loss can be reduced by 50 % [69]. This is the reason that different DPWM methods with different clamping locations are proposed (i.e.,

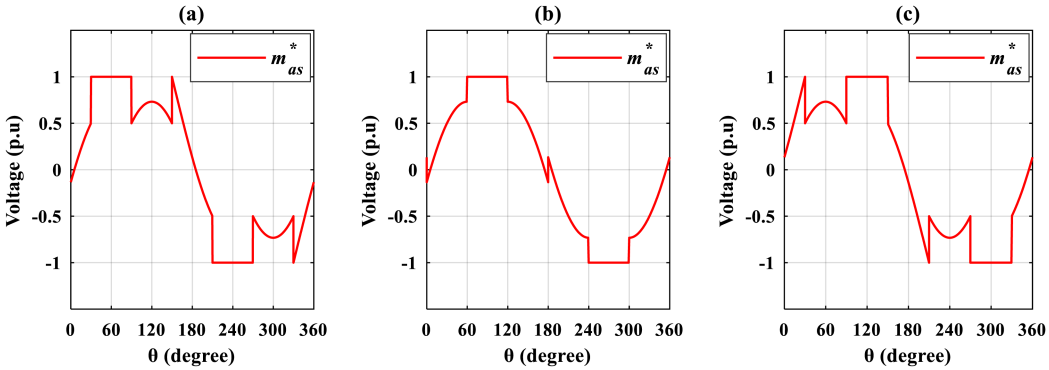

FIGURE 14. Phase-*a* modulating signals with (a) DPWM0, (b) DPWM1, (c) DPWM2 [5].

to maximize loss saving at different power factors). The DPWM1 has been tested in [55] on the DP25H1200T101667 (1200 V/25 A) IGBT module with 650 V dc-bus voltage, 5 kHz switching frequency, and unity power factor load. It has been shown that the thermal stress increase due to the increase of the load power from 75 to 100 % can be completely compensated by changing the PWM strategy from SPWM (i.e., 0° clamping angle) to DPWM1 with 60° clamping duration. Due to this outstanding capability, an ATC strategy using DPWM1 is proposed in [55]. The clamping duration is changed from 0 to 60° as a function of the load to compensate the thermal cycling. This result in more stable junction temperature with less fluctuations.

The DPWM can also be used to alter the loss distribution among the upper and lower devices in a three-phase two-level converter. The two DPWM strategies, DPWM+ and DPWM-, clamps a phase leg continuously for 120° duration to the positive and negative dc-bus, respectively. Apparently, the switching loss of the upper and lower devices under the two DPWM strategies is same (i.e., both the devices are clamped for 120° with DPWM+ or DPWM-). However, the conduction loss is not the same. The DPWM+ result in reduced conduction loss in the lower device, while DPWM- decrease the conduction loss of the upper device. This feature is used in [57] to compensate for power loss difference and consequent temperature difference between two devices in a bridge arm, which can be caused, for example, due to the device's parameter mismatch or unequal temperature distribution. The temperature balance control (TBC) method proposed in [57] is shown in Fig. 15. After the junction temperatures are acquired, the temperature difference between the upper and lower devices in each phase is calculated and the maximum and minimum difference (ΔT_{jmax} and ΔT_{jmin}) are identified. Based on ΔT_{jmax}, ΔT_{jmin}, and the thresholds (T_{th+} and T_{th-}) the modulation strategy is selected. When ΔT_{jmax} and ΔT_{jmin} lies between the thresholds, the modulation strategy is chosen as the conventional SPWM. If ΔT_{jmax} is above T_{th+}, DPWM- is selected to decrease the losses and consequently the thermal stress of the upper device, while if ΔT_{jmin} is below T_{th-}, DPWM+ will be used. The method is tested considering the C2M0080120D SiC MOSFET as the switching devices. It has

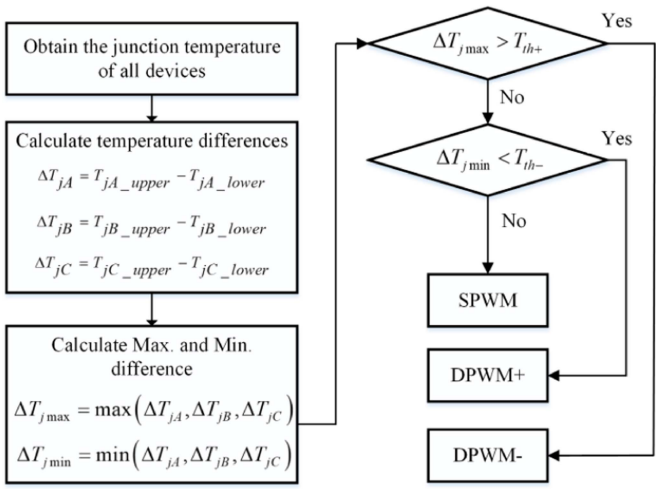

FIGURE 15. Temperature balance control using DPWM+ and DPWM- [57].

been shown that a temperature difference can be controlled from 20°C to 3°C when the TBC method is applied.

PWM strategies was also reported to balance the thermal stress among the different devices in a multilevel converter structure. The three-level diode neutral point clamped converter (3L-DNPC) shown in Fig. 16(a) is among the most widely investigated topologies. A drawback of this topology is the unequal thermal stress distribution between the outer devices T_{out} and D_{out}, inner devices T_{in} and D_{in}, and the clamping diodes D_{npc} under the conventional space vector PWM (SVPWM). A study conducted in [70], analyzed the thermal stress of different devices in the 3L-DNPC in grid-connected applications under different voltage sag ratios. It has been concluded that T_{in} and D_{npc} take over the place of T_{out} to become the hottest devices at low sag ratios (low and medium modulation index). In this regard, a sequences of space vectors are investigated in [70] and [71] to reduce the thermal stress of these devices under medium and low modulation index.

The space vector diagram of the three level three-phase converter is shown in Fig. 16(b). It shows all the possible voltage vectors that can be produced, with P, O, and N

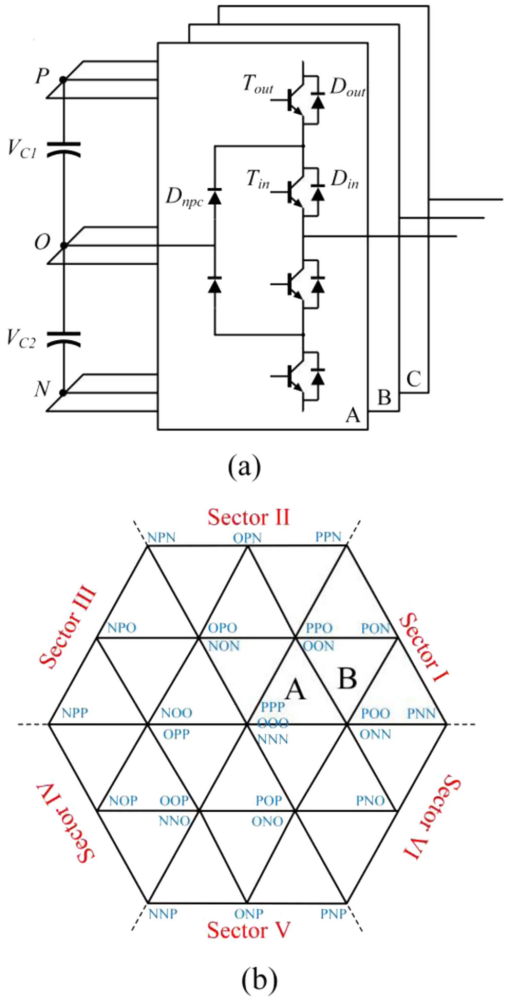

FIGURE 16. (a) 3L-DNPC converter [73], (b) three level space vector diagram [72].

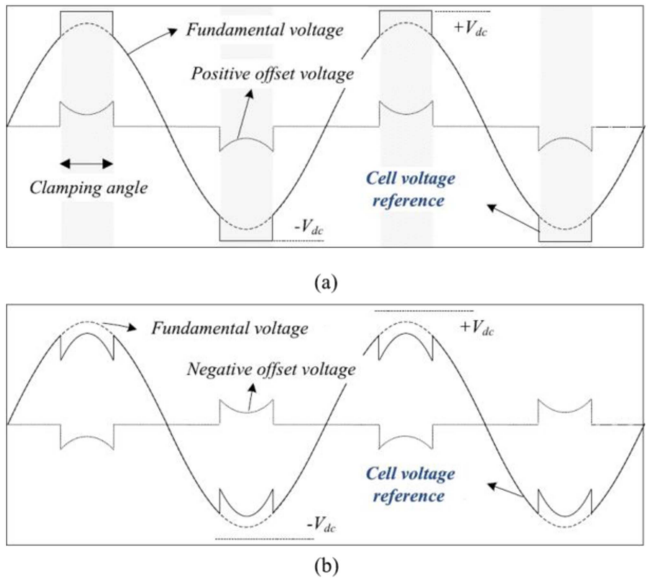

FIGURE 17. (a) DPWM for thermal stress reduction (b) modulation signal for the compensation of offset voltage introduced by the DPWM [75].

representing that a certain phase leg is connected to the positive, zero, and negative dc-bus voltage, respectively. A convenient way to reduce the thermal stress of the inner devices and clamping diodes is to avoid using the voltage vectors which contains the most O states. For a voltage reference in sector I and a moderate modulation index (regain B), the N2 PWM proposed in [70] avoids the two states POO and OON by applying their redundancies ONN and PPO for the whole vector duration. As a result, the switching sequence becomes ONN-PON-PPO. Note that the dwelling time of the zero-voltage vector is minimized with respect the conventional SVPWM, which employes sequences, such as ONN-OON-PON-POO or OON-PON-POO-PPO in the same region. In other words, the conduction time (or conduction loss) of T_{in} and D_{in} is minimized. Similarly, the DPWM named as DPWMPN was investigated in [72] at low modulation index (regain A). This DPWM employs sequences, such as POO-PPO-PPP in sector I, which clamps a phase leg to the positive and the negative dc-bus resulting in no current flow in the neutral bus (clamping diodes) for 120° duration of the fundamental cycle. The validity of the N2 PWM compared to SVPWM at moderate modulation index was investigated in [70]. The outcome was that the temperatures of the most stressed device (T_{in} and D_{in}) are reduced with N2 PWM. Meanwhile, the devices utilization becomes more equal. A similar outcome with DPWMPN was also observed at low modulation index in [72].Therefore, by actively changing the modulation strategy according to the converter operating conditions a better thermal distribution can be achieved compared to the SVPWM.

An ATC using PWM methods for thermal stress balancing between devices in 3L-DNPC (using carrier-based PWM) [73], H-bridge [74] and active NPC (ANPC) [35] converters and for RUL equalization between the cells in single-phase cascaded H-bridge (CHB) converter [9], [75] are also investigated. For instance, the DPWM strategy in [9] and [75] are proposed to overcome the disadvantage of unequal aging between the different cells in a single-phase CHB converter. The method is similar to the DPWM1 described for three-phase converters, where an offset voltage is injected to clamp the original sinusoidal signal to the positive and negative dc-bus. The offset voltage can be a first-harmonic (as shown in Fig. 17(a)) or third-harmonic signal like in three-phase systems. Note that the third harmonic can be obtained by generating two virtual phase-shifted signals of 120° and 240° in the controller. The first-harmonic signal allows higher clamping duration (i.e., up to 180°) compared to the third-harmonic signal, and thus allows for higher switching loss and thermal stress reduction. However, it should be noticed that, the first-harmonic signal affects the fundamental voltages and thus the power delivered by the cells. This is known as power routing and will be introduced in part C of this section.

Unlike three-phase systems where the injected common mode clamping signal is internally compensated, the offset voltage appears at the output voltage in single-phase systems. To solve this issue, the cells of the CHB converter are divided into pairs. The more aged cell in the pair is modulated with DPWM in order to reduce its thermal stress and consequently to reduce its lifetime consumption, while the less aged cell is modulated with a compensating PWM (see Fig. 17(b)) so that the output voltage is not affected. To obtain the lifetime of each cell in real time, the method described in Fig. 7 can be used. The accumulated damage of each cell for a specific time period (e.g., 1 hour) is calculated and added to the initial damage to obtain the total damage. Then, based on the total damage, the modulation strategy of each cell in the pair can be determined.

2) CONTROL LEVEL ATC

ATC in the converter control level is implemented by manipulating control variables, such as the switching frequency, dc-bus voltage, and current limit. At this stage, ATC is usually performed to reduce thermal cycling, to limit the junction temperature rise during abnormal or transient conditions, or to increase the overload capability of the converter by pushing the devices into their thermal limits. An ATC for achieving the later target is investigated in [15], [28], [58], and [34] and have been illustrated in Section II. For thermal cycling reduction in PV applications, a hybrid Power Control [76], [12] and modified MPPT algorithm [77] have been investigated. The latter actively modifies the duty cycle of the dc/dc converter in the presence of fast solar irradiation changes in order to limit the junction temperature derivative. On the other hand, the hybrid power control change from MPPT to constant power generation (CPG) once the MPPT algorithm power output or junction temperature of the devices reach a certain threshold in order to limit the upper value of the junction temperature swing. The two algorithms show considerably reduced thermal cycling and improved lifetime, but at the expense of relatively reduced energy yields.

In traction applications, an ATC based on reactive current injection was proposed in [78]. Traction drives are usually operated with maximum torque per ampere (MTPA), which produce the minimum stator current at a given torque value. However, an infinite number of current amplitudes can be used to generate the same torque level. In other word, it is possible to inject reactive current to heat up the devices during light load conditions to reduce thermal cycling without affecting the operating point.

Another strategy that can be used to reduce thermal stress in electric drives fed by a dc/dc converter or controlled rectifier is the use of variable dc-bus voltage control. Common variable dc-bus voltage control very the dc-bus as a function of the motor speed [79], [80]. Because of the speed dependent EMF, a lower dc-voltage is required at low speed resulting in a reduced switching loss. Although, the conduction loss of the devices will be affected, the total power loss is still greatly reduced because of the large switching loss reduction following the linear relationship with the dc-bus voltage. This can greatly reduce the thermal cycling at low speed. However, it has been shown in [81] that the minimum dc-bus voltage is not the optimum control at stall conditions, where the electric machine switch to the dc operation mode. For a number of distinct rotor positions, a single device in a phase leg can carry the peak dc current almost continuously resulting in large conduction loss and unbalanced thermal distribution [34], [82]. Therefore, a method which calculate the optimum dc-bus voltage (ODV) that minimize the total losses in the device with the highest thermal stress under stall condition is proposed [81]. The ODV works in parallel with the minimum dc-bus voltage method and it only take place once stall condition is predicted. However, these methods require dc/dc converter or controlled rectifier which limits their application. Alternatively, an optimal phase angle (OPA) method to redistribute the thermal stress under stall conditions was proposed in [83]. In this method, the phase angle of the rotor position and consequently the speed reference is recalculated such that the current stress on the phase suffering the severest thermal stress is reduced. With the ODV and OPA a large thermal stress reduction can be achieved under the stall condition of the electric drive.

3) FINITE CONTROL SET MODEL PREDICTIVE CONTROL (FCS-MPC) FOR THERMAL STRESS REDUCTION

Power switches in the converter can be either driven by a modulator or the switching signals are directly generated by the controller. The later can be realized using a finite control set model predictive control (FCS-MPC). The FCS-MPC uses a model of the system to predict the output for every switching state of the converter. Based on the difference between every prediction and the actual measurement, a cost function is computed. The switching state that obtains the minimum cost function is applied to the converter in the next sample. One significant advantage of FCS-MPC is the possibility to control multiple secondary objectives by simply adding them to the cost function of the primary objective (e.g., current control). This means that more than one ATC objective can be achieved simultaneously without the need for cascaded control loops. The study in [41] has demonstrated this idea in a three-phase two level converter by designing a cost function which takes into account the temperature variance between the devices, accumulated damage, and the total power losses in addition to the primary current control. The results show that the designed FCS-MPC is capable of balancing the thermal stress between the devices, minimizing the power losses, and reducing the thermal cycling. Following this study, multiple ATC strategies are realized using FCS-MPC on other converter types. An example of these is the balancing of thermal stress within the devices in ANPC [36], [84] DNPC [61], and CHB [85] converters.

Every objective function is usually multiplied by weighting factor to emphasize the significance in the problem formulation. A challenge for FCS-MPC lies in the proper tuning of the

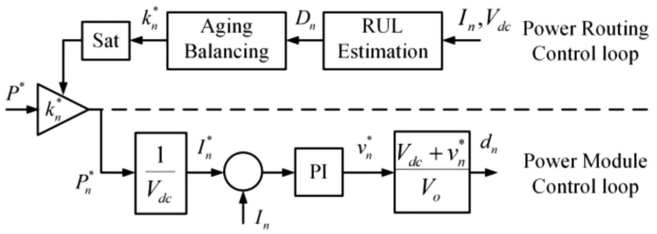

FIGURE 18. Power routing concept of an interleaved dc/dc converter [52].

secondary weighting factors (λ_s). A higher value of λ_s implies better impact on the secondary objective but may result in a violation in other important requirements. The impact of the weighting factor on the performance of a grid-connected inverter (i.e., thermal cycling, power losses, and THD) under different power levels have been demonstrated in a study in [60]. One of the observations was that the value of λ_s that meet grid code requirement and minimize the thermal stress at certain power level does not necessarily do the same at other power levels.

C. SYSTEM LEVEL

1) POWER ROUTING

The principle of power routing (or sharing) for ATC is to redistribute the power among the converters in a system in order to equalize their RUL or to achieve an equal thermal distribution during operation. This principle has been applied to many applications such as in between the converters in microgrid applications [29], [86], [87], parallel dc-dc converters in aircraft and wind energy applications [54], [52], and the converters in multi-phase drives [88], [89].

Most power routing methodologies are targeting the RUL equalization of the converters. In case of parallel connected converters, such as in the interleaved dc/dc converter, the power routing can be performed as shown in Fig. 18 [52]. Based on electrical measurements, the accumulated damage of each converter for a specific time period (e.g., 1 hour) is calculated as shown in Fig. 7 and added to the initial damage. Then, based on the total damage D_n and the maximum allowed current in each converter, the power sharing optimizer determines the most proper power (current) sharing K_n between the cells that contribute to more RUL equalizations. Finally, the calculated $P_n{}^*$ is commanded via the converter closed loop controller. In case any converter receives a current reference higher than the rating, the current exceeding the rating is redistributed to the other converters [18].

Another converter configuration which has received considerable attention is the input series output parallel configuration shown in Fig. 19. This modular structure is composed of multiple power electronic building blocks and each block is composed of CHB cell and a dual active bridge (DAB) cell. In this configuration, the power routing among the output parallel DAB converters can be performed by varying the fundamental voltage among the different cells in the CHB converter. Of course, the modulation index M must remain

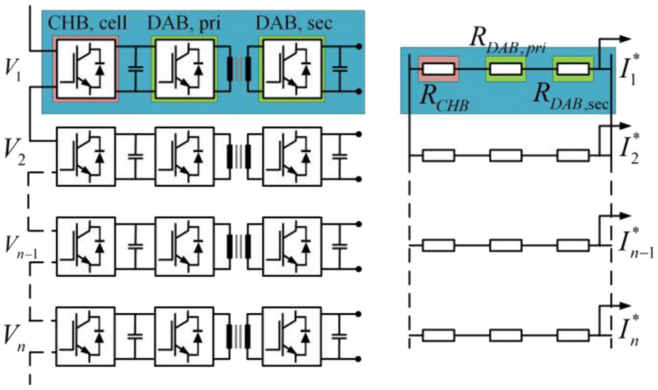

FIGURE 19. Input series output parallel converter configuration with the virtual resistance concept [37].

within the linear modulation range in order to avoid overmodulation, which causes a very high distortion of the output voltage of converters. In other words, a maximum modulation index of M=1 with sinusoidal modulation must be respected. However, it can be extended up to 1.15 and 1.27 with third harmonic injection and first harmonic DPWM, respectively [90].

If the dc-bus voltage balance is achieved via the DAB stage, then a difference in the reference voltages among the CHB cells will cause different current flow among the DAB cells, which can be used to perform the power routing [9].

Although, the current flowing in each bridge of the CHB remains unchanged, the current sharing between the switches and diodes will change resulting in variation of the losses. This means that the aging of the different cells in the CHB can be affected following the power routing employed for the DAB's [91]. This problem can be addressed using the virtual resistance concept [37], or graph theory representation [92]. The virtual resistance concept is illustrated in Fig. 19, where each path is represented by three resistances indicating the accumulated damage of the CHB, primary side DAB, and secondary side DAB cells. Then, a power sharing is implemented based on the total virtual resistance of each path.

The impact of the power routing ATC has been tested in many studies using the B_x lifetime, which represents the time when each cell has x% probability of failure [37], [39]. With power routing ATC, not only the failure probability of the weakest cell has been delayed, but also the failure probability of all the cells has been converged in time which can reduce the maintenance cost.

2) REACTIVE POWER SHARING AND CIRCULATION

The reactive power is a system control reference that is ideally not limited by the electrical or mechanical power processed by the converter, but it can affect the device loading considerably, and thus, can be used as a control variable for ATC. In grid connected applications, the maximum reactive power that can be injected by the converter is restrained by the grid standard. However, for parallel connected converters, the reactive power can be circulated among the converters and not necessarily be

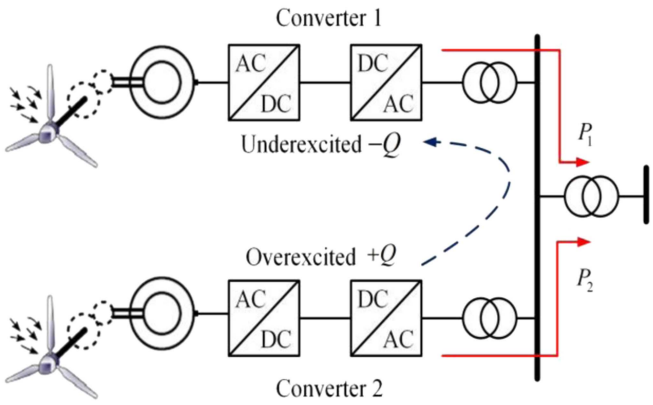

FIGURE 20. Concept of reactive power circulation in parallel connected converters [23].

seen at the point of common coupling as shown in Fig. 20. If one converter is operating under over excited condition (i.e., generating reactive power), the other converter can absorb the same amount of reactive power (i.e., under excited operation). In both cases, the two converters will experience more thermal stress because of the higher current amplitude. Therefore, this strategy can be utilized to heat up the devices during light load conditions in order to reduce thermal cycling [19]. Note that no oversizing of power semiconductors is required, because the maximum allowed circulating reactive power is decided based on the rated power of converters and the reference real power.

This concept was investigated for parallel converters in hydro generating unit [93] and between the generator and the back-to-back power converter in a DFIG [94]. For N number of converters, a generalized approach using an optimization problem is proposed in [95].

A temperature droop-based dynamic reactive power sharing (TDDRPS) in a microgrid consisting of PV and battery converters is presented in [31]. Unlike conventional strategies, which distribute the load reactive power among battery converters, the TDDRPS allows PV converters to share certain amount of reactive power in order to compensate for the load fluctuation and the intermittent PV generation. In addition, a certain amount of circulated reactive power among the converters is enabled within the converter's ratings. The TDDRPS is realized through the adjustment of the conventional Q-V droop law based on the junction temperature swing.

V. CHALLENGES AND FUTURE WORK

The previous review and discussion have made it clear that the ATC is a key to achieving substantial requirements in several applications. However, to make ATC widely applicable, there are several challenges still have to be addressed by future research. These challenges include the extraction of accurate thermal variables, considering the interaction with other reliability critical components, and minimizing the impact of ATC on the system performance. Furthermore, the potential of ATC on next-generation wide-band gab devices is another important topic that shall be more emphasized by future research.

Table 1 summarize the disadvantages and/or limitations of different ATC strategies as illustrated in the literature. The increased THD, power losses, and operational cost in addition to the potential instability issues are the main drawbacks of introducing ATC strategies on the system performance. In fact, some studies have managed to mitigate some of these impacts in different ways. These are shown summarized in Table 2. However, there are still other issues which needs further consideration and are going to be highlighted in the following.

A. MINIMIZING THE IMPACT OF ATC ON SYSTEM PERFORMANCE

1) SMART TRANSFORMER APPLICATIONS

The solid-state transformer or smart transformer interface the medium voltage and low voltage grids, replacing the conventional transformers, with the aim of providing more functionalities. From this perspective, the three-stage configuration (AC-DC, DC-DC, and DC-AC), is the most promising as it provides dc-connectivity and allows for independent control of the reactive power at the medium voltage and low voltage grid sides.

Power converters for ST can be classified into modular and non-modular architectures. A non-modular architecture based on tow-level converter for the AC-DC and DC-AC stages and possibly a DAB for the DC-DC stage can be seen as more reliable due to the lower number of components required. However, high blocking voltage devices are required for the medium voltage side converters, which cause large switching loss and the devices are not readily available in the market. Although the converter can be designed with low voltage devices by series connection, a special sometimes complex or lossy, voltage balancing approaches are required to solve the voltage sharing issues between the switches. Furthermore, the scalability in voltage and power is unavailable, large output filters are required, and no-fault tolerant operation is possible.

On the other hand, a modular power converter is based on the concept of using several power electronic building blocks. One of the widely recognized configurations for the AC-DC and DC-DC stages is shown in Fig. 19, while for the DC-AC low voltage stage a parallel connection as shown in Fig. 5 is possible. This architecture solves all the above-mentioned limitations for the non-modular architecture. However, a major drawback is large number of converters and components, which can be seen as a reason for the low reliability and large maintenance cost. For this reason, the Power routing concept has been proposed to realize a system level reliability improvement and optimized maintenance schedule. However, the huge impact of the unbalanced operation on the quality of the output voltage and current is a big obstacle that needs to be carefully considered.

At the medium voltage side, for example, the CHB converters are usually operated using the phase-shifted PWM

TABLE 1. Limitations and Disadvantages of Different ATC Methods

Control Method	Limitations/ Disadvantages
Turn-off delay control - Via a variable snubber resistance [32] or capacitance [63].	• Require a parallel auxiliary switch to each main switch with comparable voltage and current ratings [32]. Therefore, can increase the cost and integration difficulty [57], [20].
Adaptive gate driver - Adjustable Gate resistance [17], [22]. - Pulse shadowing for multichip power module [56].	• Gate resistance control can't be effectively used with devices operated at high switching transients [22]. • Pulse shadowing increase the losses around the nominal load [65].
Modulation & switching frequency	• Many of the modulation methods for thermal stress reduction have shown adverse impact on the THD [72], [73], [55], [71]. The DPWM can lead to more than twice the THD of conventional SVPWM [69]. • The THD increase almost linearly with reduced Switching frequency [33].
Profile shaping - Current limitations in traction drives [34]. - PV Power limitations via hybrid power control [76] or thermally modified MPPT [77].	• In traction drives, current limitation implies less performance (i.e., reduced torque) once the drive reaches thermal limit [24], [34]. • Less energy yields in PV applications [77], [76].
Via the cost function in FCS-MPC	• Complexity in weighting factor tuning. For instance, a weighting factor which minimize the thermal stress and meet other constraints, like the THD, at a specific power level does not necessarily do the same at other power levels [60].
Power routing - In applications with CHB or interleaved parallel converters [52], [37]. - In microgrid applications [86], [53]. - In multi-phase drives [88].	• Appearance of lower order harmonics in applications employing phase shifted PWM, such as the interleaved converter and the CHB converter [97]. • Introduce extra operational cost [87] and give raise to potential instability issues [111] in microgrid applications. • Large increase of stator copper losses in multiphase drives, as the current imbalance between the stator windings becomes larger [112].
Reactive power control - Reactive current injection in motor drives [78]. - Reactive power circulation in parallel connected converters [19], [95].	• The reactive current injection in electric drives increase both the machine and converter losses [78]. • Reactive power circulation increases the power loss of all converters participating in the thermal stress reduction (over or under excited). Thus, may lead to large power losses [7]. [95].

TABLE 2. Methods for Mitigating the Adverse Effect of ATC on the System Performance

Control Method	Converter and/ or application	Addressed issue	Mitigation method
DPWM	Parallel converters in wind applications	High current THD of DPWM	• The converters with shorter RUL were modulated with the DPWM, while the other converters with longer RUL employed a modulation strategy to maintain an acceptable current quality at the point of common coupling (compensating PWM) [55].
Switching frequency	Wind power converter applications	Higher current THD at lower switching frequency	• The return on investment (ROI) [33] and thermal control efficiency (ηtc) [13] concepts are proposed, which allow to minimize ATC intervention but without losing the benefit of increased lifetime. • In [113], the switching frequency is selected based on a trade-off between the THD and the ΔTj reduction. A partitioning into different regions according to the current amplitude is done to realize the trade-off.
Via FCS-MPC	Grid connected applications	High current THD at certain power levels	• A dynamic weighting factor according to the power level is proposed [60].
	Electric train applications	Compromised dynamic performance	• A dynamic weighting factor during speed switching process is proposed [61].
Power Routing	Microgrid	Operational cost	• The droop gains of the units are calculated based on both the operational cost and accumulated damage [87].
	Microgrid	Stability issues	• The stability criteria was added as a constraint to the conventional reliability oriented power routing strategies [111].
	CHB and interleaved converters	Low order harmonics with unequal power sharing	• A variable phase shifted PWM is proposed which adapts the angles between the carriers dynamically considering the power imbalance between the cells [38], [97], [99], [96], [98].
	Smart Transformers & Microgrid applications	Efficiency	• In smart transformer, a graph theory representation is proposed, where wights are given to power flow path based on the RUL and the efficiency of each converter [92]. • In microgrid, A hierarchical control is proposed, with the primary control responsible for thermal management and the secondary control for activating/ deactivating units to improve the efficiency [114].

(PS-PWM) strategy which can produce an output voltage with superior quality. If the switching frequency of the devices in each cell is f_{sw}, the first harmonic group in the output voltage will be at $2Nf_{sw}$ (N is the number of cells), by applying a suitable fixed angles between the carriers. However, this advantage is feasible when all the cells manage the same power (i.e., same modulation index). When the power routing concept is applied, the advantage of the PS-PWM is partially lost and a non-negligible harmonic distortion appears around twice the switching frequency and its multiples. The consequence is an increase of the output filter size, cost, and weight [38].

To overcome this issue, a variable-angle phase-shifted PWM (VAPS-PWM) technique has been developed. This method adapts the angles between the carriers in order to eliminate the low frequency harmonic distortion under unbalanced operation. The method has been first developed for a CHB converter with three cells based on an analytical solution [38], [96]. However, as the number of cells increase, the analytical solution can be hard to obtain or even do not exist. Furthermore, these solutions only take into account the harmonic distortion located at $2f_{sw}$ and lets the other harmonics completely uncontrolled. This fact opens the way to explore other methods, for example, by looking for the angles that minimize a cost function that not only include the harmonic around $2f_{sw}$ but also other harmonic of interest (e.g., around $4f_{sw}$) [97], [98], [39]. In this regard, future research shall focus on how algorithms such as numerical computation approaches, metaheuristic searching algorithms, and others can be used to face this kind of multi-objective, multi-variable cost function in real time [99]. Of course, these methods shall be evaluated under realistic mission profile and considering a wide range of power imbalance between the cells.

2) RENEWABLE ENERGY APPLICATIONS

In renewable energy systems, such as wind power or photovoltaic converters, there are various ATC strategies that can be employed as have been illustrated in the literature review throughout this article. Although, the promising approaches to meet the high reliability requirements in these applications are the active power sharing and reactive power circulation among parallel converters and profile shaping via hybrid power control [7]. These control possibilities offer wide loss manipulation range, as they influence both switching and conduction losses, and thus can reduce the thermal stress considerably.

Reactive power circulation among parallel connected converters reduces thermal cycling by increasing the losses during light load conditions. A drawback, however, that still need careful consideration is its large impact on the power losses. Setting a lower reference ΔT_j can further improve the lifetime. However, the impact is higher power losses and reduced efficiency because the ATC will be more engaged in order to smooth these small temperature swings. Therefore, it is highly desirable in this case to reduce the ATC intervention, but without losing the benefit of the improved lifetime. In other words, the best reference ΔT_j at which the benefits of increased lifetime outweigh the disadvantage of reduced energy yield due to increased losses, should be investigated from an economical viewpoint. Future research can address these conflicting goals by using indicators such as the return on investment (ROI) [33] and thermal control efficiency (η_{tc}) [13]. For example, the ROI using reactive power control is the ratio between the extended lifetime to the reduced efficiency under a specific reference ΔT_j. These indicators have been employed to find the best reference ΔT_j under switching frequency control for wind power applications, and thus, it's interesting to see how they can be used to find the best trade-off under reactive power control.

On the other hand, the reduced energy yields under hybrid power control still needs to be justified in comparison with the benefits. Hybrid power control not only improve the lifetime of the converter but also reduce the replacement cost of the system as have been demonstrated in [12]. An interesting future research in this regard is the determination of the best trade-off between the lifetime and the energy yield considering the overall cost (including the replacement cost). The optimum power limit, once the controller moves from MPPT to CPG, can be determined based on a multi-objective optimization that minimize the lifecycle cost while maximizing the lifetime under a given mission profile.

3) ELECTRIC VEHICLE APPLICATIONS

Although, the two-level voltage source converter is still the prevailing traction drive technology in light and heavy-duty electric vehicles, the multi-level converter, especially the NPC converter, is seen as a promising solution to overcome some of the challenges in this industry.

The trend in light and heavy-duty electric vehicle applications is to move into higher dc-bus voltages (i.e., 800 V instead of the currently prevailing 400 V systems). This offers several advantages, such as the enabling of extreme fast charging and the possibility to reduce the size and weight of the cabling required to transfer a certain amount of power. In addition, operating at higher voltages can reduce the current required by the motor, and thus leads to higher motor efficiency. However, there are also some challenges of employing higher voltage which includes high *dv/dt* stress and larger switching loss of the devices. The *dv/dt* issue can be even more serious with modern inverters that uses wide band gab (WBG) devices with faster transitions. The Multilevel inverter, such as NPC inverter, can compensate these two issues by employing low-voltage devices and reducing *dv/dt* transitions [100], [101].

However, as previously mentioned, the drawback of the NPC topology is the unequal thermal stress distribution among the devices. This can deteriorate the power density and increase the cost of the converter because the maximum achievable output power will be limited by the junction temperature of the hottest devices.

Thermal balancing between devices in NPC converters have been investigated for many applications, such as the grid side converter in wind power applications [70], electric train application [61], and others. However, the thermal balancing of multi-level converter devices in electric vehicle applications can be more challenging due the wide speed and torque variations and the frequent operation under low speed and high torque conditions. Under low speed operations, the junction temperature shows larger fluctuations and reach higher peak values compared to the same torque level at higher speeds [102], [34]. Therefore, causing the temperature of the hottest devices to go even higher. An efficient ATC for multi-level converters in these applications shall ensure the reduced and balanced stress among the devices at all operating conditions. This requirement together with other requirements, such the voltage balancing of capacitors, can be simply satisfied with FCS-MPC. However, a major drawback of FCS-MPC is the secondary weighting factors tuning. Future research shall focus on the design of weighting factors which can achieve the best trade-off between the electric drive performance (e.g., reference tracking and torque ripple) and thermal balancing for multi-level converters in electric vehicle applications. Moreover, the design of dynamic weighting factors is also a possibility to realize this trade-off [61], [60].

B. IMPROVING THE ACCURACY AND BANDWIDTH OF TEMPERATURE DATA

Obtaining temperature information with high accuracy, zero phase lag, and high bandwidth is of high importance for the realization of ATC. However, with most of the existing temperature extraction methods it is difficult to meet these requirements. As mentioned previously, TSEPs often inherently comes with low temperature sensitivity and low signal to noise ratio. The sufficient sensitivity of some TSEPs only during certain operating point limits their use as a single temperature measurement technology. In addition, the high sensitivity to noise and the intermittency in the temperature measurements may require low pass filtering which strongly reduce the bandwidth and introduce phase lags in the temperature information. On the other hand, thermal predictors are too sensitive to inaccuracies and their loss models requires large calibration effort. Furthermore, the parasitic and characteristics of the devices in different converters, even those realized with the same power modules, vary. This means that the loss model shall be calibrated for every converter individually, which makes the process costly and unfeasible for the majority of applications [51].

Thermal observers can compensate for these inaccuracies. However, the potential of the observer depends on the feedback bandwidth that is designed considering the temperature measurement technology. Therefore, for the successful implementation of the thermal observer as a temperature monitoring technique, the accuracy and bandwidth of the measurement technologies shall be improved. For instance, Sensor fusion in which two or more measurement technologies are combined in one sensing solution, is demonstrated as a possible solution to improve the accuracy and precision of the temperature data. An interesting research topic as stated in [49] is to investigate how observers can combine several measurement technologies (e.g., several TSEPs), in one sensing solution to increase the bandwidth, accuracy, and availability of the measured data.

Another interesting research topic is to investigate how the loss model can be substituted by a self-learning artificial neural network that shall after a small learning interval be able to estimate the losses precisely without the need for the large calibration effort.

C. CONSIDERING INTERACTIONS AMONG COMPONENTS

Interaction among different components is another important aspect that shall take more focus by future research on ATC. In fact, dc-bus capacitors are also reported as a fragile component in the power electronic system and the hotspot temperature is identified as the main stress factor [12]. An ATC strategy such as based on power routing, affect the converter loading and consequently can influence the thermal stress and the RUL of the capacitors. In this regard, few studies have employed the power routing between the different converters by talking into account the RUL of both the capacitors and power semiconductor devices in each converter, such as in dc microgrid applications [53], [87]. The study in [103] and [104] has gone further and demonstrated that the capacitor failure in an output parallel DAB converter is more dominant than the power semiconductors. It is concluded that the power routing among the different converters can be performed by only talking the capacitor damage into consideration.

Most ATC based on power routing do not account for the capacitor damage. This can impair the ATC capability especially if the capacitor damage dominates the converter reliability. Therefore, a question that shall be raised in every application is whether the capacitor damage is worth to be considered in the power routing strategy. Moreover, it has to be demonstrated how the reliability of the system can be influenced in the two cases (i.e., with and without considering the capacitor damage).

D. INTELLIGENT MONITORING AND MAINTENANCE AS AN ENABLING TECHNOLOGY FOR NEXT GENERATION WIDE BAND GAB DEVICES

With the rapid development of semiconductor technology, wide-band gab (WBG) semiconductor devices such as silicon carbide (SiC) has been recognized as next-generation power semiconductors. The low losses, high switching frequency, high blocking voltage, and high operating temperature compered to Si based devices are advantages that can bring considerable performance improvement to many systems and applications [105], [106].

Despite the above-mentioned advantages, SiC devices are still slowly penetrating into the market. One of the reasons can be the high selling price of SiC MOSFETs, which is around 4 to 5 times higher than Si counterparts [8]. Another important reason is that the packaging reliability of SiC power

modules is not so promising and the field reliability has not been demonstrated in various applications. It is reported in [2] that the SiC MOSFETs have lower thermal cycling capability compered Si IGBTs with conventional packaging. There are mainly two reasons for this. First, SiC devices can be made with much smaller sizes compered to Si devices with the same voltage and current rating. While this allows for more compact power modules, it results in poorer thermal heat dissipation path with larger thermal resistance and smaller thermal capacitance. Correspondingly, larger temperature variation for SiC devices compared to Si ones at the same power level is anticipated [8]. The second reason is related to the mechanical properties of the SiC power module. SiC material is much stiffer and has higher Young's modulus compered to Si counterparts. This would bring in larger stress to the solder interface between the SiC chip and the substrate during thermal cycling, and thus the crack initiation would be more likely to occur [107]. Another possible reason for the slow penetration of SiC devices is related to their current packaging structures which can't exploit their full capability. For example, despite their high temperature capability, the commercially available SiC power modules still have a maximum junction temperature around 175 °C. This is in fact not because of the device itself, which can withstand more than 500 °C according to theoretical studies, but rather because of the components and materials that make the package which are not suitable for high temperature operation (>200 °C) [8], [108].

From the previous discussion it is evident that more advanced packaging technologies and cooling systems and probably thermal monitoring and control strategies are indispensable to exploit the full capability of the SiC devices, reduce the cost, and achieve the desired reliability of the applications. Advanced packaging technologies and cooling strategies that can decrease the thermal resistance, increase thermal cycling reliability, and post the peak temperature capability of the module have been summarized in [2] and [8]. On the other hand, Intelligent monitoring and maintenance (IMM) technologies that are capable of reducing the cost by reducing the design margins and increasing the lifetime of power electronic system are proposed [109]. This is an emerging principle, which include broad spectrum of technologies as shown in Fig. 21 and is intended for monitoring and maintenance of power electronic systems in high reliability applications in the future. The cost of implementing such system depends on the applied technology. The least implementation effort can be performed with thermal predictors and empirical lifetime models as shown in Fig. 7. In this case, the additional cost is only due to the additional computational power required. However, it is evident that the models are not highly accurate, and thus the design margins can't be completely eliminated. On the other hand, by combining models with sensors more accurate thermal monitoring and lifetime estimation is possible. For example, thermal observers can be used for temperature measurements, while failure precursor parameters such as on-state resistance R_{ON} of MOSFET can be used to update the lifetime models parameters in real-time

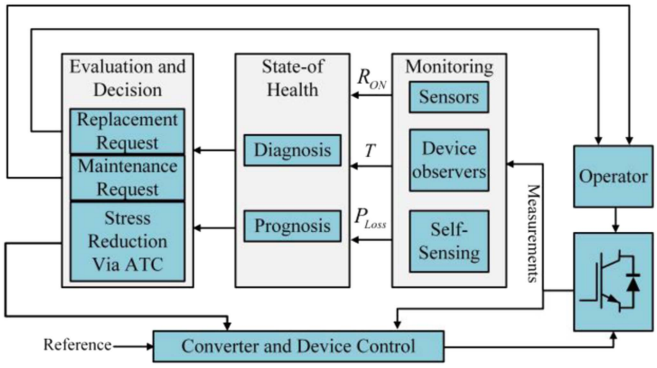

FIGURE 21. High performance monitoring and maintenance of power converters [109].

[110]. With such technology, the lifetime of the system can be increased by operating the power converters up to their critical limits rather than replacing them based on the B_1 or B_{10} lifetimes that are estimated during the design stage. Furthermore, ATC can be used to delay the failure in the weakest part allowing for even higher lifetime improvement. For more acceptance of the IMM as an enabling technology for future WBG devices, the following two topics must be investigated.

First, the validity of the IMM have been investigated on an IGBT modules. However, it is highly desirable to investigate the performance improvement on future WBG devices. Furthermore, the economical impact and the best implementation effort shall be investigated for every application individually. This is because for some applications like reliability critical applications (e.g., aerospace or automotive) and cost critical applications (e.g., off-shore wind applications where maintenance cost is high) the cost of the extra sensors may be justified. However, for maintainable applications such as in power systems, the best economical choice may be to employ the technology with less implementation effort (i.e., less number of sensors). This is due to the fact that in this case availability is the measure of system performance [10].

Second, the lifetime extension due to ATC part in the IMM shall be validated experimentally based on WBG devices. Experimental validation of lifetime enhancement is in fact one of the limitations in all referenced ATC strategies in this paper. Even ATC which directly targets lifetime equalization and lifetime enhancement are only validated in simulation. Future research can address this limitation through load emulators, which allow performing the tests based on more realistic mission profiles and more realistic accelerated aging tests. Furthermore, most of the ATC strategies in the literature are based on Si MOSFETs and Si IGBTs. Future research shall give more attention to WBG devices, which are expected to dominate the market in the future.

VI. CONCLUSION

ATC is a promising technique to address the continuous demands of low cost, small size, and high reliable power electronics. It also enables the reduction of the replacement cost

and optimization of the maintenance schedule in power system applications. These benefits are realized by controlling the main critical stressor of power semiconductors, the junction temperature, during real-time operation. The control actions can happen at different levels, starting from the device level at the snubber circuit and gate driver to the converter level at the control and modulation stages and finally to the system level where the real and reactive power reference among parallel or modular converters can be exploited.

Although, in order to make ATC widely applicable, there are still several challenges that must be addressed by future research. Among them is minimizing the impact of ATC strategies on the system performance. In fact, many ATC strategies that features large loss manipulation range and consequently large impact on the thermal stress, such as the reactive power circulation and hybrid power control, still have not been justified in terms of their impact on the energy yields and power losses. Similarly, the mitigation of the adverse impacts of unequal power sharing on the current and voltage quality in CHB and interleaved converters still need to be further investigated. These and others are discussed throughout this article and a motivation to mitigate their impact with optimization and other algorithms are also discussed. Other challenges which have been discussed in this article include the extraction of high bandwidth and highly accurate temperature information and the consideration of other reliability critical components, such as the dc-bus capacitors. Finally, the reliability challenges with the next-generation WBG devices are introduced and the potential to address them with high performance monitoring and maintenance technologies are discussed.

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