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A Negative Sequence Impedance Design and Regulation Strategy for Negative Sequence Current Sharing Among Grid-Forming Sources in Microgrids Considering Topology Impacts

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ABSTRACT The accurate control of negative sequence (NS) current distribution among multiple grid-forming (GFM) sources can lower the requirement on NS current capability of the sources. Existing control approaches mainly focus on microgrids (MGs) with fixed points of common couplings and on only the NS current distribution among inverter-based resources (IBRs). As MG configuration has been rapidly evolving to be more complicated, it is critical to take into consideration the impact of MG topologies on the NS current sharing. Moreover, synchronous generators (SGs) are still commonly applied as sources in MGs. The NS current distribution among IBRs and SGs also needs to be considered. In this paper, a novel NS impedance design and regulation approach is proposed to achieve accurate and flexible NS current sharing among different GFM sources (IBRs and SGs). The approach accounts for MG topology impacts by including MG's NS admittance matrix in the impedance design. The effectiveness of the proposed approach is evaluated through simulations and compared to existing solutions in a MG with four different source locations. Results show improved flexibility and accuracy in NS current sharing when MG topology impacts are considered. The proposed approach is also validated through experimental testing on a converter-based hardware testbed.

INDEX TERMS Negative sequence current distribution, grid-forming inverters, synchronous generators, virtual impedance control.

I. INTRODUCTION

Load unbalance is a common occurrence in an ac microgrid (MG), leading to negative sequence (NS) and zero sequence (ZS) currents [1]. An islanded MG is usually formed by distributed energy resources (DERs), including synchronous generators (SGs) and/or inverter-based resources (IBRs) with grid-forming (GFM) inverters [2]. Unbalanced loads require sufficient NS current capability of DERs. In a MG with multiple sources, to meet the unbalanced load current needs, overdesigning the NS capabilities of all sources is usually a direct solution, but it is not cost-efficient [3]. Accurate control of NS current sharing among sources enables the distribution of NS currents among sources with a specific objective, allowing for lower but safe NS current requirements on individual sources.

For IBRs with GFM inverters, it is difficult to achieve precise and controllable NS current sharing as their output power is dependent on the load and other conditions within the MG. While synchronous generators (SGs) also function as GFM sources in a MG, they provide less control flexibility compared to IBRs. Achieving controllable NS current sharing among IBRs and SGs becomes even more challenging.

From the system perspective, different from conventional MGs that usually have fixed points of common couplings (PCCs), MGs are evolving to include more complicated topologies and configurations, such as MGs with dynamic PCCs [4], MGs with multiple source buses [5], [6], and networked MGs [7]. In these MGs, the NS currents have multiple paths to result in a more complicated NS current distribution. Meanwhile, in the MG with dynamic PCC, the MG topology can be changed during the operation, as a result, the NS current sharing can be significantly changed. To deal with these issues, controlling the NS current sharing considering the topology impacts becomes critical.

In the existing literature, numerous research efforts have been spent on the NS current sharing among GFM inverters. NS impedance-based approaches have been proposed to realize accurate sharing of NS currents. A negative NS reactive power (Q^-) and NS impedance (Z^-) based droop control is proposed in [8] to realize the NS power sharing based on a predefined Q^--Z^- droop curve. However, due to the impedance mismatch caused by MG lines, these methods cannot guarantee accurate sharing. To mitigate the impact of line impedance, a secondary control strategy is applied to compensate for the DER power mismatch [9] but such secondary NS control is not applicable to SGs.

To deal with the line impedance impacts of the Q^--Z^- droop, adaptive virtual impedance control is applied to directly control the NS impedance for unbalanced power sharing [10], [11], [12], [13], [14]. A small signal injection-based virtual NS impedance control is proposed in [10], [11] to share the NS current based on a proposed droop relationship between NS power and the injected small signal. However, this approach still targeted MGs with fixed PCCs and cannot be implemented on SGs. Ref. [12] reshaped the NS impedance based on transient real power variation. Ref. [13] compensated for the impedance mismatch by regulating the inverter's virtual impedance through reactive power correction. Ref. [14] regulated the NS impedance based on the output NS current of the DER considering different X/R ratios of the DERs' tied lines. Ref. [15] proposed a four-stage strategy to regulate the NS impedance iteratively. Ref [16] proposed an event-triggered, centralized NS impedance strategy to regulate the NS impedance based on neighbor DER's information. Ref [17] proposed a consensus-based strategy to adjust DERs' NS virtual impedance and the unbalanced power sharing is realized through communication between two neighboring DERs. Ref [18] utilized NS voltage injections to compensate NS voltage and realize power sharing. All the approaches in [10], [11], [12], [13], [14], [15], [16], [17], [18] aim at compensating for line impedances between the DER output and a fixed PCC, which are not sufficient for accurate unbalanced power sharing in a MG that has a dynamic PCC. Meanwhile, the NS current sharing with SGs has not been considered in [10], [11], [12], [13], [14], [15], [16], [17], [18].

Furthermore, in recent years, the impact of MG topology on DER power distribution has received attention. Ref. [19] proposed a secondary control-based Q^-- Z^- droop strategy to share unbalanced power and limit the voltage unbalance of critical load buses. However, this approach does not consider the unbalanced power sharing with SGs, and fast communication links among DERs are needed. Ref. [20] proposed a predictive secondary control to realize unbalanced power sharing by directly regulating and coordinating the single-phase reactive power through a communication link. However, direct single-phase control requires four-wire sources, and the three-phase currents of a three-wire source are not independent ($i_a + i_b + i_c = 0$). Ref. [21] proposed a virtual impedance optimization design method to realize the reactive power sharing in networked MGs. An extended impedance-power droop control approach is adopted in [22] to deal with reactive power sharing in a multi-bus MG. However, in [21] and [22], the unbalanced load impacts are not considered. Moreover, existing solutions are mainly designed to support a certain NS current sharing objective. With different source and load conditions, the NS current sharing strategy can be different.

In response to the aforementioned research gaps, a NS impedance design and regulation strategy is proposed to take into consideration the impact of MG topology and the NS power sharing among IBRs and SGs. The proposed approach solves the NS current distribution issue from the NS impedance design perspective that accounts for both IBRs and SGs. Meanwhile, the impact of topology is also considered by introducing the admittance matrix of the NS network of the MG into the impedance design. The proposed approach is verified in simulation and demonstrated on a converter-based hardware testbed (HTB) [23]. The main contributions of this paper can be summarized as follows:

1) A NS impedance design and regulation approach for GFM sources is proposed, which can be used to achieve different NS current distribution objectives.
2) The impact of MG topology is considered in the impedance design to realize accurate unbalanced power sharing in MGs with dynamic PCCs or even networked MGs.
3) The proposed approach can control the NS current sharing among inverters and SGs.

The rest of the paper is organized as follows: The MG unbalanced load sharing analysis is discussed in Section II. The proposed strategy is presented in Section III. The simulation verification and experimental demonstration are provided in Sections IV and V, respectively. The conclusion is drawn in Section VI.

II. UNBALANCED LOAD IN A MG

An example MG is shown in Fig. 1, which includes multiple DERs at different locations and has no fixed PCC. In islanded mode, since the grid is disconnected, the voltage and frequency will be maintained by DERs. Existing DERs are usually three-wire sources, which do not provide the MG with a neutral line. A grounding transformer is applied to form the neutral of the MG [24], [25]. Due to the simultaneously served single-phase, and three-phase loads, the phase current will be unbalanced in an islanded MG. In this scenario, the

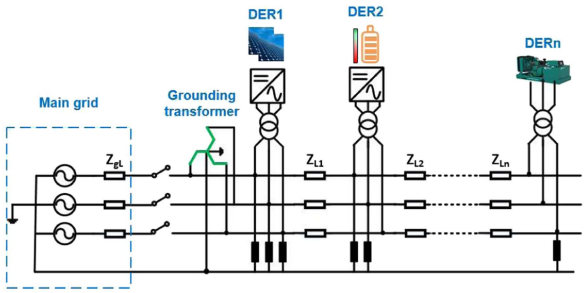

FIGURE 1. MG with DERs at different locations.

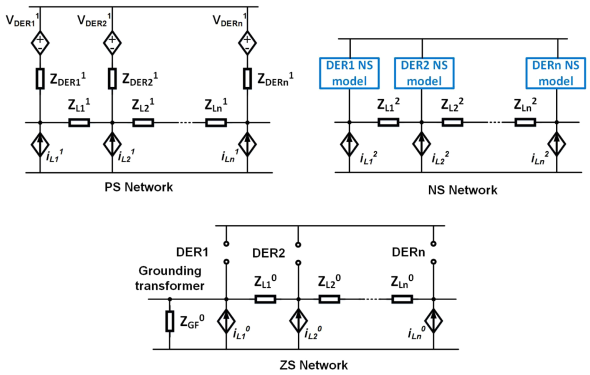

FIGURE 2. Sequence networks: (a) PS network; (b) NS network; (c) ZS network.

NS currents will flow into sources and ZS currents will flow into grounding transformers.

In order to effectively analyze the unbalanced load current distribution in a MG, the impact of MG topology must be considered. The MG can be decomposed to be positive sequence (PS), NS, and ZS networks, which are shown in Fig. 2. In all the networks, the loads are modeled as current sources [26]. In the PS network, since the control target for a GFM source is usually to balance the output voltage, the sources in the PS network can be modeled as controlled voltage sources plus impedances (transformer impedances and/or added virtual impedances if needed). In the ZS network, since the ZS currents are all provided by the grounding transformer, there is no voltage source in the ZS network and all the ZS current will flow into the grounding transformer.

In the NS network, the NS current distribution will be impacted by the line impedances, topology connections, source NS impedances, and source control strategies. For example, If the sources control their output NS voltages, there will be voltage sources in the NS network. In order to realize controllable NS current distribution, all these impact factors need to be considered in a coordinated manner.

III. PROPOSED NS CURRENT DISTRIBUTION CONTROL STRATEGY

A. DER NS PERFORMANCE

1) SYNCHRONOUS GENERATOR

The NS performance of a SG can be modeled as an impedance, which is shown in Fig. 3. The generator

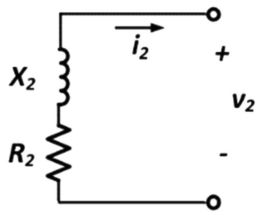

FIGURE 3. NS model of a synchronous generator.

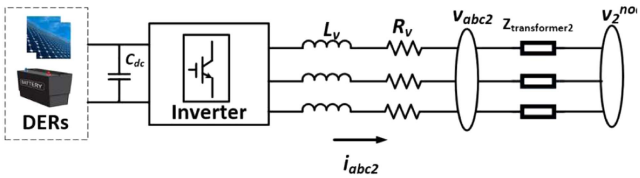

FIGURE 4. Inverter with NS virtual resistance and inductance.

impedance is written as [27]

$$Z_{SG(2)} = R_2 + jX_2 \tag{1}$$

where $X_2 = \frac{X''_d + X''_q}{2}$, $R_2 \approx R_a + \frac{R_r}{2}$. X''_d and X''_q are the sub-transient reactance of the generator, and R_a and R_r are the stator and rotor resistance. The typical range of X''_d, X''_q and R_a are defined as:

$$\begin{cases} R_2^{\min} \le R_2 \le R_2^{\max} \\ X_2^{\min} \le X_2 \le X_2^{\max} \end{cases} pu \tag{2}$$

where $R_2^{\min}$, $R_2^{\max}$, $X_2^{\min}$ and $X_2^{\max}$ are the minimum and maximum requirements of SG's impedance. For large SGs in [27], these values are $R_2^{\min} = 0.0015$, $R_2^{\max} = 0.005$, $X_2^{\min} = 0.12$, and $X_2^{\max} = 0.25$.

2) GFM INVERTER

The NS performance of a GFM inverter is highly related to its control strategy. To be consistent with the SG, the inverter's NS control target is assigned to be impedance. Since the generator's NS model can be viewed as an inductor plus a resistor, the NS control of the inverter also needs to achieve virtual inductance and resistance. The NS current $\boldsymbol{i_{abc2}}$ in Fig. 4 can be written as:

$$\begin{cases} i_{a2} = I_2 \cos(\omega t + \theta_2) \\ i_{b2} = I_2 \cos\left(\omega t + \theta_2 + \frac{2\pi}{3}\right) \\ i_{c2} = I_2 \cos\left(\omega t + \theta_2 - \frac{2\pi}{3}\right) \end{cases} \tag{3}$$

As shown in Fig. 4, if a NS virtual inductance and resistance are applied, when the current in (3) flows through a virtual inductance and resistance, the NS voltage drop is:

$$\begin{cases} v_{av2} = R_v I_2 \cos(\omega t + \theta_2) - \omega L_v \sin(\omega t + \theta_2) \\ v_{bv2} = R_v I_2 \cos\left(\omega t + \theta_2 + \frac{2\pi}{3}\right) - \omega L_v \sin\left(\omega t + \theta_2 + \frac{2\pi}{3}\right) \\ v_{cv2} = R_v I_2 \cos\left(\omega t + \theta_2 - \frac{2\pi}{3}\right) - \omega L_v \sin\left(\omega t + \theta_2 - \frac{2\pi}{3}\right) \end{cases} \tag{4}$$

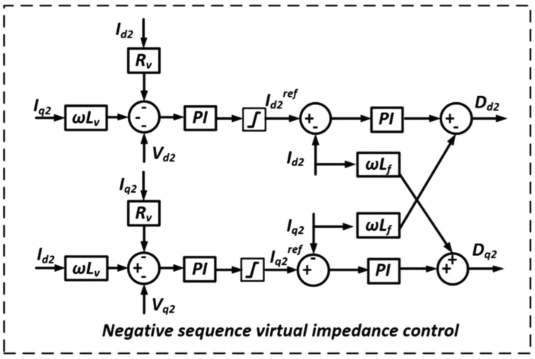

FIGURE 5. NS virtual inductance and resistance control diagram.

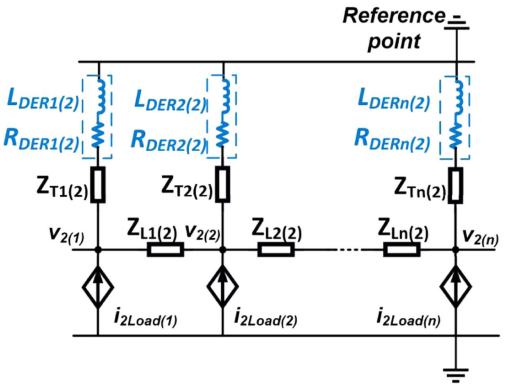

FIGURE 6. NS network when all the sources can be modeled as an impedance.

where R_v and L_v are the virtual resistance and inductance, respectively. Considering the NS dq transformation, the transformation matrix can be written as:

$$T_{dq2} = \frac{2}{3}\begin{bmatrix} \cos\omega t & \cos\left(\omega t + \frac{2\pi}{3}\right) & \cos\left(\omega t - \frac{2\pi}{3}\right) \\ \sin\omega t & \sin\left(\omega t + \frac{2\pi}{3}\right) & \sin\left(\omega t - \frac{2\pi}{3}\right) \end{bmatrix} \tag{5}$$

After the NS dq transformation, the current and voltage drop in (3) and (4) will become:

$$\begin{cases} I_{d2} = I_2 \cos\theta_2 \\ I_{q2} = -I_2 \sin\theta_2 \end{cases} \tag{6}$$

$$\begin{cases} V_{dv2} = R_v I_{d2} + \omega L_v I_{q2} \\ V_{qv2} = R_v I_{q2} - \omega L_v I_{d2} \end{cases} \tag{7}$$

Assuming the inverter current direction is flowing out of the inverter and considering the virtual impedance, the inverter NS output voltage is:

$$\boldsymbol{v}_{\boldsymbol{abc}2} = -[v_{av2}, v_{bv2}, v_{cv2}]^T \tag{8}$$

where $\boldsymbol{v}_{\boldsymbol{abc}2}$ is the inverter output voltage after the virtual impedance. Therefore, the inverter NS impedance control diagram is shown in Fig. 5.

Based on the SG NS model and inverter's NS control design, the NS network can be viewed as load current injections and impedances, as shown in Fig. 6. Mathematically, both the real and imaginary parts of inverters' NS impedances can be positive or negative. In the NS network, the DER is connected to the rest of the system through the transformer. The equivalent NS impedance of the DER is the inverter's NS impedance plus the transformer's NS impedance. If the DER's equivalent NS impedance (inverter plus transformer) is capacitive or has negative resistance, the system damping capability will be decreased to affect the system stability [28]. To reduce the impact on the rest of the system, the DER's equivalent NS impedance should be inductive and have positive resistance. The range of the inverter's NS impedance is given as:

$$\begin{cases} R_v \geq -R_T \\ L_v \geq -L_T \end{cases} \tag{9}$$

where R_T and L_T are the normalized equivalent resistance and inductance of the inverter's step-up transformer, respectively.

B. MG TOPOLOGY IMPACT ANALYSIS

According to Fig. 6, the NS network is composed of current injections and impedances. To analyze the NS current distribution, the admittance matrix is introduced. The admittance matrix includes information on the network connection and line impedances, which can describe MG's topology impacts. For a MG with n buses, since all the DERs are modeled as impedances, the NS network can be described as:

$$\begin{bmatrix} v_{2(1)} \\ \vdots \\ v_{2(n)} \end{bmatrix} = \begin{bmatrix} Y_{11} & \cdots & Y_{1n} \\ \vdots & \ddots & \vdots \\ Y_{n1} & \cdots & Y_{nn} \end{bmatrix}^{-1} \begin{bmatrix} i_{2Load(1)} \\ \vdots \\ i_{2Load(n)} \end{bmatrix} \tag{10}$$

where $Y_{ij} = \begin{cases} y_{i0} + \sum_{m=1, m\neq i}^{n} y_{im}, i = j \\ -y_{ij}, i \neq j \end{cases}$, $y_{ij} = \frac{1}{Z_{ij}}$ is the admittance between node i and j; $v_{i(2)}$ is the NS voltage of node i; $y_{i0} = \frac{1}{Z_{i0}}$ is the admittance between node i and the reference point (ground point in the circuit). Note that the DER NS impedances are covered in the admittance matrix. By solving the node NS voltage, the NS current distribution can be determined.

C. NS IMPEDANCE DESIGN METHODOLOGY

The proposed methodology is to design and implement the NS impedance of DERs considering the SGs and MG topology impacts. The overall NS impedance design methodology is summarized in Fig. 7, including MG information gathering, NS current distribution objective determination, NS network formulation, NS impedance calculation, and NS impedance realization.

1) MG INFORMATION GATHERING

The MG information is gathered first for the NS impedance design, which is summarized as follows:

- MG topology (connection and line impedances)
- DER inverter rating (overall rating and NS rating)
- Load (historical data or forecasting results)

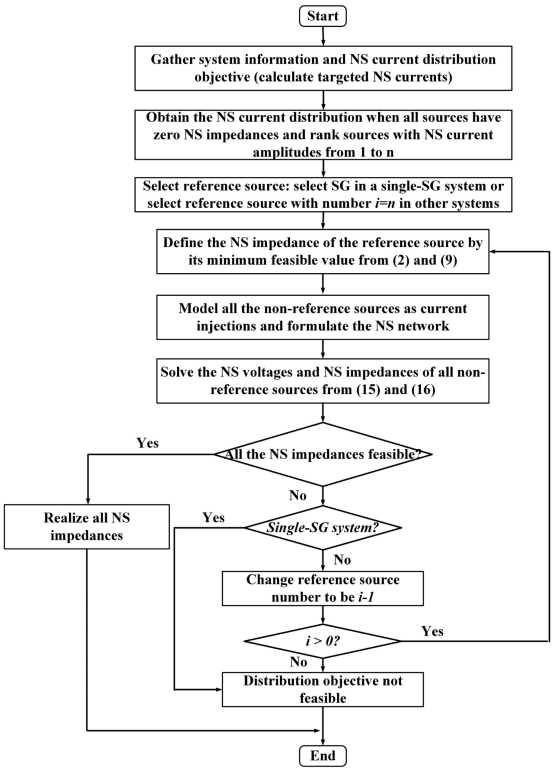

FIGURE 7. NS impedance design process.

Note that the NS current ratings of DER inverters are gathered because the NS rating of inverters can be significantly different from the overall rating. Meanwhile, in a MG, the load condition is time-variant. The controllable NS current distribution needs to consider different load conditions. Load forecasting technology is developing rapidly, and high forecasting accuracy can be achieved [29]. The NS impedance design is conducted for all the forecasted load conditions to generate a look-up table of DER NS impedances.

2) TARGETED NS CURRENTS CALCULATION

The targeted NS currents of different sources are calculated by total loads and NS current distribution strategies. The distribution objectives are usually determined through system planning to achieve certain operation targets (economic operation, reliable operation, etc.). The proposed approach is applicable to different NS current distribution objectives. For a given distribution objective, the inverter NS impedance is designed correspondingly to realize the target.

In this paper, two examples of NS current distribution targets are utilized. The first one is sharing in proportion to source' NS current rating because the NS current rating is the actual NS capability of a source. The distribution objective is:

$$\sum_{j=1}^{n} i_{2Load(j)} = \sum_{j=1}^{n} i_{2DER(j)} \tag{11}$$

$$\frac{i_{2DER(j)}}{i_{2DER(m)}} = \frac{i_{2DER(j)}^{Rat}}{i_{2DER(m)}^{Rat}} \tag{12}$$

where $i_{2Load(j)}$ is the NS current is load j; $i_{2DER(j)}$ is the NS current output of DER j; $i_{2DER(j)}^{Rat}$ is the NS current rating of DER j. The second example strategy is to realize a balanced SG current, meaning that the NS currents are provided by the inverters and the inverters share the NS current equally.

Moreover, if the total load NS current is higher than the total inverter NS current rating, then load change, or compensation is needed to reduce the load unbalance. The NS impedance design will be conducted after load restoration/compensation is finished. For the targeted NS current calculation, the NS currents of sources are known from (11). Meanwhile, the relationships of different sources' NS currents are determined by the distribution objectives such as (12). Therefore, according to these known factors, the targeted NS currents of inverters can be solved.

3) NS NETWORK FORMULATION

Considering a node of the inverter, as shown in Fig. 4, the node NS voltage can be calculated as:

$$v_2^{node} = -i_{abc2}\left(R_v + j\omega L_v + Z_{transformer2}\right) \tag{13}$$

where $Z_{transformer2}$ is the NS impedance of the DER's step-up transformer. The NS currents are calculated from (11) and the NS sharing objective. According to (13), the inverters' NS impedances can be obtained if the node NS voltages can be solved.

To solve the NS voltages, inverters are considered as current sources, and the NS network equations will be reformulated using current injections and line impedances. Since all the NS sources are modeled as current injections, the sources' transformers are not included in the admittance matrix. For each entry in the admittance matrix, y_{i0} in (10) will be zero. In this condition, in (10), for the ith row,

$$\sum_{j=1}^{n} Y_{ij} = 0 \tag{14}$$

The admittance matrix in (10) will not be invertible and the node voltages cannot be solved. To deal with this issue, at least the node voltage of one of the sources needs to be known. In this paper, one of the sources (reference source) in the system will be modeled as an impedance with a predefined value in the NS network to ensure that the admittance matrix of the NS network is invertible.

To select the source that will be modeled as an impedance, the NS network condition and source types are considered. When all the sources are IBRs, their NS impedances can be regulated through control. In this case, assuming all the sources have zero NS impedance, the NS network is composed of line NS impedances, transformer NS impedances, and load current injections. The NS current distribution is determined by the line and transformer impedances. The amplitudes of the NS currents of different sources are ranked, and

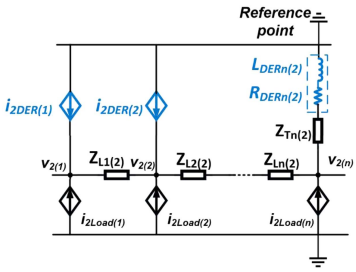

FIGURE 8. NS network after sources are modeled as current injections.

the sources will be labeled by the NS current ranking. For a MG with n sources, the one with the least NS current will be labeled as source n and the one with the most NS current will be labeled as 1.

The source with the least NS currents can be viewed as having the maximum equivalent NS impedance from the network. This source is considered as having the least NS impedance design flexibility compared to other sources. Therefore, this source (source n) is selected as the first reference source with its NS impedance predefined by its minimum value from (9).

The NS impedances of SGs cannot be flexibly regulated through the control. They are realized through hardware design. Therefore, when the MG contains SGs, two scenarios are considered: single-SG case and multiple-SG case. In the single-SG case, the SG will be selected as the reference source and its impedance is selected to be its minimum value from (2). In this case, the SG's impedance is determined, and the impedance design will be conducted to IBRs under different load conditions to generate the look-up table of NS impedances. In the multiple-SG case, the impedance design of SGs will be based on the worst unbalanced load condition. The reference source selection follows the approach in the case where all the sources are IBRs. The impedance of the reference source is predefined by its minimum value from (2) or (9).

After the reference source is selected, the rest of the sources can all be modeled as current injections in the NS network. In Fig. 8, after ranking and labeling, the *nth* source is the reference source, and the NS voltages of different nodes are solved as:

$$\begin{bmatrix} v_{2(1)} \\ v_{2(2)} \\ \vdots \\ v_{2(n)} \end{bmatrix} = \begin{bmatrix} Y'_{11} & \cdots & Y'_{1n} \\ Y'_{21} & & Y'_{n1} \\ \vdots & \ddots & \vdots \\ Y'_{n1} & \cdots & Y'_{nn} \end{bmatrix}^{-1} \begin{bmatrix} i_{2Load(1)} + i_{2DER(1)} \\ i_{2Load(2)} + i_{2DER(2)} \\ \vdots \\ i_{2Load(n)} \end{bmatrix} \tag{15}$$

where the NS impedance of the reference source is included in the updated admittance matrix Y'. When node NS voltages are calculated, the NS impedances are calculated as:

$$\begin{bmatrix} Z_{2inv(1)} \\ \vdots \\ Z_{2inv(n)} \end{bmatrix} = \begin{bmatrix} \frac{1}{i_{2DER(1)}} & \cdots & 0 \\ \vdots & \ddots & \vdots \\ 0 & \cdots & \frac{1}{i_{2DER(n)}} \end{bmatrix}^{-1} \begin{bmatrix} v_{2(1)} \\ \vdots \\ v_{2(n)} \end{bmatrix} \tag{16}$$

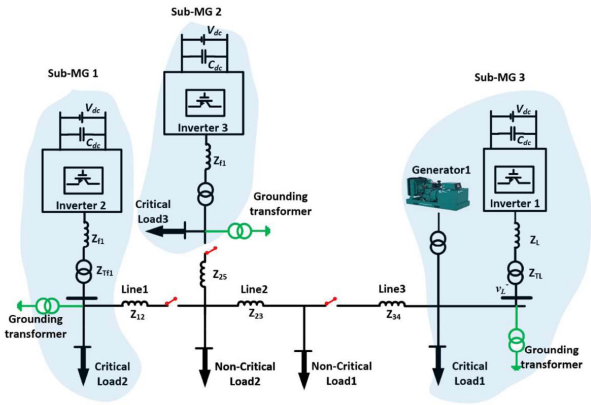

FIGURE 9. Microgrid topology in simulation.

In the multiple-SG case, under the non-worst unbalanced load conditions, at least one of the SGs will become non-reference sources. Since the SGs' NS impedances cannot be modified, the NS network (15) will become overdetermined. Eq. (16) may not have a solution. The most extreme scenario is that when all the sources are SGs, the NS current distribution cannot be changed once the SGs' NS impedances are selected. Therefore, in the multiple-SG case, the NS impedance design is only conducted to the worst unbalanced load conditions.

4) NS IMPEDANCE REALIZATION

The designed NS impedances will be realized by sources. For IBRs, the NS impedance will be realized by the control in Fig. 5. For SGs, the NS impedances should be realized by hardware design. However, according to (2) and (9), the NS impedances of sources have limitations. If the calculated NS impedances cannot meet the requirements in (2) and (9), the NS current distribution objective cannot be realized in this NS network.

In this case, different system configuration needs to be considered. In a single-SG system, the SG is selected to be the reference source, and the NS network is determined. If no feasible solution can be found, the distribution objective is viewed as not feasible.

In a purely IBR-based system or a multiple-SG system (the worst unbalanced load condition), the reference source will be changed to the source with label $n1$. Then the NS impedance calculation will be reconducted. If feasible NS impedances can be obtained for all the sources, the designed impedance will be realized. However, if no feasible solution can be found after all the sources have served as reference sources, the distribution objective is viewed as not feasible.

IV. SIMULATION VERIFICATION

The MG used for simulation verification is a MG with dynamic boundaries and multiple source locations [5], which contains three IBRs and one SG. As shown in Fig. 9, the example MG can have three different sub-MGs in the islanded

TABLE 1. Simulation Parameters

	Parameter values
Inverter 1	$V_{ac(l-l)} = 480\,V, S_{base} = 1120\,kVA$ $Q_{NS} = 180\,kVA, Z_T = 0.01 + j0.04$ (pu, Yg -Yg)
Inverter 2	$V_{ac(l-l)} = 480\,V, S_{base} = 1120\,kVA$ $Q_{NS} = 180\,kVar, Z_T = 0.01 + j0.04$ (pu, Yg -Yg)
Inverter 3	$V_{ac(l-l)} = 480\,V, S_{base} = 1120\,kVA$ $Q_{NS} = 360\,kVar, Z_T = 0.01 + j0.04$ (pu, Yg -Yg)
Generator electrical model	$X_d = 1.8\,(pu), X_q = 1.7\,(pu), R_a = 0.0015\,(pu)$ $X'_d = 0.3\ (pu)\ X'_q = 0.25\ (pu)$ $T'_{d0} = 8\,s, T'_{q0} = 0.4\,s, T''_{d0} = 0.03\,s, T''_{q0} = 0.05\,s$ $V_{ac(l-l)} = 480\,V, S_{base} = 560\,kVA$ $Q_{NS} = 90\,kVar, Z_T = 0.01 + j0.04$ (pu, Yg-Yg)
System information (12.47 kV)	CL 1: $P_a = 100\,kW, P_b = 200\,kW, P_c = 200\,kW$ NS current (rms): $I_{2(CL1)} = 4.63\angle 180.0^\circ$ CL 2: $P_a = 100\,kW, P_b = 300\,kW, P_c = 200\,kW$ NS current (rms): $I_{2(CL\ )} = 8.02\angle 150.0^\circ$ CL 3: $P_a = 120\,kW, P_b = 250\,kW, P_c = 200\,kW$ NS current (rms): $I_{2(CL3)} = 15.8\angle 157.6^\circ$ NCL 1: $P_a = 100\,kW, P_b = 50\,kW, P_c = 60\,kW$ NS current (rms): $I_{2(NCL1)} = 2.12\angle -10.9^\circ$ NCL 1: $P_a = 100\,kW, P_b = 250\,kW, P_c = 200\,kW$ NS current (rms): $I_{2(NCL2)} = 6.12\angle 160.9^\circ$ $Z_{12} = 0.3375 + j1.5699\,\Omega, Z_{23} = 0.1687 + j0.7849\,\Omega$ $Z_{34} = 0.3375 + j1.5699\,\Omega, Z_{35} = 0.0844 + j2.8421\,\Omega$

Note: DER transformers' ratios 1:25.98 and ratings are the same as sources; CL is for critical load; NCL is for non-critical load.

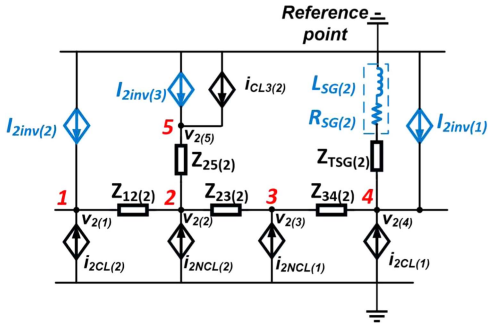

FIGURE 10. NS circuit of the microgrid in the simulation after inverters are modeled as current injections.

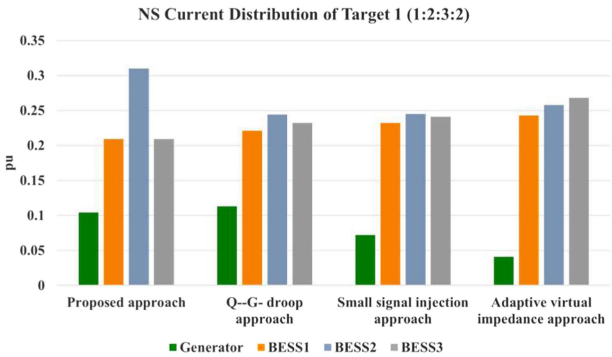

FIGURE 11. NS current distribution of target 1 (sharing in proportion to Source NS capabilities).

mode. When the three sub-MGs are merged into one MG, the unbalanced load in the MG will be supported by four sources simultaneously. The detailed system parameters are summarized in Table 1. The source NS capability is defined by the NS reactive power [10]. In the simulation, the synchronous machine model in Simulink is used to model Generator 1. Two different unbalanced current distribution objectives are realized: 1) sharing in proportion to source NS capabilities; 2) balancing generator output and equal sharing among three inverters. The NS current sharing performance will be compared with three other state-of-the-art strategies.

A. SHARING IN PROPORTION TO SOURCE NS CAPABILITIES

According to the load power, the NS load currents are calculated by assuming balanced load bus voltages. The NS currents are also summarized in Table 1. Based on the distribution objective, the targeted NS currents of four sources are $I_{2SG} = 2.69\angle -20.72^\circ A$, $I_{2inv(1)} = 5.83\angle -20.72^\circ A$ $I_{2inv(2)} = 8.07\angle -20.72^\circ A$, $I_{2inv(3)} = 5.83\angle -20.72^\circ A$

Meanwhile, this MG is a single-SG system, where the SG is selected as the reference source in the NS network with its minimum NS impedance $Z_{2SG} = 0.0015 + j0.12(pu)$. The formulation of the NS network is described in Fig. 10. According to (15)-(16), the normalized impedances of three inverters are:

$$\begin{cases} Z_{2inv(1)} = j0.12pu \\ Z_{2inv(2)} = 0.0036 + j0.0747pu \\ Z_{2inv(3)} = 0.0084 + j0.1325pu \end{cases} \quad (17)$$

where all the impedance values meet the requirement in (9).

The calculated impedances are implemented in the simulation model. The NS current distribution is summarized in Fig. 11. The current waveforms of four sources are shown in Fig. 12(a). With the same load and SG conditions, the control algorithms in [10], [11], and [14] are implemented in three inverters for comparison. The current waveforms are shown in Fig. 12(b)–(d), respectively. Since the NS rating ratio of sources is 1:2:2:3, the NS currents of sources should meet this ratio. From Fig. 12(a), using the proposed design approach, the NS current distribution matches the source NS rating ratio, while the other three existing approaches are not able to realize the desired distribution.

For the Q^--G^- droop approach in [10], the droop curve design follows the NS capability ratio of sources. The slope of inverter 2's Q^--G^- droop is set to be 1.5 times those of inverter 1 and inverter 3 so that inverter 2 can provide more NS current than the other two inverters. However, due to the topology and line impedance impacts, the Q^--G^- droop approach cannot realize this targeted distribution. For the small signal injection approach in [11], the fourth-order harmonics are injected. The

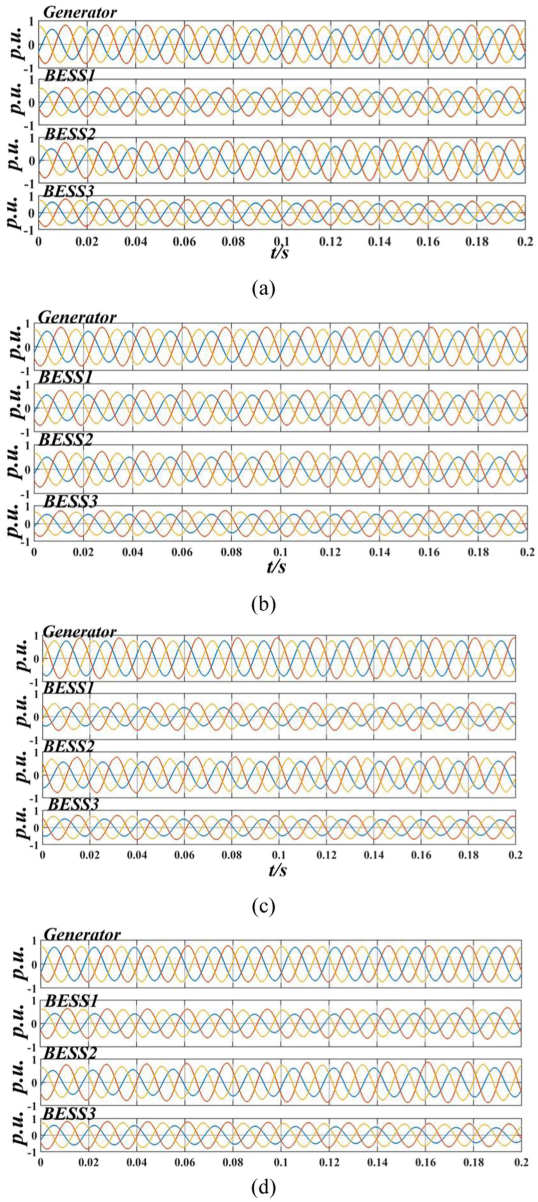

FIGURE 12. Current waveforms of target 1 (sharing in proportion to Source NS capabilities): (a) proposed approach; (b) Q-G droop approach; (c) small signal injection approach; (d) adaptive virtual impedance approach.

reference magnitude of the small signal injection is set to be 0.015 pu and the droop slope also considers the NS capability of sources. From the simulation results, the small signal injection approach also cannot achieve the distribution target. For the adaptive virtual impedance approach in [14], the adaptive virtual impedance design considers the NS capability ratio of sources. The regulation rate of inverter 2's virtual impedance is 1.5 times faster than the other two inverters. Inverters 1 and 3 have the same curves of adaptive virtual impedance. Meanwhile, this approach requires PCC currents for impedance control. Since the MG in the simulation does not have a fixed PCC, in this paper, the current after the DER transformer is used for impedance control. From the simulation results, the adaptive approach cannot fully compensate for the line and topology impacts.

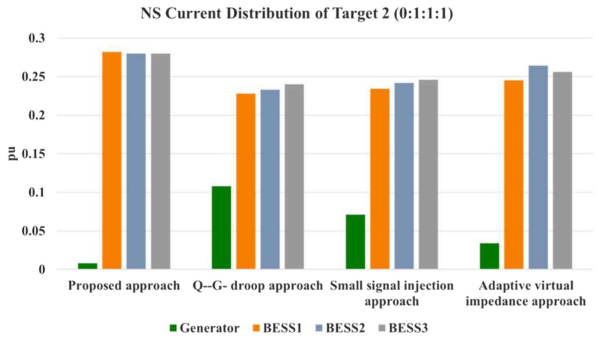

FIGURE 13. NS current distribution of target 2 (balanced SG output).

B. EQUAL IBR SHARING AND BALANCED GENERATOR OUTPUT

In this case, the targeted NS currents of different sources are $I_{2inv(1)} = I_{2inv(2)} = I_{2inv(3)} = 7.18\angle -20.72°\text{A}$, $I_{2SG} = 0\text{A}$. According to (15) and (16), the normalized NS impedances of sources are:

$$\begin{cases} Z_{2inv(1)} = -0.01 - j0.04pu \\ Z_{2inv(2)} = -0.0023 - j0.0317pu \\ Z_{2inv(3)} = -0.0043 - j0.0379pu \end{cases} \tag{18}$$

where all the impedances can meet the requirements in (9). By implementing the NS impedances in the inverters, the NS current distribution and sources' currents are shown in Figs. 13 and 14(a). From the simulation results, the targeted NS current distribution can be realized. Three inverters share the NS current equally (0.5% sharing error) and the generator does not provide NS current. The proposed approach is also compared with three existing approaches, where the results are also summarized in Fig. 14. For the existing approaches, the control parameters (droop curves, etc.) are designed to be the same for the three inverters.

From the simulation results, the existing approaches cannot balance the generator current. The NS currents of the three inverters are not equally shared. The results demonstrate that existing approaches designed for the MG with a fixed PCC and IBRs cannot achieve accurate NS current sharing control while the proposed approach can realize accurate NS current sharing control for different NS current distribution objectives.

V. EXPERIMENTAL DEMONSTRATION

In the experimental setup, the MG is emulated on a converter-based HTB, where two-level voltage source inverters are used to emulate different grid components [23]. The MG topology and hardware setup are shown in Fig. 15. The example MG for testing has three sources. In the HTB, all the inverter emulators are three-wire, which can only emulate the PS and NS circuits of the MG. Since the test target is the NS current distribution, the HTB can be used. In this case, the unbalanced

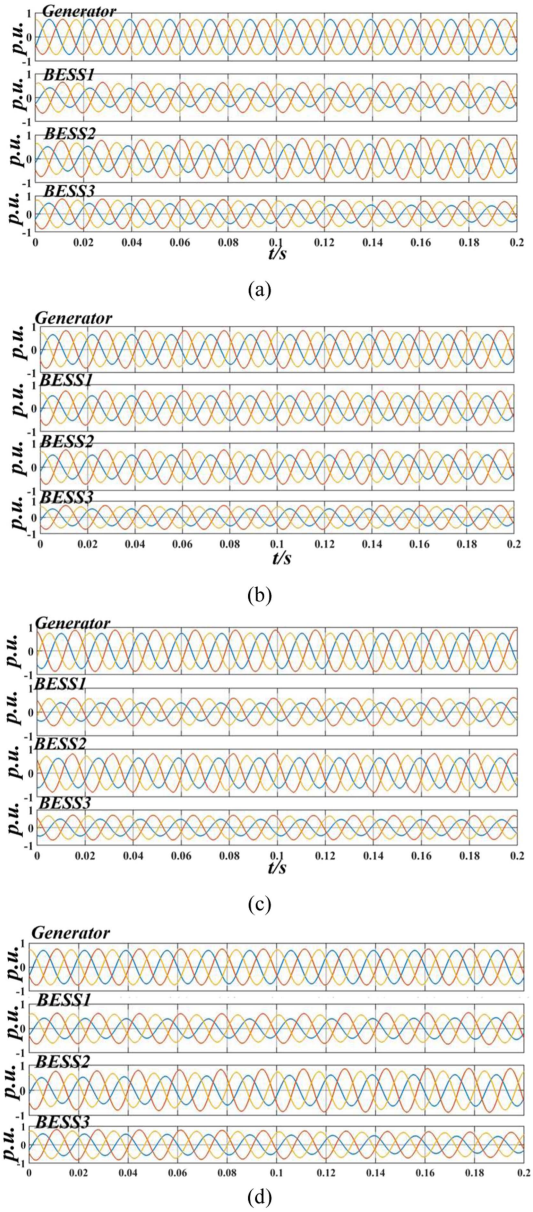

FIGURE 14. Current waveforms of target 2 (balanced SG output): (a) proposed approach; (b) Q⁻-G⁻ droop approach; (c) small signal injection approach; (d) adaptive virtual impedance approach.

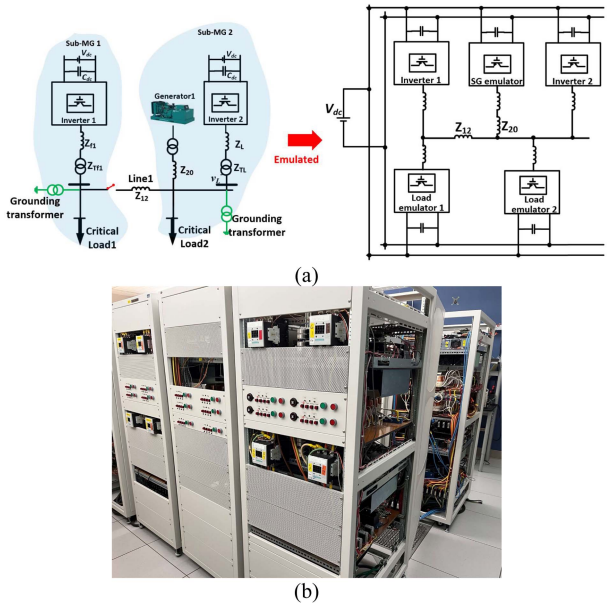

FIGURE 15. Testing setup: (a) testing circuit; (b) hardware setup.

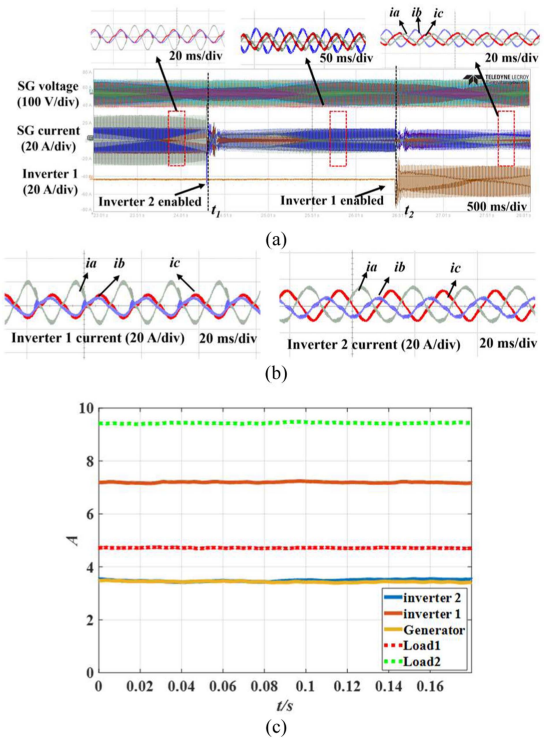

FIGURE 16. Testing results for target 1: (a) SG current; (b) inverter currents; (c) NS current distribution.

load emulator directly regulates its PS and NS currents in *dq* coordinates to serve as a current source [30]. The SG emulator uses the sixth-order (6^{th}-order) electrical model in [31]. The normalized values of SG's electrical model are the same as the ones in Table 1. All the source transformer impedances are assumed to be zero. The detailed parameters are shown in Table 2. This testing system is also a single-SG system. The SG will serve as the reference source in the NS network and the minimum value is applied.

In the testing, two NS current distribution targets in the simulation are also realized. For target 1, when the NS current distribution follows the negative sequence capability ratio, the targeted NS current distribution will be 2:1:1. The normalized NS impedances of two inverters are:

$$\begin{cases} Z_{2inv(1)} = 0.017 + j0.0719pu \\ Z_{2inv(2)} = 0.0236 + j0.1242pu \end{cases} \tag{19}$$

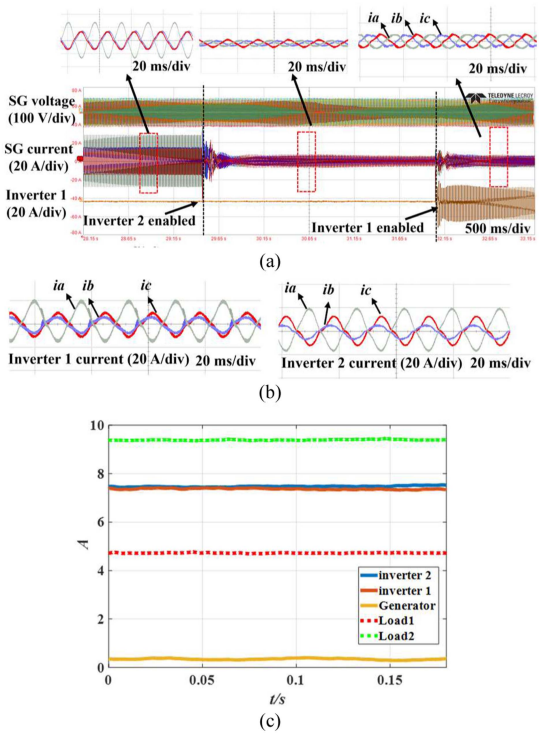

FIGURE 17. Testing results for target 2: (a) SG current; (b) inverter currents; (c) NS current distribution.

TABLE 2. Testing Setup Parameters

	Parameter values
Inverter 1	$V_{dc} = 200\ V, V_{ac(l-l)} = 100\ V, S_{base} = 3.46\ kVA,$ $Q_{NS} = 2\ kVA, L_f = 0.5\ mH, R_L = 50\ m\Omega, f_s = 10\ kHz$
Inverter 2	$V_{dc} = 200\ V, V_{ac(l-l)} = 100\ V, S_{base} = 1.73\ kVA,$ $Q_{NS} = 1\ kVA, L_f = 0.5\ mH, R_L = 50\ m\Omega, f_s = 10\ kHz$
Generator emulator	$V_{dc} = 200\ V, V_{ac(l-l)} = 100\ V, S_{base} = 5.19\ kVA,$ $Q_{NS} = 1\ kVA, L_f = 0.5\ mH, R_L = 50\ m\Omega, f_s = 10\ kHz$
System information	critical load 1 (rms): $I_1 = I_2 = 6.92\angle 180^\circ$ critical load 2 (rms): $I_1 = I_2 = 3.46\angle 180^\circ$ $Z_{12} = 0.05 + j0.4524\ \Omega, Z_{20} = 0.1 + j0.1885\ \Omega$

Note: L_f and R_L are the inductance and resistance of inverter filters

For NS distribution target 2, two inverters share all the NS currents, and the SG emulator outputs a balanced current. The normalized NS impedances of the two inverters are calculated as:

$$\begin{cases} Z_{2inv(1)} = 0pu \\ Z_{2inv(2)} = 0.0058 + j0.0523pu \end{cases} \tag{20}$$

The NS impedances are realized in two inverters. The testing results of target 1 are shown in Fig. 16. In the testing, an eight-channel (4 voltage channels and 4 current channels) scope LeCroy MDA810 is used. Due to limited channel numbers, the current waveforms of the three sources are measured separately. In Fig. 16(a), the SG emulator is enabled first to support two loads. Inverter 2 is enabled at time t_1 and inverter 1 is enabled at time t_2. During this process, the current of SG becomes less unbalanced. When the three sources all reach steady states, the current waveforms of two inverters are shown in Fig. 16(b). The NS currents are calculated based on current waveforms. The results are shown in Fig. 16(c). The NS current of inverter 1 is 2.02 times that of inverter 2 and the SG emulator. The targeted distribution is realized.

The results of target 2 are shown in Fig. 17. In the testing shown in Fig. 17(a), when inverter 2 is enabled at t_1, the SG current becomes balanced. After inverter 1 is enabled at t_2, two inverters share the unbalanced currents. The current waveforms of two inverters in the steady state are shown in Fig. 17(b). The NS current distribution is shown in Fig. 17(c). When the three sources are all enabled, inverters 1 and 2 share the NS current equally with a 0.6% sharing error. The distribution target can be reached.

VI. CONCLUSION

In a MG with dynamic PCCs and a mix of GFM IBRs and SGs, the accurate control of NS current distribution among different GFM sources is challenging. In this paper, a NS impedance design and regulation approach is proposed to achieve flexible and accurate NS current sharing among different GFM sources. The NS impedance control is applied to GFM inverters to be consistent with SG's NS performance. Then the NS current distribution is realized by the NS impedance design.

For the impedance design, the proposed approach takes into consideration the MG topology information through the admittance matrix of the MG's NS network. The proposed approach is applicable to different NS current distribution objectives. If all the designed NS impedances are feasible, the calculated NS impedances of the IBRs will be implemented through inverter control, and the NS impedances of SGs will be realized by the hardware design. If no feasible NS impedance design can be found after the whole design process, the NS current distribution objective is viewed as not realistic in the current system configuration and it is advised to resort to other alternatives through system redesign or resource addition.

The proposed approach is compared with three state-of-the-art solutions through simulations of a MG with four source locations. Two different NS current distribution objectives are realized. The results show that in the MG that contains both SGs and IBRs and at the same time has flexible PCCs, the proposed approach can still achieve the NS current distribution targets, which existing approaches cannot handle. The proposed approach is also validated through experimental testing on a HTB, where two different NS current distribution targets are also achieved accurately. Compared with existing approaches, the proposed approach can be applied to a MG with more complicated configurations. Meanwhile, it achieves NS current sharing with SGs and is capable of various NS current sharing objectives. Therefore, the proposed approach is more general for the NS current sharing issue and can eventually reduce the source sizing cost the MG.

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