IEEE Open Journal of
Power Electronics

Received 8 December 2023; revised 1 February 2024; accepted 10 February 2024. Date of publication 21 February 2024;
date of current version 29 February 2024. The review of this article was arranged by Associate Editor Lingxiao Xue.

Digital Object Identifier 10.1109/OJPEL.2024.3366165

A New High Step-Up SC-Based Grid-Tied Inverter With Limited Charging Spike for RES Applications

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ABSTRACT Switched capacitor multilevel inverter topologies are attractive among industrial power electronics researchers due to their applicability in sustainable energy systems such as renewable energy source (RES) applications. In this paper, a new switched capacitor (SC)-based grid-tied seven-level inverter is proposed for renewable energy sources (RES) applications. The proposed inverter can generate a seven-level output voltage waveform with voltage boosting ability and a gain factor of 3. Also, the proposed topology can provide the self voltage balancing for capacitors. The most important challenge of the SC-based topologies, i.e., the capacitor charging spike current, is solved by applying a soft charging circuit in the charging loop of the capacitors. The soft charging circuit consists of an inductor and a power diode in the capacitor charging path. Using a small size inductor in the soft charging circuit, the proposed inverter can limit the input current spikes. Comprehensive experiment results and comparisons are presented to verify the accurate performance of the proposed inverter.

INDEX TERMS Switched-capacitor inverters, grid-tied inverter, transformer-less inverter, voltage-boosting feature, soft charging, limitation of capacitor charging current spike.

I. INTRODUCTION

Nowadays, the clean energy transition is a key to overcoming the CO2 emission of fossil fuels. The use of RES is increasing to provide a green future. Power electronic converters are needed to exploit the energy produced by PV systems and use them in industry and residential sectors [1], [2], [3]. Multi-level inverters are promising solutions to enhance the performance of electric vehicles (EVs), PV systems, and other power electronic devices in medium- and high-power applications due to many advantages like requiring small size filter, low total harmonic distortion (THD), high efficiency, etc. [4], [5].

They can be categorized into three main basic structures, including flying capacitor (FC), neutral point clamped (NPC), and cascaded H-bridge (CHB) topologies [6], [7], [8]. Meanwhile, the mentioned inverters suffer from the high number of circuit elements and require complex control systems, especially to provide a higher number of output levels. To generate higher output voltage levels, both NPC and FC topologies have to use more capacitors, power switches, and diodes. Balancing the capacitors' voltages in these structures is also a serious challenge. The reduced component-based topologies can solve the necessity of the higher number of switches and diodes of conventional structures [9]. However, these topologies cannot provide the voltage boosting feature at the output. Some topologies have been proposed with additional circuits or using complex control strategies to overcome the capacitors' voltage balancing [10].

In these topologies, using additional circuits or complex control systems leads to increasing the cost, volume, and structural complexity. In order to solve the disadvantages of the conventional and reduced element structures, switched capacitor-based multilevel inverters have been proposed [11]. In the switched capacitor topologies, by series-paralleling of capacitors with input dc power supply, the voltage boosting feature and capacitor voltage balancing can be obtained. [12], [13]. Note that, in the switched capacitor topologies, the voltage boosting capability can be provided without using an extra boost stage. In the proposed topology of [14], to generate the negative half cycle of the output voltage waveform, an H-bridge circuit at the back end is used.

The recently-introduced switched capacitor-based MLIs, without using H-bridge units, require a large number of components, such as power switches and diodes to produce the output voltage waveform. Although a lower number of components are used in switched capacitor MLIs with H-bridge units, the total standing voltage (TSV) is very high.

Based on the voltage gain of switched capacitor-based inverters, the seven-level topologies can generally be classified into two groups. The seven-level SC-based multilevel inverters with a voltage gain of 1.5 have been presented in [15], [16], [17], [18], [19], [20]. Also, the seven-level SC-based inverters with a voltage gain factor of 3 are proposed in [21], [22], [23], [24], [25]. The presented SC-based inverters in [21] and [15] need more than one input DC power supply, which makes them improper for certain applications. In addition, the need for multiple input power supplies leads to increasing the cost and size of the power converter. In [19], a new cascaded seven-level topology is suggested. Meanwhile, the proposed topology needs auxiliary and complex control systems to balance the capacitor voltage.

The major challenge of the SC-based multilevel inverters is the charging current spike passage through the capacitors in the charging loop. This current spike can cause harmful current stress on the power electronic switches and diodes [26]. In [27], the used capacitors are in charging mode during every switching cycle, and they are not discharged completely. So, without using an inductor, the amplitude of the inrush current can be limited. Meanwhile, these unwanted inrush currents cannot be eliminated completely. The presented topology in [5] can overcome the instant inrush currents in the series-connected capacitors using the quasi-resonant inductor.

Regarding the above-mentioned challenges, a new switched capacitor-based seven-level inverter using a single DC power supply is proposed in this paper. The proposed topology can generate a seven-level output voltage waveform with voltage-boosting capability. Moreover, the proposed inverter provides voltage-boosting capability with a gain factor of 3 without using any extra DC-DC boost converter. As discussed, the major drawback of the switched capacitor-based inverters is the current spike during the capacitor charging modes. The proposed inverter also mitigates the capacitor charging spike current and provide soft charging employing a soft charging

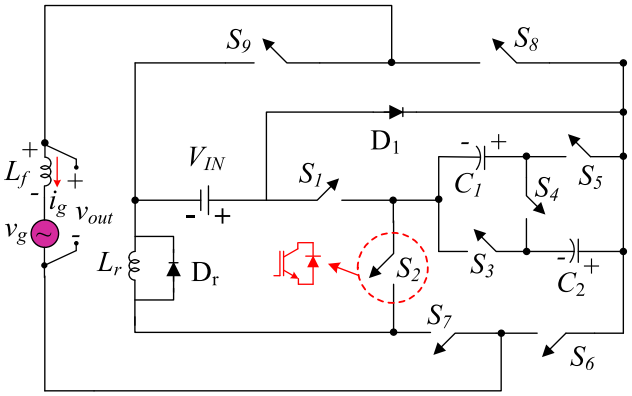

FIGURE 1. Seven-level SC-based boost grid-tied inverter.

circuit that consists of an inductor and one diode. The rest of the paper is organized as follows:

First, the proposed inverter is briefly introduced, and its operational modes are explained. Then, the duty cycle calculations will be carried out for three operating zones of the introduced converter. In addition, the inductance value of the output filter and the capacitance values of the implemented capacitors are computed. Also, soft-charging circuit design consideration is provided. Furthermore, the applied closed-loop control system is presented, which adjusts injected active and reactive power to the grid and generates switching gate pulses for the proposed seven-level inverter. Moreover, the reliability of this converter is assessed using the Markov approach, to guarantee the proposed inverter's durability and solidity. Furthermore, power losses and efficiency analysis is performed. In order to highlight the advantages of the proposed inverter, a comparison of this structure with some resembling topologies is conducted and presented in detail. Finally, a laboratory prototype of the proposed inverter is assembled at 620 W output power, and the captured waveforms are illustrated in the experimental result section.

II. PROPOSED SEVEN-LEVEL SC-BASED INVERTER

The proposed seven-level SC-based grid-tied inverter is illustrated in Fig. 1. It uses a single DC-source, nine switches (S_1~S_9), one diode (D_1), and two switched capacitors (C_1 & C_2) to generate seven-level output voltage waveform. Note that all the used power switches are unidirectional. In order to limit the capacitor charging spike during charging modes of the capacitors, a soft charging circuit is used in the proposed inverter. The soft charging circuit consists of a diode (D_r) and an inductor (L_r) connected in parallel.

In the switched capacitor-based topologies, the basic idea involves redistributing charges among the capacitors in a way that ensures their voltages are balanced [11], [12], [13]. In the proposed grid-tied inverter, controlled switches connect and disconnect capacitors, allowing charges to flow between them. The switching sequence is carefully controlled to maintain balance. Switches are operated in a specific order to transfer charge between capacitors, adjusting their voltages.

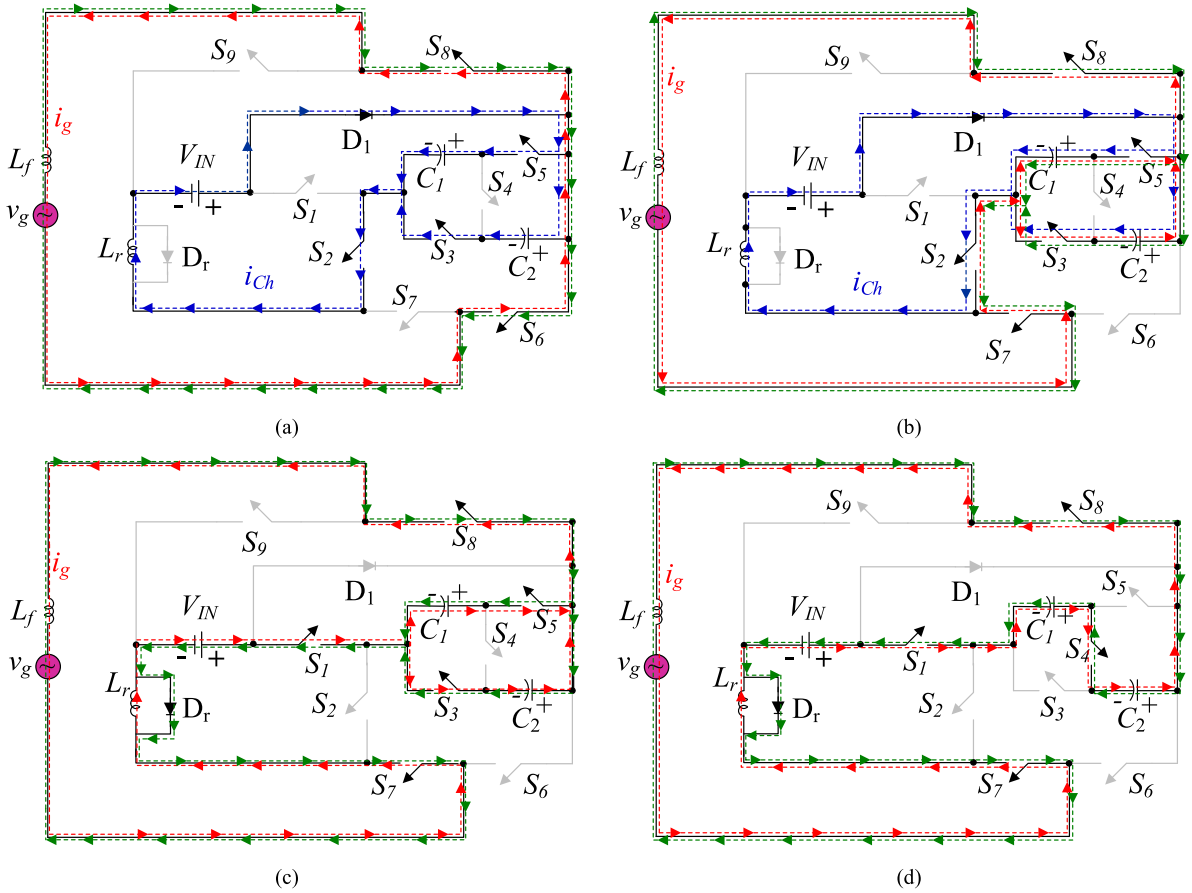

FIGURE 2. Operation modes during the positive half cycle: (a) first operation mode, (b) second operation mode, (c) third operation mode, and (d) fourth operation mode.

Self-balancing of capacitors in switched-capacitor-based inverters is an inherent feature and can be accessed without the need for an external controller system.

In the proposed topology, the utilized capacitors can be charged to $V_{IN} = V_{dc}$ by connecting to input dc source, individually. Therefore, the voltage boosting capability with voltage gain of 3 can be achieved. Here's how the proposed SC-based inverter facilitates triple voltage gain:

1) *Charge Transfer Mechanism:*
   - In the proposed switched-capacitor grid-tied inverter, the capacitors C_1, and C_2 is connected to the input DC source in parallel by controlling the switching gate pulses of switches. So, the energy of input DC source is transferred to the capacitors and they are charged to V_{IN}.
2) *Series Connection of Capacitors:*
   - By appropriately configuring the switches, capacitors can be connected in series during specific phases of the switching cycle.
3) *Voltage Tripling Effect:*
   - When capacitors are connected in series with the input DC source, the effective voltage across the combination is the sum of the individual capacitor voltages and input SC source voltage ($V_{out} = V_{C1} + V_{C2} + V_{IN} = 3V_{IN}$).
   - This series connection allows for voltage tripling, leading to an increase in the overall output voltage.

In the proposed configuration, the maximum blocked voltage (MBV) of the switches $S_1 \sim S_5$ is V_{IN} and the MBV value of switches $S_6 \sim S_9$ is $3V_{IN}$.

III. OPERATION MODES OF SEVEN-LEVEL SC-BASED INVERTER

The operation modes of the proposed inverter during both positive and negative half cycles are shown in Figs. 2 and 3. In the mentioned figures, the red-dash line, blue-dash line, and green-dash line denote to the injected current to the grid path, charging current path of capacitors, and reactive power path, respectively.

Positive half cycle:

A. FIRST OPERATION MODE

The First operation mode is illustrated in Fig. 2(a). It can be seen that in order to generate the zero level of output voltage waveform during the positive half cycle, the switches S_6, and S_8 should be in on-state. Regarding Fig. 2(a), during the first

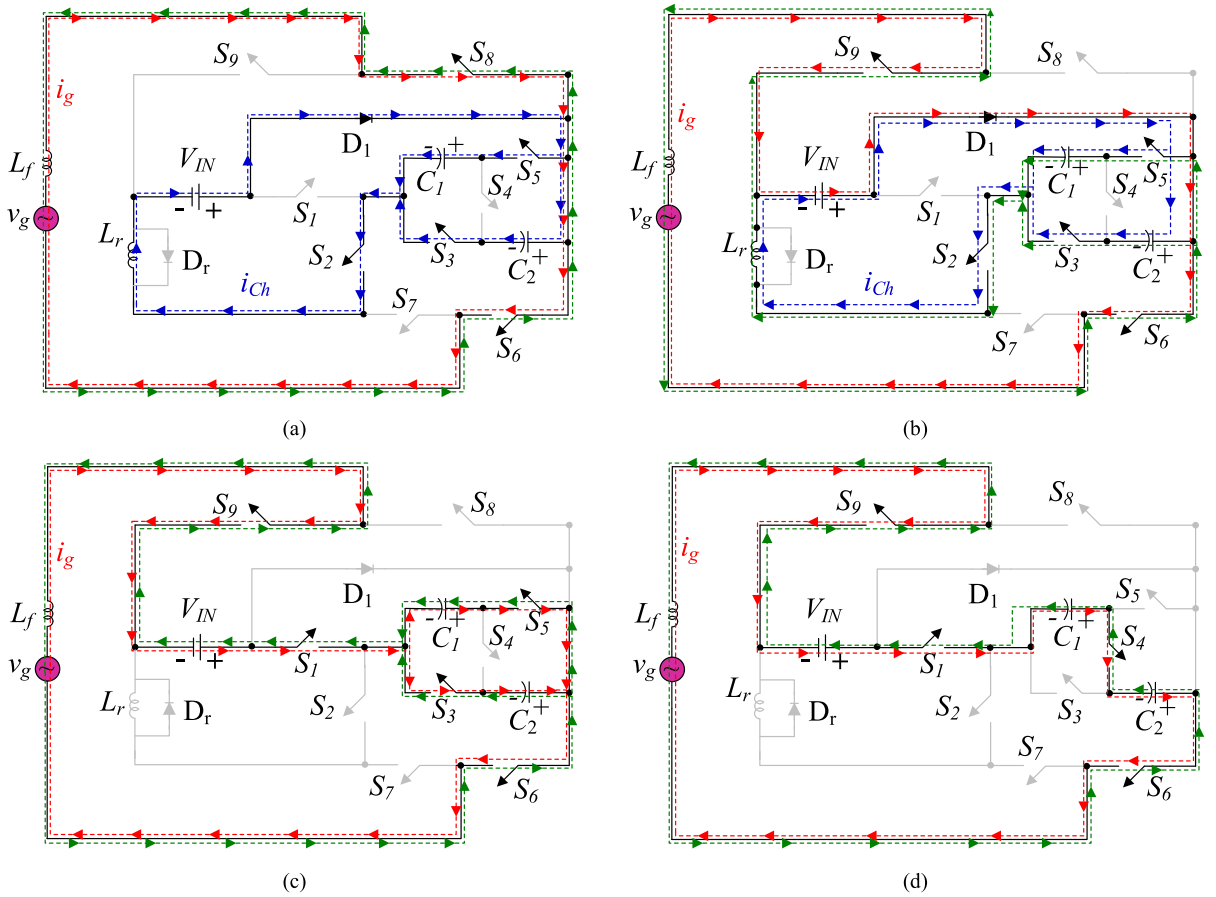

FIGURE 3. Operation modes during the negative half cycle: (a) first operation mode, (b) second operation mode, (c) third operation mode, and (d) fourth operation mode.

operation mode, both capacitors C_1&C_2 are in charging mode. By turning on the switches S_2, and S_5, and conducting diode D_1, the capacitor C_1 is connected to the input DC source in parallel and charged to V_{IN}. Also, by turning on the switches S_2, and S_3, and conducting diode D_1, the charging loop of capacitor C_2 is generated. So, capacitor C_2 is tied to the input DC source in parallel and charged to V_{IN}. So, it can be mentioned that the proposed SC-based inverter provides the self-balancing feature for capacitor voltages. As a result, during this mode, both capacitors C_1, and C_2 are in charging mode. Considering Fig. 2(a), in this mode, the switches S_1, S_4, S_7, and S_9 are in off-state.

B. SECOND OPERATION MODE

The equivalent electrical circuit of the proposed inverter in the second operation mode during positive half cycle is illustrated in Fig. 2(b). Regarding this figure, as in the first operation mode, both capacitors C_1, and C_2 are still charged to V_{IN}. In this mode, in order to generate the second level of output voltage in the positive half cycle, the switches S_3, S_7, and S_8 are in on-state. As a result, the stored energy of capacitor C_2 is discharged to the output. Therefore, the amplitude of output voltage is equal to V_{C2} or V_{IN}. Also, by turning on the switches S_5, S_7, and S_8, the stored energy of capacitor C_1 is discharged to the output. So, this path is another way to generate the first level of output voltage waveform during positive half cycle. Based on Fig. 2(b), in this mode, the switches S_1, S_4, S_6, and S_9 are in off-state.

C. THIRD OPERATION MODE

The third operation mode of the proposed inverter in the positive half cycle is shown in Fig. 2(c). Regarding Fig. 2(c), the capacitors C_1, and C_2 are in discharging mode in the third operation mode. Considering Fig. 2(c), in this mode, in order to generate the second level of output voltage waveform, there are two current paths. The first path is generated by turning on the switches S_1, S_5, S_7, and S_8. During this path, the capacitor C_1, and input DC source are connected in series to the output of the inverter. So, the amplitude of output voltage will be equal to sum of capacitor C_1 voltage and input voltage ($V_{out} = V_{C1} + V_{IN} = 2V_{IN}$). So, the second level of output voltage waveform can be generated.

In addition, the second path is generated by turning on the switches S_1, S_3, S_7, and S_8. By using this current path, the capacitor C_2, and input DC source are connected in series to the output of the inverter. Therefore, the amplitude of output

voltage will be equal to sum of capacitor C_2 voltage and input voltage ($V_{out} = V_{C2} + V_{IN} = 2V_{IN}$). As a result, the second level of output voltage waveform can be generated. Note that in this mode, the switches S_2, S_4, S_6, and S_9 are in off-state. Also, the diode D_1 is in disconnected state.

D. FOURTH OPERATION MODE

Fig. 2(d) illustrates the fourth operation mode of the proposed SC-based inverter.

Considering Fig. 2(d), both switched capacitors are in discharging mode in this mode. In order to generate the third level of output voltage waveform during positive half cycle, the switches S_1, S_4, S_7, and S_8 should be in on-state. Under this switching pattern, the capacitor C_1, and C_2, and input power supply are connected in series to the output of the inverter.

So, the amplitude of output voltage is equal to the sum of the voltages of capacitors C_1, and C_2, and input voltage ($V_{out} = V_{C1} + V_{C2} + V_{IN} = 3V_{IN}$). Therefore, the third level of output voltage waveform in the positive half cycle can be generated. Based on this operation mode, it can be verified that the proposed inverter can provide the voltage boosting capability with the gain factor of 3. Note that in this mode, the soft charging circuit along with diode D_1 are in disconnected mode. In addition, the switches S_2, S_3, S_5, S_6, and S_9 are in off-state.

Negative half cycle:

E. FIRST OPERATION MODE

Fig. 3(a) indicates the first operation mode in the negative half cycle. During this operation mode, the zero level of output voltage waveform in the negative half cycle is generated. Considering Fig. 3(a), in this mode, similar to first mode in the positive half cycle, both switched capacitors C_1, and C_2 are in charging mode.

In this mode, in order to generate the zero level of output voltage waveform in the negative half cycle, the switches S_6 and S_8 should be in on-state. Based on Fig. 3(a), in this mode, the switches S_1, S_4, S_7, and S_9 are in off-state.

F. SECOND OPERATION MODE

The equivalent electrical circuit of the second operation mode in the negative half cycle is illustrated in Fig. 3(b). Like the first operation mode in the negative half cycle, in this mode, the capacitors are still in charging mode. Regrading Fig. 3(b), to generate the first level of output voltage waveform in the negative half cycle, the switches S_6, S_9 and diode D_1 should be in on-state. By using this switching pattern, the Input DC source is connected to the output of inverter in parallel. So, the amplitude of output voltage is equal to $-V_{IN}$. Therefore, the first level in the negative half cycle can be generated. With respect to Fig. 3(b), in this mode, the switches S_1, S_4, S_7, and S_8 are in off-state. Also, diode D_r of soft charging circuit diode is in off-state.

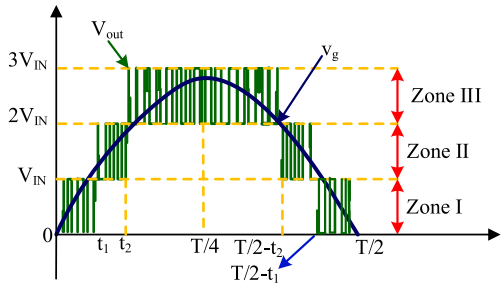

FIGURE 4. Positive half cycle output voltage waveform, grid voltage, and three operation zone.

G. THIRD OPERATION MODE

The third operation mode is shown in Fig. 3(c). In this mode, the aim is generating the second level of output voltage waveform during the negative half cycle. Regarding Fig. 3(c), there are two current paths to obtain the mentioned aim. The first current path can be provided by turning on the switches S_1, S_5, S_6, and S_9. By using this current path, the capacitor C_1 and input DC source are connected to output in series. So, the amplitude of output voltage is the sum of input DC voltage and voltage of capacitor C_1 ($V_{out} = -V_{C1}-V_{IN} = -2V_{IN}$).

The second current path is generating by turning on the switches S_1, S_3. S_6, and S_9. By using this path, the stored energy of capacitor C_2 along with input DC voltage are discharged to output. So, the amplitude of output voltage is the sum of input DC voltage and voltage of capacitor C_2. As a result, the second level of output voltage in the negative half cycle can be generated. Regarding Fig. 3(c), in this mode, the switches S_2, S_4, S_7, and S_8 are in off-state. Also, the diode D_1 and soft charging circuit (D_r & L_r) are disconnected.

H. FOURTH OPERATION MODE

The fourth operation mode in the negative half cycle is shown in Fig. 3(d). This mode aims to generate the upper level of output voltage level during negative half cycle. To obtain this target, the switches S_1, S_4, S_6, and S_9 should be in on-state. Under this switching pattern, the stored energies of capacitor C_1 and C_2 along with input DC voltage are injected to the output. So, the output voltage amplitude is the sum of capacitors C_1 and C_2 voltages, and input voltage ($V_{out} = -V_{C1}-V_{C2}-V_{IN} = -3V_{IN}$). Therefore, the third level of output voltage waveform in the negative half cycle can be generated. Considering Fig. 3(d), in this mode, both capacitors C_1, and C_2 are in discharging state. Also, the switches S_2, S_3, S_5, S_7, and S_8 are in off-state. In addition, the diode D_1 and soft charging circuit (D_r & L_r) are disconnected in this mode.

IV. DUTY CYCLE CALCULATIONS IN THREE OPERATION ZONES OF THE PROPOSED INVERTER

Fig. 4 shows the output voltage waveform during positive half cycle along with grid current waveform. Based on Fig. 4, the seven-level output waveform of inverter has three operation zones (Zone I ~ Zone III) in the positive half cycle.

Considering Fig. 4, it can provide the control system of the proposed grid-connected inverter. The sampling frequency and maximum switching frequency can be denoted by f_{smp}, and f_m respectively. Furthermore, the sampling frequency is two times of maximum switching frequency.

The equations of grid voltage and injected current to the grid can be written as:

$$v_g(t) = V_{g,\max}\sin(\omega t) \tag{1}$$

$$i_g(t) = I_{g,\max}\sin(\omega t) \tag{2}$$

Where, $V_{g,max}$, and $I_{g,max}$ are maximum values of grid voltage and injected current to the grid, respectively. Regarding Fig. 4, V_{out} and v_g denote the output voltages of inverter and grid, respectively.

A. OPERATION ZONE I

Considering Fig. 4, in the zone I, the output voltage waveform of the inverter is between zero and V_{IN}. The switching duty cycle (d_1) of the inverter during zone I can be obtained as follows, applying the inductor volt-second balanced (IVSB) law.

$$\int_0^{d_1T_S}\left(V_{IN}-v_g\right)dt+\int_{d_1T_S}^{T_S}\left(-v_g\right)dt=0 \quad 0\le t<t_1, \tag{3}$$

$$d_1(t)=\frac{v_g}{V_{IN}} \quad ; \quad 0\le t<t_1. \tag{4}$$

Replacing (1) in (4), the duty cycle of zone I can be obtained as follows:

$$d_1(t)=\frac{V_{g,\max}\cdot\sin(\omega t)}{V_{IN}} \quad ; \quad 0\le t<t_1. \tag{5}$$

B. OPERATION ZONE II

As seen from Fig. 4, the output voltage waveform of the inverter is located between V_{IN} and $2V_{IN}$. The switching duty cycle of the inverter (d_2) during zone II can be obtained by applying IVSB law for the voltage across the inductor and can be written as follows:

$$\int_0^{d_2T_S}\left(2V_{IN}-v_g\right)dt+\int_{d_2T_S}^{T_S}\left(V_{IN}-v_g\right)dt=0 \quad ; \quad t_1\le t<t_2, \tag{6}$$

$$d_2(t)=\frac{v_g}{V_{IN}}-1=\left(\frac{V_{g,\max}\cdot\sin(\omega t)}{V_{IN}}-1\right) \quad ; \quad t_1\le t<t_2. \tag{7}$$

With respect to (5), the (7) can be rewritten as:

$$d_2(t)=d_1(t)-1 \quad ; \quad t_1\le t<t_2 \tag{8}$$

C. OPERATION ZONE III

It can be seen from Fig. 4, that the output voltage waveform is between $2V_{IN}$ and $3V_{IN}$ during operation zone III. The switching duty cycle (d_3) of the proposed inverter in the zone III can be calculated by applying the IVSB law for the voltage across the output filter inductor and can be expressed as:

$$\int_0^{d_3T_S}\left(3V_{IN}-v_g\right)dt+\int_{d_3T_S}^{T_S}\left(2V_{IN}-v_g\right)dt=0\,;$$

$$t_2\le t<\frac{T}{2}-t_2, \tag{9}$$

$$d_3(t)=\left(\frac{v_g}{V_{IN}}-2\right)=\frac{V_{g,\max}\cdot\sin(\omega t)}{V_{IN}}-2 \;;\; t_2\le t<\frac{T}{2}-t_2. \tag{10}$$

Considering (7), the (10) could be rewritten as:

$$d_3(t)=d_2(t)-1 \quad ; \quad t_1\le t<t_2 \tag{11}$$

Finally, the equations of t_1 and t_2 can be expressed as:

$$t_1=\frac{1}{\omega}\sin^{-1}\left(\frac{V_{IN}}{V_{g,\max}}\right), \tag{12}$$

$$t_2=\frac{1}{\omega}\sin^{-1}\left(\frac{2V_{IN}}{V_{g,\max}}\right). \tag{13}$$

V. CALCULATION OF THE INDUCTANCE VALUE OF OUTPUT FILTER AND CAPACITANCE VALUES OF UTILIZED CAPACITORS

Here, the inductance value of the output filter and the capacitance values of the implemented capacitors are computed. In order to calculate the inductance value of L_f, the passing current through it can be expressed as:

$$i_{Lf}(t)=\frac{1}{L_f}\int_0^t V_{Lf}dt+i_{Lf}(0) \quad ; \quad t_2\le t<\frac{T}{2}-t_2. \tag{14}$$

Regarding (14), the current ripple of the inductor can be calculated as:

$$\Delta I_{Lf}=i_{Lf}(t=d.T_S)-i_{Lf}(0)=\frac{\left(3V_{IN}-v_g\right)d_3(t)}{L_f f_S} \quad ;$$

$$t_2\le t<\frac{T}{2}-t_2 \tag{15}$$

Therefore, using (1) and (10), the current ripple of the inductor can be rewritten as follows

$$\Delta I_{Lf}=\frac{\left(3V_{IN}-V_{g,\max}\cdot\sin(\omega t)\right)\cdot\left(V_{g,\max}\cdot\sin(\omega t)-2V_{IN}\right)}{\left(L_f f_S\right)\cdot V_{IN}} \;;$$

$$t_2\le t<\frac{T}{2}-t_2 \tag{16}$$

By solving (16), the final value of current ripple of inductor L_f can be obtained as:

$$\Delta I_{Lf}=\frac{1}{I_{Lf}\cdot f_S}\left[5V_{g,\max}\sin(\omega t)-\frac{V_{g,\max}^2}{V_{IN}}\cdot\sin^2(\omega t)-6V_{IN}\right] \tag{17}$$

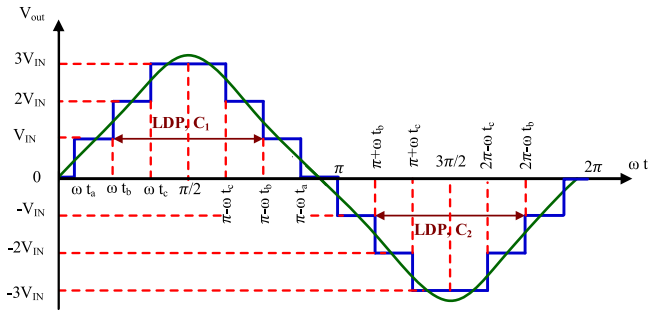

FIGURE 5. Seven-level output voltage waveform with charging and discharging modes of the capacitors.

Therefore, considering (17), the final value of L_f can be calculated as:

$$L_f = \frac{1}{\Delta I_{Lf} \cdot f_S}\left[5V_{g,\max}\sin(\omega t) - \frac{V_{g,\max}^2}{V_{IN}} \cdot \sin^2(\omega t) - 6V_{IN}\right] \tag{18}$$

Also, the desired values of capacitors in the proposed inverter are computed. In order to calculate the capacitance of the capacitors C_1, and C_2, the longest discharging period (LDP) of each capacitor during an output cycle is considered. Fig. 5. Shows the LDP cycles of capacitors C_1, and C_2 in a full switching period (T). Regarding LDP of each capacitor C_1, and C_2, the optimal capacitance values of C_1, and C_2 by considering the permissible maximum value of the voltage ripple can be calculated as follows:

$$C_1 = C_2 = \frac{I_{g,\max} \cdot (\Delta\omega t)}{\omega \cdot \Delta V_{\max}} \tag{19}$$

Where, $\omega = 2\pi f$. Also, f, and $\Delta V_{\max}$ denote grid frequency, and the maximum voltage ripple, respectively. Also, $\Delta\omega t$ is the discharging period of the capacitor and can be calculated as follows:

$$\Delta\omega t = (\pi - \omega t_b) - (\omega t_b) \tag{20}$$

Regarding Fig. 5, the sinewave with a peak of 3.5 V_{IN} cuts the seven-level output voltage waveform at points (ωt_a, $1.5V_{IN}$), (ωt_a, $2.5V_{IN}$) and (ωt_a, $2.5V_{IN}$). So, the ωt_a, ωt_b, and ωt_c can be calculated as:

$$\begin{cases} 0.5V_{IN} = 3.5V_{IN}\cdot\sin(\omega t_a) \Rightarrow \omega t_a = \sin^{-1}\left(\frac{0.5}{3.5}\right) = 0.14(Rad) \\ 1.5V_{IN} = 3.5V_{IN}\cdot\sin(\omega t_b) \Rightarrow \omega t_b = \sin^{-1}\left(\frac{1.5}{3.5}\right) = 0.44(Rad) \\ 2.5V_{IN} = 3.5V_{IN}\cdot\sin(\omega t_c) \Rightarrow \omega t_c = \sin^{-1}\left(\frac{2.5}{3.5}\right) = 0.79(Rad) \end{cases} \tag{21}$$

VI. SOFT-CHARGING CIRCUIT DESIGN AND VERIFICATION

As mentioned in the manuscript file, a soft charging circuit is used in the charging loop of used capacitors of the proposed topology to limit the capacitor charging current spike. This soft charging circuit includes an inductor (L_r) and a power electronics diode (D_r). To answer your comments, the following revisions have been performed:

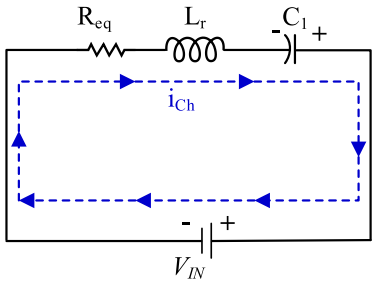

FIGURE 6. Equivalent circuit of charging loop of capacitor C_1.

In the following, the detailed equations and analysis are provided.

The equivalent circuit of the charging loop of capacitor C_1 is shown in Fig. 6. Regarding Fig. 6, R_{eq}, denotes the equivalent resistance of the charging loop.

Based on Fig. 6, by applying the KVL law in the charging loop of capacitor C_1, the following equations can be obtained:

$$\begin{cases} R_{eq}\cdot I_{Ch} + L_r\frac{dI_{Ch}}{dt} + \frac{1}{C_1}\int I_C(t)dt = 0 \\ \frac{d^2I_{Ch}}{dt^2} + \frac{R_{eq}}{L_r}\frac{dI_{Ch}}{dt} + \frac{I_{Ch}}{L_r\cdot C_1} = 0 \end{cases} \tag{22}$$

By solving (22), the resonance frequency (ω_r) and damping factor (α) are obtained as follows:

$$\begin{cases} \alpha = \frac{R_{eq}}{2L_r} \\ \omega_r = \frac{1}{\sqrt{L_r\cdot C_1}} \end{cases} \tag{23}$$

To design the optimal size of the inductor L_r which is applied to limit the capacitor charging current spike, the value of the damping index should be smaller than the resonance frequency, so it can be expressed as:

$$\alpha < \omega_r \Rightarrow \frac{R_{eq}}{2L_r} < \frac{1}{\sqrt{L_r\cdot C_1}} \tag{24}$$

By squaring both sides of (24) and simplifying it, the desired inductance of inductor L_r can be obtained as:

$$L_r > \frac{(R_{eq})^2.C_1}{4} \tag{25}$$

Where R_{eq} is the equivalent resistance of the charging loop of capacitor C_1 and can be expressed as:

$$R_{eq} = R_{D1} + 2R_{DS} + r_{ESR,C} + r_{Lr} \tag{26}$$

Where, R_{D1}, R_{DS}, $r_{ESR,C}$, r_{Lr} denote the forward-voltage drop of power diode D_1, on-state resistance of the switches S_2, S_5, the equivalent series resistance of the capacitor, and the internal resistance of the inductor L_r in the charging loop, respectively.

Further, the capacitor charging current can be calculated as follows:

$$i_{Ch}(t) = \frac{V_{IN} - V_{C1}}{\sqrt{\frac{L_r}{C_1} - \frac{R_{eq}^2}{4}}} \times e^{-\frac{R_{eq}}{2L_r}t} \times \sin\left(\sqrt{\frac{1}{L_rC_1} - \frac{R_{eq}^2}{4L_r^2}}\right)t \tag{27}$$

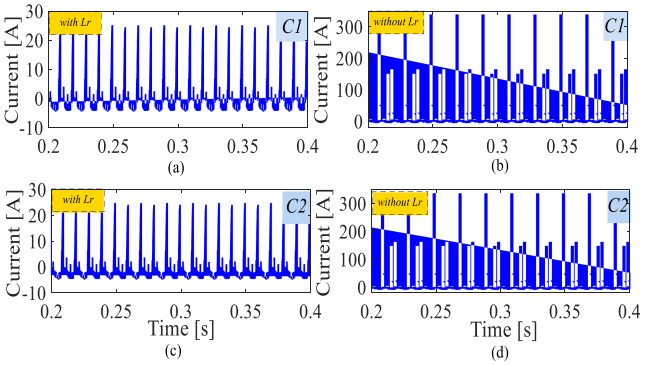

FIGURE 7. Simulation results: (a) chagrin current of capacitor C_1 in the presence of L_r, (b) charging current of C_2 in the absence of L_r, (c) chagrin current of capacitor C_2 in the presence of L_r, and (d) charging current of C_2 in the absence of L_r.

During the time interval of t_P, this current reach to its maximum value obtained by the below equation:

$$t_P = \frac{\pi}{2 \times \sqrt{\frac{1}{L_r C} - \frac{R_{eq}^2}{4L_r^2}}} \tag{28}$$

Now, the maximum value (peak) of the charging current during t_P can be obtained as:

$$I_{Ch,\max} = i_{C1}(t_p) = \frac{V_{IN} - V_{C1}}{\sqrt{\frac{L_r}{C_1} - \frac{R_{eq}^2}{4}}} \times e^{-\frac{R_{eq} \times \pi}{4L_r \times \sqrt{\frac{1}{L_r C_1} - \frac{R_{eq}^2}{4L_r^2}}}} \tag{29}$$

The maximum value of the charging current of the capacitors without using the inductor L_r in the charging loop can be calculated as:

$$I'_{Ch,\max} = \frac{V_{IN} - V_{C1}}{R_{eq}} \tag{30}$$

So, the percentage of reduction in inrush current magnitude of capacitors can be calculated as:

$$\frac{I_{Ch,\max}}{I'_{Ch,\max}} \times 100 = \frac{R_{eq}}{\sqrt{\frac{L_r}{C_1} - \frac{R_{eq}^2}{4}}} \times e^{-\frac{R_{eq} \times \pi}{4L_r \times \sqrt{\frac{1}{L_r C_1} - \frac{R_{eq}^2}{4L_r^2}}}} (\%) \tag{31}$$

In order to verify the soft charging feature of the proposed inverter, the simulation has been performed by MATLAB/Simulink software in the presence and absence of the L_r inductor and investigates the effect of L_r on the capacitor current spike. In the simulation, L_r has been assumed a very small inductor with the inductance value of 0.1 mH as the same as it's experimental description (see Table 3). The capacitor charging current waveforms of capacitor C_1 in the presence and absence of the inductor L_r are shown in Fig. 7(a) and (b), respectively. Also, the capacitor charging current waveforms of capacitor C_2 in the presence and absence of the inductor L_r are illustrated in Fig. 7(c) and (d), respectively. According to these figures, the capacitor current spike of each capacitor is limited to 25 A in the presence of the L_r. While, in the absence of the L_r, the current spike of each capacitor has reached to 300 A. So, regarding (31), the percentage of reduction in inrush current magnitude of capacitor C_1 and C_2 are equal to 8.33 %.

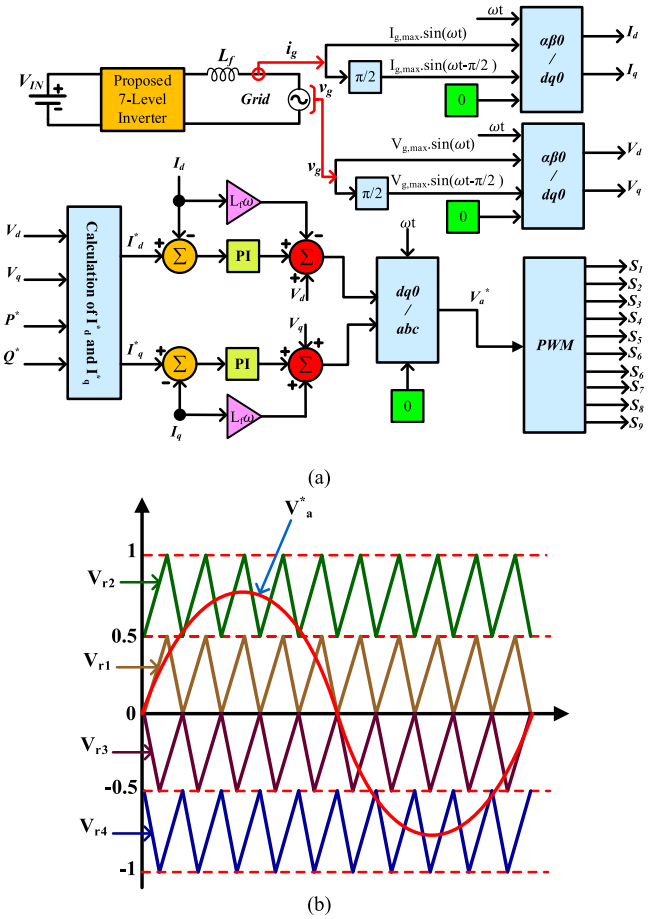

FIGURE 8. (a) Closed loop control block diagram (b) carrier waveforms and V_a^* waveform.

VII. APPLIED CLOSED LOOP CONTROL SYSTEM FOR GRID-TIED INVERTER

The block diagram of the applied control system in the proposed grid-connected seven-level inverter is illustrated in Fig. 8(a). The control system is designed to regulate the operation of a seven-level grid-tied inverter. This control system adjusts both injected active and reactive power flows to the grid and generate switching gate pulses of the switches (S_1~S_9) of the introduced inverter. By using this control strategy, a sinusoidal current waveform can be injected to the grid.

The conversion unit is a crucial component responsible for transforming quantities between different coordinate systems. Utilizes transformation techniques (dq transformation) to generate the d-axis (active power) and q-axis (reactive power) components of the grid current. Similar transformation is applied to generate the d-axis and q-axis components of the grid voltage.

Regarding Fig. 8(a), in this control system, the $(a\beta 0/dq0)$ conversion unit is used to generate the d-axis and q-axis of grid current which are denoted by (I_d), and (I_q), respectively. Also, the d-axis of grid voltage (V_d) and q-axis of grid voltage (V_q) are generated by using the $(a\beta 0/dq0)$ conversion unit. Note that here, I_d and I_q denote active and reactive power flows, respectively. Regarding control system, the reference values d-axis (I_d^*) and q-axis (I_q^*) of the injected grid current are obtained as:

$$I_d^* = \frac{2}{3}\left[\frac{(\mathrm{P}^*.V_d + Q*.V_q)}{{V_d}^2 + {V_q}^2}\right] \tag{32}$$

$$I_q^* = \frac{2}{3}\left[\frac{(\mathrm{P}^*.V_q - Q^*.V_d)}{{V_d}^2 + {V_q}^2}\right] \tag{33}$$

Using above-mentioned reference values, both active and reactive power can be controlled. Considering closed loop control system, it is obvious that the AC components are delivered to d-q axis. Also, the desired value of the injected grid current can be obtained by using a proportional-integral (PI)-based current controller in the control system of the inverter.

At last, the V_a^* is delivered to the pulse width modulation (PWM) unit so, the switching gate pulses of the switches $(S_1 \sim S_6)$ can be generated and applied to gate drivers.

The control logic of the system can be summarized as follows:

- Compares the actual d-axis ($\mathrm{I_d}$) and q-axis ($\mathrm{I_q}$) components of the grid current with the reference values ($\mathrm{I_d^*}$ and $\mathrm{I_q^*}$).
- Generates error signals based on the differences between the actual and desired values.
- Utilizes a control algorithm (a PI controller) to process these error signals.
- The controller generates control signals that drive the inverter to adjust the switching gate pulses ($\mathrm{S_1 \sim S_9}$).

A typical PWM method is shown in Fig. 8(b). Based on this figure, V_{r1}, V_{r2}, V_{r3}, and V_{r4} are the shifted level carrier waveforms.

In summary, the control system involves a conversion unit for transforming quantities, a control system for regulating active and reactive power flows, and a feedback mechanism to adjust the inverter's switching gate pulses.

VIII. POWER LOSSES AND EFFICIENCY ANALYSIS

In order to derive the loss break-down and efficiency of the proposed seven-level inverter, the power losses of the components are derived in this section. There are two types of losses in this inverter: switching losses, and conduction losses. Switch loss includes the turn-on and turn-off switching losses and conduction losses. Furthermore, diode loss consists of conduction losses. Finally, capacitors and inductors only have conduction losses. Also, the utilized inductor's Ferrite core has a 2.2 W core losses.

A. CONDUCTION LOSS

Conduction losses arise due to various factors during the operation of power switches, power diodes, and passive components in the circuit. These factors include the on-state resistance of the switches (R_{DS}), the forward-voltage drop of power diodes $(V_{Fw\text{-}D})$, the equivalent series resistance of the capacitor (R_C), and the internal resistance of the inductor (R_L). Taking into account the aforementioned factors:

$$P_{Cond-Switch} = \frac{q(t)}{2\pi}\left[\int_0^{2\pi} R_{DS} i^2(t) d(\omega t)\right] \tag{34}$$

$$P_{Cond-Diode} = \frac{p(t)}{2\pi}\left[\int_0^{2\pi} R_D i^2(t) d(\omega t) + \int_0^{2\pi} V_{Fw-D} i(t) d(\omega t)\right] \tag{35}$$

$$P_{Cond-Inductor} = \frac{1}{2\pi}\left[\int_0^{2\pi} R_L i^2(t) d(\omega t)\right] \tag{36}$$

$$P_{Cond-Capacitor} = \frac{1}{2\pi}\left[\int_0^{2\pi} R_C i^2(t) d(\omega t)\right] \tag{37}$$

Where $q(t)$ and $p(t)$ refer to the number of power switches and power diodes in the current trajectory. The overall conduction losses of the proposed inverter can be derived as follows:

$$P_{Cond-Overall} = \sum_{i=1}^{9} P_{Cond-Switch_i} + P_{Cond-D_1} + P_{Cond-D_r} + P_{Cond-L_r} + \sum_{i=1}^{2} P_{Cond-C_i} \tag{38}$$

B. SWITCHING LOSS

The switching losses of the circuit includes the on-state and off-state losses of the switches. In order to ease the analysis, the across voltage and passing current of the switches are linearized. As a result, the on-state and off-state switching loss for each power switch will be attained as follows:

$$P_{Switching-ON} = \frac{1}{T_S}\left[\int_0^{t_{ON}} V_{S-ON}(t) i(t) d(t)\right] = \frac{N_{ON} t_{ON}}{6} f_S V_{ON} I_{SW} \tag{39}$$

$$P_{Switching-OFF} = \frac{1}{T_S}\left[\int_0^{t_{OFF}} V_{S-OFF}(t) i(t) d(t)\right] = \frac{N_{OFF} t_{OFF}}{6} f_S V_{Block} I'_{SW} \tag{40}$$

I_{SW} and I'_{SW} are the passing currents of each power switch after turning on and just before turning off, respectively. $\mathrm{N_{ON}}$, and $\mathrm{N_{OFF}}$ denote the number of turning on and turning off of the switches during a full switching period, respectively. Also, $\mathrm{t_{ON}}$ is the sum of Turn-On Delay Time and Turn-On

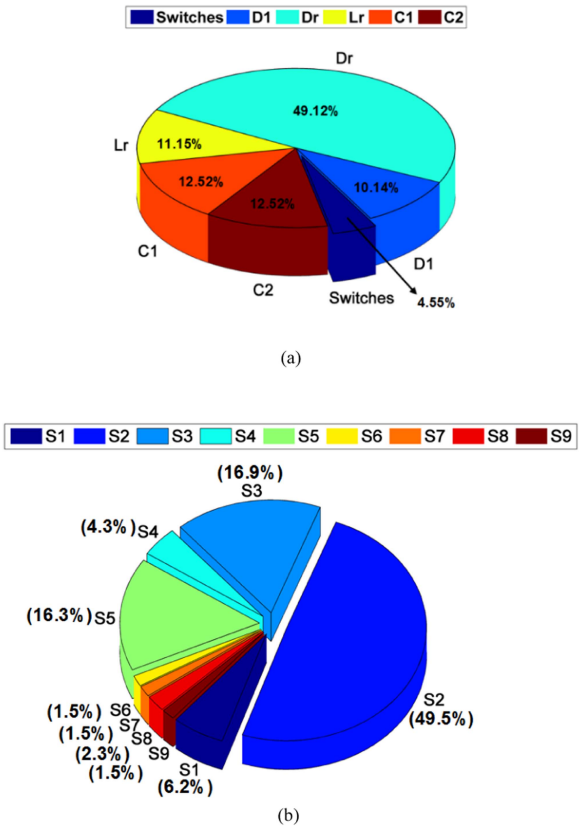

FIGURE 9: **Pie charts of the percentage of losses in circuit components, (a) share of losses percentage for the all components of the inverter, (b) share of losses percentage for the power switches.**

Rise Time. t_{OFF} is sum of Turn-Off Delay Time and Turn-Off Fall Time. It should be mentioned that the values t_{ON} and t_{OFF} can be accessed in the data sheet of the utilized power switches in the proposed inverter. Moreover, T_S and f_S are the switching period and the switching frequency of the inverter, respectively. The overall switching losses of the proposed inverter will be achieved as follows:

$$P_{Switching-Overall} = \sum_{i=1}^{9} (P_{Switching-ON_i} + P_{Switching-OFF_i}) \tag{41}$$

Considering (5) and (8), the overall losses of the proposed inverter will be obtained:

$$P_{Loss-Overall} = P_{Cond-Overall} + P_{Switching-Overall} \tag{42}$$

Fig. 9 visualizes the proportion of losses for each power component of the introduced inverter. In Fig. 9(a), the pie chart of the percentage of losses of the power switches, power diodes, inductor, and capacitors are shown. It is evident that the conduction losses hold a higher share of overall losses in comparison with the switching losses. Furthermore, the power switches hold 4.55% of the overall losses of the proposed inverter. What's more, in Fig. 9(b), the detailed share percentage of switches' losses (sum of switching and conduction losses of the power switches) for each power switch is derived and displayed.

TABLE 1. **Failure Rates and Other Associated Parameters of Each Component in the Circuit, Utilized in the Reliability Assessment**

Components		Failure Rates (λ)(*10^{-8})	Associated Parameters
Switches	S_1	6.3	T_a=25(°C) (Ambient temperature) θ_{CA}=65(°C/W) (Case to ambient thermal resistance) θ_{JC}=2.5(°C/W) (Junction to case thermal resistance) $R_{on\text{-}resistance}$=0.001(Ω) (Drain-Source ON resistance) λ_b=5e-9 (Basic failure rate)
	S_2	6.26	
	S_3	1.15	
	S_4	0.51	
	S_5	1.15	
	S_6	0.52	
	S_7	0.51	
	S_8	0.51	
	S_9	0.51	
Diodes	D_1	40	T_a=25(°C) θ_{CA}=75(°C/W) θ_{JC}=2.5(°C/W) V_F=0.8(V)(Forward Voltage) $R_{on\text{-}resistance}$=0.001(Ω) (Diode ON resistance) λ_b=1e-9
	D_r	50.2	
Inductor	L_r	0.0282	A = 1.39(inch^2) (Radiating surface area of the case) λ_b=3e-5
Capacitors	C_1	0.0287	A = 8.46(inch^2) (Radiating surface area of the case) λ_b=3e-5
	C_2	0.0287	

The overall power losses of the proposed inverter using the above equations is 28.42 W. Therefore, the theoretical efficiency of the proposed inverter for 620 W output power is obtained 95.6%. It is worth mentioning that the experimental efficiency for the mentioned output power is 94.8%, which is lower than the calculated analytical efficiency, due to the assumptions of components to be ideal in theory.

IX. RELIABILITY ASSESSMENT

The reliability analysis of converters provides a systematic approach for assessing the reliability of these complicated systems, which is important for assuring their safe and efficient operation in different applications. The reliability assessment of the proposed inverter in this article is performed using Markov Approach [4], which is a mathematical tool used to assess the probabilities of transitions between different states in a system over time. In case of multi-level inverters, the Markov chain refers to the possible states of the system, such as normal operation, partial failure, and complete failure, and the probabilities of transitions among these states as a result of component failures.

The reliability analysis using the Markov approach involves calculating the reliability function, which is the probability that the system will remain in a specified state. Using MIL-HDBK-217F handbook and the equations in [28], the failure rates of the proposed inverter is derived, which is mentioned in Table 1. According to the mentioned rates, the failure rates of active semiconductor devices in the proposed structure hold a

TABLE 2. Comparison of the Proposed Inverter With Some Other Seven-Level Topologies

Ref	Number of components					Voltage boosting	Gain factor	Spike current limitation	MBV_{pu}	TSV_{pu}	P_{out} (W)	Total volume (mm^3)	Power density (W/mm^3)	CF/N_{level}	
	N_{SW}	N_{gd}	N_d	N_c	N_{Supply}									$\beta = 0.5$	$\beta = 1.5$
[16]	9	9	1	3	1	Yes	1.5	No	1	6.7	200	50502.7	3.9×10^{-3}	3.62	4.65
[21]	10	10	0	0	3	Yes	3	No	3	8	150	1745.3	85×10^{-3}	10.28	13.71
[19]	10	10	0	1	1	Yes	1.5	No	1	6	600	15015.4	39×10^{-3}	3.42	4.28
[17]	10	10	0	3	1	Yes	1.5	No	1	5.3	200	238981.9	0.83×10^{-3}	3.66	4.42
[15]	7	7	2	1	2	Yes	1.5	No	1	9.3	250	7636.2	32×10^{-3}	6.18	8.84
[18]	7	7	2	2	1	Yes	1.5	No	1.5	5	550	100289.5	5.4×10^{-3}	2.92	3.64
[29]	8	8	0	1	1	Yes	1.5	No	3	8	50	26277.85	1.9×10^{-3}	3	4.14
[20]	9	9	0	3	1	Yes	1.5	No	1.5	5.3	375	2061463.7	0.2×10^{-3}	3.37	4.13
[24]	10	10	0	2	1	Yes	3	No	3	6	2000	37464.30	53×10^{-3}	3.57	4.42
[22]	16	14	0	2	1	Yes	3	No	2	5.3	45	1388105.9	0.03×10^{-3}	4.95	5.71
[25]	14	14	0	2	1	Yes	3	No	3	6.3	500	61031.21	8.1×10^{-3}	4.74	5.64
[23]	12	11	0	2	1	Yes	3	No	2	5.3	600	338624.6	1.7×10^{-3}	3.95	4.71
Prop osed	9	9	2	2	1	Yes	3	Yes	3	5.7	620	7134.6	8.6×10^{-3}	2.26	3.07

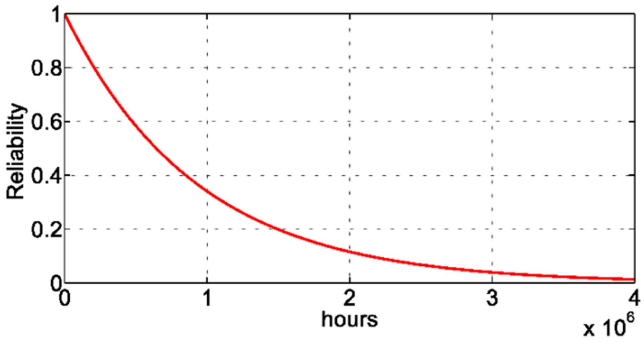

FIGURE 10. Reliability figure of the proposed inverter versus time.

higher total share in comparison with the passive components like inductors and capacitors.

In addition, based on the current path throughout the inverter, the rate at which the current passes through each component have a close relation with the reliability of the whole inverter, as well as many other factors like power dissipation, the ambient temperature, and basic failure rates of each component. The reliability equation of the proposed inverter after computing the failure rates is attained using the following equation:

$$R(t) = \exp\left[-\left(\sum_{i=1}^{9}\lambda_{S_i} + \sum_{i=1}^{2}\lambda_{D_i} + \sum_{i=1}^{2}\lambda_{C_i} + \lambda_{L_r}\right)t\right] \tag{43}$$

Considering the failure rates and (21), the reliability curve of the proposed inverter versus time will be achieved. Fig. 10 portrays the exponential reliability curve versus time. Actually, as time passes, the reliability of the proposed inverter is reduced. Based on this figure, in order to ensure the reliability, it is important to take into consideration of several aspects during the design, assembly, and applying the proposed inverter. Therefore, a thorough reliability study like this assessment, is helpful in projecting the durability of the inverter.

X. COMPARISON

In this section, in order to highlight the advantages of the proposed inverter, a comparison of this structure with some resembling topologies is conducted and presented in detail. The comparison is conducted based on some items such as the number of components, voltage boosting feature, voltage gain factor, spike current limitation, per unit value of maximum blocked voltage (MBV_{pu}), per unit value of total standing voltage (TSV_{pu}), output power (P_{out}), total volume (mm^3), power density (W/mm^3), and CF/N_{level}. The comparison results are presented in Table 2.

Note that in order to calculate the total volume of each topology, the volume of utilized switches, diodes, and capacitors in each inverter are considered. Also, in order to obtain the implementation cost for each inverter, the CF/N_L (cost function/number of levels) is calculated as follows:

$$CF = N_{dc} \times \left(N_{SW} + N_{gd} + N_{diode} + N_{cap} + \beta.TSV_{pu}\right). \tag{44}$$

Note that the power density of the modified topology and other compared topologies are calculated as (23).

$$Power\ density\ (W/mm^3) = \frac{P_{out}\ (W)}{Total\ volume\ (mm^3)} \tag{45}$$

where P_{out} and total volume denote the output power and total volume of each topology.

Regarding Table 2, it can be seen that among other compared topologies, only the proposed inverter can limit the capacitor charging current spike of capacitors during charging mode. Compared with topologies of [16], [17], [18], [20], [22], [23], [25], and [29], the proposed inverter has the maximum value of power density. Considering Table 2, from the point of CF/N_{level}, the proposed inverter has the minimum vale of this cost factor compared with all of topologies. Therefore,

TABLE 3. Listed of Utilized Components and Needed Descriptions of Laboratory Prototype

Component	Type	Description
S_1, S_2, S_3, S_4, S_5, S_6, S_7, , S_8, and S_9	FQPF20N60	600 V/20 A
D_1 and D_r	STPR860DF	600 V/8 A
Microcontroller (Texas Instrument)	DSP TMS320F28335	C2000
Current transducer	LA55P	Hall effect
Gate Driver	TLP-250	IC
Local grid frequency	50 Hz	-
Switching frequency	5 KHz	-
Input voltage	120 V	-
Output power	620W	-
Output voltage	400 V	-
Grid voltage	311 V (peak) / 220 V (rms)	-
C_1 and C_2	160 V	2200 μF
Inductor L_r	Ferrite core	0.1 mH
Inductor L_f	Iron core	3 mH

it can be said that the proposed structure is cost-effective, compared to other compared topologies.

Considering Table 2, compared with topologies of [15], [16], [19], [21], [24], [25], and [29], the proposed inverter has the minimum value of TSV_{pu}. Also, the proposed inverter can provide the voltage boosting feature with a gain factor of 3, unlike the topologies of [16], [17], [18], [19], [20]. They have a larger value of CF/N_{level} than the proposed inverter. Therefore, these structures are not economically viable compared to the proposed structure. Based on Table 2, it can be concluded that the proposed inverter provides an overall enhancement on the number of components, boosting factor, reduced TSV_{pu}, reduced CF/N_{level}, spike current limitation, and power density.

XI. EXPERIMENTAL RESULTS

In this section, a laboratory prototype of the proposed inverter is assembled at 620 W output power, and the captured waveforms are illustrated. The specifications of the used components in the experimental laboratory prototype are summarized in Table 3. In addition, the photograph of the experimental laboratory prototype of the proposed inverter is illustrated in Fig. 11.

Fig. 12(a) shows the seven-level output voltage and injected current to the grid at the unity power factor (PF). Regarding Fig. 12(a), it can be seen that the maximum value of output voltage of the inverter and the injected current to the local grid are about 400 V and 4 A, respectively.

So, by using the applied control strategy the proposed inverter can inject a 620 W active power to the grid. Regarding Fig. 9(a), the proposed grid-connected inverter has good tracking capability of the reference current through the output inductor-based filter.

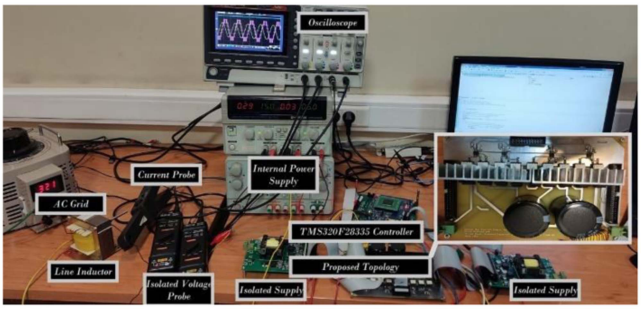

FIGURE 11. Photograph of the experimental prototype of the proposed grid-tied inverter.

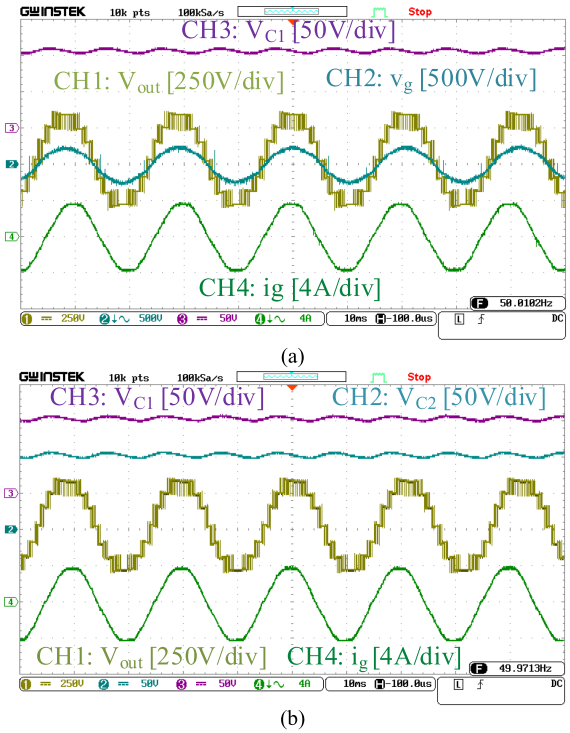

FIGURE 12. Experimental results at unity PF: (a) CH1: seven-level output voltage, CH2: grid voltage, CH3: voltage across capacitor C_1, CH4: injected current to the grid, (b) CH1: output voltage, CH2: voltage across capacitor C_2, CH3: voltage across capacitor C_1, CH4: grid current.

Also, the voltage across the capacitor C_1 is illustrated in channel 3 (CH3) of Fig. 12(a). Regarding this figure, it can be seen that the capacitor C_1 is charged to about 120 V or input voltage (V_{IN}). Fig. 12(b) shows the grid voltage and injected current to the grid at the unity PF. Also, Fig. 12(b) indicates the voltage across capacitors C_1, and C_2 at the unity PF. Regarding this figure, both of capacitors C_1, and C_2 are charged to input power supply. So, the self-balancing capacitor voltages feature of the proposed inverter can be verified. Based on Fig. 12, it can be verified that the proposed inverter and the applied closed-loop control system work together appropriately.

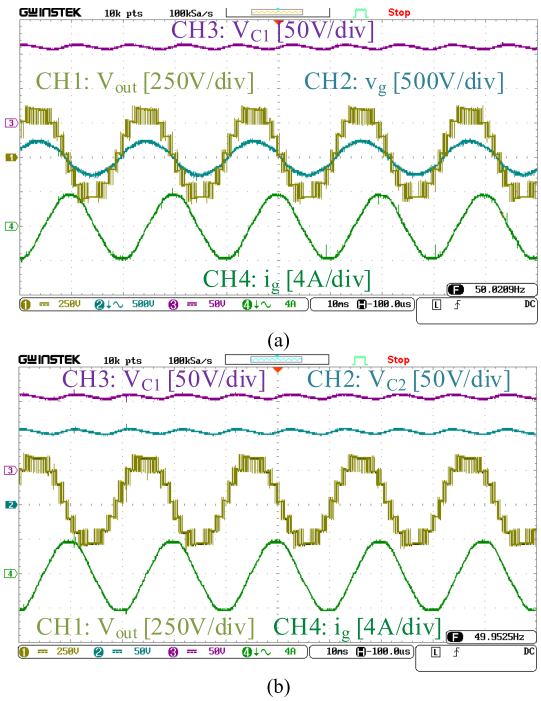

FIGURE 13. Experimental results at leading PF: (a) CH1: seven-level output voltage, CH2: grid voltage, CH3: voltage across capacitor C_1, CH4: injected current to the grid, (b) CH1: output voltage, CH2: voltage across capacitor C_2, CH3: voltage across capacitor C_1, CH4: grid current.

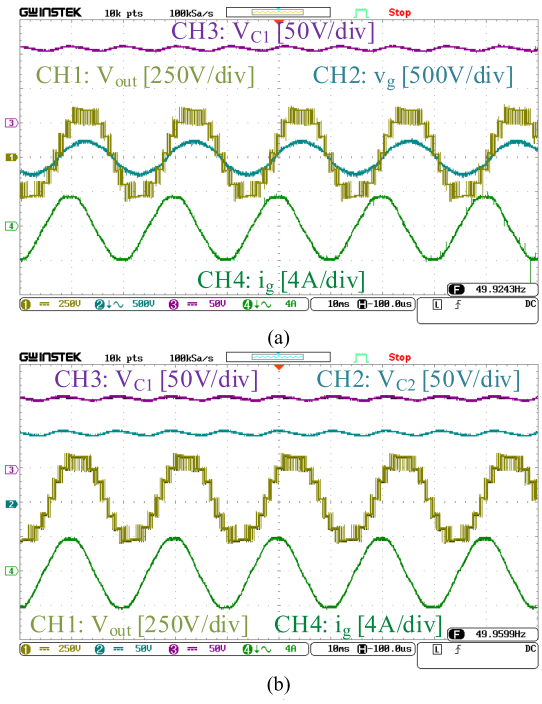

FIGURE 14. Experimental results at lagging PF: (a) CH1: seven-level output voltage, CH2: grid voltage, CH3: voltage across capacitor C_1, CH4: injected current to the grid, (b) CH1: output voltage, CH2: voltage across capacitor C_2, CH3: voltage across capacitor C_1, CH4: grid current.

The seven-level output voltage waveform, grid voltage, grid current, and voltage across capacitor C_1 are shown at the leading PF in Fig. 13(a).

Also, the output voltage, voltage across capacitors C_1, and C_2, and grid current waveforms at leading PF condition are shown in Fig. 13(b). Fig. 14(a) indicates the voltage across capacitor C_1, seven-level output voltage, grid current, and grid voltage at the lagging PF. Also, the grid current, output voltage, and voltage across capacitors C_1, and C_2 waveforms are illustrated at lagging PF in Fig. 14(b).

Regarding Figs. 12, 13, and 14, the proposed inverter, by applying the closed-loop control system, can inject the sinusoidal current into the grid under different conditions of power factor.

In order to study and investigate the dynamic response of the proposed grid-connected inverter, a step change of the reference current (I*) is applied and the obtained results are shown in Fig. 15. The step change of the injected grid current is a change from 4 A to 6 A. Therefore, the injected active power increases from 620 W to 920 W.

Regarding Fig. 15, it can be concluded that the proposed inverter has a good response under the applied step change in the amplitude of the reference current from 4 A to 6 A.

The voltage stress of the switches S_1~S_9 are shown in Fig. 16(a)–(c). The voltage stress waveforms of switches S_1, S_2, and S_3 are illustrated in channel 1, 2, and 3 (CH1-CH3) of Fig. 16(a), respectively. Regarding this figure, the MBV of switches S_1, S_2, and S_3 are about 120 V or V_{IN}.

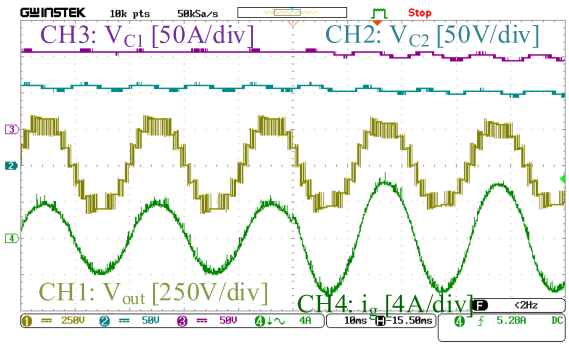

FIGURE 15. Experimental results under a step change in the amplitude of reference current: CH1: output voltage, CH2: voltage across capacitor C_2, CH3: voltage across capacitor C_1, CH4: grid current.

The voltage stress waveforms of switches S_4, S_5, and S_6 are shown in CH1-CH3 of Fig. 16(b), respectively. Considering Fig. 16(b), the MBV of switches S_4, and S_5 are about 120 V or V_{IN}. Also, the MBV of the switch S_6 is about 360 V or 3VIN.

Fig. 16(c) indicates the voltage stress waveforms of switches S_7, S_8, and S_9 in CH1-CH3, respectively. Considering Fig. 16(c), it can be seen that MBV of the switches S_7, S_8, are about 120 V or V_{IN}. Also, the MBV of the switch S_9 is about 360 V or $3V_{IN}$.

In addition, THD (%) of the grid current in the experiment results, for unity, leading, and lagging power factor (PF) are determined according to Table 4. Considering Table 4, it can

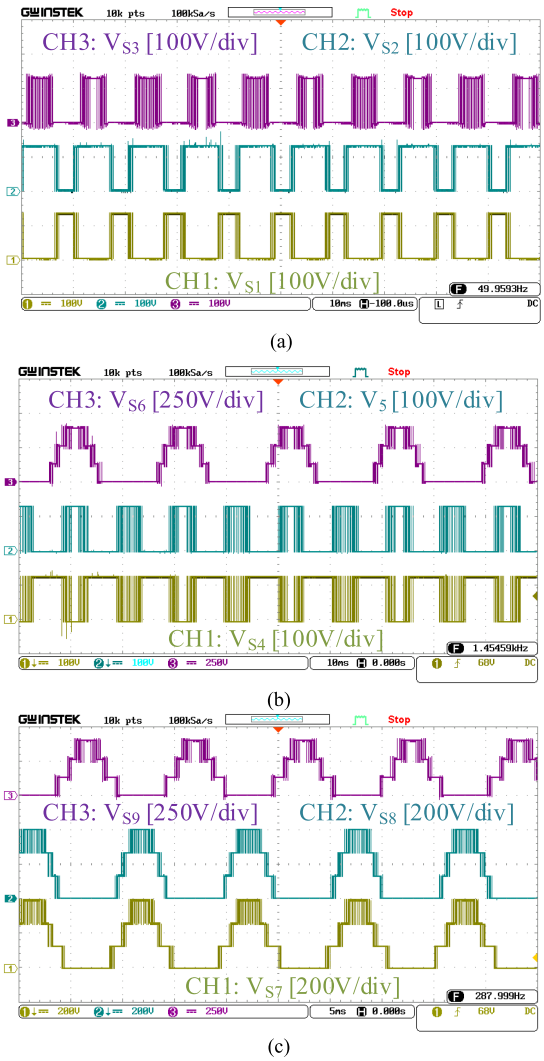

FIGURE 16. Experimental results for voltage stress of switches: (a) CH1: V_{S1}, CH2: V_{S2}, CH3: V_{S3}, (a) CH1: V_{S4}, CH2: V_{S5}, CH3: V_{S6}, (c) CH1: V_{S7}, CH2: V_{S8}, CH3: V_{S9}.

TABLE 4. THD (%) of the Grid Current in the Experiment Results

PF load	THD (%)
Unity PF	3.56%
Leading PF	3.45%
Lagging PF	3.73%

be observed that the THD of injected current to the grid under different conditions of PF such as unity PF, leading PF, and lagging PF are 3.56%, 3.45%, and 3.73%, respectively. Based on IEC 61000-3-2 and IEEE 1547.2-2008 standards the limit of THD of injected current to the grid is less than 5%. Therefore, the proposed grid-tied inverter can pass these mentioned standards.

Considering the experimental results presented above, it can be concluded that the proposed grid-tied switched capacitor-based inverter has a good performance and all the mentioned features can be confirmed for it.

XII. CONCLUSION

In this paper, a new high step-up switched-capacitor-based seven-level grid-connected inverter is presented. The proposed inverter uses only a single input power supply to generate a seven-level output voltage waveform with high step-up gain factor of 3. In order to control both active and reactive power, and generate the switching gate pulses of the switches, a closed loop control system has been applied.

In order to provide the soft charging feature and limit the spike current of the capacitors during the capacitor charging mode, a soft charging circuit is used in the proposed inverter. In the proposed inverter, to provide the voltage boosting feature, the series-parallel switching pattern of the capacitors has been applied. Regarding the applied closed-loop control system, by using a small filter inductor, the injected current can be completely controlled at any desired power factor.

In this research study, to show the advantages of the proposed inverter, a comprehensive comparison with some other recently-presented seven-level inverters has been performed and the comparison results proved the benefits of the suggested grid-tied inverter over other topologies. Also, the design consideration of passive components such as capacitors and filter inductor has been done. In addition, the reliability analysis of the proposed switched capacitor-based inverter has been considered in the paper.

Finally, in order to verify the accurate performance of the proposed inverter and its advantages and features, an experimental laboratory prototype for the proposed inverter at 620 W output power has been built and the obtained results have been presented.

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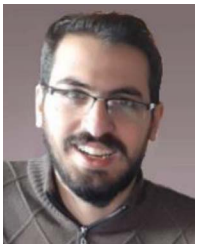

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