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Paralleled SiC MOSFETs Circuit Breaker With a SiC MPS Diode for Avalanche Voltage Clamping

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ABSTRACT This paper proposes a solid-state circuit breaker comprising silicon carbide (SiC) MOSFETs and a SiC diode, based on the principle of avalanche voltage clamping. The key challenge in realizing a solid-state circuit breaker lies in reducing conduction loss. A parallel connection of power semiconductor devices is the suitable configuration that can meet these requirements. However, in such a configuration, the current balance during cutoff operation may be affected by the variation in the breakdown voltage characteristics of the power semiconductor devices. To address this issue, the proposed circuit breaker employs clamping with a SiC merged pin Schottky (MPS) diode, with high avalanche tolerance and robust characteristics under repetitive avalanche events. The effectiveness of the proposed solid-state circuit breaker is validated through experiments conducted in an unclamped inductive switching (UIS) test circuit using a 400-V, 50-A DC distribution system. Eventually, the demonstrations indicate that the SiC diode clamping method contributes to more compact implementations for solid-state circuit breakers.

INDEX TERMS Avalanche breakdown, clamping component, parallel connection, silicon carbide, solid-state circuit breaker, unclamped inductive switching.

I. INTRODUCTION

High-performance DC circuit breakers are necessary to attain high reliability in electric vehicles (EVs), aircraft applications, and low-voltage DC (LVDC) distribution systems [1], [2], [3]. The performance requirements for safety equipment in the DC distribution systems include robustness, high cutoff speed when detecting over-currents, and an increased number of repetitive cutoff operations. However, mechanical circuit breakers, which are widely used in existing DC systems, have problems with slow interrupting speed and contact degradation.

As part of the solution to these problems, solid-state circuit breakers have been widely discussed [4], [5], [6], [7]. They offer several advantages, including compactness, fast current cutoff, and robustness against repetitive uses. These features make them preferable compared to conventional mechanical circuit breakers. Furthermore, these technologies can be applied as multifunctionality and power flow control functions for future DC distribution systems [8], [9], [10], [11].

Silicon carbide (SiC) power semiconductor devices exhibit excellent characteristics of low on-resistance and low failure risk in high junction-temperature environments when compared to Si power semiconductor devices [12], [13], [14]. SiC MOSFETs exhibit these advantages and are one of the leading candidates used in solid-state circuit breakers.

DC circuit breakers serve as the main current path during the steady-state operation of the DC distribution system. During this state, the power devices incur conduction losses because of the on-resistance. Therefore, in solid-state circuit breakers, many power devices should be connected in parallel to share the current to reduce the conduction loss [15], [16].

Simultaneously, the circuit breaker faces substantial energy burdens due to the unclamped inductive loads switching, leading to avalanche breakdown in power semiconductor devices. Major manufacturers and researchers have discussed the avalanche behavior of SiC MOSFETs leveraging the latest power semiconductor technology [17], [18], [19], [20], [21], [22], [23]. These discussions revolve around extending the design possibilities of power electronics circuits, including device usage that allows a certain extent of avalanche operation while prioritizing reliability [18]. Based on this discussion, a design method emerges where SiC power semiconductor devices in a solid-state circuit breaker absorb the cutoff energy themselves [19].

However, in the case of the parallel connection configuration, a current imbalance issue occurs in power semiconductor devices. The phenomenon is caused by the breakdown voltage characteristics of paralleled power devices [24], [25], [26]. Such operations create high thermal conditions biased toward devices with lower breakdown voltage characteristics. Simultaneously, repetitive avalanche breakdown events lead to the degradation of the gate-oxide in SiC MOSFETs, resulting in decreased switching performance and reliability [27], [28], [29]. To address this issue, voltage clamping components are employed to counteract the current imbalance issue to avoid biased stress on the power semiconductor devices.

To reduce the burden on power semiconductor devices, voltage clamping components such as metal-oxide varistors (MOVs) [30], [31], [32], and parallel and/or series connected transient voltage suppression (TVS) diodes [33], [34], as well as snubber circuits [35] are widely discussed to improve cutoff capability and reliability. In the methods, immediately after the current cutoff, the clamping components consume the energy, instead of the power devices. However, MOVs have several issues about degradation through repetitive uses [32], [36] and bulky volume. Additionally, multiple TVS diodes require more mounting area than a single device chip to achieve the same breakdown voltage [37], contributing to higher costs for these implementations. Therefore, these considerations are necessary for achieving more compact module-based solid-state circuit breakers.

SiC merged pin Schottky (MPS) diodes exhibit excellent performance under high surge current events and possess a high avalanche capability [38], [39]. Furthermore, the diodes exhibit beneficial properties in resisting device degradation under repetitive avalanche stress [40], [41]. These attributes render the SiC diodes well-suitable for managing energy dissipation in solid-state circuit breakers for LVDC distribution systems. Moreover, the clamping component use of a single chip contributes to excellent implementation, playing a significant role in the miniaturization of solid-state circuit breakers. The previous paper [16] focused on the application of the diode clamping method to address current imbalance issues. It lacked discussion on component design, circuit implementation, and clamp performance issues.

This paper proposes a circuit breaker comprising paralleled SiC MOSFETs with a SiC MPS diode for avalanche voltage clamping. To discuss the current imbalance issue during avalanche operation, devices with varying breakdown characteristics are verified using two paralleled SiC MOSFETs without clamping components. The results show that the breakdown voltage difference must be suppressed to less than 0.9% of the rated voltage of 1.2-kV SiC MOSFETs. To address this issue, the proposed solid-state circuit breaker incorporates clamping by the SiC MPS diode, which has a breakdown voltage lower than that of SiC MOSFETs. Therefore, during the cutoff period, all current flows through the SiC diode, enabling the circuit breaker to achieve both low conduction loss and avalanche capability in all states of operation. Additionally, a comparison of voltage clamping components shows that the SiC diode clamping method offers a mounting volume advantage over MOVs designed for the same cutoff condition. The proposed method is verified through unclamped inductive switching (UIS) tests conducted on 400-V, 50-A DC distribution systems.

II. UNCLAMPED INDUCTIVE SWITCHING CONDITION

Fig. 1 shows a configuration of the UIS test circuit and ideal waveforms. Due to the energy stored in the wiring inductance in the DC distribution system, the avalanche breakdown of power devices must be modeled to evaluate solid-state circuit breakers. Thus, the UIS test circuit is suitable for evaluating the avalanche breakdown phenomenon in a solid-state circuit breaker.

During steady-state, a gate-source voltage v_{gs} remains on-state. The drain current i_{d} is equivalent to the cutoff current i_{L}. The drain current i_{d} is designed to flow at a maximum cutoff current I_{L}.

The cutoff operation starts at T_1, and the gate-source voltage v_{gs} switches to the off-state. Due to the avalanche breakdown phenomenon, the drain-source voltage v_{ds} reaches the breakdown voltage $V_{\mathrm{BD(MOS)}}$ beyond the rated voltage $V_{\mathrm{DSS(MOS)}}$. After that, the magnetic energy of the line inductance affects the power device.

The avalanche energy E_{AV} is given by

$$E_{\mathrm{AV}} = \frac{1}{2} L {I_{\mathrm{L}}}^2 \frac{V_{\mathrm{BD(MOS)}}}{V_{\mathrm{BD(MOS)}} - V_{\mathrm{DD}}} \ [\mathrm{J}], \tag{1}$$

where $V_{\mathrm{BD(MOS)}}$ is the breakdown voltage of a MOSFET, L is the inductance, and V_{DD} is the input DC voltage. The obtained avalanche energy E_{AV} is given by

$$E_{\mathrm{AV}} = \int_{T_1}^{T_2} v_{\mathrm{ds}}(t) i_{\mathrm{d}}(t) \mathrm{d}t \ [\mathrm{J}] \tag{2}$$

$$= \int_{T_1}^{T_2} p_{\mathrm{MOS}}(t) \mathrm{d}t \ [\mathrm{J}], \tag{3}$$

where p_{MOS} is the dissipated power of the MOSFET. The peak value of p_{MOS} is observed as $V_{\mathrm{BD(MOS)}} I_{\mathrm{L}}$ when the cutoff operation starts.

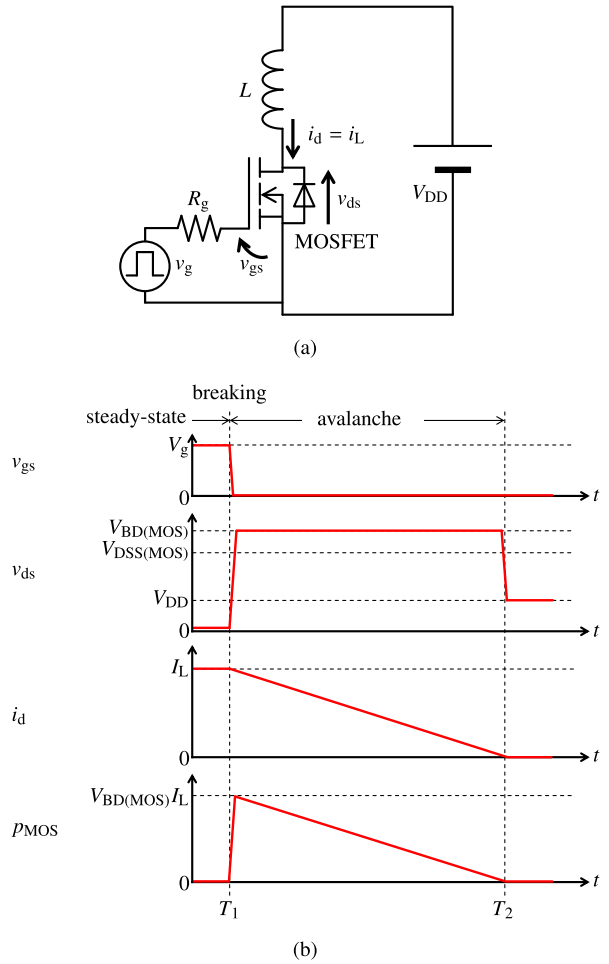


FIGURE 1. UIS test: (a) circuit configuration and (b) waveforms.

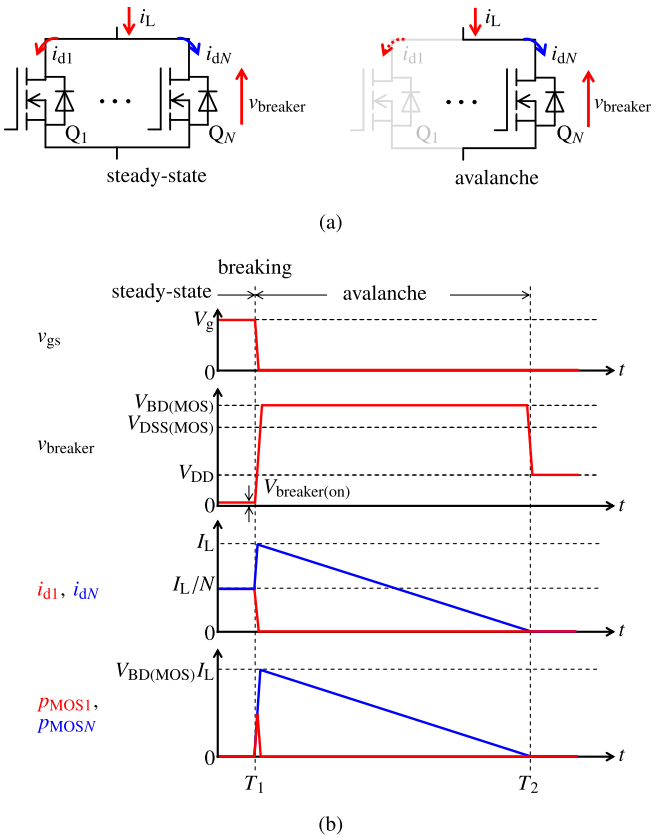


FIGURE 2. Paralleled MOSFETs circuit breaker: (a) configurations and (b) waveforms.

After the avalanche energy E_{AV} in the power devices has been completely consumed at T_2, the avalanche current converges to zero and the cutoff operation is complete. In the case of the solid-state circuit breaker, all the avalanche energy E_{AV} generated during cutoff operation is consumed by the power devices.

III. PARALLEL CONNECTED DEVICES FOR A SOLID-STATE CIRCUIT BREAKER

A. CURRENT IMBALANCE DUE TO VARIATIONS IN INDIVIDUAL DEVICE CHARACTERISTICS

Fig. 2 shows the circuit configurations and waveforms of a paralleled MOSFETs circuit breaker. When the distribution system is in steady-state operation, the rise in self-heating due to the conduction losses in the power devices must be suppressed. Therefore, it is essential to reduce the breaker's on-resistance $R_{breaker(on)}$ by power devices connected in parallel. During the period before T_1, the current flows as a steady-state. During this operation, a conduction loss P_{on} is generated by the breaker's voltage drop $V_{breaker(on)}$. The conduction loss of the circuit breaker P_{on} is given by

$$P_{on} = {I_L}^2 R_{breaker(on)}\,[\mathrm{W}], \tag{4}$$

Because the $R_{breaker(on)}$ of a circuit breaker connected in parallel can be reduced by the power device connected in parallel,

$$R_{breaker(on)} = \frac{R_{ds(on)}}{N}\,[\Omega], \tag{5}$$

where $R_{ds(on)}$ is the drain–source on-resistance of the device and N is the number of power devices connected in parallel. Therefore, the more power devices that are connected in parallel, the lower the loss that occurs. The conduction loss P_{on} affects the thermal design of the device during steady-state operation. The current balance during the steady-state depends on the on-resistance of the power devices or the resistance due to the wire and soldered mounting. The variation in on-resistance, among the few commercially available power devices, does not affect the current balance significantly.

During the cutoff operation, the solid-state circuit breaker is in avalanche operation. However, the current balance during the cutoff operation is affected by the difference in the breakdown voltage characteristics of the power semiconductor devices. Therefore, it is correspondingly difficult to prepare the suitable breakdown voltage characteristics of power devices.

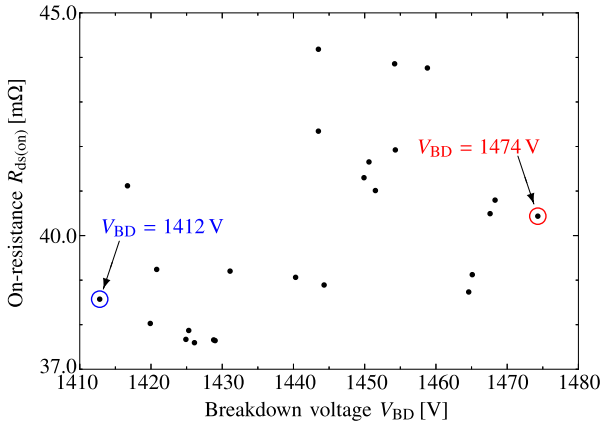


FIGURE 3. Device characteristics of 25 SiC MOSFETs.

TABLE 1. Measurement Results of DUTs Characteristics

Device	V_{BD}	$\lvert\Delta V_{BD}\rvert$	$R_{ds(on)}$
Q_A	1468 V	—	37.5 mΩ
Q_B	1467 V	1.0 V	37.6 mΩ
Q_C	1458 V	10 V	37.8 mΩ
Q_D	1449 V	19 V	37.8 mΩ
Q_E	1440 V	28 V	40.4 mΩ
Q_F	1431 V	37 V	39.0 mΩ
Q_G	1419 V	49 V	38.5 mΩ

B. EXPERIMENTAL INVESTIGATION

Fig. 3 shows the measurement results of the 1.2-kV rated SiC MOSFETs (Infineon IMW120R030M1H [42]) and Table 1 lists the measurement results of devices under test (DUTs) selected for the experiments. Each power device was measured using a semiconductor curve tracer (Iwatsu CS-3200). Twenty-five SiC MOSFET samples exhibited breakdown differences of up to 62 V (marked with red and blue circles in Fig. 3). This voltage value corresponds to 5.1% compared to the device rating. Among these devices, the breakdown voltages V_{BD} of various conditions are in the following Table 1 that verified the impact of the device characteristics on the current balance. The experimental circuit consisted of input voltage $V_{DD} = 400$ V, an air-core inductance $L = 300$ µH, and cutoff current $I_L = 50$ A. The investigations are based on two MOSFETs connected in parallel with an UIS test circuit.

Fig. 4 shows the experimental results of the investigation of the current imbalance with two paralleled SiC MOSFETs. Fig. 4(a) shows the result of using devices with the same characteristics with breakdown voltage difference $\Delta V_{BD} = 1.0$ V (0.08% compared to the rated voltage). In the case of using the same characteristics devices, until the cutoff operation is initiated, the drain currents i_d flow equally. The current balance during the steady-state is affected by the on-resistance $R_{ds(on)}$ and the mounting soldering of devices.

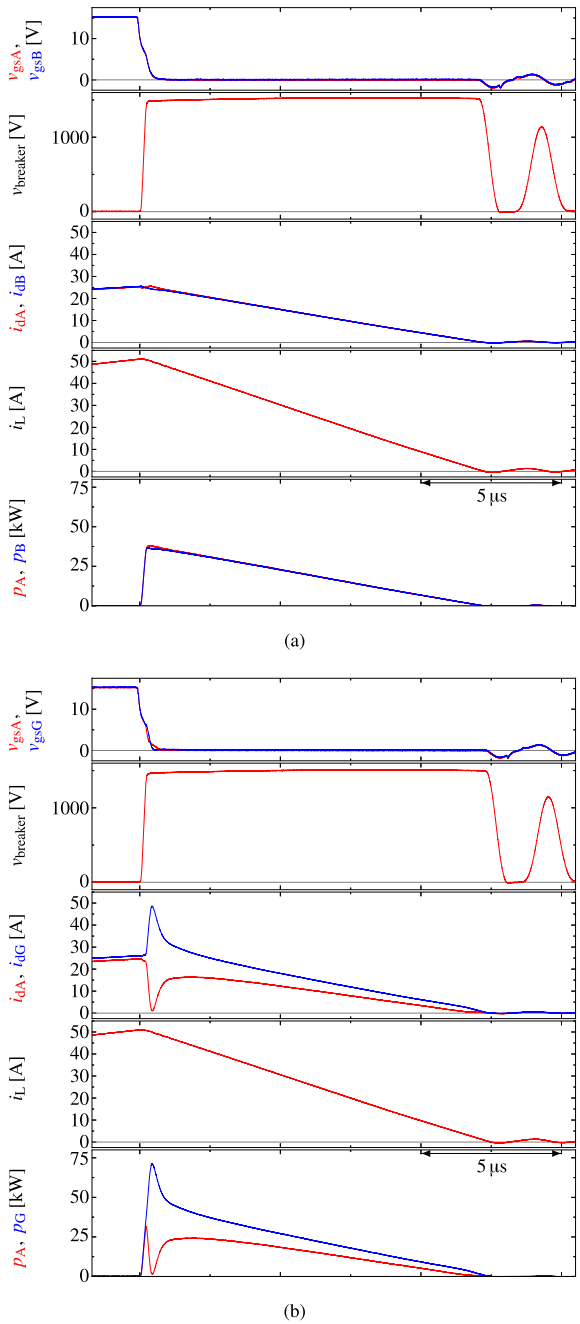


FIGURE 4. Experimental results of the investigation of the current imbalance with paralleled SiC MOSFETs with (a) same characteristics and (b) different characteristics.

The gate-source voltages v_{gs} are set to zero, and the cutoff operation starts. The breaker voltage $v_{breaker}$ immediately reaches the breakdown voltage V_{BD}. During the transition period to the avalanche breakdown, the energy consumption of the devices is still low because the breaker voltage $v_{breaker}$ has not reached the breakdown voltage V_{BD}. During the cutoff operation, the breaker voltage $v_{breaker}$ reaches the breakdown voltage V_{BD}. The cutoff current I_L gradually comes to zero

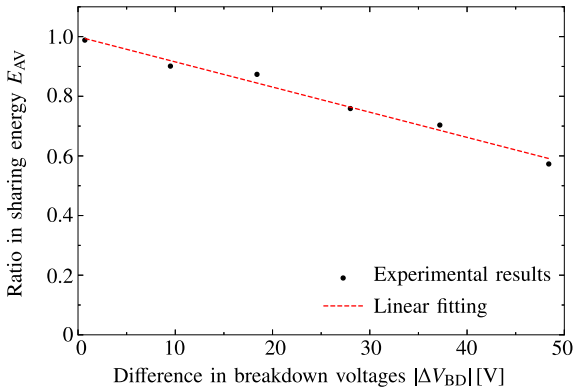


FIGURE 5. Influence of the sharing avalanche energy as a function of the difference in breakdown voltages.

TABLE 2. Comparison of the Shared Avalanche Energy Using Devices With Various Breakdown Voltage Differences

Case	Device	E_{AV}
$\|\Delta V_{BD}\| = 1.0$ V	Q_A	230.6 mJ
	Q_B	227.9 mJ
$\|\Delta V_{BD}\| = 49$ V	Q_A	167.5 mJ
	Q_G	292.4 mJ

as avalanche energy is consumed by the MOSFETs. Regarding the current balance during the cutoff operation, the currents are always equally shared between the MOSFETs. As such, the consumed avalanche energy E_{AV} is also shared equally.

Conversely, Fig. 4(b) shows the result of using different characteristics devices with the breakdown difference $\Delta V_{BD} = 49$ V (4.0% compared to the rated voltage). In the case of using different devices, during the cutoff operation, the drain current is biased toward device Q_G, which has a lower breakdown voltage V_{BD}. The current balance is temporarily $i_{dA} = 1.34$ A and $i_{dG} = 48.6$ A, indicating the current bias. However, the shared current gradually approaches equilibrium after about 2.5 µs. The breakdown voltage tends to increase the voltage value due to the device heating under the avalanche operation, results become equal to V_{BD}, and explains the progressive shift in drain currents [25]. Nevertheless, the current imbalance phenomenon affects the overall consumed avalanche energy and results in imbalanced thermal and avalanche stress.

Fig. 5 shows a summary of the measured sharing of avalanche energy consumption measured with breakdown voltage variations and Table 2 lists a summary of the results. The result shows a nearly linear correlation between energy sharing defects and breakdown voltage characteristic differences. The avalanche energy sharing ratio is impacted by 0.84% per breakdown voltage difference $\Delta V_{BD} = 1.0$ V. Therefore, the breakdown voltage difference ΔV_{BD} must be suppressed to less than 0.9% of the rated voltage of the SiC MOSFET to limit current imbalance to within 10%. Allowing such a current imbalance is deemed unacceptable in the circuit breaker, as the application of avalanche energy under these conditions promotes the degradation of SiC MOSFETs [27], [28], [29].

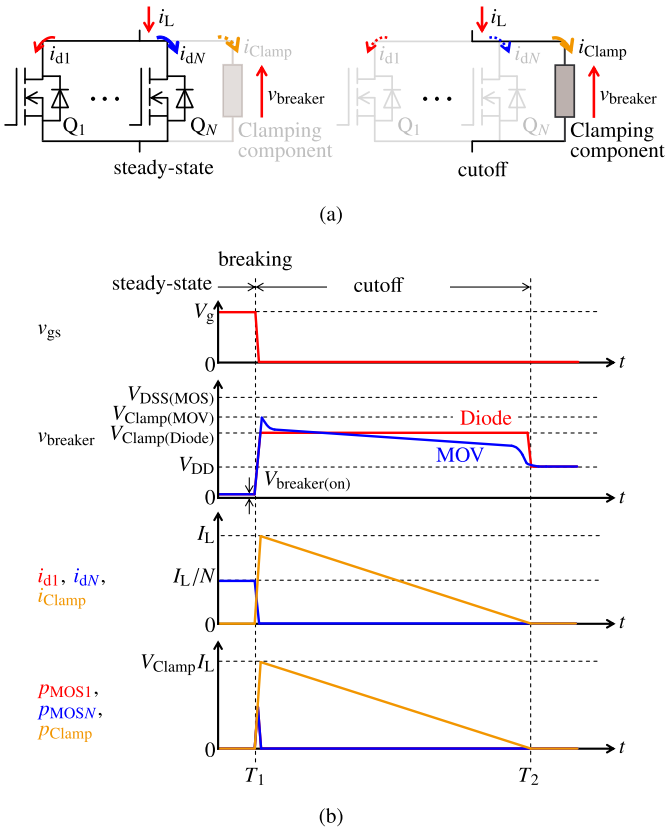


FIGURE 6. Paralleled MOSFETs circuit breaker with a clamping component: (a) configurations and (b) waveforms.

IV. VOLTAGE CLAMPING COMPONENT SELECTION FOR ADDRESSING CURRENT IMBALANCE ISSUE

A. ROLE AND DESIGN CONCEPT OF THE CLAMPING COMPONENT

Although paralleled SiC MOSFETs have sufficient avalanche capability for DC circuit breakers, a challenge in energy sharing during the cutoff operation. Therefore, a clamping component is needed to divert the cutoff current and consume the energy.

Fig. 6 shows circuit configurations and waveforms of the solid-state circuit breaker with a clamping component. In this scenario, the discussion centers around the use of an MOV or a SiC MPS diode as the clamping component.

The clamping component should be rated with a clamping voltage lower than that of the SiC MOSFET rating. Accordingly, the clamp voltage of the clamping component V_{Clamp} must ensure that

$$V_{DD} < V_{Clamp} < V_{DSS(MOS)}. \quad (6)$$

It is also required for the clamping components to have a rated voltage rating that maintains the input DC voltage at the

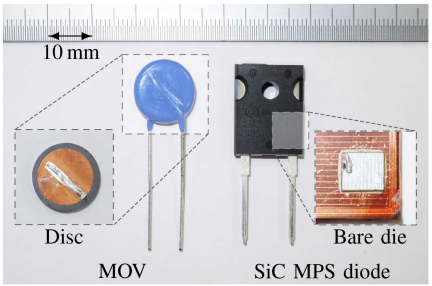


FIGURE 7. Picture of a MOV and a SiC MPS diode for the clamping components.

TABLE 3. Characteristics Comparison of the Components

		MOV	SiC MPS diode
DC rated voltage		560 V	650 V
Clamp voltage		1120 V	930.4 V*
Energy capability		90 J	841 mJ
Size**	Package	14.0 × 14.4 × 6.10	15.9 × 20.9 × 5.02
	Element	13.0 × 13.0 × 2.71	3.90 × 3.50 × 0.40

* Measured breakdown voltage
** width × height × depth [mm]

steady-state. Therefore, the clamping component is required to have

$$V_{DD} < V_{Rated(DC)}, \tag{7}$$

where $V_{Rated(DC)}$ represents the DC rated voltage of the clamping component. Additionally, the clamping components must possess sufficient energy capability for cutoff operations to the condition as

$$E_{CO} = \int_{T_1}^{T_2} v_{Clamp}(t) i_d(t) \mathrm{d}t \ [\mathrm{J}], \tag{8}$$

where E_{CO} represents the cutoff energy consumed by the devices, and v_{Clamp} is the transient clamp voltage.

Considering the long-wiring inductance expected in the DC distribution system, the cutoff energy increases accordingly. Therefore, the energy capability of clamping components should be designed considering the scale of DC distribution systems. The design conditions in this paper are an input voltage $V_{DD} = 400$ V, cutoff current $I_L = 50$ A, and wire inductance $L = 300$ µH.

B. COMPARISON DISCUSSION

Fig. 7 shows a picture of selected MOV (TDK B72214S0421K101 [43]) and SiC MPS diode (GeneSiC GC50MPS06-247 [44]) as clamping components, Table 3 lists a comparison of their characteristics. These components satisfy the design requirements (6)–(8).

It is important to highlight the difference in size between these components. While the packages have similar dimensions for the MOV and the SiC MPS diode, an examination of the internal elements shows that the semiconductor chip

TABLE 4. Feature Comparison of the Voltage Clamping Components

	MOV	Multiple TVS	Proposal
Implementation	—	✓	✓✓
Energy capability	✓✓	✓	✓
Degradation	—	✓	✓

TABLE 5. Measurement Results of the DUTs Characteristics

Device	V_{BD}	$\lvert\Delta V_{BD}\rvert$	$R_{ds(on)}$
Q_H	1474 V	—	40.4 mΩ
Q_I	1440 V	34 V	39.0 mΩ
Q_J	1412 V	62 V	38.5 mΩ
MOV	671.5 V*	—	—
SiC MPS diode	930.4 V	—	—

* Measured at leakage current region.

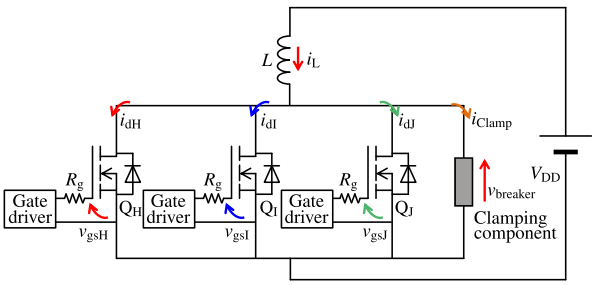
volume of the SiC MPS diode is only 1.51% of that of the MOV disc. As an alternative, using multiple TVS diodes connected in parallel and/or series has been discussed as a similar solution. This method provides more flexibility in designs than MOVs because TVS diodes are available in various clamp voltage lineups [45]. However, achieving the desired clamping voltage and energy capability requires the use of multiple devices. Therefore, the appropriate approach involves employing multiple TVS diodes for energy consumption and voltage clamping [33], [34], resulting in additional mounting volumes.

On the contrary, the clamping method using the SiC MPS diode surpasses others regarding implementation, as the cutoff energy is consumed without the need for sharing among multiple devices. In comparison to the Si material, the use of SiC material provides the clamping diodes with sufficient avalanche capability specifically designed for solid-state circuit breakers. Furthermore, the SiC MPS diodes indicated negligible fluctuations in electrical characteristics even after repetitive UIS events [40], [41], signifying their suitability for long-term usage. These contributions are valuable for prototypes integrating solid-state circuit breakers into high-density power module-based implementations for applications requiring repetitive cutoff uses. Table 4 lists a summary of the features of the clamping components.

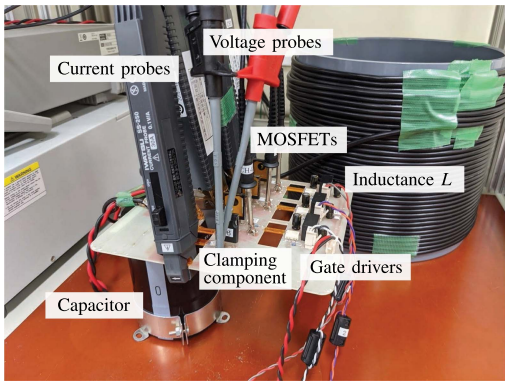
V. EXPERIMENTAL RESULTS

Fig. 8 shows the experimental circuit configuration and a picture of the experimental setup. The demonstrated circuit configuration is based on the UIS test. The circuit consists of three 1.2-kV rated SiC MOSFETs (Infineon IMW120R030M1H [42]) Q_H–Q_J connected in parallel, voltage clamping component MOV [43] or SiC MPS diode [44], gate resistances $R_g = 47\,\Omega$, an air-core inductance $L = 300$ µH, a DC voltage source $V_{DD} = 400$ V, and cutoff current I_L was set to 50 A.

Table 5 lists the measurement results of the device characteristics of the DUTs. The SiC MOSFETs Q_H–Q_J had a



(a)



(b)

FIGURE 8. Experimental setup: (a) circuit configuration and (b) picture of the circuit board.

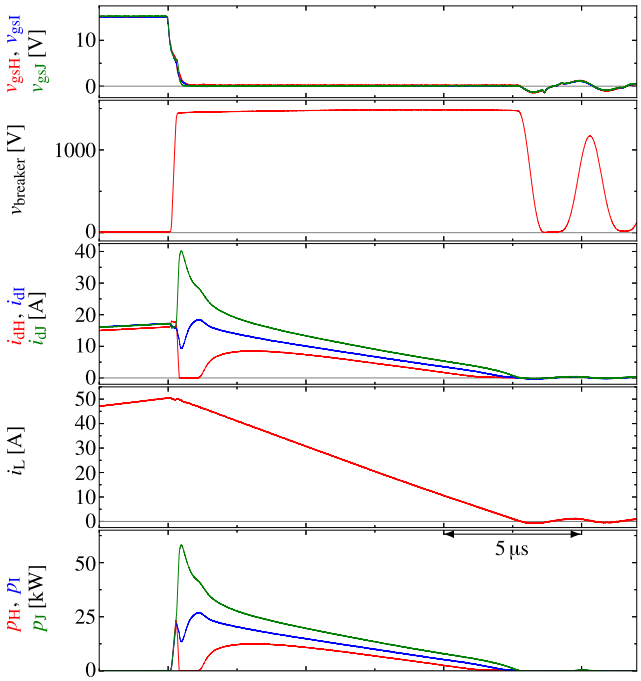


FIGURE 9. Experimental results of the case without the clamping component using MOSFETs with different breakdown characteristics.

breakdown voltage difference ΔV_{BD} of up to 62 V, which corresponds to 5.1% of the rated voltage of the SiC MOSFET. To reduce the conduction losses and verify the current balance of the parallel connected devices, three MOSFETs were used in the prototype circuit.

Fig. 9 shows the experimental results of a paralleled SiC MOSFETs circuit breaker without the clamping component. When the breakdown voltage characteristics are different, the currents are not balanced. The cutoff energies consumed by the MOSFETs were calculated to be 82.5 mJ, 151 mJ, and 225 mJ. From the result, the difference in breakdown voltage characteristics affects the bias of cutoff energy consumption and results in imbalanced avalanche stress.

Fig. 10 shows the results of the experiment conducted on a solid-state circuit breaker with an MOV serving as a voltage clamping component. At the onset of the cutoff operation, the breaker voltage $v_{breaker}$ reaches the clamp voltage of the MOV $V_{Clamp} = 1138$ V, diverting the current flows through the MOV, instead of the paralleled MOSFETs. Consequently, the breaker voltage $v_{breaker}$ continues to be clamped by the MOV with non-linearity. During this time, the avalanche current flows through the MOV, consuming the cutoff energy. Therefore, the paralleled MOSFETs avoid consuming the energy. In contrast, the calculated cutoff energy consumed by the MOV is 571 mJ.

Fig. 11 shows the results of the experiment conducted on with the SiC MPS diode clamping. At the initiation of the cutoff operation, the breaker voltage $v_{breaker}$ reaches the breakdown voltage of the SiC MPS diode, and the current flows through the SiC MPS diode similarly to using the MOV. However, in the case of the SiC diode clamping method, the breaker voltage $v_{breaker}$ remains almost constant at the breakdown voltage $V_{BD(Diode)} = 984$ V during the cutoff operation. Consequently, the calculated cutoff energy consumed by the diode is 550 mJ. The diode rated avalanche energy is 841 mJ [44], indicating that the diode maintains a margin of avalanche energy. These experimental results show that the SiC MPS diode can withstand a cutoff of up to 50-A without device destruction. Moreover, the diode clamping performs comparably to the MOV clamping method.

TABLE 6. Comparison of the Shared Cutoff Energy With Each Clamping Method

Clamping method	Device	E_{CO}
Without	Q_H	82.5 mJ
	Q_I	151 mJ
	Q_J	225 mJ
With MOV	Q_H	5.00 mJ
	Q_I	2.22 mJ
	Q_J	1.15 mJ
	MOV	571 mJ
With diode	Q_H	4.07 mJ
	Q_I	2.30 mJ
	Q_J	4.33 mJ
	SiC MPS diode	550 mJ

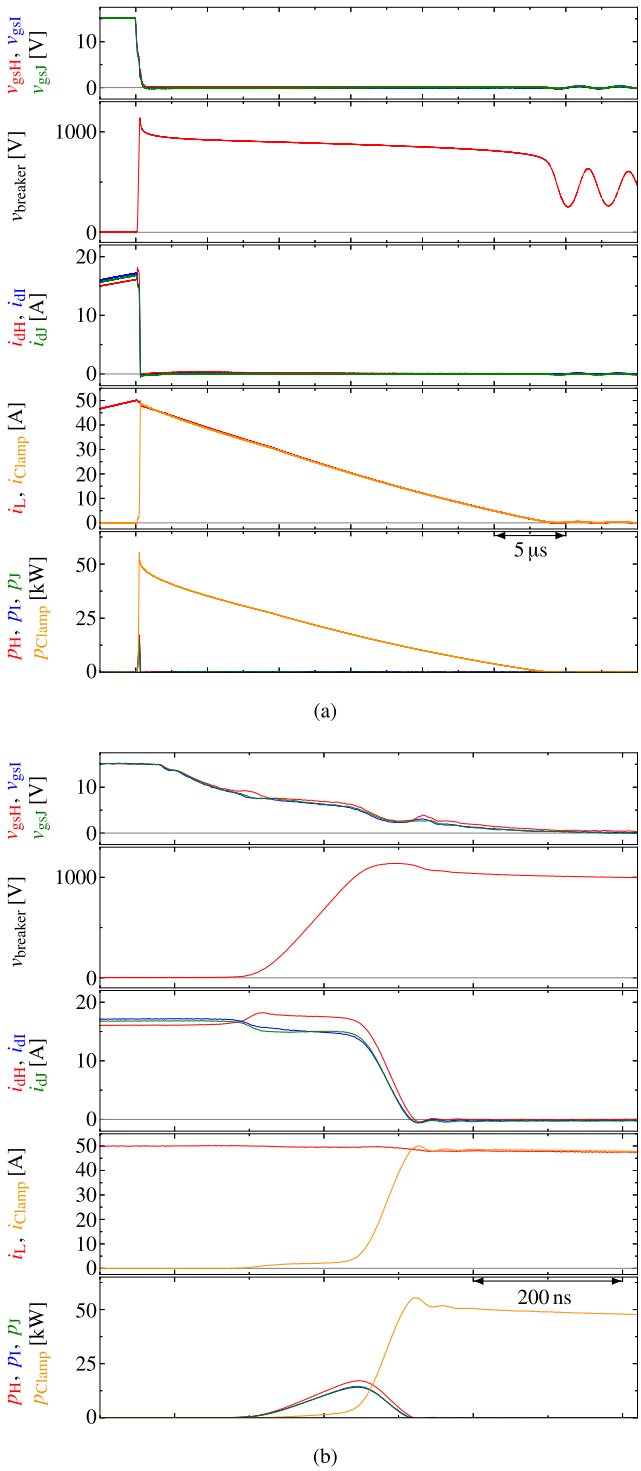


FIGURE 10. Experimental results of solid-state circuit breaker with a MOV clamping: (a) cutoff operation and (b) expanded waveforms.

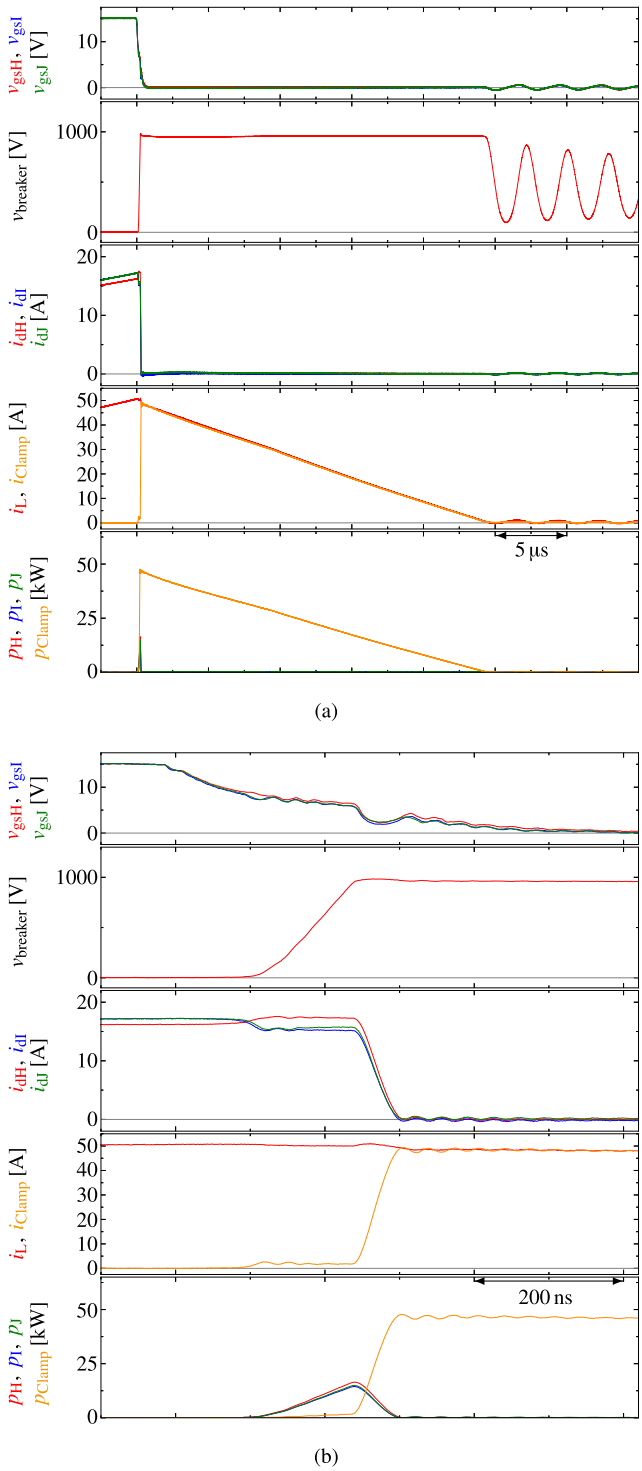


FIGURE 11. Experimental results of solid-state circuit breaker with a SiC MPS diode clamping: (a) cutoff operation and (b) expanded waveforms.

Table 6 lists a summary of the shared cutoff energy using different methods and Table 7 lists the comparison of cutoff energy densities with each voltage clamping component under the same cutoff condition. From the perspective of the energy consumption densities, the SiC MPS diode method demonstrated a significant improvement, approximately

TABLE 7. Experimental Results of Consumption Energy Densities

Component	Cutoff energy	Size	Energy density
MOV	571 mJ	359 mm^3	1.58 J/cm^3
SiC MPS diode	550 mJ	5.46 mm^3	100 J/cm^3

63.5 times better than the MOV method under the same cutoff condition. Therefore, using the SiC diode as a clamping component contributes to achieving high cutoff energy density and facilitates the miniaturization of solid-state circuit breakers.

VI. CONCLUSION

This paper proposed a solid-state circuit breaker comprising paralleled SiC MOSFETs and a SiC MPS diode for avalanche voltage clamping. The experimental results reveal that the circuit breaker effectively addresses the current imbalance issue in the case of 1.2-kV SiC MOSFETs under UIS tests conducted with a 400-V, 50-A DC distribution system. Simultaneously, the proposed solid-state circuit breaker was clamped by a single chip SiC diode consuming the cutoff energy. Thus, the SiC diode possesses sufficient avalanche capability to serve as a voltage clamping component in solid-state circuit breakers. Moreover, the SiC diode clamping method demonstrates a 63.5 times higher consumption energy density than the MOV clamping method while providing comparable clamp performance. The demonstration indicates more compact implementations for solid-state circuit breakers.

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