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A Delta-Sigma Modulated Power Converter With Inherent Zero-Voltage Switching

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ABSTRACT In this paper an advanced modulation strategy is proposed that generates the switch control signals of a power converter while inherently guaranteeing zero-voltage switching (ZVS) operation. The proposed modulator is based on a first-order $\Delta\Sigma$-modulator combined with a hold-off circuit. This hold-off circuit consists of a D-latch and maintains the converter's switching state until ZVS commutation can be achieved while an integrator ensures the correct average output. Furthermore, features are implemented to improve start-up and transient behavior. The operating principle and stability of the proposed modulator is discussed and simulation results are presented. Finally, the proposed modulator is validated on a 2 kW GaN-based synchronous buck converter. Results show that the converter naturally operates under ZVS conditions by continuously varying its switching frequency without having to compute switching times or frequencies. The proposed method is an interesting alternative to pulse-width modulation especially when operating at high switching frequencies or when the switching loss in the power converter is significant.

INDEX TERMS Modulation strategy, delta-sigma modulation, zero-voltage switching, high frequency power converter, variable frequency, elektromagnetic interference, dc-dc converter.

I. INTRODUCTION

Power converters are essential in many applications such as renewable energy systems, electric vehicles and consumer electronics. Development of more efficient, compact and robust power converters is fueled by modern wide-bandgap semiconductor materials such as Silicon Carbide (SiC) and Gallium Nitride (GaN). Their superior performance characteristics allows to operate power converters at ultra-high switching frequencies and, as a result, reduce the size of passive components [1]. However, despite the fast switching speeds and lower switching energy of wide-bandgap semiconductors, operating at very high switching frequencies can result in significant switching loss. To reduce switching loss, operating under so-called zero-voltage switching (ZVS) conditions can be beneficial [2]. Power converters which allow ZVS operation have been extensively studied, for example by Henze et al. in 1988, which addressed conventional non-isolated buck, boost, and buck-boost converter topologies [3]. In scenarios requiring isolation, the single- and three-phase dual active bridge (DAB) dc/dc converters are preferred, as introduced by De Doncker in 1991 [4]. Everts and colleagues further expanded upon this by describing a procedure to achieve ZVS across the entire operating range of a single-phase single-stage DAB ac-dc converter [5].

For non-isolated power converters like the conventional buck converter and quasi-resonant (QR) converters, there has been a significant research effort to develop ZVS control techniques. This includes work by Tabisz in 1989, which laid foundational research in this area [6]. Chiang et al. demonstrated the operation of a buck converter in discontinuous conduction mode (DCM) to achieve ZVS operation using pulse-width modulation [7]. An innovative approach was presented by Lee in 2014, where an auxiliary switch, a diode, and coupled inductor were added to the buck converter to facilitate ZVS operation [8]. Huang et al. took a different approach by manipulating the switching frequency

of a dual-buck converter, calculated numerically, to maintain ZVS operation [9]. Additionally, Marxgut and colleagues introduced the triangular current modulation (TCM) method in 2010, which achieves ZVS operation over a broad operating range by computing switching times [10].

The pursuit of modulation techniques that result in ZVS operation encompasses a variety of approaches, each suited to specific conditions that include converter topology. This study concentrates on the traditional non-isolated half-bridge switching leg. When equipped with an LC-output filter, it is frequently referred to as a synchronous buck converter. In this type of converter, the inductor current ripple is influenced by several factors: supply voltage, inductance, duty cycle, and switching frequency. When outputting a large dc current, the inductor current ripple may be relatively minor in comparison to the load current. This scenario leads to hard-switching in one of the semiconductor switches. Moreover, as the converter operates in continuous conduction mode (CCM) it makes Chang's method inapplicable and, alternatively, adding auxiliary components to the converter is not favored. While Huang's strategy involves calculating an switching frequency and the triangular current modulation (TCM) method proposes to calculate switching times, neither approach reliably ensures ZVS operation during transient conditions, which limits the converter's dynamic performance. Furthermore, the TCM's reliance on an iterative numerical calculations makes it challenging to implement in real-time. An alternative solution is to pre-compute data and store it in multidimensional lookup tables for various steady-state operating points. However, this approach faces its own set of challenges, such as computational delays during interpolation or the requirement for considerable memory space to enhance table density.

The proposed modulator obtains ZVS operation by actively checking whether natural commutation is possible before changing its switching state. As a result, ZVS operation is obtained regardless of the converter design and the modulator naturally varies its switching frequency resulting in a minimized inductor current ripple. The inductor current when using the proposed solution is similar to the inductor current seen when using a zero-voltage switching hysteresis current controller (ZVS-HCC) [11]. Despite this similarity, a ZVS-HCC naturally controls the output current whereas the proposed method controls the output voltage. A current controlled converter behaves as a current source, which can be beneficial depending on the application. The proposed ZVS-DSM modulator combines several desired features such as variable frequency operation, guaranteed ZVS and low computational effort. The modulator requires the instantaneous inductor current to determine if switching is allowed or not. In combination with the integrator present in the first-order $\Delta\Sigma$-modulator, the correct average output is ensured. Information about the instantaneous can be obtained using hardware comparators, analog-to-digital converters, estimators or other methods. Which method is most suited depends on the application and allowable measurement latency. In the next section, a brief introduction to $\Delta\Sigma$ modulation is given before discussing the proposed modulator in Section III. Simulation results are presented in Section IV. Implementation details and verification on a 2 kW GaN-based prototype are discussed in Section V.

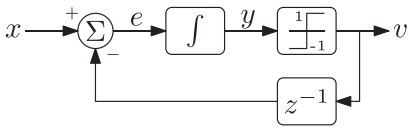

FIGURE 1. First-order $\Delta\Sigma$-modulator with a two-level quantizer.

II. FIRST-ORDER DELTA-SIGMA MODULATORS

Delta-Sigma ($\Delta\Sigma$) modulators, also known as noise-shapers, are often used in data communication systems, audio amplifiers and analog-to-digital converters. Their main benefit is that they can generate a low-bandwidth high-quality signal using a high-bandwidth low-resolution signal at an increased sample rate. When used in a power converter, the low-resolution signal is generated by a switching leg operated at a high switching frequency. This low-resolution signal is filtered using the power converter's output filter to obtain the desired high-quality output signal.

Fig. 1 depicts an overview of a first-order $\Delta\Sigma$-modulator in its most basic configuration. It consists of an integrator which integrates the difference of the input x and the feedback signal. The resulting integral y is fed into a quantizer before outputting the quantized signal v. This integrator ensures that, on average, the generated output data v is equal to the input x. Due to the inherent nature of a first-order $\Delta\Sigma$-modulator, the generated output data might contain a repeating sequence of pulses especially when the input is a dc reference. This repeating sequence of pulses can be seen as limit cycles present on the output. Methods have been proposed to attenuate these limit cycles, for example by adding pseudo-random white noise to the input reference [12] or by adding a feedback-loop that acts on non-idealities in the modulator output [13].

Several methods have been proposed to analyze the behavior of a $\Delta\Sigma$-modulator and a commonly used method is the additive-noise approach. This method replaces the quantizer by a linear gain and white-noise source which models the noise introduced by the quantizer. A detailed analysis of a first-order $\Delta\Sigma$-modulator using the additive-noise approach is given in [14]. It shows that a first-order modulator has a unity signal-transfer function (STF) and a noise-transfer function (NTF) of

$$\mathrm{NTF} = 1 - z^{-1}, \tag{1}$$

meaning that it provides only 20 dB of noise attenuation per decade for frequencies below the sampling frequency. This value is lower compared to higher-order modulators. However, the first-order modulator has the unique property of being inherently stable for input signals that are within in the quantizer bounds [15]. Especially for a power converter, this

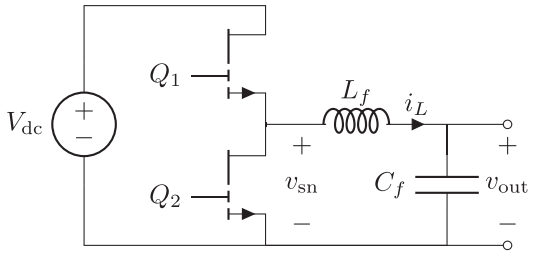

FIGURE 2. Controlled half-bridge power converter.

stability property is convenient when using a $\Delta\Sigma$-modulator to generate the switch control signals.

The basic principle of $\Delta\Sigma$-modulator, i.e. integrating an error feedback signal and comparing the integral against a threshold value to generate the switch control signals of a power converter dates back to the 1970's. In [16], Schwarz proposed an Analog-Signal-to-Discrete-Time-Interval converter (ASDTIC) to control a power converter. The ASDTIC works by integrating a voltage error and feeding the integral to a pulse generator, resulting in "excellent" voltage regulation. A modified concept of the original ASDTIC provided a second control loop to the ASDTIC to further improve its dynamic performance and provide overload protection [17]. Some of the control aspects can still be used nowadays albeit in the digital domain.

III. A FIRST-ORDER $\Delta\Sigma$-MODULATOR WITH INHERENT ZERO-VOLTAGE SWITCHING

One of the benefits when using the $\Delta\Sigma$ modulation principle is that the modulator structure can easily be adjusted. In this section, the structure of a first-order $\Delta\Sigma$-modulator is modified to guarantee ZVS operation in a half-bridge power converter. The half-bridge circuit as used in this work is shown in Fig. 2. It consists of a high-side switch Q_1, low-side switch Q_2, filter inductor L_f, output capacitor C_f and an input source V_{dc}. To reduce the switching loss, voltage stress on the semiconductors and electromagnetic interference (EMI), ZVS operation is favorable [18]. First, the requirements to achieve ZVS operation are discussed.

A. ZERO-VOLTAGE SWITCHING

In practice, semiconductor switches have a parasitic output capacitance often denoted as C_{oss}. During a switching action, these capacitors have to be charged and discharged. If the switching is forced, i.e. hard-switching, the energy stored in these capacitors is dissipated in the switch resulting in significant switching loss and increased EMI. Ideally, to reduce the switching loss, natural charging and discharging of the output capacitors is desired. This so called soft-switching, or zero-voltage switching, can be achieved by charging and discharging the capacitors utilizing charge displacement of the filter inductor L_f. For the considered application, ZVS

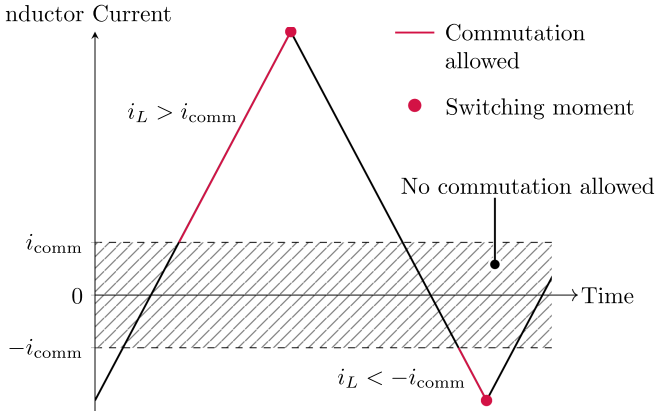

FIGURE 3. Allowed switching moments to achieve soft switching.

operation can be achieved when

$$\begin{cases} i_L > i_{comm} & \text{when turning off } Q_1 \\ i_L < -i_{comm} & \text{when turning off } Q_2. \end{cases} \tag{2}$$

for

$$i_{comm} \geq \frac{1}{Z_0}\sqrt{(2\,v_{out} - V_{dc}) \cdot V_{dc}} \tag{3}$$

where $Z_0 = \sqrt{L_f/C_{sn}}$ and C_{sn} is the total lumped switch-node capacitance [2]. If the lower bound for i_{comm} is used, the worst-case commutation time is a quarter of the resonance period. In reality, the selected i_{comm} is a trade-off between multiple aspects such as the commutation speed, required blanking time, RMS currents in the converter and blanking-time related distortion. For example, a larger value for i_{comm} results in increased RMS currents flowing in the power converter hence more conduction loss in the switching leg. However, increasing i_{comm} also reduces the required amount of blanking-time reducing the reverse conduction loss and blanking-time related distortion. Selecting an appropriate commutation current essentially is an optimization problem and outcomes vary depending on converter specifics such as the topology and semiconductor switches. In this work, C_{sn} is assumed to be linear to simplify the choices for i_{comm} and blanking time as detailed in the experimental chapter. A more in-depth analysis of the blanking time effect is provided in [19].

B. MODULATOR STRUCTURE

The ideal inductor current envelope, excluding commutation, is visualized in Fig. 3. In the band between $-i_{comm}$ and i_{comm}, switching is not allowed. Once switching is allowed, indicated with the red line, the actual switching moments depend on the output of the modulator. To generate this type of inductor currents, a modifcation to the standard first-order $\Delta\Sigma$-modulator is needed. In [20], a so-called hold-off circuit between the integrator and quantizer is proposed. This hold-off circuit essentially is a D-latch meaning that the output holds its value while the control signal is logic low. As a result, the converter

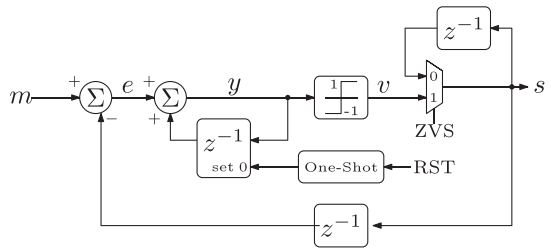

FIGURE 4. Proposed ΔΣ-modulator with hold-off circuit and reset functionality for the peak current limiter and $\frac{di}{dt} = 0$ detection.

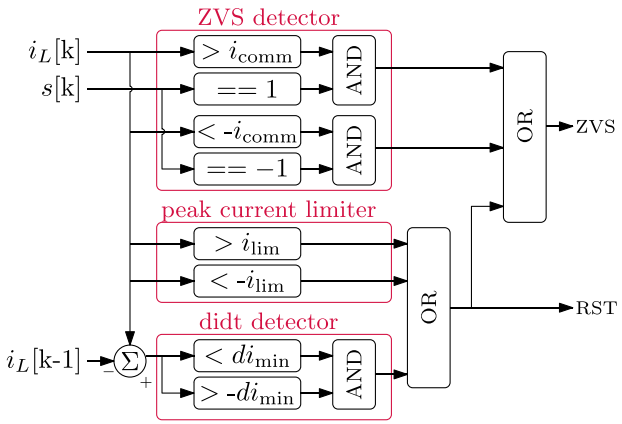

FIGURE 5. Circuit for generating the ZVS and RST control signals.

holds its current switching state while the requirements for ZVS operation are not met. In the mean time, the integrator remains active and ensures that on average the correct output signal is generated. For example, when an output signal with 50% duty cycle is requested and the high-side turn-on time is extended, the integrator will naturally extend the low-side turn-on time to reach the desired 50% duty cycle. An overview of a digital first-order ΔΣ-modulator with hold-off circuit in the form of a multiplexer is shown in Fig. 4. The modulator output is a switch control signal s having a value of either -1 or $+1$, as defined by the quantizer. When the switch control signal s equals $+1$, switch Q_1 is enabled while Q_2 is enabled if s equals -1.

In the overview of Fig. 4, two additional control signals are introduced, called RST and ZVS. The reset signal RST can reset the integrator memory to zero, resulting in a switching action of the modulator. To guarantee this switching action, it is important to implement the quantizer in such a way that it changes the output value when the value equals zero. The second signal, ZVS, is used to hold the modulator output when soft-switching operation is not posssible. Once ZVS operation is achieved, the ZVS signal is logic high and the quantizer output v determines the modulator output. Generation of the control signals RST and ZVS is realized using a digital circuit with relational and logical operators, as shown in Fig. 5. Both signals are based on the sampled inductor current i_L[k] and switch control signal s[k]. Levels are defined for the commutation current i_{comm}, peak current limit i_{lim} and minimum difference between two successive inductor currents di_{min}. As the modulator is implemented on a digital control platform, everything is running at a fixed sample frequency $f_{\Delta\Sigma}$.

C. PEAK CURRENT LIMITER

During a transient, the proposed ΔΣ-modulator ramps the inductor current to go to the new setpoint as quickly as possible. Given that the modulator operates without a fixed switching frequency, it tends to a low switching frequency with long on times for the switches, leading to a substantial inductor current. This behavior is undesired as it can damage the power converter. To address this, a peak current limiter is introduced. The peak current limiter sets a maximum inductor current, and once this threshold is surpassed, the modulator will switch. Importantly, this limitation doesn't compromise the ZVS operation. Rather it serves to cap the maximum current supplied by the switching leg. Consequently, during a transient, the output capacitance is (dis)charged at a constant rate for a certain duration, resulting in an almost linear change in the output voltage according to

$$\frac{\mathrm{d}v_C}{\mathrm{d}t} = \frac{i_C}{C}. \tag{4}$$

The average current supplied by the switching leg during this mode equals

$$\langle i_L \rangle = \frac{i_{lim} - i_{comm}}{2}, \tag{5}$$

where i_{lim} is the maximum allowed inductor current. Once the modulator detects that the inductor current i_L exceeds i_{lim}, it will change the switching state by resetting the integrator to zero using the RST control signal. After resetting the integrator, the modulator can continue to operate normally. During a large transient, the inductor current reaches the peak current during several cycles before transitioning naturally to the new setpoint.

D. DETECTION OF $\frac{di}{dt} = 0$ EVENTS

When the power converter's output voltage v_{out} is close to either of the power rails, the proposed modulator does not naturally switch when the derivative of the inductor current is zero. This can happen when the output voltage is too small, for example during start-up, and the inductor current can not reach the value $-i_{comm}$. If the output voltage is close to the positive power rail V_{dc}, the filter inductor L_f and output capacitance can also start to resonate due to the small voltage difference across the inductor. This undesired behavior is described in [19] and can be detected by analyzing the change of inductor current $\mathrm{d}i_L$ between two consecutive samples. When the change in inductor current equals zero, a switching action is forced using the previously defined RST control signal. By forcing a switching action, the power converter continues to run and will not enter an undesired operating point. In practice, a minimum difference di_{min} is defined between

two successive current samples i_L[k]. When this minimum is reached, the switching action is forced by asserting the RST signal as shown in Fig. 5.

The forced switching action might impact ZVS operation depending on the situation. For example during start-up, when $-i_{\text{comm}}$ is not reached due to v_{out} being zero, natural commutation of the switching-node is lost as the energy stored in the inductor is too small.

E. STABILITY

A first-order $\Delta\Sigma$-modulator is stable as long as the input signal is located inside the quantizer bounds. This can be easily seen from the modulator behavior. For this explanation, the modulator as shown earlier in Fig. 1 is used. First, assuming that the integral is positive, the quantizer outputs a +1. Given that the input value lays within the quantizer range, thus $-1 < x < 1$, the error signal e is negative. A negative error signal results in a decreasing integral until, at some point, it becomes negative and thus the output changes to -1. Now, with a negative output, it is clear that the error signal is positive given $-1 < x < 1$ and thus the integral is increasing. This process is continuously repeating and since the integral is bounded, the modulator is stable.

After adding the proposed hold-off circuit it is important to understand its influence on the modulator stability. Regardless of the hold-off circuit, the integrator still counts upwards when the output equals -1 and downwards when the output is +1. Additionally, the converter's behavior needs to be considered so that it is guaranteed that the hold-off ZVS signal repetitively becomes high. For this, the inductor current slope is analyzed. The change of inductor current i_L depends on the voltage across the inductance

$$\frac{\mathrm{d}i_L}{\mathrm{d}t} = \frac{v_L}{L}. \tag{6}$$

When the integral is positive and the modulator enables the high-side switch Q_1, the voltage v_{sn} applied by the switching leg is V_{dc}. Assuming the output voltage is below V_{dc}, the voltage across the inductance is positive thus the inductor current is increasing. As both the inductor current is increasing and the integral is decreasing, at some point the modulator is allowed to turn-on the low-side switch Q_2. Then the switching leg voltage v_{sn} equals 0 V and the inductor voltage is negative. This results in a decreasing inductor current, an increasing integral and the modulator is heading towards a state where the high-side switch Q_1 is allowed to turn on.

The proposed modulation strategy is implemented digitally and therefore it is important that the integrator bandwidth is set appropriately to prevent overflow. Based on the inductor current envelope, upper and lower bounds for the integral value $\Delta\Sigma_{\text{integral}}$ can be calculated. The bounds depend on the output current i_{out} during a switching cycle, if i_{out} is positive the integral is bounded between

$$-1 < \Delta\Sigma_{\text{integral}} \leq \frac{4L_f \cdot (i_{\text{out}} + i_{\text{comm}})}{t_{\Delta\Sigma} V_{\text{dc}}} \tag{7}$$

where $t_{\Delta\Sigma}$ is the time period at which the modulator is updated, L_f the filter inductance, i_{comm} the commutation current and V_{dc} the input voltage. For a negative average output current during a switching cycle, the bounds equal

$$\frac{4L_f \cdot (i_{\text{out}} - i_{\text{comm}})}{t_{\Delta\Sigma} V_{\text{dc}}} \leq \Delta\Sigma_{\text{integral}} < 1. \tag{8}$$

Since the modulator behavior is cyclic and the $\Delta\Sigma$ integral is bounded for a finite output current, the modulator is considered stable.

F. SWITCHING FREQUENCY RANGE

The proposed modulator inherently operates at a variable switching frequency. The peak-to-peak inductor current ripple continuously varies for changes in the output voltage and average load current. Compared to PWM operated power converters, the designer cannot force a switching frequency as it is governed by the component values and operating conditions. Based on the DC-link voltage and expected operating conditions, the filter inductance should be chosen to match the desired frequency range.

The inductor current envelope is analyzed to derive an equation for the switching frequency range. For positive output currents, the inductor current varies between $-i_{\text{comm}}$ and i_{peak} where

$$i_{\text{peak}} = 2 \cdot (i_{\text{out}} + i_{\text{comm}}). \tag{9}$$

When the high-side switch is enabled, the inductor current increases since the voltage across the inductance equals $V_{\text{dc}} - v_{\text{out}}$. Using (6), the time it takes for the inductor current to rise from $-i_{\text{comm}}$ to i_{peak} is calculated. Similarly, the time that the low-side switch is enabled can be calculated. By adding those two time periods, an equation is obtained to calculate the steady-state switching frequency for a specific operating point:

$$f_{\text{sw}} = \frac{v_{\text{out}} \cdot (V_{\text{dc}} - v_{\text{out}})}{2L_f V_{\text{dc}} \cdot (|i_{\text{out}}| + i_{\text{comm}})}. \tag{10}$$

Based on (10), an upper bound for the switching frequency is visible. Under no-load conditions, i.e. i_{out} equals zero, the converter is switching between $-i_{\text{comm}}$ and i_{comm} at its maximum switching frequency. The switching frequency reduces with increasing power as the frequency is inversely proportional to the supplied output current. The minimum frequency the converter can operate at is defined by the resonance frequency of the output filter: after a half resonant period, the $\frac{\mathrm{di}}{\mathrm{dt}} = 0$ detector asserts a switching action.

IV. SIMULATION RESULTS

Behavior of the proposed $\Delta\Sigma$-ZVS modulator is initially verified using MATLAB. The converter as depicted in Fig. 12 is implemented in Plexim PLECS. The converter is controlled in open-loop and modulation index setpoints are sent to the proposed $\Delta\Sigma$-modulator. Since the converter is controlled in open-loop, an output capacitance C_d is connected across the

TABLE 1. Simulation Parameters

Parameter	Symbol	Value
Input Voltage	V_{dc}	200 V
Switch Resistance	$R_{Q_{1,2}}$	50 mΩ
Filter inductor	L_f	15 µH
Filter capacitor	C_f	2.8 µF
Damping capacitor	C_d	30 µF
Damping resistor	R_d	3 Ω
Load resistor	R_{load}	50 Ω
Modulator frequency	$f_{\Delta\Sigma}$	40 MHz
Modulator period	$t_{\Delta\Sigma}$	25 ns
Commutation current	i_{comm}	2 A
Blanking time	t_{bt}	75 ns

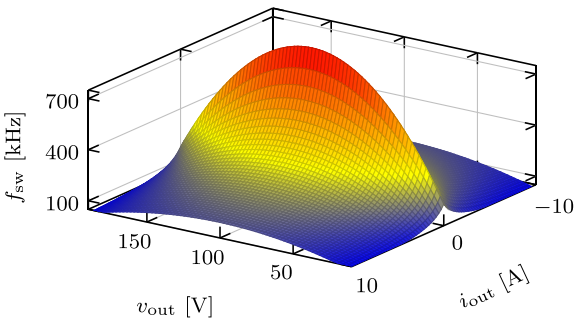

FIGURE 6. Calculated steady-state switching frequencies.

output terminals with a series resistance R_d to dampen oscillations of the LC-circuit. Furtermore, a resistive load R_{load} is connected to the output terminals of the converter. Simulation parameters are given in Table 1. Based on these parameters, the steady-state switching frequencies can be calculated using (10) resulting in the surface plot depicted in Fig. 6.

The modulator is updated at a rate of 40 MHz, meaning that a new switching state is calculated every 25 ns. To determine whether ZVS operation is achievable, a sampled version of the inductor current $i_L[\mathrm{k}]$ is needed. For these ideal simulations, the current is sampled every 25 ns with one sample delay. However, this is difficult to achieve in a practical application and the impact of this delay on the sampled inductor current is discussed in the implementation chapter.

A. STEADY-STATE BEHAVIOR

First, a dc modulation index m of 0 is fed to the proposed $\Delta\Sigma$-modulator to visualize the behavior explained in Section III. Given the input voltage of 200 V, the expected output voltage equals

$$\langle v_{\mathrm{out}} \rangle = \frac{1}{2}(m+1) \cdot V_{\mathrm{dc}} = 100\,\mathrm{V}. \tag{11}$$

In Fig. 7, the modulator waveforms are shown. In the top plot, the integral y and hold-off signal ZVS are shown. The modulator output is depicted in the middle plot and the bottom plot shows the inductor current and output voltage of the converter.

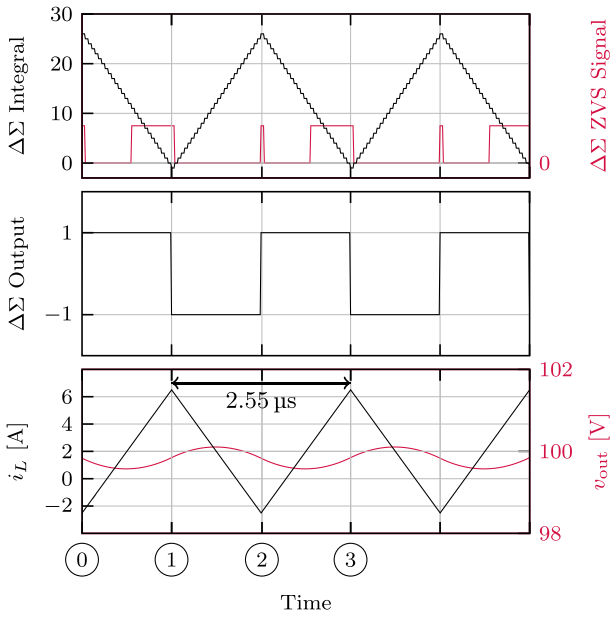

FIGURE 7. Simulated modulator behavior for a dc operating point.

To explain the modulator's behavior, the converter states are discussed starting at the period between ⓪ and ①. During this period, the high-side switch Q_1 is enabled, the inductor current i_L is increasing and the integral y is decreasing. In order to turn-on the low-side switch Q_2, i_L must be larger than i_{comm} (chosen to be 2 A) to guarantee soft-switching and the integral must be negative. Once this is realized, the hold-off signal ZVS becomes high. The modulator then switches at time instance ① as the integral becomes negative. Now the low-side switch Q_2 is enabled, the inductor current is decreasing and the integral increases. The enable signal is low and remains low until the inductor current i_L is smaller than $-i_{\mathrm{comm}}$ (−2 A). Once this signal becomes high at time instance ②, the integral is already positive and thus the high-side switch Q_1 is enabled immediately. This cycle is repeating continuously and, at this operating point, the converter is switching at a frequency of approximately 392 kHz whereas the calculated switching frequency equals 406 kHz. It differs marginally as the inductor current ripple is assumed to be between −2 A and 6 A while in the simulation it is slightly larger due to measurement and control delays effectively lowering the frequency.

B. STABILITY

As seen in Fig. 7, the proposed modulator is continuously going to a state where an other switch is enabled, i.e. it will not stay in one switching state. This implies that the integral always stays around zero as both a positive and negative integral values are needed for switching. The integral range depends on the input sent to the modulator where a larger modulation index results in a larger swing. The integral swing can be analyzed, especially whether it is bounded for various operating points. A continuously increasing maximum integral for a dc

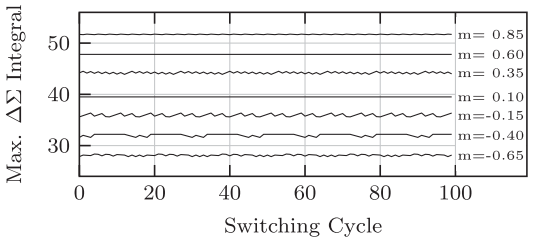

FIGURE 8. Simulated maximum integral during multiple switching cycles for varying dc modulation indices.

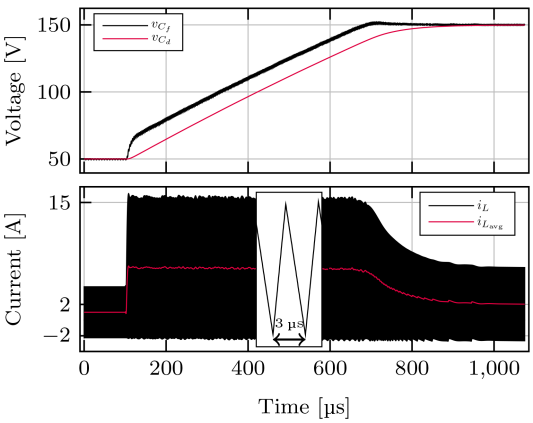

FIGURE 9. Simulated transient response where the modulation index is stepped from −0.5 to 0.5 resulting in a voltage step from 50 V to 150 V as seen in the top graph. The bottom graph depicts the inductor and average output current. The rectangular area shows a zoomed in portion of the inductor current.

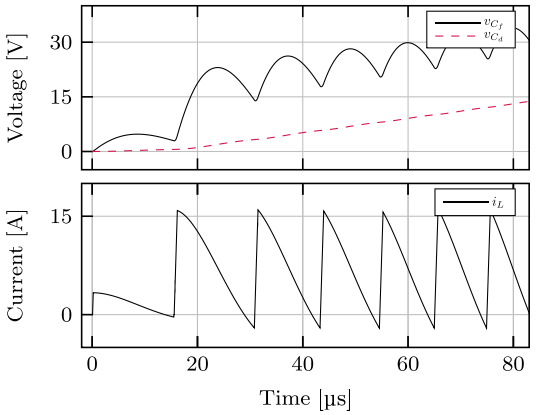

FIGURE 10. Simulated startup response with $\frac{di}{dt} = 0$ detection and peak current limiter.

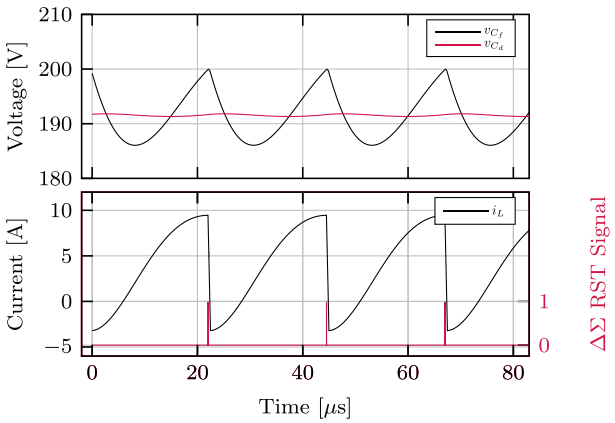

FIGURE 11. Simulated behavior when the output voltage is close to the dc-link supply voltage and the $\frac{di}{dt} = 0$ detection forces a switching action by asserting the RST signal.

operating point means that at some point, an overflow can occur. Therefore, simulations are carried out where the maximum integral value is logged in steady-state for 100 switching cycles with varying modulation indices. The maximum $\Delta\Sigma$ integral values are plotted in Fig. 8 for varying modulation indices. None of the setpoints show a continuously increasing integral. At certain modulation indices, the integral shows a cyclic behavior which is also visible when looking at the inductor current at those setpoints. The expectation is that noise in the inductor current measurement is sufficient to disturb the limit cycles seen in the simulation.

C. TRANSIENT AND START-UP BEHAVIOR

A peak current limiter and $\frac{\mathrm{di}}{\mathrm{dt}} = 0$ detection are added to the proposed $\Delta\Sigma$-modulator to improve transient and start-up behavior. Behavior of the peak current limiter is depicted in Fig. 9 where the output voltage is stepped from 50 V to 150 V. The top plot shows a nearly linear increase of the output voltage. In the bottom plot, the inductor current envelope is clearly visible. While charging the output capacitor with a constant current of approximately 6.5 A, the converter is switching between the predefined bounds of −2 A and 15 A. When the output voltage reaches the set output voltage of 150 V, the converter naturally decreases the average inductor current $i_{L_{\mathrm{avg}}}$ to the average load current flowing through the load resistance.

The $\frac{\mathrm{di}}{\mathrm{dt}} = 0$ detection feature is especially important when the output voltage is close to either of the power supply rails. For example during startup, when the output voltage equals 0 V, the RST circuitry acts resulting in the behavior as shown in Fig. 10. At time 0 μs, the converter turns on the high-side switch Q_1 resulting in a rapidly increasing in inductor current i_L. The output voltage v_{C_f} starts to rise and shortly after, the low-side switch Q_2 is enabled. Before again turning on the high-side switch Q_1, the integral must be positive and i_L should be smaller than $-i_{\mathrm{comm}}$. This last criteria cannot be reached due to the small output voltage and when $\frac{\mathrm{di_L}}{\mathrm{dt}}$ is smaller than di_{min}, the modulator forces a switching action at the time 17 μs. Afterwards, the high-side switch Q_1 is enabled and the peak current limiter limits the inductor current to just over 15 A while continuing to charge the output capacitors. After the first switching cycle, the output voltage is high enough such that i_L can reach the value set for $-i_{\mathrm{comm}}$.

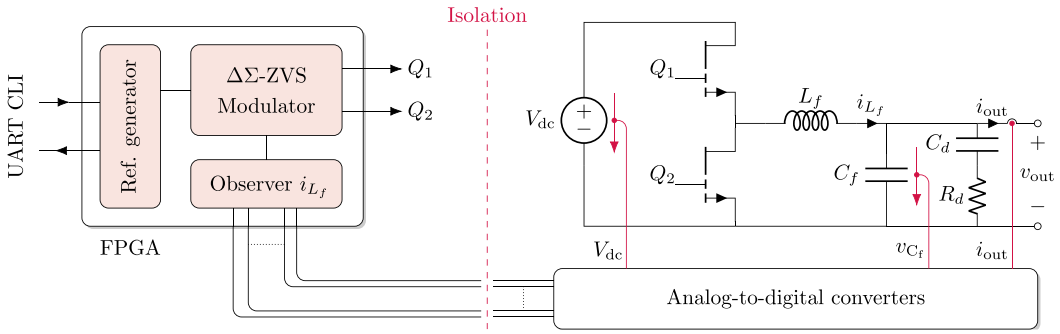

FIGURE 12. High-level overview of the protype setup including passively damped output filter. An isolation barrier between the FPGA and power converter is present for safety.

Moreover, the $\frac{di}{dt} = 0$ detection feature also acts when the output voltage is close to the dc-link supply voltage. This effect is shown in Fig. 11. The voltages in the upper plot are close to the supply voltage of 200 V. As a result, switching actions are forced by asserting the RST signal after the inductor current in the bottom plot finishes a half resonant cycle.

V. MEASUREMENTS

To validate the simulation results, an experimental setup is built. A high-level overview of the setup is given in Fig. 12. It consists of an FPGA running the reference generator, an observer for the inductor current and the proposed modulator. The switch control signals are send to the power converter through isolated gate drivers. Parameters such as the dc-link voltage V_{dc}, output voltage v_{C_f} and output current i_{out} are measured using analog-to-digital converters as they are used by the observer. Based on the observer output, the modulator determines whether switching is allowed as well as the peak current limiter and $\frac{di}{dt} = 0$ events. The power converter is controlled in open-loop to visualize the proposed modulator's behavior without seeing influences of a controller.

A. PROTOTYPE SETUP

A picture of the developed prototype is shown in Fig. 13. The prototype consists of three boards, the first one being the half-bridge with GaN semiconductors, gate drivers, decoupling capacitors and measurement points. This board generates the unfiltered switch-node voltage which goes to the output filter board. The output filter board contains the filter inductance and output capacitance. A large film capacitor and resistor are connected externally for passive damping. In practice, the passive damping circuitry can be omitted if a closed-loop controller is added that limits the control bandwidth. Removing the damping circuitry is prefered as the damping resistance adds loss which can be removed using an appropriate controller. The component values are identical as previously mentioned in Table 1. The half-bridge consists of GaN semiconductors from GaN Systems, type GS66508 T. The semiconductors are driven using the SI8271GB-IS isolated gate drivers from Skyworks. Additionally, several measurements are included on the output filter board and isolation

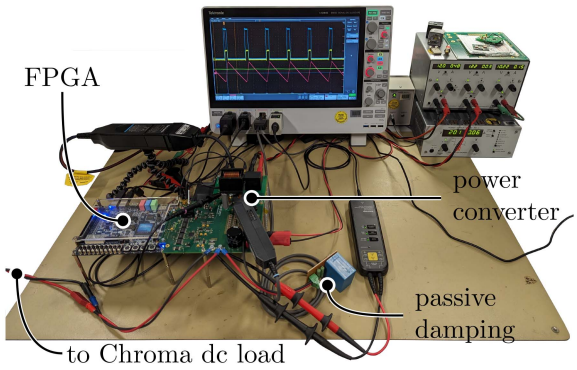

FIGURE 13. Setup for experimental validation of the proposed modulator.

between the HV and LV part is provided. The data is transferred to the FPGA development board which contains an Intel Cyclone V FPGA. A Delta SM400-AR-4 power supply provides the DC-link voltage and a Chroma Programmable DC load is connected to the output.

B. SWITCHING WAVEFORMS

The switching behavior of the half-bridge is measured to verify whether ZVS operation is achieved. A picture of a turn-off and turn-on switching event is shown in Fig. 14. The top plot shows the switched-node voltage. In the middle plot the gate-source voltage of both the low- and high-side switch are shown and in the bottom plot the inductor current is depicted. Soft switching can be observed because of the natural commutation of v_{sn} to the opposite rail once the switch is turned off. The speed of the commutation to the complementary power rail is dependent on the inductor current. In the right plot, the converter switches at the selected commutation current of -2 A and it can be seen that the blanking time of 75 ns is sufficiently long for the commutation to take place.

C. STARTUP BEHAVIOR

When starting the power converter with the proposed modulation strategy, the lumped output capacitance is charged while the modulator limits the maximum current supplied to

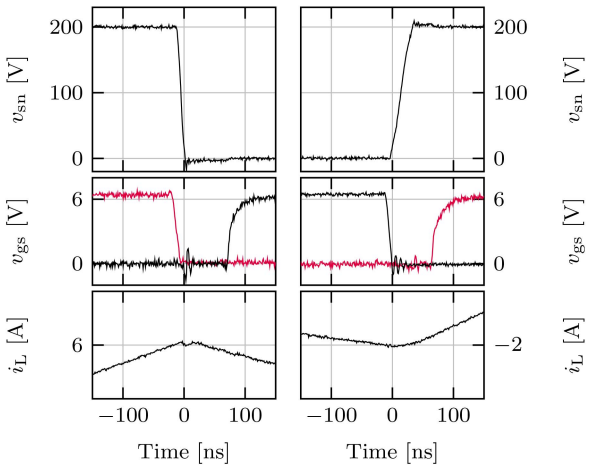

FIGURE 14. Switching behavior when turning-off (left) and turning-on (right) the high-side switch. Reverse conduction of the switches during the blanking time is just visible.

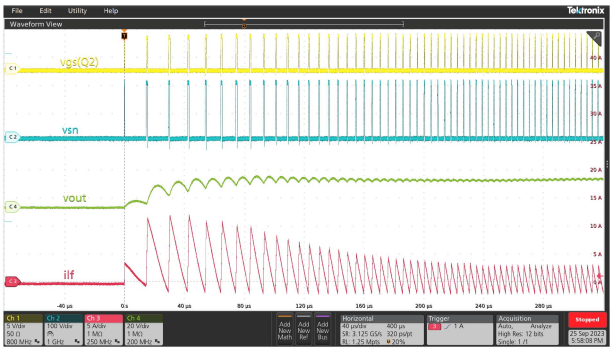

FIGURE 15. Measurement of the output voltage (green), inductor current (red), switch-node voltage (blue) and high-side gate-source voltage (yellow) during startup.

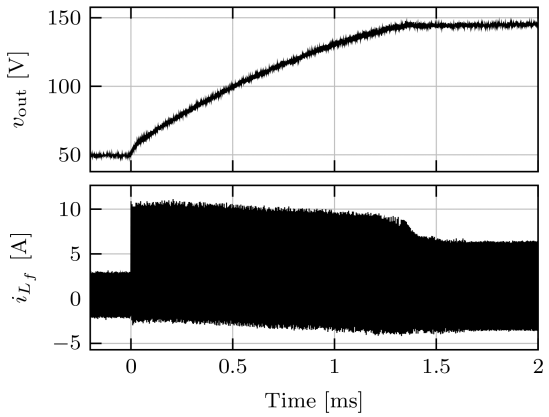

FIGURE 16. Step response when the modulation index is stepped from −0.5 to 0.5. The converter is continuously operating under ZVS conditions.

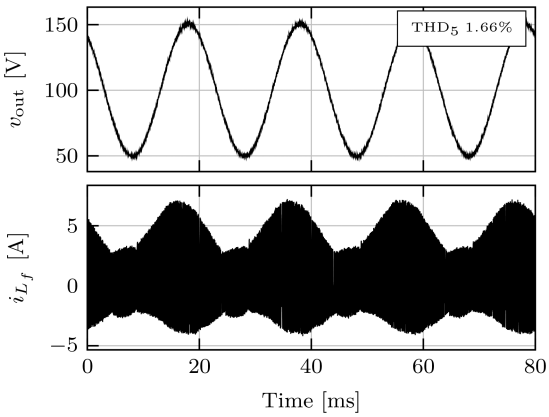

FIGURE 17. Generation of an 50 Hz sinusoidal voltage that is centered around 100 V and has an amplitude of 50 V.

the output. This behavior is captured in Fig. 15. Initially, the high-side switch is turned-on shortly and the inductor current rises quickly. During the first switching cycles, the inductor current does not reach the set commutation current threshold and therefore $\frac{di}{dt} = 0$ events are triggered ensuring that the converter continues switching. After some time, the output capacitance is charged and the voltage is proportional to the specified modulation index of −0.8. Initially, the capacitor voltage ripple is relatively large due to the low switching frequency when the peak current limiter is active. Afterwards, the frequency is higher due to the small inductor current ripple and thus the output voltage ripple also decreases.

D. STEP RESPONSE

To demonstrate the transient behavior, the outputs during a step are shown. In Fig. 16, the modulation index is stepped from −0.5 to 0.5 corresponding to a voltage step from 50 V to 150 V. The converter is continuously operating under ZVS conditions demonstrating the modulators transient capabilities. While charging the output capacitances, the peak current limiter is active. When the output voltage increases, a small undesired offset error is introduced in the observed inductor current. This can be seen by looking at the lower bound of the inductor current when the voltage is increasing. The converter is not switching at the set commutation current of −2 A but at a larger commutation current of −3.5 A. This offset can be reduced by improving the Luenberger observer that is running in the FPGA.

E. SINUSOIDAL REFERENCE

Moreover, a sinusoidal reference signal is sent to the modulator. The reference signal has a frequency of 50 Hz and is biased around a modulation index of 0. The amplitude is set to 0.7 and the resulting output voltage is depicted in Fig. 17. The frequency spectrum is analyzed and the total harmonic distortion, up to and including the fifth harmonic, (THD$_5$) equals 1.66%. From the bottom plot, showing the inductor current, it is clear that the current ripple is constantly varying and thus also the switching frequency varies. Ideally, the minimum value of the inductor current would constantly equal the set i_{comm} of −2 A however, as a result of imperfections in

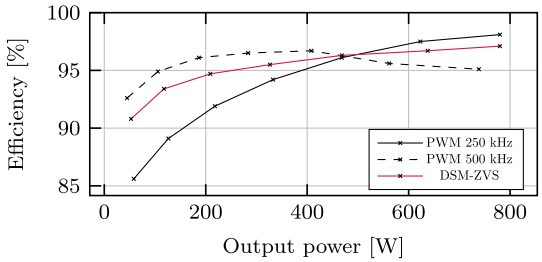

FIGURE 18. Measured efficiency for various modulation methods.

the Luenberger observer, the current ripple is slightly larger. Effectively, the switching frequency varies during the 50 Hz period and ranges from 200 kHz to 1.1 MHz.

F. A NOTE ON EFFICIENCY

In order to validate the effectiveness of the proposed DSM-ZVS modulator, efficiency measurements were conducted. The power supply used, a Delta SM400-AR-4, is limited to an output power of 800 W. Consequently, the efficiency tests are not extended to the prototype's maximum power. These measurements were executed using a N4L PPA500 power analyzer and a load resistance of 30 Ω is selected. Output power is increased by incrementing the duty cycle in steps of 10%. The efficiency of the DSM-ZVS modulator was assessed in comparison to that achieved using conventional PWM at switching frequencies of 250 kHz and 500 kHz.

The observed efficiencies, illustrated in Fig. 18, show several interesting phenomena. When using PWM with a switching frequency of 250 kHz, a significant inductor current ripple is present, leading to increased circulating currents and subsequently reduced efficiency at lower power levels. Increasing the f_{sw} to 500 kHz reduces the inductor current ripple, enhancing efficiency at lower power. However, at around 500 W output power, the reduced ripple was insufficient to maintain ZVS operation, resulting in an increase of switching loss and decreased efficiency. Similar behavior would occur for the lower f_{sw} at an output power around 900 W, clearly showing the problem with fixed frequency PWM.

Contrastingly, the ΔΣ-ZVS modulator consistently maintained ZVS operation by adjusting its switching frequency in response to changes in output current. This capability yielded an improved efficiency at lower power compared to 250 kHz PWM. Around an output power of 800 W, the DSM-ZVS modulator demonstrated higher efficiency than 500 kHz PWM, though it was marginally less efficient than 250 kHz PWM. This can be attributed to the previously observed voltage-dependent offset in the estimated inductor current. With an increase in output voltage, the modulator does not switch at the selected commutation current i_{comm} of −2 A. An improvement in the Luenberger observer will enhance this efficiency further. Additionally, dynamic scaling of i_{comm} based on v_{out} according to (3) would further reduce the circulating currents and improve efficiency.

It is essential to recognize that efficiency metrics are heavily influenced by the converter's design. Achieving state-of-the-art efficiencies, such as those exceeding 99%, requires a proper optimization, taking into account relevant load conditions specific to the intended application. For a fair and accurate comparison, it is crucial to optimize the converter while also considering the capabilities of the selected modulation strategy.

VI. CONCLUSION

In this work, a new advanced modulation strategy suitable for very high frequency operation is proposed. It converts a modulation index into an average voltage while continuously achieving ZVS operation. Compared to other methods, the proposed method is computationally less intensive, it naturally operates at a variable switching frequency and maintains soft switching during transient operation. The modulator is based on a first-order ΔΣ-modulator with a hold-off circuit and protection features are implemented to limit the peak inductor current and detect $\frac{di}{dt} = 0$ events. Both simulation and experimental results validate the working principle of the modulation strategy. Due to the continuously changing inductor current ripple, the conduction loss is reduced while eliminating turn-on losses of the semiconductors. The conduction loss can be further reduced by improving the inductor current measurement. The currently used observer has a voltage dependent offset error resulting in a varying commutation current i_{comm}. A switching frequency just above 100 kHz is seen during start-up, and a peak switching frequency of 1.1 MHz is reached while generating the sinusoidal output waveform. Those MHz-range switching frequencies are enabled by the inherent ZVS capabilities and are desired properties especially when going to ultra-high switching frequencies with modern wide-bandgap semiconductors. In future work, the power converter with proposed DSM-ZVS modulator is benchmarked against other control strategies in literature and an extension of the proposed modulation strategy to more complex converters needs to be explored such as multilevel topologies.

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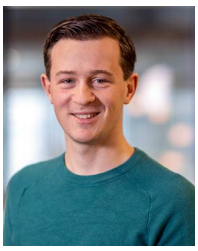

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