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A Bidirectional DC–DC Converter With Direct Power Transfer

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ABSTRACT This paper presents a novel bidirectional DC–DC converter for several applications such as energy storage systems. The proposed power circuit topology not only has inherent soft switching but also offers reduced conduction losses. The reduction in conduction losses is achieved through a direct power transfer (DPT) path, which can effectively bypass the transformer as well as power semiconductors at the primary side, and transfer power directly to the secondary side. In addition, The power circuit offers flexibility to shape the input current waveform to have lower peak values, resulting in further reduction in conduction losses. Thus, the proposed circuit can potentially provide high efficiency by reducing both the conduction losses and switching losses simultaneously. Theoretical analysis, simulation results, and experimental results demonstrate the feasibility of the proposed circuit and its superior performance.

INDEX TERMS Bidirectional converters, coupled inductors, DC–DC converters, direct power transfer (DPT), dual active bridge (DAB), soft switching, zero voltage switching (ZVS).

I. INTRODUCTION

Bidirectional DC–DC converters have become an integral part of several emerging applications such as energy storage systems. In particular, power conversions needed for the charge-discharge of batteries in many applications require bidirectional power flow [1], [2]. Electric vehicles and energy storage systems are among the main applications where bidirectional DC–DC converters are required [3], [4], [5].

Bidirectional DC–DC converters are typically categorized as either isolated or non-isolated. Within the non-isolated category, two prominent options for higher power ranges are the two-stage interleaved buck/boost converters and multilevel buck/boost converters [6], [7]. In [6], an advanced interleaved bidirectional buck/boost converter is presented, which can provide high voltage gains and minimal current ripples through a new power circuit and modulation techniques. Similarly, in [7], a high-power non-isolated multilevel DC-DC converter is introduced that offers reduced switching losses in a five-level bidirectional structure. However, non-isolated configurations lack stringent safety requirements, essential for many applications such as electric vehicles and grid-connected energy storage systems.

Many types of isolated bidirectional DC–DC converters have been proposed for battery charging applications in the literature [8], [9]. A bidirectional flyback converter has been proposed in [10], [11], which can provide zero current switching (ZCS) for power semiconductors. However, the proposed converter may not be a good candidate for high power applications (i.e., kW range) due to the inherent limitations of the flyback topology.

A new bidirectional three-phase push-pull converter has been proposed in [12], [13], which can be used for higher power applications. This power circuit topology can provide ZVS and achieve a balanced three-phase current at the low-voltage side. However, the topology suffers from the excessive circulating current within some operating conditions.

The dual active bridge (DAB) converter is the industry standard for bidirectional DC–DC converters. This topology is capable of transferring high amounts of power and efficiently utilizing the high-frequency transformer [14], [15], [16]. Comprehensive analyses of the operation, design, and control of DAB converters are presented in [17]. Moreover, DAB converters can easily provide soft switching to reduce the switching losses [18], [19]. However, this topology has some disadvantages among which is handling a wide range of input/output voltages. Since battery voltage ranges are usually very wide, the current slopes in DAB converters can result

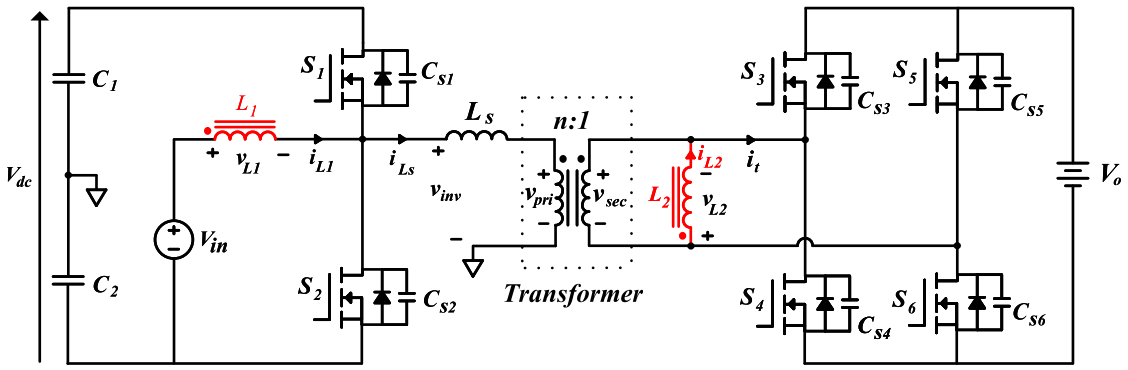


FIGURE 1. Bidirectional DC–DC converter with direct power transfer (DPT) capability.

in excessive conduction losses specifically [20], [21], [22]. Moreover, maintaining soft switching for light load conditions is difficult for DAB converters [23], [24], [25], [26]. In [27], a new bidirectional Current-Fed half-bridge converter (CF-DAB) is presented, which can potentially address the challenges of DAB converters. This topology is suitable for applications where the input current ripple should be minimized due to the presence of an inductor. However, this topology still suffers from high conduction losses in applications where the current waveforms become triangular and can have very high peaks.

In order to extend the soft switching range of DAB, resonant-type converters have been proposed in the literature [28], [29]. Series resonant converters [30], [31], [32], and series-parallel resonant converters have been the main focus and well-studied in the literature (e.g., CLLC, CLC, CLTC resonant circuits) [33], [34], [35], [36], [37], [38]. These circuit topologies can offer several advantages such as soft switching, wide voltage gains, and minimized circulating currents. However, the high number of resonant components used in these circuits and many resonant components process the full amount of power, which results in excessive conduction losses in applications where the range of voltage variations is wide.

In order to address the issues with resonant-type converters, non-resonant converters have been proposed with bidirectional power flow capability. Isolated full-bridge bidirectional DC–DC converter (IFBDC) is a non-resonant power circuit topology proposed for higher power applications [39], [40], [41]. This topology requires a simple control and utilizes a DC inductor as compared to a high-frequency AC inductor in DAB or resonant converters [42], [43]. This allows for lower core losses and lower proximity/fringing losses in the winding [39], [40], [44]. However, this circuit suffers from high conduction losses for applications with a wide range of voltage variations. Moreover, the other drawbacks of this circuit are the duty-cycle loss, free-wheeling intervals, and hard switching at light loads.

In summary, most of the research work on bidirectional DC–DC converters is focused on soft switching to improve the switching losses. However, the improvements in conduction losses have received little interest. In [45], a new unidirectional DC–DC topology is introduced which can potentially offer lower conduction losses and higher efficiency. However, this converter can only offer uni-directional power flow and the existence of a diode at the input side may offset any reduction in conduction losses. The control variable used in [45] is the switching frequency. Thus, the range of switching frequencies is very wide for applications with a wide range of voltage variations, leading to sub-optimal magnetic design and in turn compromised performance.

In this paper, we propose a new bidirectional power circuit topology, which can offer a wide soft-switching range and provide Direct Power Transfer (DPT) capability to reduce conduction losses. In addition, the proposed circuit can shape the input current to reduce its peak values, further decreasing conduction losses. In terms of control variables, the converter can utilize many control variables such as the phase shifts to optimally control the power flow.

This paper is structured as follows. Section II presents the proposed topology and its modes of operation. The steady-state analysis is provided in Section III, followed by the design considerations in Section IV. Simulation results are presented in Section V, while Section VI presents the experimental results. Finally, Section VII concludes the paper.

II. PROPOSED BIDIRECTIONAL DC–DC CONVERTER WITH DPT

In this section, the proposed bidirectional DC–DC converter is introduced. Fig. 1 shows the schematic of the proposed topology. According to this figure, the proposed circuit provides two paths for power transfer. A portion of the power is transferred to the output through the coupled inductor and the rest through the primary side power semiconductors and the high-frequency transformer. Thus, the coupled inductor provides a path for direct power transfer (DPT) to the secondary side of the transformer. The DPT results in a reduction in the amount of current flowing through the primary side power switches and magnetics, and reduces the conduction losses. Moreover, this circuit allows for shaping the input current to reduce its peak values. This further decreases the conduction losses. In

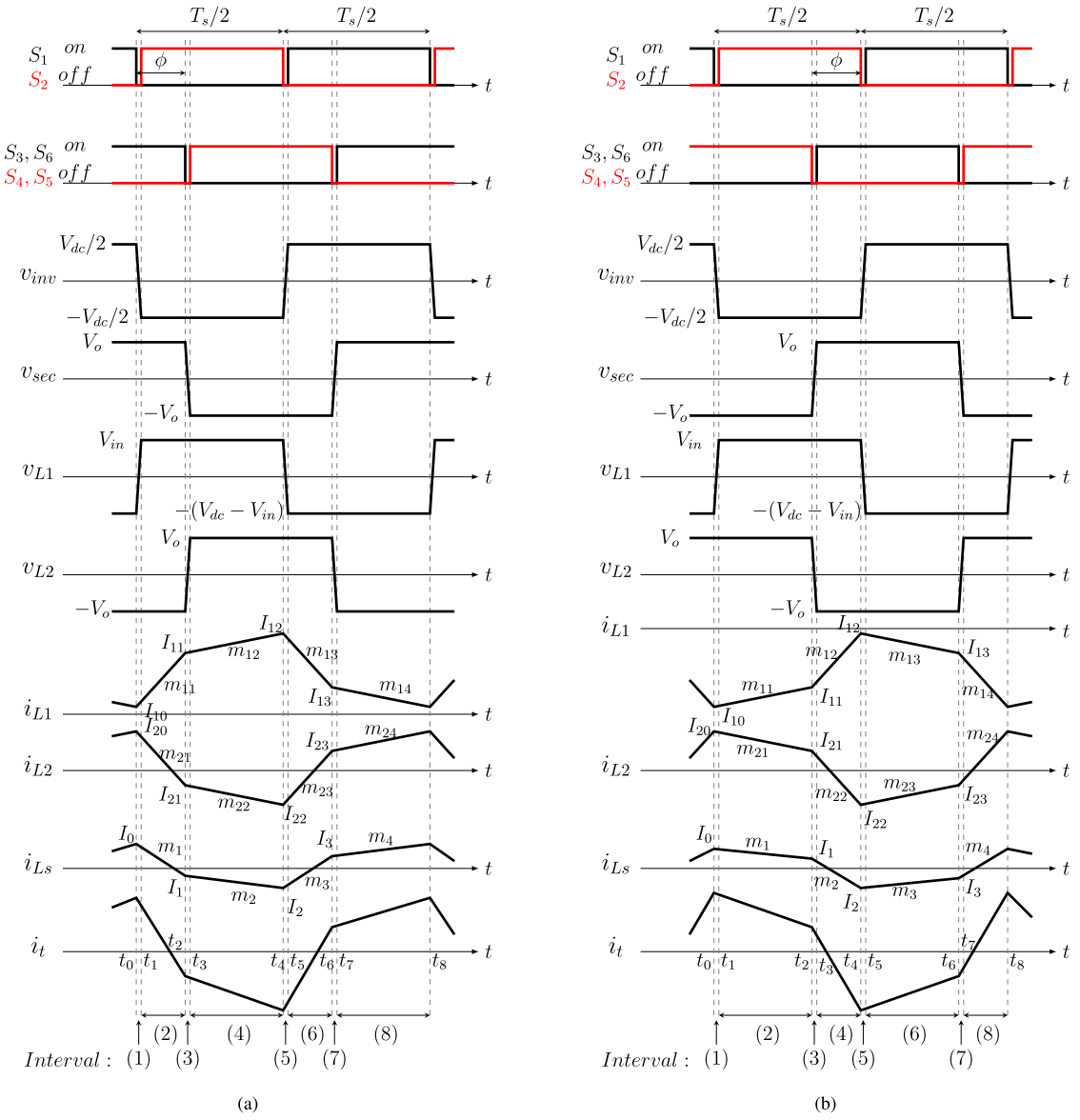


FIGURE 2. Key waveforms of the proposed converter for the bidirectional power flow: (a) HV2LV, (b) LV2HV.

summary, the proposed circuit can effectively reduce the overall conduction losses of the converter, in addition to utilizing the inherent soft-switching in a wide range of operations.

The proposed converter provides bidirectional power flow: the high voltage to low voltage (HV2LV) power flow and the low voltage to high voltage (LV2HV) power flow. Fig. 2(a) and (b) respectively show the key waveforms for the HV2LV and LV2HV. According to this figure, the current waveforms of the coupled inductor and the series inductor are piecewise linear with different slopes during each interval. For the coupled inductor, the current slopes are given by:

$$\frac{di_{L_1}}{dt} = \frac{L_2}{L_t^2}v_{L_1} - \frac{M}{L_t^2}v_{L_2}$$
$$\frac{di_{L_2}}{dt} = -\frac{M}{L_t^2}v_{L_1} + \frac{L_1}{L_t^2}v_{L_2} \quad (1)$$

where $L_t = \sqrt{L_1L_2 - M^2}$.

In the following subsection, different modes of operation will be described for the HV2LV power flow.

A. HV2LV POWER FLOW

Fig. 3 shows the equivalent circuits for each interval of HV2LV. It is assumed that the power switches S_1, S_3 and S_6 are ON before the interval 1.

Interval 1 [t_0, t_1]: At the beginning of this interval, S_1 turns OFF at t_0. The voltage across the capacitor C_{S1}, and across S_1 is zero. Thus, the switch turns OFF under zero voltage (ZVS). In this interval, i_{Ls} is positive and charges C_{S1} and discharges C_{S2} such that the voltage across S_1 increases to the bus voltage, while the voltage across S_2 decreases to zero.

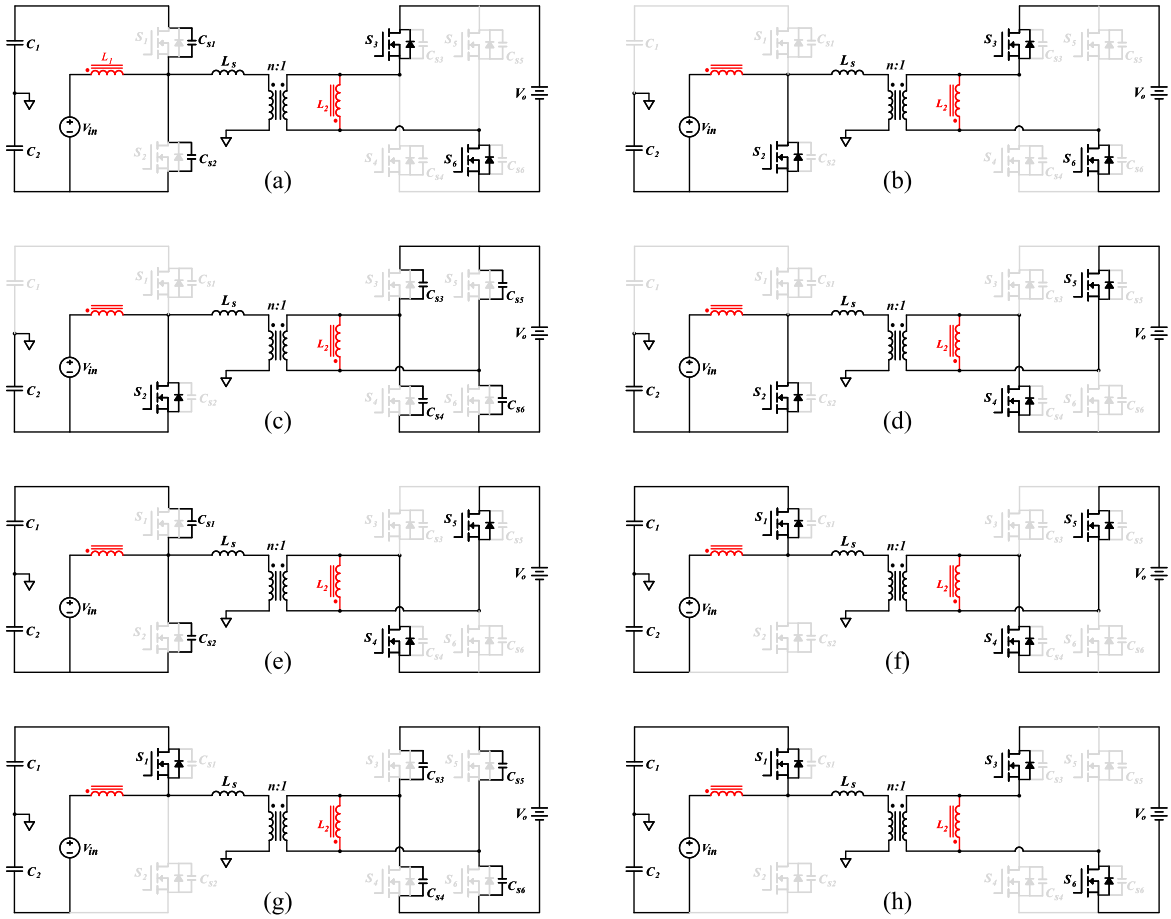


FIGURE 3. Equivalent circuits of each interval for the HV2LV mode of operation in the proposed converter: (a) interval 1, (b) interval 2, (c) interval 3, (d) interval 4, (e) interval 5, (f) interval 6, (g) interval 7, and (h) interval 8.

Interval 2 [t_1, t_2]: At t_1, the anti-parallel diode of switch S_2 is conducting while the switch S_2 turns ON; hence, the switching occurs under ZVS condition. In this interval, $v_{inv} = -V_{dc}/2$ and $v_{L1} = V_{in}$. Since S_3 and S_6 are ON, the voltage across the secondary side of the transformer is $v_{sec} = V_o$, and consequently, the voltage across the series inductor can be calculated as $v_{L_s} = v_{inv} - nv_{sec}$. In this interval, the voltage across the L_2 is $v_{L2} = -V_o$, and the slope of i_{L1} and i_{L2} can be calculated from (1). Moreover, the current i_t is the sum of $n \times i_{Ls}$ and i_{L2}, which both decrease in this interval; hence, i_t decreases as well.

Interval 3 [t_2, t_3]: This interval starts with a change in the status of the secondary side switches, and the pair S_3 and S_6 turn OFF. At t_2, the voltage across C_{S3} and C_{S6} are zero, and the switches S_3 and S_6 turn OFF under ZVS condition. In this interval, i_t is negative and charges the capacitors C_{S3} and C_{S6}, and discharges the capacitors C_{S4} and C_{S5} such that the voltage across S_3 and S_6 increases to the output voltage, while the voltage across S_4 and S_5 decreases to zero.

Interval 4 [t_3, t_4]: At t_3, the voltage across the switches S_4 and S_5 are zero because their anti-parallel diodes are conducting; hence both of the switches turn ON under ZVS condition. In this interval, $v_{sec} = -V_o$ and $v_{L2} = V_o$, and in the primary side of the transformer, $v_{inv} = -V_{dc}/2$ and $v_{L1} = V_{in}$. Consequently, the slopes of currents i_{L1} and i_{L2} can be calculated from (1).

Interval 5 [t_4, t_5]: At t_4, switch S_2 turns OFF while the voltage across the snubber capacitor C_{S2} is zero, so the switch turns OFF under ZVS condition. In this interval, both of the switches S_1 and S_2 are OFF, and the negative i_{Ls} charges C_{S2} to the bus voltage, and discharges C_{S1} to zero.

Interval 6 [t_5, t_6]: At the beginning of this interval, switch S_1 turns ON while its anti-parallel diode is conducting. Thus, the switching happens under the ZVS condition. In this interval, $v_{inv} = V_{dc}/2$ and $v_{L1} = -(V_{dc} - V_{in})$, and consequently, the current slopes of the series and coupled inductors can be calculated from (1). Since i_{L2} and i_{Ls} both increase in this interval, i_t increases as well.

Interval 7 [t_6, t_7]: At t_6, switches S_4 and S_5 turn OFF while the voltage across the snubber capacitors C_{S4} and C_{S5} are zero. Thus, the switching happens under ZVS condition. Since all of the switches are OFF during this interval, the positive i_t charges C_{S4} and C_{S5}, and discharges C_{S3} and C_{S6}. This will continue until the voltage across S_3 and S_6 gets to zero.

Interval 8 [t_7, t_8]: At the beginning of this mode, the anti-parallel diodes of the switches S_3 and S_6 are conducting,

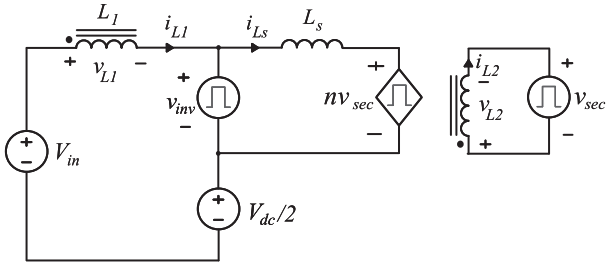


FIGURE 4. Circuit diagram in steady-state.

while the switches S_3 and S_6 turn ON. Thus, the switching happens under ZVS condition. During this interval, $v_{sec} = V_o$ and $v_{L2} = -V_o$, and the voltages v_{inv} and v_{L1} do not change. Using (1), the current slopes for the coupled inductors and series inductor can be calculated. Both of the currents i_{Ls} and i_{L2} are ascending, so the current i_t is also ascending. Modes of operation for the LV2HV power direction are discussed in Appendix A.

III. STEADY-STATE ANALYSIS

In this section, the mathematical analysis is performed for the proposed converter during the steady-state operation.

A. HV2LV POWER FLOW

Fig. 4 shows the simplified circuit of the proposed converter in the steady state. In this figure, the half-bridge inverter in the primary side of the transformer is modeled with a square-wave voltage source with an alternating value between $V_{dc}/2$ and $-V_{dc}/2$ (50% duty cycle is assumed). Also, the voltage of the rectifier in the secondary side of the transformer (v_{sec}) is modeled as a square-wave voltage source with alternating values between V_o and $-V_o$ (50% duty cycle). The primary side of the transformer is modeled as a voltage-controlled voltage source since it is dependent on v_{sec}.

The DPT is characterized by calculating the power transferred through the primary side power switches and the high-frequency transformer, P_{tr}, and the power transferred through the coupled inductor, P_{DPT}. P_{tr} is calculated based on i_{Ls} and P_{DPT} is calculated based on i_{L2}.

According to Fig. 2(a), and by neglecting intervals 1, 3, 5, and 7, i_{Ls} can be calculated as follows ($t_0 = 0$).

$$i_{Ls,1}(t) = -\frac{V_{dc} + 2nV_o}{2L_s}t + I_0 \qquad t \in [0,\ t_\phi] \tag{2}$$

$$i_{Ls,2}(t) = -\frac{V_{dc} - 2nV_o}{2L_s}(t - t_\phi) + I_1 \qquad t \in \left[t_\phi,\ \frac{T_s}{2}\right] \tag{3}$$

$$i_{Ls,3}(t) = \frac{V_{dc} + 2nV_o}{2L_s}\left(t - \frac{T_s}{2}\right) + I_2 \quad t \in \left[\frac{T_s}{2},\ \frac{T_s}{2} + t_\phi\right] \tag{4}$$

$$i_{Ls,4}(t) = \frac{V_{dc} - 2nV_o}{2L_s}\left(t - \frac{T_s}{2} - t_\phi\right) + I_3 \ t \in \left[\frac{T_s}{2} + t_\phi,\ T_s\right] \tag{5}$$

The constant values I_1, I_2, and I_3 can be specified based on the I_0 by evaluating (2), (3), and (4) at t_ϕ, $T_s/2$, and $T_s/2 + t_\phi$, respectively. In order to calculate P_{tr}, the integral of instantaneous power $v_{inv}.i_{Ls}$ should be taken over one switching cycle. Using (2)–(5), the averaged transformer power P_{tr} is given by:

$$P_{tr} = \frac{V_{dc}nV_o}{2L_s f_s}\phi\,(1 - 2\phi) \tag{6}$$

where $\phi = t_\phi/T_s$. Equation (6) is proportional to ϕ. The maximum amount of P_{tr} would be achieved when $\phi = 0.25$. Also, it can be seen that P_{tr} is inversely proportional to the switching frequency, and by increasing the switching frequency, the P_{tr} would be reduced.

In the next step, we are going to calculate the direct power transfer portion of the whole power P_{DPT}, and to do that, i_{L2} should be calculated first. According to Fig. 2(a), i_{L2} can be formulated as follows:

$$i_{L2,1}(t) = -\frac{MV_{in} + L_1V_o}{L_t^2}t + I_{20} \qquad t \in [0,\ t_\phi] \tag{7}$$

$$i_{L2,2}(t) = \frac{-MV_{in} + L_1V_o}{L_t^2}(t - t_\phi) + I_{21} \quad t \in \left[t_\phi,\ \frac{T_s}{2}\right] \tag{8}$$

$$i_{L2,3}(t) = \frac{M(V_{dc} - V_{in}) + L_1V_o}{L_t^2}\left(t - \frac{T_s}{2}\right) + I_{22} \qquad t \in \left[\frac{T_s}{2},\ \frac{T_s}{2} + t_\phi\right] \tag{9}$$

$$i_{L2,4}(t) = \frac{M(V_{dc} - V_{in}) - L_1V_o}{L_t^2}\left(t - \frac{T_s}{2} - t_\phi\right) + I_{23} \qquad t \in \left[\frac{T_s}{2} + t_\phi,\ T_s\right] \tag{10}$$

The constant values I_{21}, I_{22}, and I_{23} can be calculated based on I_{20} by solving (7)–(9) at the end of their intervals. The instantaneous P_{DPT} passing through the coupled inductors is equal to $P_{DPT}(t) = -v_{L2}.i_{L2}$, and its average value can be achieved by taking an integral over one switching cycle using (7)–(10).

$$P_{DPT} = \frac{MV_o}{L_t^2 f_s}\left[V_{in}\,(\phi - 0.25) + V_{dc}\left(\frac{1}{8} - \phi^2\right)\right] \tag{11}$$

Equation (11) shows that P_{DPT} is inversely proportional to the switching frequency, and by increasing the switching frequency, the amount of power directly transferred to the output will be reduced. Assuming the loss is negligible, the total amount of power transferred to the output is equal to $P_o = P_{tr} + P_{DPT}$.

In the next step, the averaged input current I_{in} is needed. Based on Fig. 2(a), i_{L1} can be formulated as:

$$i_{L1,1}(t) = \frac{L_2V_{in} + MV_o}{L_t^2}t + I_{10} \qquad t \in [0,\ t_\phi] \tag{12}$$

$$i_{L1,2}(t) = \frac{L_2V_{in} - MV_o}{L_t^2}(t - t_\phi) + I_{11} \quad t \in \left[t_\phi,\ \frac{T_s}{2}\right] \tag{13}$$

$$i_{L1,3}(t) = -\frac{L_2(V_{dc}-V_{in})+MV_o}{L_t^2}\left(t-\frac{T_s}{2}\right)+I_{12} \quad t\in\left[\frac{T_s}{2},\ \frac{T_s}{2}+t_\phi\right] \tag{14}$$

$$i_{L1,4}(t) = \frac{-L_2(V_{dc}-V_{in})+MV_o}{L_t^2}\left(t-\frac{T_s}{2}-t_\phi\right)+I_{13} \quad t\in\left[\frac{T_s}{2}+t_\phi,\ T_s\right] \tag{15}$$

The constant values I_{11}, I_{12}, and I_{13} can be calculated based on I_{10} by evaluating (12)–(14) at the end of their intervals. Finally, the averaged input current is as follows:

$$I_{in} = \frac{MV_o}{L_t^2 f_s}(\phi-0.25) - \frac{V_{dc}-4V_{in}}{8L_t^2 f_s}L_2 \tag{16}$$

The average input current is inversely proportional to the switching frequency, so the average input current decreases by increasing the switching frequency. The steady-state analysis for LV2HV mode is discussed in Appendix B.

IV. DESIGN CONSIDERATION

In this section, the design procedure for the proposed converter is described in both HV2LV and LV2HV power flow directions. The design method is based on the equations presented in the previous section. Our desire is to achieve the maximum P_{DPT} for a given power rating, and have lower peak and higher RMS values for a constant average input current.

For coupled inductors, the mutual inductance is $M = k\sqrt{L_1L_2}$, where k is the coupling coefficient. The amplitude of k directly affects the amplitude of L_1, L_2, and M. While k goes toward unity, the amplitude of coupled inductance increases. The range $0.9 < k < 0.95$ is quite suitable for the coupling coefficient, where the coupled inductances are small, and at the same time, the implementation of coupled inductors is not complicated; hence, we choose $k = 0.95$ for the design.

According to Fig. 2(a), the input current waveform can have lower peaks and higher RMS values if it is more like a square wave rather than a triangular wave. This would be achieved by decreasing m_{12} as positive and close to zero as possible.

$$m_{12} = \frac{L_2V_{in}-MV_o}{L_t^2} > 0 \Rightarrow x < \frac{V_{in}}{V_o} \tag{17}$$

where $x = M/L_2$. For the input/output characteristics mentioned in Table 1, the proper value for x would be lower than 8.3, and the more the amplitude of x, the lower the input current peaks. Thus, x can be considered as $x = 7$.

Since the duty cycle in the primary side of the transformer is 50%, the gain of the primary half bridge is 2 and we have $V_{dc} = 2V_{in}$. However, by changing the duty cycle of the switches, different values for V_{dc} can be achieved which directly affects the power (6) and (11).

In order to find the maximum amount of transmitted power through the DPT path for a given output power, a new parameter called normalized direct power transfer, $P_{DPT,n}$, can be derived as:

$$P_{DPT,n} = \frac{P_{DPT}}{P_o}$$

TABLE 1. Simulation Parameters for the Proposed Converter

Parameter	Value
Output Power P_o	$1.5\ kW$
Output Voltage V_o	$45-60\ V$
Input Voltage V_{in}	$350-450\ V$
Switching Frequency f_s	$200\ kHz$
Coupled Inductors L_1	$770\ \mu H$
Coupled Inductors L_2	$14.2\ \mu H$
Coupled Inductors M	$99.3\ \mu H$
Series Inductor L_s	$102\ \mu H$
Transformer Turns Ratio n	8
DC bus Capacitors C_1, C_2	$10\ \mu F$

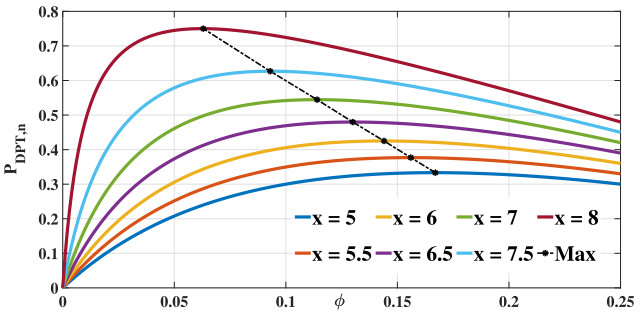


FIGURE 5. The normalized direct power transfer curve with respect to ϕ for different values of x parameter.

$$= \frac{xV_o}{V_{in}}\frac{V_{in}(\phi-0.25)+V_{dc}\left(\frac{1}{8}-n_\phi^2\right)}{xV_o(\phi-0.25)+\frac{1}{2}V_{in}-\frac{1}{8}V_{dc}} \tag{18}$$

Fig. 5 shows the $P_{DPT,n}$ curve respect to ϕ for different values of parameter $x = M/L_2$. The maximum amount of $P_{DPT,n}$ can be achieved by adjusting the ϕ based on the parameter x. The maximum possible amount of $P_{DPT,n}$ is 0.545 at $\phi = 0.12$ for the $x = 7$. It means that 54.5% of the whole power can be transferred to the output through the DPT path. Thus, the designed value for ϕ is selected as 0.12.

In the next step, inductor L_2 can be formulated by doing some manipulations on (16) as:

$$L_2 = \frac{k^2}{I_{in}f_sx^2\left(1-k^2\right)} \times\left(xV_o(\phi-0.25)+\frac{1}{2}V_{in}-\frac{1}{8}V_{dc}\right) \tag{19}$$

where $I_{in} \approx P_{out}/V_{in}$. By substituting all the known parameters into the (19), the designed value for the inductor L_2 is $L_2 = 14.2\,\mu$H. Using the definition of x, the mutual inductance will be calculated as $M = 99.3\,\mu$H. Again, by doing some manipulations on (16), we have:

$$\frac{L_2}{L_t^2} = \frac{I_{in}f_s}{xV_o(\phi-0.25)+\frac{1}{2}V_{in}-\frac{1}{8}V_{dc}} \tag{20}$$

Using (20), the inductor L_1 is designed as $L_1 = 770\,\mu$H.

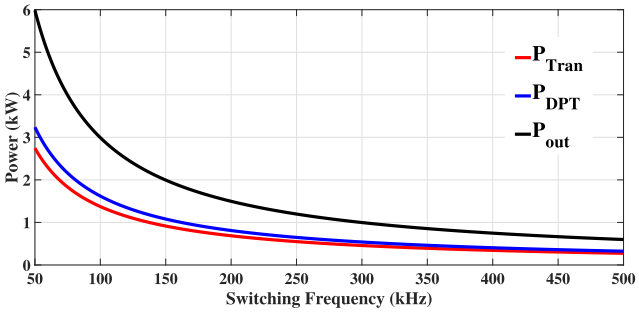


FIGURE 6. Variation of power with respect to changes in the switching frequency.

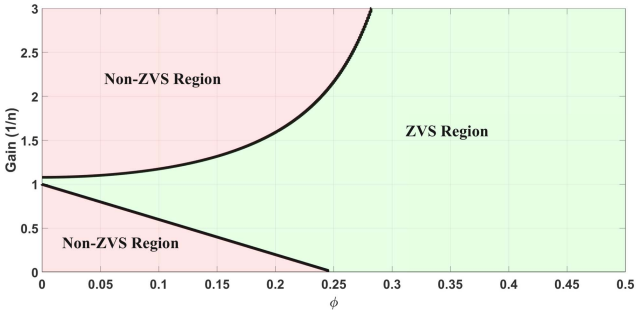


FIGURE 7. ZVS region of the proposed converter.

The RMS value of the series inductor current, i_{Ls}, can be increased by decreasing the voltage difference on the two sides of the series inductor. This would result in $n = 8$.

Finlay, the ratio L_s/n can be calculated using (6) as:

$$\frac{L_s}{n} = \frac{V_{dc}V_o}{2f_sP_o\left(1 - P_{DPT,n}\right)}\phi(1-2\phi) \tag{21}$$

Using the designed value of n, L_s can be calculated as $L_s = 102\,\mu$H. Design considerations for the LV2HV mode are discussed in Appendix C.

Equations (6) and (11) show that power is inversely proportional to the switching frequency in both P_{tr} and P_{DPT}. Using the designed parameters in Table 1 and evaluating the P_{tr} and P_{DPT} in a range of frequencies, the distribution of power for the switching frequency can be illustrated in Fig. 6. As Fig. 6 shows, the output power can be higher in lower frequencies. Thus, the switching frequency can be designed properly to have maximum efficiency.

A. ZVS REGION

The proposed converter has an inherent soft-switching advantage. To identify the ZVS region of the proposed converter under variations in the converter gain, it is essential to ensure that the inductive energy stored in the inductors exceeds the capacitive energy stored in the C_{oss} of the switches at the time of switching. Due to the non-symmetric current waveforms within the primary half-bridge, there is an elevated risk of ZVS loss for the lower switch S_2. To verify the ZVS condition, the current flowing through S_1 and S_2 should charge C_{S1} and discharge C_{S2} at time t_0, i.e., $I_0 - I_{10} > 0$. The expression for I_0 is given by:

$$I_0 = \frac{V_{dc} - 2nV_o}{4L_s} \cdot \frac{T_s}{2} + \frac{nV_o}{L_s} \cdot t_\phi \tag{22}$$

Similarly, for the coupled inductor current I_{10}, the expression is:

$$I_{10} = \frac{P_{tr} + P_{DPT}}{V_{in}} - I_{in} \tag{23}$$

Here, P_{tr}, P_{DPT}, and I_{in} are defined in (6), (11), and (16), respectively. Fig. 7 illustrates the ZVS range under different operating conditions. For the unity gain in the converter, ZVS is guaranteed. However, for the gains exceeding unity, the ZVS range becomes smaller at lower phase shifts. This implies that under light-load conditions, ZVS for switch S_2 might be compromised. Additionally, for gains below unity, ZVS for the LV side switches will be lost with small phase shifts.

V. AC MODEL OF THE PROPOSED CONVERTER

To investigate the dynamic behavior of the proposed converter, it is essential to establish the AC model of the system. One approach involves using the average model and determining the small signal model by introducing a perturbation in the control variable. However, as indicated by the analysis in [46], this method may lack accuracy. Alternatively, another method is to derive the discrete-time model of the system through a set of state space equations and determine the transfer function as presented in [47] for the DAB converter. In this section, the same approach is employed to find the transfer function of the proposed converter.

A. DYNAMICAL EQUATIONS OF THE PROPOSED CONVERTER

Fig. 2 illustrates the voltage and current waveforms of the proposed converter. By excluding the converter's behavior during the deadtime intervals (1), (3), (5), and (7), the system's operation becomes piecewise linear. Consequently, the dynamical equations of the inductors and capacitors can be calculated. For the series inductor, the rate of change of the current is proportional to the voltage across the inductor and is given by:

$$\frac{di_{L_s}}{dt} = \begin{cases} \frac{1}{L_s}(-v_{C_2} - n.v_{C_o}) & t \in T_{n1} \\ \frac{1}{L_s}\left(-v_{C_2} + n.v_{C_o}\right) & t \in T_{n2} \\ \frac{1}{L_s}\left(v_{C_1} + n.v_{C_o}\right) & t \in T_{n3} \\ \frac{1}{L_s}\left(v_{C_1} - n.v_{C_o}\right) & t \in T_{n4} \end{cases} \tag{24}$$

where:

$$\begin{cases} T_{n1} = \forall\, t \in [0,\ \phi T_s] \\ T_{n2} = \forall\, t \in [\phi T_s,\ 0.5T_s] \\ T_{n3} = \forall\, t \in [0.5T_s,\ (0.5+\phi)T_s] \\ T_{n4} = \forall\, t \in [(0.5+\phi)T_s,\ T_s] \end{cases}$$

For the coupled inductor L_1, the rate of change of current can be calculated from (1) and is given by:

$$\frac{di_{L_1}}{dt} = \begin{cases} \frac{L_2}{L_t^2}V_{in} + \frac{M}{L_t^2}v_{C_o} & t \in T_{n1} \\ \frac{L_2}{L_t^2}V_{in} - \frac{M}{L_t^2}v_{C_o} & t \in T_{n2} \\ \frac{L_2}{L_t^2}\left(V_{in} - v_{C_1} - v_{C_2}\right) - \frac{M}{L_t^2}v_{C_o} & t \in T_{n3} \\ \frac{L_2}{L_t^2}\left(V_{in} - v_{C_1} - v_{C_2}\right) + \frac{M}{L_t^2}v_{C_o} & t \in T_{n4} \end{cases} \tag{25}$$

The rate of change of current for the coupled inductor L_2 is given by:

$$\frac{di_{L_2}}{dt} = \begin{cases} -\frac{M}{L_t^2}V_{in} - \frac{L_1}{L_t^2}v_{C_o} & t \in T_{n1} \\ -\frac{M}{L_t^2}V_{in} + \frac{L_1}{L_t^2}v_{C_o} & t \in T_{n2} \\ -\frac{M}{L_t^2}(V_{in} - v_{C_1} - v_{C_2}) + \frac{L_1}{L_t^2}v_{C_o} & t \in T_{n3} \\ -\frac{M}{L_t^2}(V_{in} - v_{C_1} - v_{C_2}) - \frac{L_1}{L_t^2}v_{C_o} & t \in T_{n4} \end{cases} \tag{26}$$

The rate of change of capacitor voltages in the HV side half-bridge are as follows:

$$\frac{dv_{C_1}}{dt} = \begin{cases} 0 & t \in [T_{n1}, T_{n2}] \\ \frac{1}{C_1}(i_{L_1} - i_{L_s}) & t \in [T_{n3}, T_{n4}] \end{cases} \tag{27}$$

$$\frac{dv_{C_2}}{dt} = \begin{cases} \frac{1}{C_2}i_{L_s} & t \in [T_{n1}, T_{n2}] \\ \frac{1}{C_2}i_{L_1} & t \in [T_{n3}, T_{n4}] \end{cases} \tag{28}$$

Finally, we assume the presence of capacitors on both the input and output sides of the converter. Specifically, we consider the input capacitor to be large, so the dynamic behavior of the input capacitor is much slower than that of the output capacitor. In this context, we can treat the input voltage as the input of the system, and the output voltage as one of the state variables. Thus, the rate of change of voltage for the output capacitor is given by:

$$\frac{dv_{C_o}}{dt} = \begin{cases} \frac{1}{C_o}\left(i_{L_2} + n.i_{L_s} - \frac{1}{R_L}v_{C_o}\right) & t \in T_{n1} \\ \frac{1}{C_o}\left(-i_{L_2} - n.i_{L_s} - \frac{1}{R_L}v_{C_o}\right) & t \in T_{n2} \\ \frac{1}{C_o}\left(-i_{L_2} - n.i_{L_s} - \frac{1}{R_L}v_{C_o}\right) & t \in T_{n3} \\ \frac{1}{C_o}\left(i_{L_2} + n.i_{L_s} - \frac{1}{R_L}v_{C_o}\right) & t \in T_{n4} \end{cases} \tag{29}$$

B. STATE SPACE MODEL OF THE SYSTEMS

As discussed in the previous section, the proposed converter has six independent energy storage elements, so the number of state variables in the system is six, and the state space vector can be defined as follows:

$$X = \left[i_{L_s}, i_{L_1}, i_{L_2}, v_{C_1}, v_{C_2}, v_{C_o}\right]^T \tag{30}$$

so, the state space model of the systems can be written for each interval as follows:

$$\dot{X} = A_i * X + B_i * V_{in} \tag{31}$$

where $i = 1, 2, 3, 4$. Using (24)–(30), the state space model is given by:

$$A_1 = \begin{bmatrix} 0 & 0 & 0 & 0 & -\frac{1}{L_s} & -\frac{n}{L_s} \\ 0 & 0 & 0 & 0 & 0 & \frac{M}{L_t^2} \\ 0 & 0 & 0 & 0 & 0 & -\frac{L_1}{L_t^2} \\ 0 & 0 & 0 & 0 & 0 & 0 \\ \frac{1}{C_2} & 0 & 0 & 0 & 0 & 0 \\ \frac{n}{C_o} & 0 & \frac{1}{C_o} & 0 & 0 & -\frac{1}{C_o.R} \end{bmatrix}$$

$$A_2 = \begin{bmatrix} 0 & 0 & 0 & 0 & -\frac{1}{L_s} & \frac{n}{L_s} \\ 0 & 0 & 0 & 0 & 0 & -\frac{M}{L_t^2} \\ 0 & 0 & 0 & 0 & 0 & \frac{L_1}{L_t^2} \\ 0 & 0 & 0 & 0 & 0 & 0 \\ \frac{1}{C_2} & 0 & 0 & 0 & 0 & 0 \\ -\frac{n}{C_o} & 0 & -\frac{1}{C_o} & 0 & 0 & -\frac{1}{C_o.R} \end{bmatrix}$$

$$A_3 = \begin{bmatrix} 0 & 0 & 0 & \frac{1}{L_s} & 0 & \frac{n}{L_s} \\ 0 & 0 & 0 & -\frac{L_2}{L_t^2} & -\frac{L_2}{L_t^2} & -\frac{M}{L_t^2} \\ 0 & 0 & 0 & \frac{M}{L_t^2} & \frac{M}{L_t^2} & \frac{L_1}{L_t^2} \\ -\frac{1}{C_1} & \frac{1}{C_1} & 0 & 0 & 0 & 0 \\ 0 & \frac{1}{C_2} & 0 & 0 & 0 & 0 \\ -\frac{n}{C_o} & 0 & -\frac{1}{C_o} & 0 & 0 & -\frac{1}{C_o.R} \end{bmatrix}$$

$$A_4 = \begin{bmatrix} 0 & 0 & 0 & \frac{1}{L_s} & 0 & -\frac{n}{L_s} \\ 0 & 0 & 0 & -\frac{L_2}{L_t^2} & -\frac{L_2}{L_t^2} & \frac{M}{L_t^2} \\ 0 & 0 & 0 & \frac{M}{L_t^2} & \frac{M}{L_t^2} & -\frac{L_1}{L_t^2} \\ -\frac{1}{C_1} & \frac{1}{C_1} & 0 & 0 & 0 & 0 \\ 0 & \frac{1}{C_2} & 0 & 0 & 0 & 0 \\ \frac{n}{C_o} & 0 & \frac{1}{C_o} & 0 & 0 & -\frac{1}{C_o.R} \end{bmatrix}$$

$$B_1 = B_2 = B_3 = B_4 = \left[0, \frac{L_2}{L_t^2}, -\frac{M}{L_t^2}, 0, 0, 0\right]^T$$

The discrete-time model is derived through a periodic sampling of the continuous-time dynamics' state variables, and can be calculated as depicted in Fig. 8.

$$\begin{aligned} X_{n1} &= f_1(X_n, \phi) = e^{A_1.t_{n1}}X_n + \psi_1 V_{in} \\ X_{n2} &= f_2(X_{n1}, \phi) = e^{A_2.t_{n2}}X_{n1} + \psi_2 V_{in} \\ X_{n3} &= f_3(X_{n2}, \phi) = e^{A_3.t_{n3}}X_{n2} + \psi_3 V_{in} \\ X_{n+1} &= f_4(X_{n3}, \phi) = e^{A_4.t_{n4}}X_{n3} + \psi_4 V_{in} \end{aligned} \tag{32}$$

where for $i = 1, 2, 3, 4$ we have:

$$\psi_i = \int_0^{t_{ni}} e^{A_i t} B_i dt = A_i^{-1}.\left(e^{A_i t_{ni}} - I\right).B_i \tag{33}$$

and $t_{n1} = t_{n3} = \phi T_s$, $t_{n2} = t_{n4} = (\frac{1}{2} - \phi)T_s$. Finally, the discrete-time model of the converter in one switching cycle

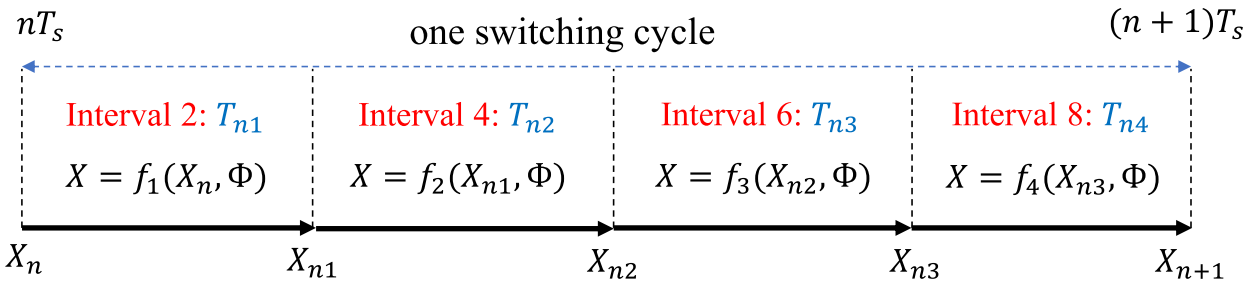
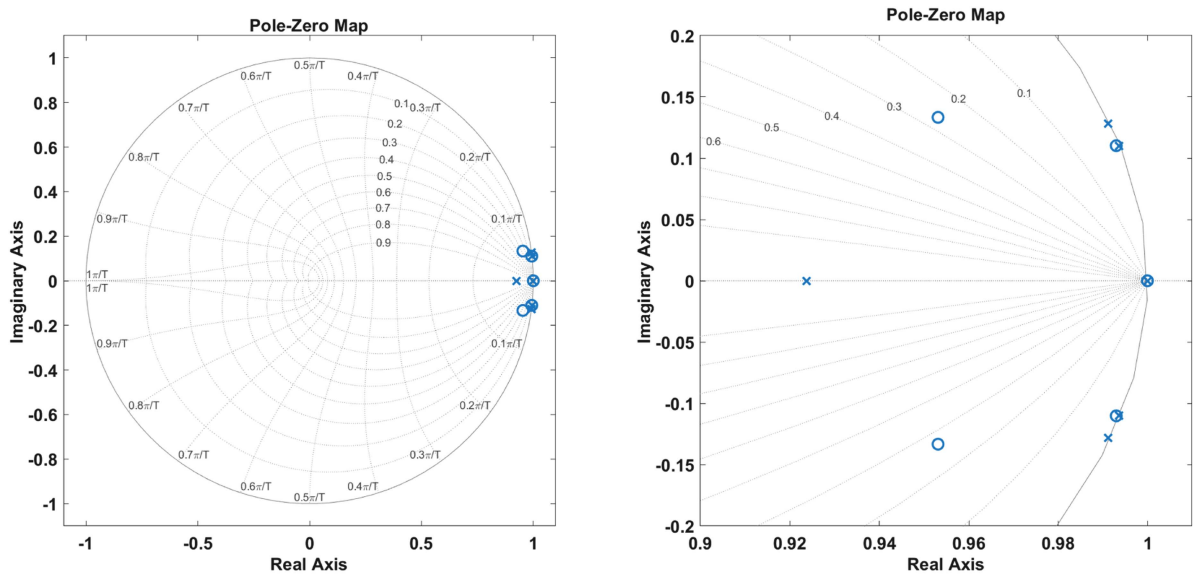


FIGURE 8. Discrete-time model of the proposed converter.



(a) (b)

FIGURE 9. Pole Zero map of the discrete-time open-loop transfer function of the system: (a) Zoom out (b) Zoom in.

is:

$$\begin{aligned} X_{n+1} &= f_4\left(f_3\left(f_2\left(f_1\left(X_n, \phi\right)\right)\right)\right) \\ &= e^{A_4 t_{n4}}\left\{e^{A_3 t_{n3}}\left[e^{A_2 t_{n2}}\left(e^{A_1 t_{n1}} X_n + \psi_1 V_{in}\right)\right.\right. \\ &\quad \left.\left. + \psi_2 V_{in}\right] + \psi_3 V_{in}\right\} + \psi_4 V_{in} \\ &= F(\phi) X_n + G(\phi) V_{in} \end{aligned} \tag{34}$$

where we have:

$$\begin{aligned} F(\phi) &= e^{A_4 t_{n4}}.e^{A_3 t_{n3}}.e^{A_2 t_{n2}}.e^{A_1 t_{n1}} \\ G(\phi) &= e^{A_4 t_{n4}}.e^{A_3 t_{n3}}.e^{A_2 t_{n2}}.\psi_1 + e^{A_4 t_{n4}}.e^{A_3 t_{n3}}.\psi_2 \\ &\quad + e^{A_4 t_{n4}}.\psi_3 + \psi_4 \end{aligned} \tag{35}$$

In the proposed converter, matrices A_1 and A_2 are rank deficient, and they do not have an inverse. In this scenario, we cannot use the closed-form equation (33) to calculate ψ_1 and ψ_2, and we should use the Taylor series expansion of $e^{A.t}$ as follows:

$$A_i^{-1}.\left(e^{A_i.t} - I\right) = A_i^{-1}\left(\sum_{k=0}^{\infty} \frac{1}{k!} A_i^k.t^k - I\right)$$

$$= A_i^{-1}\left(\sum_{k=1}^{\infty} \frac{1}{k!} A_i^k.t^k\right) = \sum_{k=0}^{\infty} \frac{1}{(k+1)!} A_i^k.t^{(k+1)} \tag{36}$$

Using (34)–(36), and by considering the parameters of the systems presented in Table 1, we can find the state space equations of the system. However, the closed-form state space equation is complex to calculate and it should be solved numerically in MATLAB software. By defining output voltage V_o as the output of the systems, the open loop transfer function of the output voltage V_o over the control variable ϕ can be calculated. Fig. 9 shows the pole-zero map of the system. The proposed converter is stable since all the poles of the discrete-time system are inside the unit circle, and by designing a proper controller, we can change the location of these poles and zeros to get the desired dynamic response.

VI. SIMULATION RESULTS

In this section, we present the simulation results for the proposed converter, conducted using the PSIM software. The simulation parameters utilized are documented in Table 1.

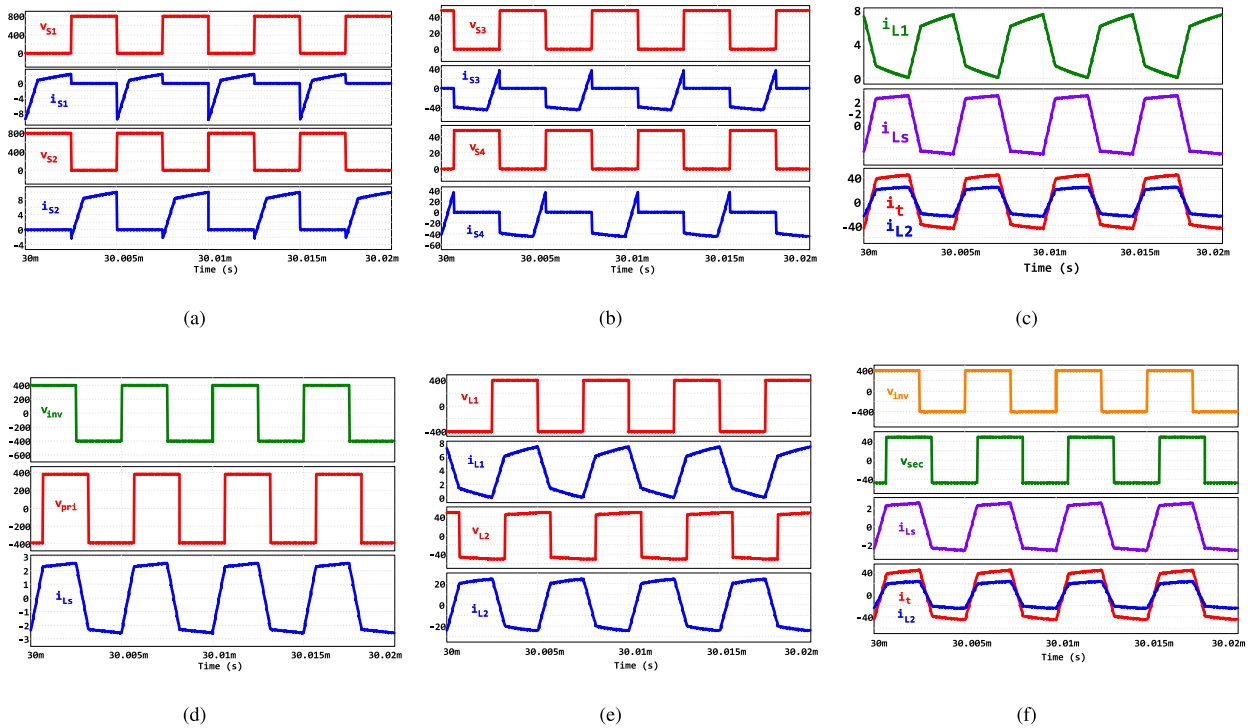


FIGURE 10. Simulation results for HV2LV power direction. (a) Waveforms of v_{DS1}, i_{DS1}, v_{DS2}, i_{DS2}. (b) Waveforms of v_{DS3}, i_{DS3}, v_{DS4}, i_{DS4}. (c) Waveforms of i_{L1}, i_{Ls}, i_{L2}, i_t. (d) Waveforms of v_{inv}, v_{pri}, i_{Ls}. (e) Waveforms of v_{L1}, i_{L1}, v_{L2}, i_{L2}. (f) Waveforms of v_{inv}, $v_{LV,Bridge}$, i_{Ls}, i_{L2}, i_t.

Fig. 10(a) displays the voltage and current waveforms of S_1 and S_2 for the HV2LV mode of operation. It can be observed that when S_1 turns ON, the current flowing into the switch is negative. During the dead time, this negative current discharges the snubber capacitor across the switch, resulting in switching under the ZVS condition. The behavior of S_2 is similar, with switching also occurring under ZVS. However, since the current is not symmetric for both switches in the half-bridge, the current for switch S_2 needs to be sufficiently high to achieve full ZVS. Fig. 10(b) illustrates the voltage and current waveforms of S_3 and S_4 for the HV2LV mode of operation. The negative current during turn ON enables ZVS during the switching process.

Fig. 10(c) presents the current distribution between the DPT path and the HV bridge. It is evident that the current i_t is divided between i_{L2} and i_{Ls}, indicating that the DPT path transfers a portion of the power to the output, reducing the amount of current flowing through the primary side power switches and thus decreasing conduction losses. Fig. 10(d) showcases the voltage across the series inductor and its current. A smaller difference between v_{inv} and v_{pri} results in a more square waveform for i_{Ls}. Fig. 10(e) illustrates the voltage and currents on both sides of the coupled inductor. Lastly, Fig. 10(f) depicts the bridge voltages and currents simultaneously.

To evaluate the performance of the proposed converter in the LV2HV power direction, another set of simulation results is presented in Fig. 11. Similar to the HV2LV mode, the top and bottom switches in the half-bridge exhibit non-symmetric behavior. However, in the LV2HV mode, the switch current during turn ON is negative, resulting in ZVS at turn ON, as depicted in Fig. 11(a). Fig. 11(b) illustrates the voltage and current waveforms of the LV side bridge, where the current is again negative during switching, leading to ZVS at the turn ON.

Fig. 11(c) demonstrates the power distribution between the DPT path and the half-bridge. The slope of the current waveforms differs compared to the HV2LV mode. Fig. 11(d) displays the voltage across the series inductor and the current slopes relative to the voltage. Fig. 11(e) depicts the voltage and current waveforms of the primary and secondary sides of the coupled inductor. Finally, Fig. 11(f) illustrates the current distribution relative to the bridge voltages in the primary and secondary sides of the converter.

To compare the bidirectional DAB converter, IFB converter, and the proposed converter, we summarize various aspects of these topologies in Table 2. One significant advantage of the proposed topology over DAB and IFB is the reduced number of switches on the HV side for the same power rating. This significantly reduces the semiconductor losses on the HV side. Additionally, the lower RMS current passing through the series inductor and high-frequency transformer leads to reduced conduction losses in these magnetic components. Furthermore, the lower current through the HV switches also results in decreased conduction losses. These advantages collectively contribute to lower overall conduction losses in the proposed topology, resulting in higher efficiency, particularly when combined with the inherent ZVS capability of the switches.

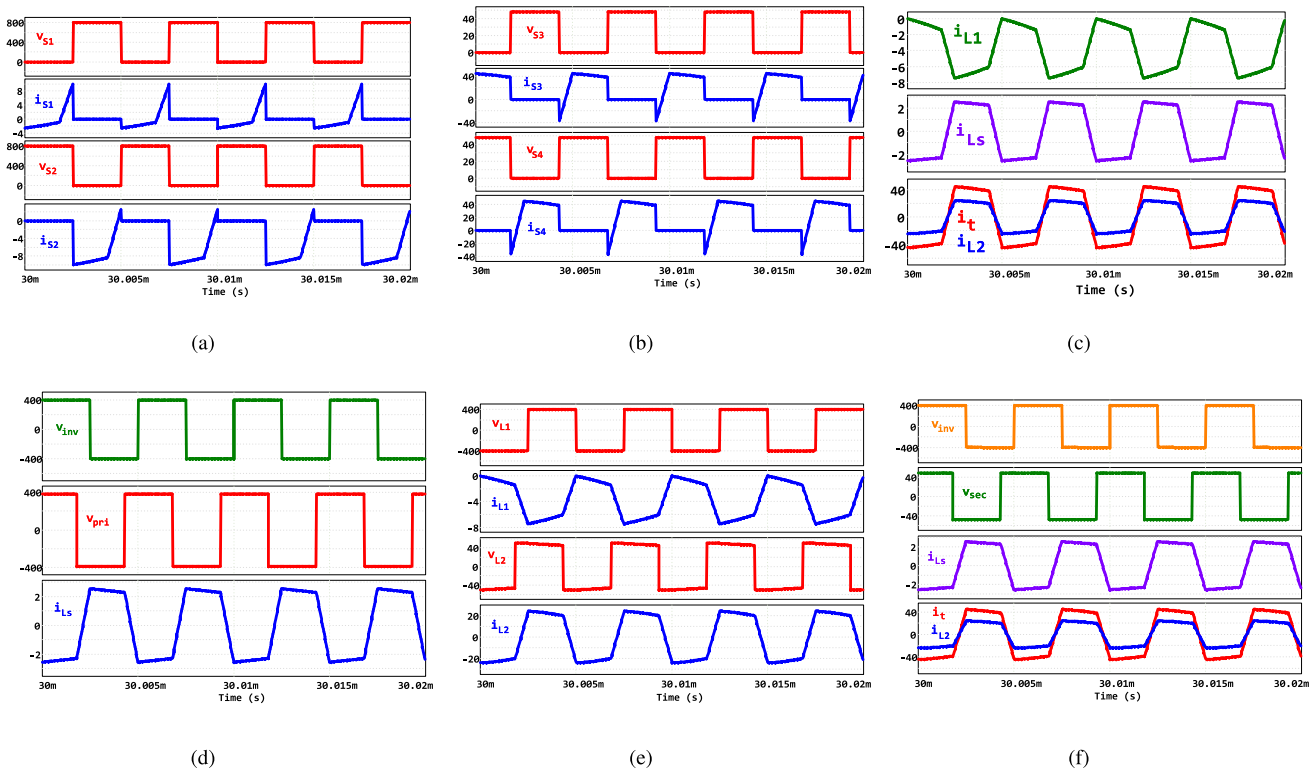


FIGURE 11. Simulation results for LV2HV power direction. (a) Waveforms of v_{DS1}, i_{DS1}, v_{DS2}, i_{DS2}. (b) Waveforms of v_{DS3}, i_{DS3}, v_{DS4}, i_{DS4}. (c) Waveforms of i_{L1}, i_{Ls}, i_{L2}, i_t. (d) Waveforms of v_{inv}, v_{pri}, i_{Ls}. (e) Waveforms of v_{L1}, i_{L1}, v_{L2}, i_{L2}. (f) Waveforms of v_{inv}, $v_{LV,Bridge}$, i_{Ls}, i_{L2}, i_t.

TABLE 2. Comparison of Bidirectional DAB, IFBDC, and Proposed Topology

Parameter	DAB	IFBDC	DPT
HV Switch	4	4	2
Magnetic components	2	2	3
ZVS at turn ON	Yes	No	Yes
HV switch current	High	High	Low
LV switch current	High	High	High
Series inductor current	High	High	Low
Coupled inductor current	–	–	High

TABLE 3. Main Components Used in the Prototype

Parameter	Value
HV SiC MOSFETs	IMW120R140M1
LV GaN HEMTs	GS61008P
Switching Frequency f_s	200 kHz
Coupled Inductors L_1	892 μH
Coupled Inductors L_2	14.3 μH
Coupled Inductors M	111 μH
Series Inductor L_s	104 μH
Transformer Turns Ratio n	8
Transformer Leakage L_{pleak}	17.1 μH
DC bus Capacitors C_1, C_2	10 μF
Input Capacitor C_{in}	20 μF
Output Capacitor C_{out}	10 μF

VII. EXPERIMENTAL RESULTS

To validate the performance of the proposed circuit, an experimental setup was designed to demonstrate its feasibility. Fig. 12 illustrates the prototype utilized in this experiment, and Fig. 13 shows the block diagram of the control algorithm used in this prototype. As an industrial product, the setup is specifically designed for a high power range of 3 kW. To achieve feasibility, two identical proposed converters are required to operate in an interleaved mode, with each converter capable of providing 1.5 kW. However, for the purpose of this paper and to focus on proving the feasibility of the proposed converter, only one converter is employed. The interleaved mode, as well as the details regarding the controller and switching operation in that mode, are not discussed in this paper. Based on the reported dimensions of the prototype in Fig. 12, the power density of the prototype is 43.4 W/in^3.

Table 3 presents the major components employed in the prototype. In the primary side of the proposed converter, 1200 V SiC MOSFETs were utilized due to the maximum DC bus voltage reaching 800 V, without considering voltage spikes at the switching frequency. Given the non-symmetric behavior of the HV side switches, the lower switch in the HV half bridge experiences a higher current stress compared to the top switch. To lower the conduction losses on the switch S_2, two SiC MOSFETs are paralleled. The selected switches and gate drivers for the HV side are IMW120R140M1 and IR2213SPBF, respectively.

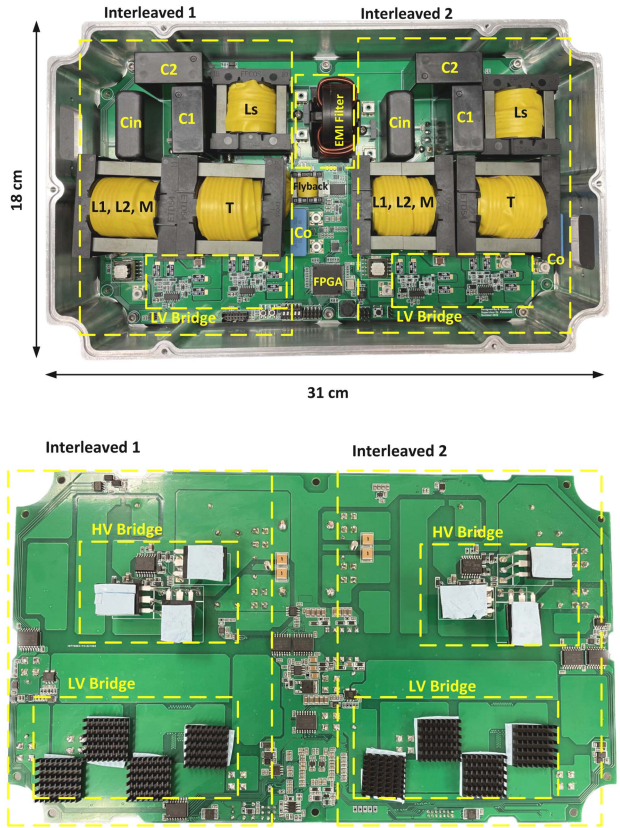


FIGURE 12. Image of the implemented prototype.

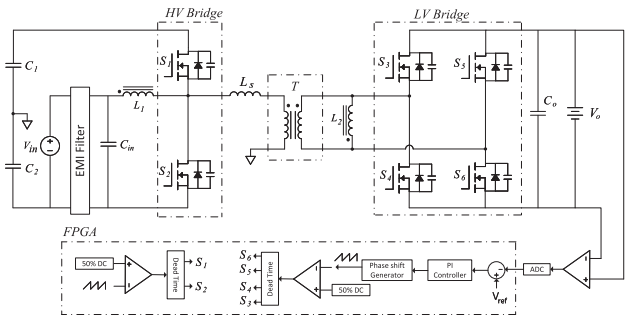


FIGURE 13. Block diagram of the implemented experimental setup.

For enhanced performance on the low voltage side, GaN HEMTs were employed. GaN HEMTs offer advantages such as lower conduction loss, switching loss, zero reverse recovery loss, lower parasitics, and ultimately improved overall performance. Considering the high current range on the LV side and to reduce the conduction losses on the switches, a parallel configuration of two GaN HEMTs was adopted for each switch in the LV bridge. The selected switches are $GS61008P$ from GaN Systems Inc. with the $V_{ds} = 100\,\text{V}$, $I_{ds} = 90\,\text{A}$. The selected gate driver for driving these GaN switches is one SI8273AB-IS1 for each pair of parallel switches.

The winded coupled inductor, with a coupling coefficient of $k = 98\%$, consists of 4 turns of 4 paralleled AWG 14 litz wire for the high current side and 32 turns of AWG 14 litz wire for the low current side. The selected cores are uncoated N87 Ferrite core ETD54 from TDK manufacturer which is capable of working up to 500 kHz switching frequency.

As a bidirectional converter, the circuit performance was initially tested in the HV2LV mode. Fig. 14 illustrates the waveform of the proposed converter operating in the HV2LV mode, with input voltage $V_{in} = 300\,\text{V}$, output voltage $V_{out} = 32\,\text{V}$, and power $P = 1.1\,\text{kW}$. The ratio of transferred power from the DPT path to the total output power is 87.1%. This indicates that 87.1% of the total power is transferred through the coupled inductor. Consequently, the current flowing through the HV switches and the high-frequency transformer is relatively low, as evidenced by the value of i_{Ls}. As a result, the conduction losses in the HV switches are expected to be minimal, thereby eliminating the need for large heat sinks for cooling purposes.

To verify the ZVS of the switches during the turn-on phase, the V_{DS} and V_{GS} characteristics of the switches are illustrated and magnified in Fig. 15. During the switching process, the V_{DS} of all the switches initially decreases to zero, and then the V_{GS} rises up to activate the switches. Consequently, ZVS is attainable for all the switches.

To assess the performance of the proposed converter in the LV2HV power direction, an additional set of experimental tests was conducted. Fig. 16 depicts the waveform of the proposed converter operating in the LV2HV mode, with an output voltage of $V_{out} = 20\,\text{V}$, input voltage of $V_{in} = 200\,\text{V}$, and power of $P = 700\,\text{W}$. The ratio of transferred power from the DPT path to the total power is 87%, indicating that conduction losses in the HV switches are expected to be minimal. Notably, the slope of the current waveforms in this mode differs from that of the HV2LV mode, aligning with both the theoretical waveforms shown in Fig. 2 and the simulated waveforms illustrated in Fig. 11.

Fig. 17 demonstrates the efficiency of the proposed prototype over a load range of 20% to 100%, considering the operation with and without the DPT path. For the operation with the DPT path, the efficiency is lower at lower power ratings compared to higher power ratings. The maximum achieved efficiency is 97.25% for HV2LV and 97% for LV2HV directions at 74% of the full load, gradually decreasing with increasing power thereafter. For the operation without the DPT path, the efficiency is lower under light load conditions due to the loss of ZVS, and it gradually improves up to 50% of the full load. However, efficiency declines beyond this point due to increased conduction loss. Notably, the gap between the two efficiency curves widens as power increases. This behavior is attributed to the high current flow through the DPT path at higher power ratings, leading to significantly reduced RMS current at the HV switches. In contrast, for the operation without the DPT path, all the current must pass through the HV switches, resulting in higher conduction losses and reduced overall efficiency.

Fig. 18 illustrates the converter efficiency at full load for different input voltages. The range of efficiency variation for

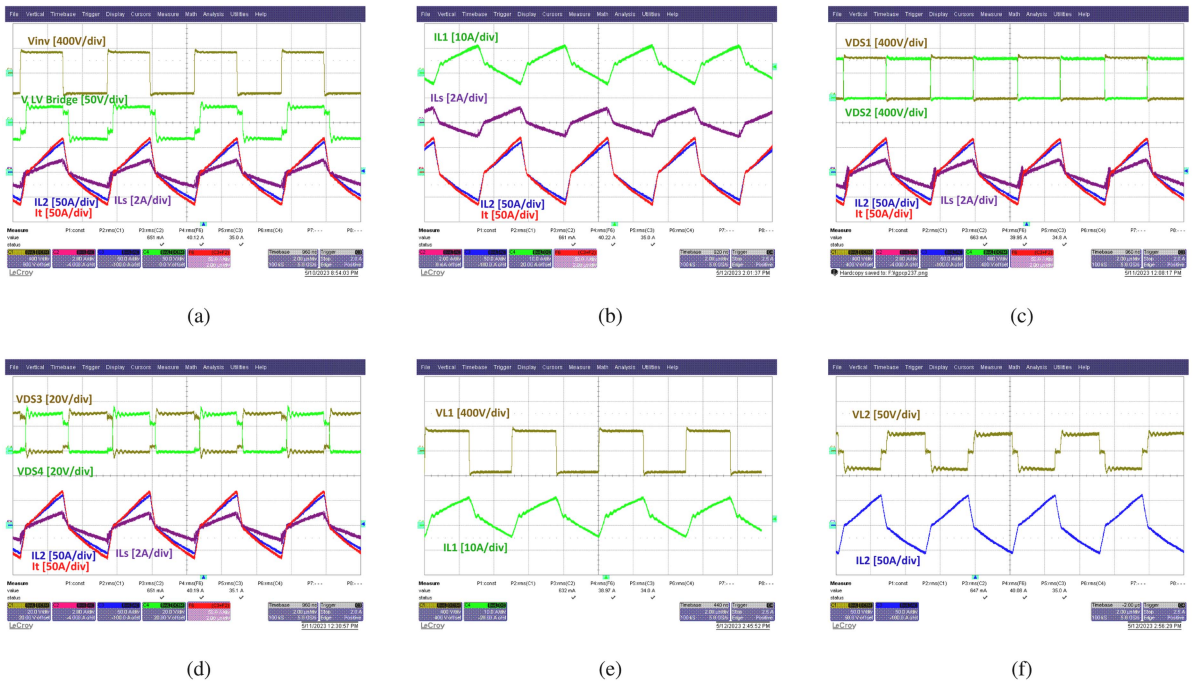


FIGURE 14. Experimental waveforms for HV2LV power direction at $V_{in} = 300\,\text{V}$, $P_{out} = 1.1\,\text{kW}$. (a) Bridge voltages and currents. (b) Currents. (c) Drain-Source voltages of HV switches, currents. (d) Drain-Source voltages of LV switches, currents. (e) Voltage and current of L1. (f) Voltage and current of L2.

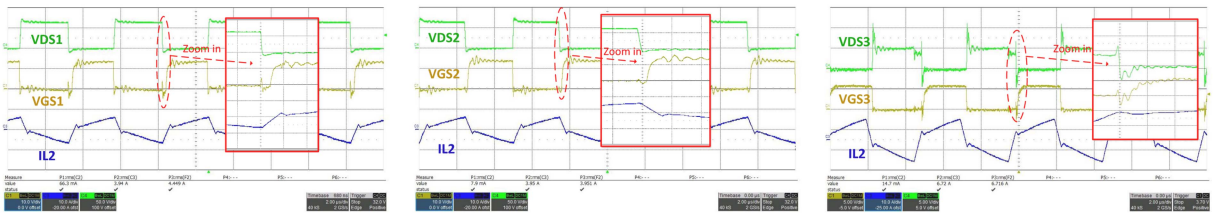


FIGURE 15. V_{DS} and V_{GS} of different switches and the magnified waveforms. (a) S_1. (b) S_2. (c) S_3.

the converter with DPT is notably lower than that for the converter without the DPT path. This discrepancy is attributed to the current sharing feature of the DPT. In the absence of the DPT, the current waveforms exhibit more triangular shapes with higher peaks, leading to increased conduction loss and reduced efficiency. However, with the DPT path, a significant portion of the current flows to the rectifier side from the coupled inductor. Consequently, the current in the high-voltage switches is smaller, resulting in reduced variation in conduction losses and a more stable efficiency.

Although it was expected to have higher efficiency in the prototype, the conduction losses on the GaN switches turned out to be higher than anticipated due to thermal issues. The prototype utilizes GS61008P GaN switches, which are packaged in compact bottom-cooled packaging called GaNPacks. This packaging posed challenges in achieving proper cooling, resulting in an increase in the channel resistance ($R_{ds,on}$) and consequently, lower efficiency.

Fig. 19 illustrates the RMS current of the HV side switches S_1 and S_2 for different loads. As depicted in the figure, the RMS current for both switches is lower in the converter with DPT compared to the converter without DPT. Additionally, the current in the HV bridge is asymmetric, with switch S_2 experiencing higher current than S_1, resulting in increased losses and temperature for S_2. To address this issue, in the designed prototype, two switches are placed in parallel for S_2 to reduce the current and losses in each, achieving a balance in the losses of HV side switches and enhancing the product's lifetime.

Fig. 20 illustrates the distribution of the $P_{DPT,n}$ over the range of the normalized output power. This parameter is calculated based on the ratio of the RMS value of current waveforms i_{L2} (blue) and i_t (red) in Fig. 14. The variation of $P_{DPT,n}$ across the power range is approximately 86–87%, as depicted in this figure. At lower power ratings, this parameter is slightly smaller, but it gradually increases with increasing power, reaching a maximum of 87.2%, after which it

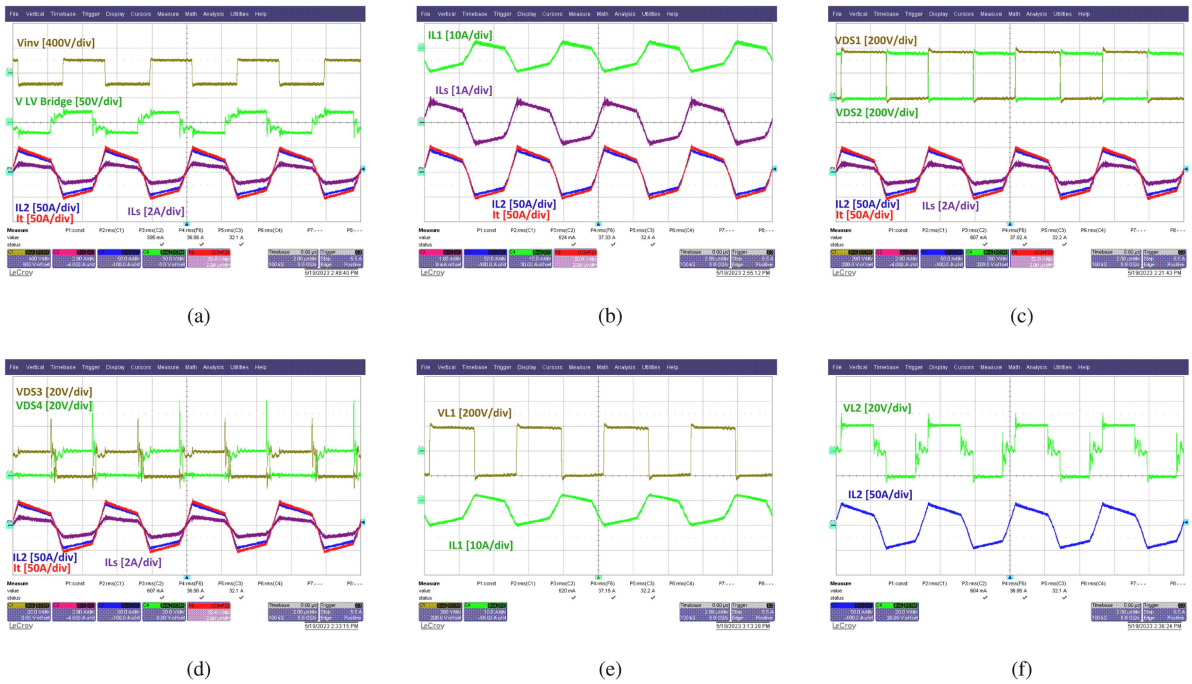


FIGURE 16. Experimental waveforms for LV2HV power direction at $V_{out} = 20\,V$, $P_{out} = 700\,W$. (a) Bridge voltages and currents. (b) Currents. (c) Drain-Source voltages of HV switches, currents. (d) Drain-Source voltages of LV switches, currents. (e) Voltage and current of L1. (f) Voltage and current of L2.

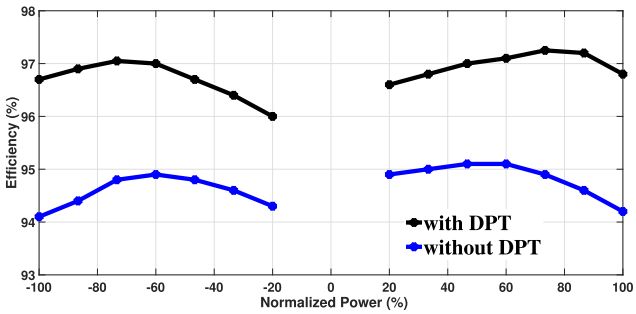


FIGURE 17. Efficiency for normalized output power at $V_{in} = 400\,V$, $V_o = 48\,V$.

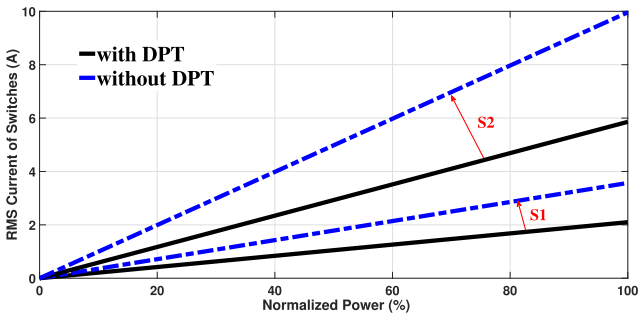


FIGURE 19. Variation of rms current of HV switches for normalized output power.

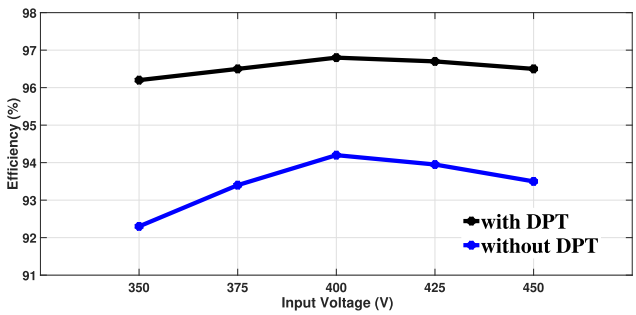


FIGURE 18. Efficiency for input voltage variation at full load and $V_o = 48\,V$.

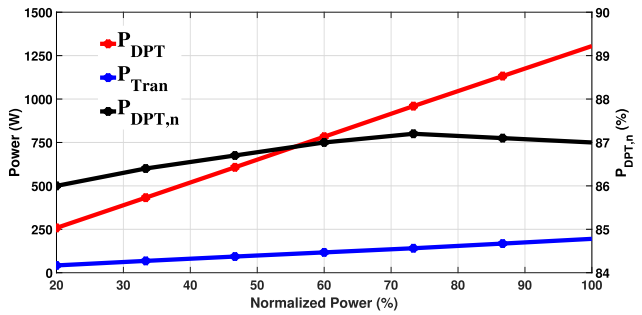


FIGURE 20. Distribution of power in different paths (P_{DPT} and P_{tr}, left axis) and the ratio $P_{DPT,n}$ (right axis) with respect to normalized output power.

decreases for higher power levels. Moreover, the ability to adjust the DPT ratio contributes to lower conduction losses and improved efficiency. However, it is essential to strike a balance between reducing conduction losses by increasing the DPT ratio and potentially lowering power density by decreasing the DPT ratio, which corresponds to a smaller coupled inductor. Finding the optimal DPT ratio involves considering trade-offs

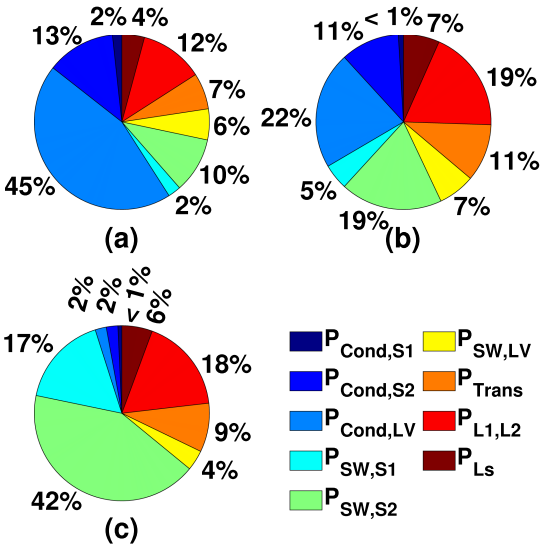


FIGURE 21. Distribution of losses for different components at $P_{DPT,n} = 54\%$. (a) Full-load. (b) Half-load. (c) Light-load.

TABLE 4. Comparison of Bidirectional DC–DC Converters

Ref.	Topology	$P_o(kW)$ $f_s(kHz)$	η_{max}	Components
[48]	CF[1]-PushPull	1 kW 50 kHz	94.5%	6S,2L,2C,1T[6]
[49]	SEPIC (Modified)	1.1 kW 20 kHz	87.78%	3S,2L,2C
[27]	CF-DAB	1.6 kW 20 kHz	94%	4S,2L,4C,1T
[8]	FB[2]-DAB HB[3]-DAB FB-CLLC HB-CLLC	1 kW 170 kHz	95.1% 93.9% 95% 96.5%	8S,1L,1T 4S, 1L,4C,1T 8S,2L,2C,1T 4S,2L,4C,1T
[50]	DAB (SPS[4]) DAB (DPS[5])	1.1 kW 100 kHz	86.8% 95.6 %	8S,2L,2C,1T
[51]	LLC-DAB	6.6 kW 120 kHz	94%	8S,2L,2C,1T
Prop.	DPT-DAB	1.1 kW 200 kHz	97.25%	6S,2L,2C,1T

[1]Current Fed, [2]Full Bridge, [3]Half Bridge, [4]Single Phase Shift Control, [5]Double Phase Shift Control, [6] S: Switch, L: Inductor, C: Capacitor, T: Transformer

between conduction losses and power density to achieve the most efficient and compact design.

The analytical assessment of the converter losses under various load conditions, full-load, half-load, and light-load is presented in Fig. 21. Conduction losses are calculated based on the RMS current flowing through each component. Additionally, switching losses during turn-off are computed by scaling the datasheet values to match the voltage and current of each switch at different load conditions. Notably, since this topology employs ZVS during turn-on, turn-on losses are only calculated for light-load conditions, and for half-load and full-load scenarios, these losses are negligible. The magnetic

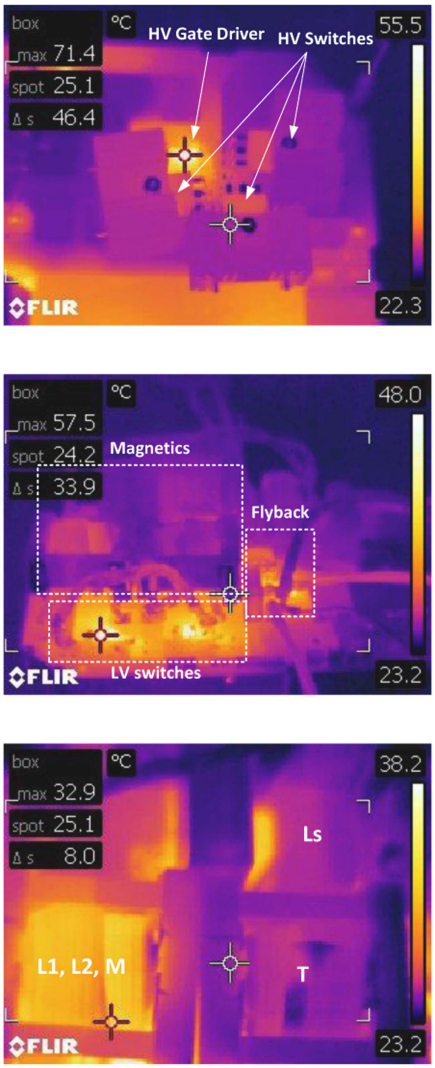


FIGURE 22. Thermal images of the prototype at 200 V input voltage, 700 W power. (Top) HV switches. (Middle) LV switches. (Bottom) Magnetic components.

losses include both core losses and copper losses in the conductors. Core losses are estimated using datasheet values for the cores. As depicted in the figure, at full-load, conduction losses on the LV side dominate, while at light-load conditions, the loss of ZVS results in higher switching losses on the HV side.

Fig. 22 presents thermal images of the prototype operating at $V_{in} = 200\,\text{V}$ and $P = 700\,\text{W}$. As anticipated, the temperatures of the HV switches remained below $30\,^{\circ}C$, while the LV switches exhibited temperatures around $57\,^{\circ}C$. Additionally, among all the magnetic components, the coupled inductor exhibited a higher temperature due to its higher RMS current, resulting in increased conduction losses. The Flyback converter in Fig. 22(b) shows the temperature of the flyback switch which is utilized for the signal supply.

Table 4 compares key features of bidirectional topologies from the literature, including maximum reported efficiency,

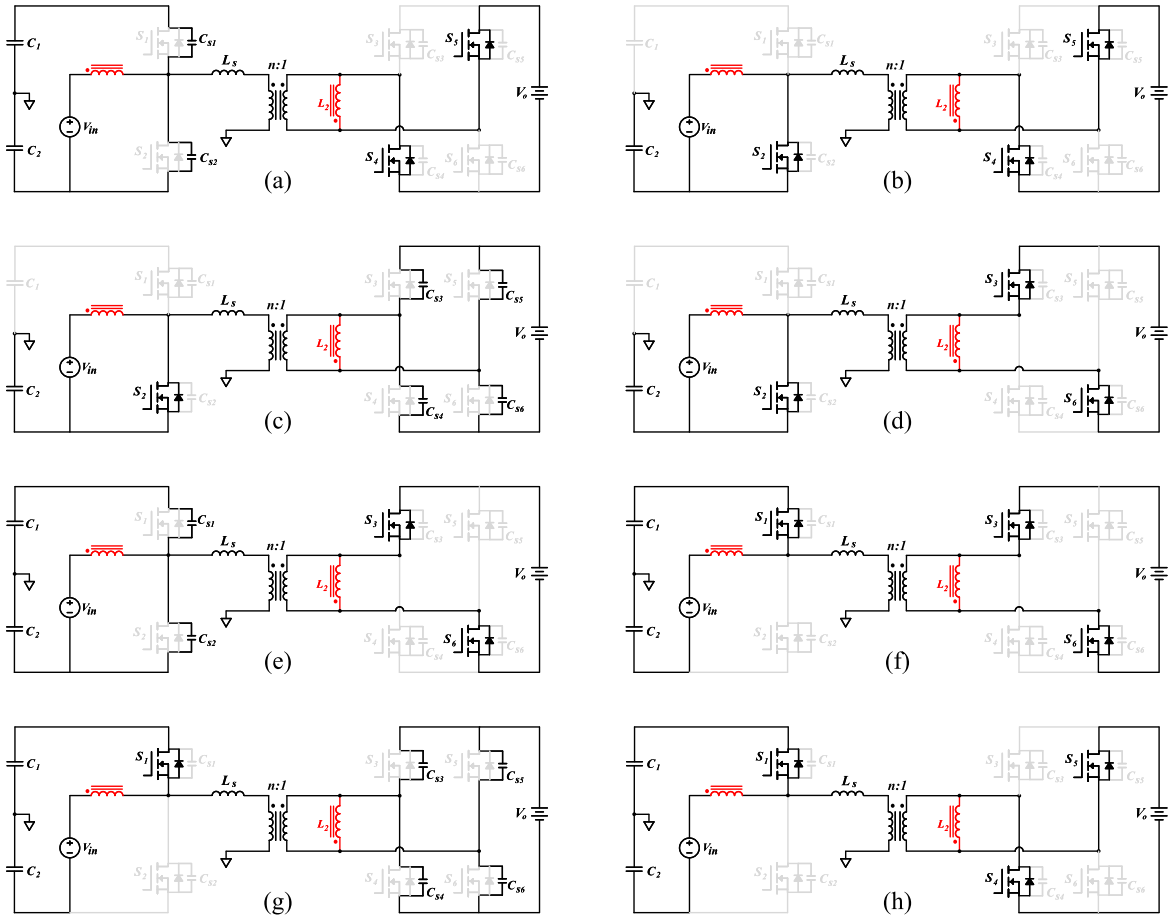


FIGURE 23. Equivalent circuits of each interval for the LV2HV mode of operation in the proposed converter: (a) interval 1, (b) interval 2, (c) interval 3, (d) interval 4, (e) interval 5, (f) interval 6, (g) interval 7, and (h) interval 8.

the number of components, output power, and switching frequency. The proposed converter exhibits promising characteristics compared to other topologies. With fewer components, higher efficiency (resulting in smaller heat sinks), and a higher switching frequency, the advantages of the proposed topology become evident in applications requiring higher power density. Furthermore, the efficiency of the proposed converter can be further improved by implementing different switching techniques, such as double phase shift (DPS).

VIII. CONCLUSION

This paper presented a novel bidirectional DC–DC converter that offers reduced conduction losses through a DPT path, allowing power to flow directly to the secondary side of the high-frequency transformer. The DPT power ratio can be adjusted through an optimal design of the circuit, leading to improved overall efficiency. Furthermore, the input current is shaped to have lower peak values, resulting in further reductions in conduction losses. The proposed topology benefits from the inherent soft switching as well and can provide a cost-effective solution for high-performance energy storage systems.

APPENDIX

A. LV2HV MODES OF OPERATION

Fig. 2(b) shows the key waveforms of the proposed converter for the LV2HV power flow. According to this figure, there are eight switching intervals in each switching cycle. Fig. 23 illustrates the equivalent circuits for each interval.

B. LV2HV STEADY STATE ANALYSIS

The steady-state analysis for the LV2HV mode is similar to the HV2LV mode. In this mode, the averaged P_{tr} is equal to:

$$P_{tr} = -\frac{V_{dc} n V_o}{2 L_s f_s} \phi \, (1 - 2\phi) \tag{37}$$

The negative sign in (37) shows the direction of power. Also, (37) is inversely proportional to the switching frequency, and has a maximum at $\phi = 0.25$.

The averaged power transferred through the DPT can be achieved as:

$$P_{DPT} = \frac{M V_o}{L_t^2 f_s} \left[V_{in} \, (\phi - 0.25) + V_{dc} \left(\frac{1}{8} - \phi + \phi^2 \right) \right] \tag{38}$$

Equation (38) shows that the P_{DPT} is inversely proportional to the switching frequency.

Finally, the averaged input current I_{in} can be achieved as:

$$I_{in} = \frac{MV_o}{L_t^2 f_s}(\phi - 0.25) - \frac{V_{dc} - 4V_{in}}{8L_t^2 f_s}L_2 \tag{39}$$

Again, the averaged input current is inversely proportional to the switching frequency.

C. LV2HV DESIGN CONSIDERATIONS

The normalized direct power transfer in the LV2HV mode is as follows:

$$P_{DPT,n} = \frac{P_{DPT}}{P_o} = \frac{-xV_o}{V_{in}} \frac{V_{in}(\phi - 0.25) + V_{dc}\left(\frac{1}{8} - n_\phi + n_\phi^2\right)}{xV_o(\phi - 0.25) + \frac{1}{2}V_{in} - \frac{1}{8}V_{dc}} \tag{40}$$

By plotting the $P_{DPT,n}$ we can find that it has a maximum of 0.545 at $\phi = 0.12$.

REFERENCES

[1] A. Chub, D. Vinnikov, R. Kosenko, E. Liivik, and I. Galkin, "Bidirectional DC–DC converter for modular residential battery energy storage systems," *IEEE Trans. Ind. Electron.*, vol. 67, no. 3, pp. 1944–1955, Mar. 2020.

[2] R. Chen, R. Lu, X. Bao, C. Li, W. Li, and X. He, "Efficiency-oriented parameter design and comparison of medium voltage isolated bidirectional DC/DC converters," *IEEE Open J. Power Electron.*, vol. 4, pp. 14–23, 2023.

[3] M. Pahlevaninezhad, J. Drobnik, P. K. Jain, and A. Bakhshai, "A load adaptive control approach for a zero-voltage-switching DC/DC converter used for electric vehicles," *IEEE Trans. Ind. Electron.*, vol. 59, no. 2, pp. 920–933, Feb. 2012.

[4] V. R. K. Kanamarlapudi, B. Wang, N. K. Kandasamy, and P. L. So, "A new ZVS full-bridge DC–DC converter for battery charging with reduced losses over full-load range," *IEEE Trans. Ind. Appl.*, vol. 54, no. 1, pp. 571–579, Jan./Feb. 2018.

[5] C. Sun, X. Zhang, J. Zhang, M. Zhu, and J. Huang, "Hybrid input-series–output-series modular DC–DC converter constituted by resonant and nonresonant dual active bridge modules," *IEEE Trans. Ind. Electron.*, vol. 69, no. 1, pp. 1062–1069, Jan. 2022.

[6] H. Bahrami, S. Farhangi, H. Iman-Eini, and E. Adib, "A new interleaved coupled-inductor nonisolated soft-switching bidirectional DC–DC converter with high voltage gain ratio," *IEEE Trans. Ind. Electron.*, vol. 65, no. 7, pp. 5529–5538, Jul. 2018.

[7] L. F. Costa, S. A. Mussa, and I. Barbi, "Multilevel buck/boost-type DC–DC converter for high-power and high-voltage application," *IEEE Trans. Ind. Appl.*, vol. 50, no. 6, pp. 3931–3942, Nov./Dec. 2014.

[8] P. He and A. Khaligh, "Comprehensive analyses and comparison of 1 kW isolated DC–DC converters for bidirectional EV charging systems," *IEEE Trans. Transp. Electrific.*, vol. 3, no. 1, pp. 147–156, Mar. 2017.

[9] H. Li, Z. Zhang, S. Wang, J. Tang, X. Ren, and Q. Chen, "A 300-kHz 6.6-kW SiC bidirectional LLC onboard charger," *IEEE Trans. Ind. Electron.*, vol. 67, no. 2, pp. 1435–1445, Feb. 2020.

[10] H. S. Chung, W.-L. Cheung, and K. S. Tang, "A ZCS bidirectional flyback DC/DC converter," *IEEE Trans. Power Electron.*, vol. 19, no. 6, pp. 1426–1434, Nov. 2004.

[11] N. M. Mukhtar and D. D. Lu, "A bidirectional two-switch flyback converter with cross-coupled LCD snubbers for minimizing circulating current," *IEEE Trans. Ind. Electron.*, vol. 66, no. 8, pp. 5948–5957, Aug. 2019.

[12] M. Kwon, J. Park, and S. Choi, "A bidirectional three-phase push–pull converter with dual asymmetrical PWM method," *IEEE Trans. Power Electron.*, vol. 31, no. 3, pp. 1887–1895, Mar. 2016.

[13] T.-T. Le, H. Jeong, and S. Choi, "A bidirectional three-phase push–pull converter with hybrid PPS-DAPWM switching method for high power and wide voltage range applications," *IEEE Trans. Ind. Electron.*, vol. 68, no. 2, pp. 1322–1331, Feb. 2021.

[14] C. Mi, H. Bai, C. Wang, and S. Gargies, "Operation, design and control of dual H-bridge-based isolated bidirectional DC-DC converter," *IET Power Electron.*, vol. 1, no. 4, pp. 507–517, 2008.

[15] D. Lyu, C. Straathof, T. B. Soeiro, Z. Qin, and P. Bauer, "ZVS-optimized constant and variable switching frequency modulation schemes for dual active bridge converters," *IEEE Open J. Power Electron.*, vol. 4, pp. 801–816, 2023.

[16] C. Jiang and H. Liu, "A novel interleaved parallel bidirectional dual-active-bridge DC–DC converter with coupled inductor for more-electric aircraft," *IEEE Trans. Ind. Electron.*, vol. 68, no. 2, pp. 1759–1768, Feb. 2021.

[17] B. Zhao, Q. Song, W. Liu, and Y. Sun, "Overview of dual-active-bridge isolated bidirectional DC–DC converter for high-frequency-link power-conversion system," *IEEE Trans. Power Electron.*, vol. 29, no. 8, pp. 4091–4106, Aug. 2014.

[18] N. Hou and Y. W. Li, "Overview and comparison of modulation and control strategies for a nonresonant single-phase dual-active-bridge DC–DC converter," *IEEE Trans. Power Electron.*, vol. 35, no. 3, pp. 3148–3172, Mar. 2020.

[19] F. Xue, R. Yu, and A. Q. Huang, "A 98.3% efficient GAN isolated bidirectional DC–DC converter for DC microgrid energy storage system applications," *IEEE Trans. Ind. Electron.*, vol. 64, no. 11, pp. 9094–9103, Nov. 2017.

[20] B. Zhao, Q. Yu, and W. Sun, "Extended-phase-shift control of isolated bidirectional DC–DC converter for power distribution in microgrid," *IEEE Trans. Power Electron.*, vol. 27, no. 11, pp. 4667–4680, Nov. 2012.

[21] H. Bai, C. C. Mi, and S. Gargies, "The short-time-scale transient processes in high-voltage and high-power isolated bidirectional DC–DC converters," *IEEE Trans. Power Electron.*, vol. 23, no. 6, pp. 2648–2656, Nov. 2008.

[22] F. Krismer, J. Biela, and J. W. Kolar, "A comparative evaluation of isolated bi-directional DC/DC converters with wide input and output voltage range," in *Proc. 14th IAS Annu. Meeting. Conf. Rec. Ind. Appl. Conf.*, 2005, pp. 599–606.

[23] Y. Li, J. Hu, F. Chen, Z. Li, Z. He, and R. Mai, "Dual-phase-shift control scheme with current-stress and efficiency optimization for wireless power transfer systems," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 65, no. 9, pp. 3110–3121, Sep. 2018.

[24] Z. Li, T. Wu, G. Zhang, and R. Yang, "Hybrid modulation method combining variable frequency and double phase-shift for a 10 kW LLC resonant converter," *IET Power Electron.*, vol. 11, no. 13, pp. 2161–2169, 2018.

[25] H. Shi et al., "Minimum-BackFlow-power scheme of DAB-based solid-state transformer with extended-phase-shift control," *IEEE Trans. Ind. Appl.*, vol. 54, no. 4, pp. 3483–3496, Jul./Oct. 2018.

[26] A. A. Gandomi, L. Parsa, and K. A. Corzine, "High efficiency isolated 5-level dual active DC–DC converter using wide band gap devices," *IEEE Trans. Ind. Electron.*, vol. 70, no. 6, pp. 5840–5849, Jun. 2023.

[27] F. Z. Peng, H. Li, G.-J. Su, and J. S. Lawler, "A new ZVS bidirectional DC-DC converter for fuel cell and battery application," *IEEE Trans. Power Electron.*, vol. 19, no. 1, pp. 54–65, Jan. 2004.

[28] G. A. Mudiyanselage, N. Keshmiri, and A. Emadi, "A review of DC-DC resonant converter topologies and control techniques for electric vehicle applications," *IEEE Open J. Power Electron.*, vol. 4, pp. 945–964, 2023.

[29] Y. Liao et al., "An LLC-DAB bidirectional DCX converter with wide load range ZVS and reduced switch count," *IEEE Trans. Power Electron.*, vol. 37, no. 2, pp. 2250–2263, Feb. 2022.

[30] L. Costa, G. Buticchi, and M. Liserre, "A fault-tolerant series-resonant DC–DC converter," *IEEE Trans. Power Electron.*, vol. 32, no. 2, pp. 900–905, Feb. 2017.

[31] W. Han and L. Corradini, "General closed-form ZVS analysis of dual-bridge series resonant DC–DC converters," *IEEE Trans. Power Electron.*, vol. 34, no. 9, pp. 9289–9302, Sep. 2019.

[32] U. Kundu, B. Pant, S. Sikder, A. Kumar, and P. Sensarma, "Frequency domain analysis and optimal design of isolated bidirectional series resonant converter," *IEEE Trans. Ind. Appl.*, vol. 54, no. 1, pp. 356–366, Jan./Feb. 2018.

[33] T. Jiang, J. Zhang, X. Wu, K. Sheng, and Y. Wang, "A bidirectional LLC resonant converter with automatic forward and backward mode transition," *IEEE Trans. Power Electron.*, vol. 30, no. 2, pp. 757–770, Feb. 2015.

[34] Y. Liao et al., "Single-stage DAB-LLC hybrid bidirectional converter with tight voltage regulation under DCX operation," *IEEE Trans. Ind. Electron.*, vol. 68, no. 1, pp. 293–303, Jan. 2021.
[35] Y. Liao et al., "Single-stage DAB-LLC hybrid bidirectional converter with tight voltage regulation under DCX operation," *IEEE Trans. Ind. Electron.*, vol. 68, no. 1, pp. 293–303, Jan. 2021.
[36] Y. Zhang, D. Zhang, J. Li, and H. Zhu, "Bidirectional LCLL resonant converter with wide output voltage range," *IEEE Trans. Power Electron.*, vol. 35, no. 11, pp. 11813–11826, Nov. 2020.
[37] C. Wang, S. Zhang, Y. Wang, B. Chen, and J. Liu, "A 5-kW isolated high voltage conversion ratio bidirectional CLTC resonant DC–DC converter with wide gain range and high efficiency," *IEEE Trans. Power Electron.*, vol. 34, no. 1, pp. 340–355, Jan. 2019.
[38] J. Zhang, J. Liu, J. Yang, N. Zhao, Y. Wang, and T. Q. Zheng, "An LLC-LC type bidirectional control strategy for an LLC resonant converter in power electronic traction transformer," *IEEE Trans. Ind. Electron.*, vol. 65, no. 11, pp. 8595–8604, Nov. 2018.
[39] R. Ramachandran and M. Nymand, "A 98.8% efficient bidirectional full-bridge isolated DC–DC GAN converter," in *Proc. IEEE Appl. Power Electron. Conf. Expo.*, 2016, pp. 609–614.
[40] R. Ramachandran and M. Nyman, "Experimental demonstration of a 98.8% efficient isolated DC–DC GAN converter," *IEEE Trans. Ind. Electron.*, vol. 64, no. 11, pp. 9104–9113, Nov. 2017.
[41] M. Nymand, U. K. Madawala, M. A. E. Andersen, B. Carsten, and O. S. Seiersen, "Reducing AC-winding losses in high-current high-power inductors," in *Proc. 35th Annu. Conf. IEEE Ind. Electron.*, 2009, pp. 777–781.
[42] H. Bai, Z. Nie, and C. C. Mi, "Experimental comparison of traditional phase-shift, dual-phase-shift, and model-based control of isolated bidirectional DC–DC converters," *IEEE Trans. Power Electron.*, vol. 25, no. 6, pp. 1444–1449, Jul. 2010.
[43] T. Wu, Y. Chen, J. Yang, and C. Kuo, "Isolated bidirectional full-bridge DC–DC converter with a flyback snubber," *IEEE Trans. Power Electron.*, vol. 25, no. 7, pp. 1915–1922, Jul. 2010.
[44] T. Wu, J. Yang, C. Kuo, and Y. Wu, "Soft-switching bidirectional isolated full-bridge converter with active and passive snubbers," *IEEE Trans. Ind. Electron.*, vol. 61, no. 3, pp. 1368–1376, Mar. 2014.
[45] M. Zareie, B. Poorali, S. Eren, and M. Pahlevani, "New DC–DC converter with direct power transfer capability," *IEEE Trans. Power Electron.*, vol. 36, no. 5, pp. 5647–5663, May 2021.
[46] S. Shao et al., "Modeling and advanced control of dual-active-bridge DC–DC converters: A review," *IEEE Trans. Power Electron.*, vol. 37, no. 2, pp. 1524–1547, Feb. 2022.
[47] L. Shi, W. Lei, Z. Li, J. Huang, Y. Cui, and Y. Wang, "Bilinear discrete-time modeling and stability analysis of the digitally controlled dual active bridge converter," *IEEE Trans. Power Electron.*, vol. 32, no. 11, pp. 8787–8799, Nov. 2017.
[48] S. Li, K. Xiangli, and K. M. Smedley, "A control map for a bidirectional PWM plus phase-shift-modulated push–pull DC–DC converter," *IEEE Trans. Ind. Electron.*, vol. 64, no. 11, pp. 8514–8524, Nov. 2017.
[49] U. Sharma and B. Singh, "A bidirectional charger for low-voltage-powered battery vehicles," *IEEE Trans. Transp. Electrific.*, vol. 9, no. 3, pp. 3994–4003, Sep. 2023.
[50] A. Kazemtarghi, S. Dey, A. Mallik, and N. G. Johnson, "Asymmetric half-frequency modulation in dab to optimize the conduction and switching losses in EV charging applications," *IEEE Trans. Transp. Electrific.*, vol. 9, no. 3, pp. 4196–4210, Sep. 2023.
[51] A. V. Mirtchev and E. C. Tatakis, "Design methodology based on dual control of a resonant dual active bridge converter for electric vehicle battery charging," *IEEE Trans. Veh. Technol.*, vol. 71, no. 3, pp. 2691–2705, Mar. 2022.

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