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High Power Density On-Board Charger Featuring Power Pulsating Buffer

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ABSTRACT Power electronics plays a key role in electric vehicle technology in areas such as the battery charging and managing, dc distribution and motor drive systems, among others. There are, however, significant challenges to be addressed in terms of cost, performance, reliability and power density. This paper aims at proposing an improved on-board charger architecture taking advantage of a power pulsating buffer topology. The proposed architecture will enable to significantly reduce the dc-link capacitor size, enabling a change in its technology, and leading to a higher power density and higher reliability implementation. The proposed architecture is analyzed, its main design considerations are discussed and, finally, a 3.6-kW experimental prototype is designed and implemented to prove the feasibility of this proposal. As a conclusion, the proposed topology is recommended as a high-performance high-power-density OBC implementation for future EVs.

INDEX TERMS Electric vehicle (EV), dc-link, on-board charger (OBC), power pulsating buffer.

I. INTRODUCTION

Electric vehicles (EV) are called to change the modern transportation paradigm, bringing high performance and environmentally friendly products. EV technology [1] has consequently arisen as a key technology to overcome important environmental and societal challenges. It has also brought the user a new product with important technological innovations powered by power electronic systems. There are, however, important technical challenges to be solved in terms of cost, power density, weight, reliability, efficiency, and range, among others.

Power electronics plays a key role in the development of current and future EV technology [2]. The power electronic system of an EV can be subdivided into 4 great areas (Fig. 1(a)): the charging system [3] which manages the charge of the vehicle battery either using mains connection or high-speed dc connection; the dc distribution system [4], [5], [6], [7], which steps down the high voltage battery voltage to supply all the low-voltage loads, typically 12 V; the motor drive system [8] that provides the traction power, typically in a single or dual motor configurations; and last but not least, the battery management system (BMS) [9] that provides high performance charging and balancing systems as well as to ensure the battery safe operation.

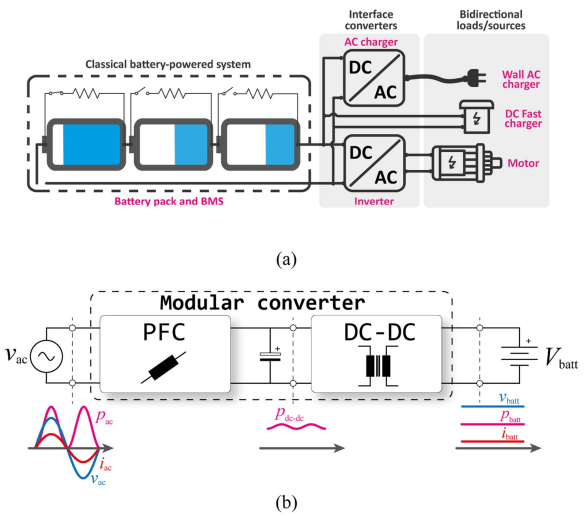

FIGURE 1. Electric vehicle powertrain diagram (a) and typical on-board charger structure (b).

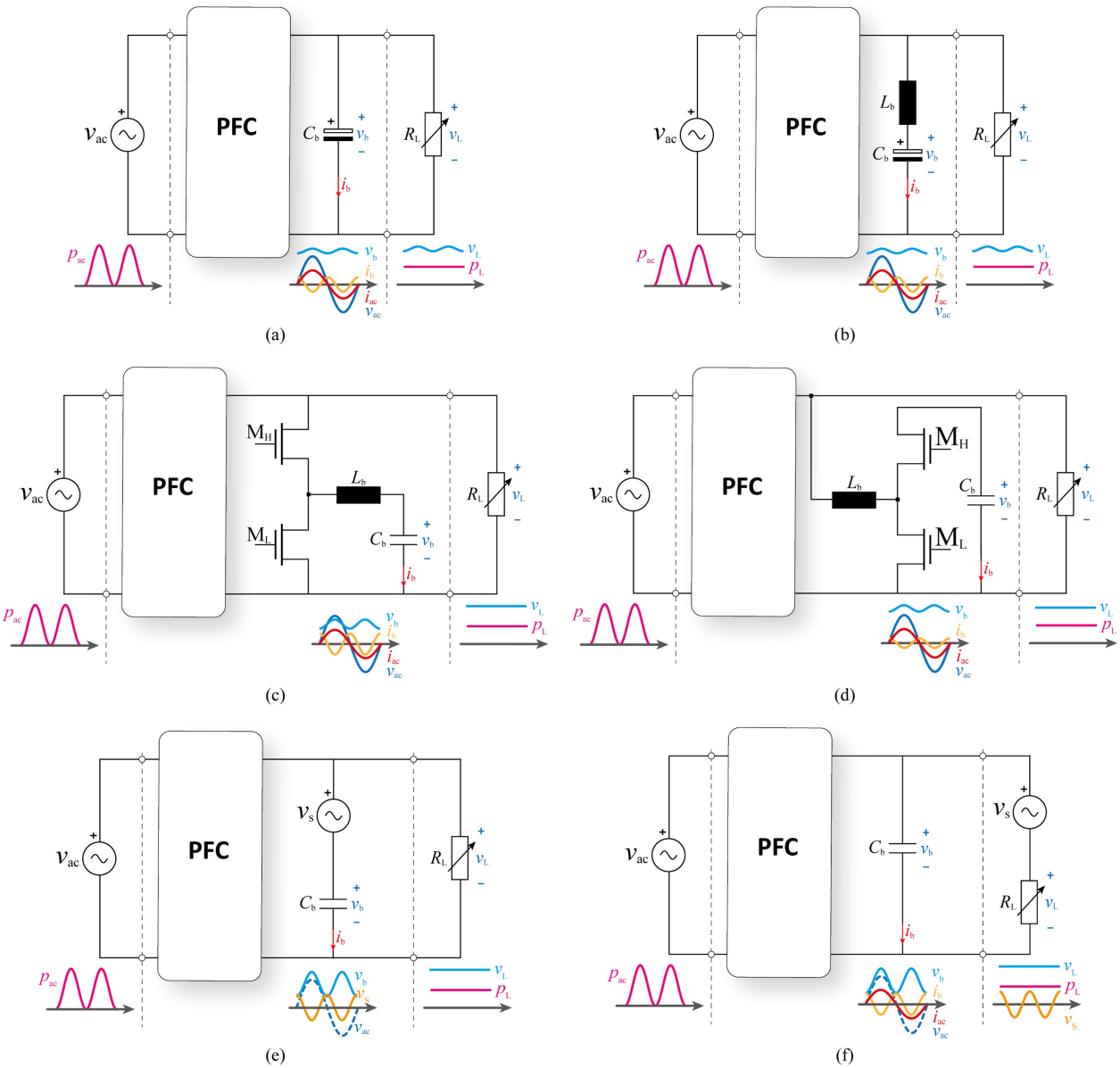

FIGURE 2. Dc-link architectures: passive dc-link using a high-ripple high-capacitance filter (a) and resonant tank filter (b); active current-source PPB using buck (c) and boost (d) configurations; and active voltage-source PPB in capacitor-series (e) and load-series (f) configurations. The resistive load, R_L, models the dc-dc converter and the battery load.

This paper deals with the charging system, focusing on the on-board charger (OBC). OBCs are connected to the mains, either in single-phase or three-phase configuration [10], [11], for recharging the main EV battery and they are typically composed of a PFC block plus a dc-dc converter block that supplies the high voltage battery to be charged (Fig. 1(b)). In the past, many different converter topologies have been proposed and analyzed [3], [12], including single and multi-phase solutions, unidirectional and bidirectional implementations, standard and totem-pole rectification strategies, and resonant, multi-level and dual-active-bridge dc-dc implementations. In all these designs and studies, the dc-link capacitor is identified as a bottle-neck element that limits the reliability of the converter by decreasing the mean time between failures (MTBF) figure of merit and degrades significantly the converter power density. For these reasons, the main contribution of this paper is the proposal of an OBC topology featuring a power pulsating buffer structure that will enable improving the converter performance, reliability and power density [13], as well as the analytical derivation of the proposed structure and capacitor technology analysis.

Nowadays, most of the dc-link implementation use passive approaches using a single dc-link capacitor (Fig. 2(a)), requiring large values, or resonant structures (Fig. 2(b)), which limits the converter operation ranges. In spite of this, significant efforts have been made in the study and optimization of the dc-link capacitor [14]. Advanced dc-link structures for improvements in photovoltaic applications have been reported

in [15], including also a 200-W inverter to remove dc-link capacitor [16], or several 2-kW inverters developed in the context of the Google Little Box challenge [17], [18]. A 1-kW split-capacitor improved power decoupling circuit is detailed in [19]. In [20], a design with special emphasis in the magnetic component optimization for improved power density is proposed.

Power pulsating buffers (PPB) has been identified also as a promising technique to alleviate dc-link capacitor requirements as well as to increase the converter performance and improve efficiency due to partial power processing [21], [22]. These structures can be classified into current-source implementations (Fig. 2(c) and (d)) and voltage-source implementations ((Fig. 2(e) and (f)), with significant variations in their required device ratings and control schemes. These structures are located usually after the PFC so they must only block positive voltages and standard unipolar transistor technology can be used. In the past, several PPB converters have been applied to grid-interfaced applications with significant dc-link capacitor reduction [23], [24], and a detailed study of the influence of the capacitor technology is presented in [25]. All these proposals enable reducing the dc-link capacitor, increasing significantly the final achieved power density.

This paper aims at proposing an OBC topology featuring a PPB that will enable addressing some of the most significant challenges in EV regarding power density and maximum operative hours. The proposed topology is based on a totem-pole rectifier plus a dual-active-bridge dc-dc converter, whereas a buck-type PPB ensures smooth dc-link voltage with a significantly reduced dc-link capacitor. The proposed buck-type structure enables a significant gain in power density, since the capacitor voltage can vary from 0 to the dc-link bus voltage, enabling a better use of the stored energy. This will enable not only a significant improvement in power density, but also the transition to other capacitor technologies with extended lifetime compared with the currently used electrolytic technology. This proposal opens the design window to new scenarios enabling the optimization of power density, by using capacitor technology, lifetime, by using film capacitor technology, or a mixed scenario with cost-effective implementation using high-ripple electrolytic capacitor technology.

The remainder of this paper is organized as follows. Section II details the proposed power converter topology, analyzes the operation of the power pulsating buffer, and details the proposed control scheme. Section III presents the implementation and experimental results, detailing the converter design procedure, the experimental setup and the main experimental results at different power levels and with different dc-link bus capacitor technologies. Finally, the conclusions of this paper are drawn in Section IV.

II. PROPOSED PPB CONVERTER

A. PPB TOPOLOGY DESCRIPTION

Classical power conversion architectures for OBCs are based on the use of a rectifier PFC plus a dc-dc converter to adapt the output voltage/current to the battery status (Fig. 1(b)). In these converters, a high value dc-link capacitor, C_b, is usually required to ensure that no low-frequency ripple is present at the battery while ensuring sinusoidal input current consumption. This capacitor not only impacts the converter power density, but his required value also implies the use of electrolytic technology, degrading significantly the maximum converter operating hours. This is limiting element that prevents the use of such technology in future EV systems.

The proposed power converter topology is depicted in Fig. 3. It is composed of a PFC totem pole rectifier PFC plus a dual-active-bridge dc-dc converter. This paper proposes the use the power pulsating buffer described in Fig. 2(c) in order to address the aforementioned limitations of current OBC technology. The proposed PPB structure follows a buck-type structure, and it is composed of a half-bridge branch, M_H, M_L, and the reactive components L_r, C_b. Thus, the proposed structure injects the required bus current to ensure that the output current i_L contains no low-frequency ripple, ensuring smooth battery operation.

The main benefit of the proposed converter is the significant reduction of the dc-link capacitor which leads not only to a significantly improved power density, but also to an increase in the lifetime due to the switch in the proposed capacitor technology. Besides, this structure benefits from partial power processing at the PPB, positively impacting the converter efficiency, and a low-ripple dc-link voltage, ensuring the smooth battery operation and simplifying the dc-dc converter design and control. To illustrate the potential benefits of the proposed architecture, Fig. 4 compares the main waveforms for a 3.6-kW OBC using the standard architecture (a) and the proposed PPB architecture (b). The proposed topology achieves smoother dc-link voltage while reducing the required capacitor from 1500 μF to 220 μF. The following lines details the analysis of the proposed structure that will enable its design and optimization. Fig. 5 compares the classical design using an electrolytic capacitor decoupled dc-link versus the proposed PBB design, considering capacitor voltage, voltage ripple and current. In this design, it can be seen that the proposed design significantly reduces the required capacitance by increasing the voltage ripple in the capacitor, providing a better usage of the energy stored in it.

B. ANALYSIS AND DESIGN CONSIDERATIONS

This subsection provides an analytical description of the proposed PPB architecture, enabling obtaining the main waveforms for design and analysis purposes. In order to perform the analysis of the proposed converter, the following hypothesis are established:

1) Sinusoidal mains input current and voltage, that can be defined by the rms voltage, $V_{ac,rms}$, the rms current, $I_{ac,rms}$, and their frequency, f_{ac}.
2) Unity input power factor ($PF = 1$). Consequently, the mains input power consumption, P_{ac}, can be calculated as $P_{ac} = V_{ac,rms} \cdot I_{ac,rms}$.

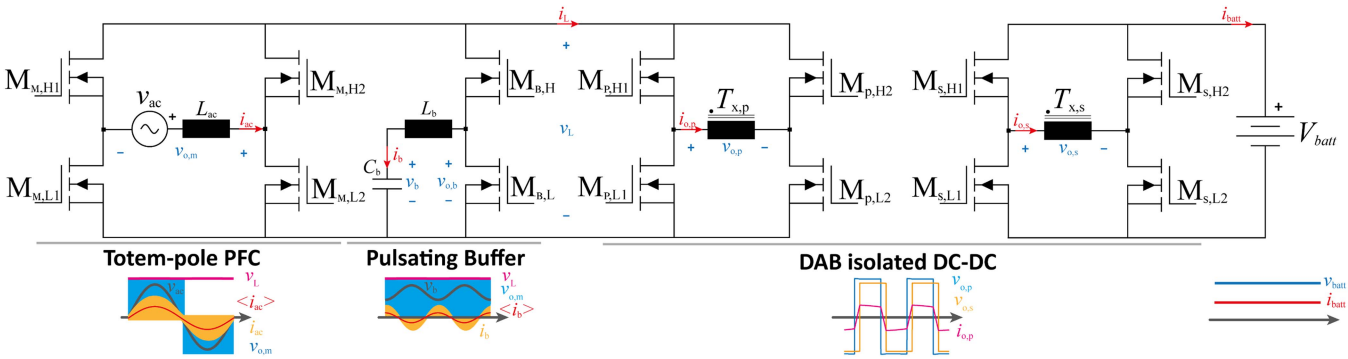

FIGURE 3. Proposed converter topology: PFC and power pulsating buffer.

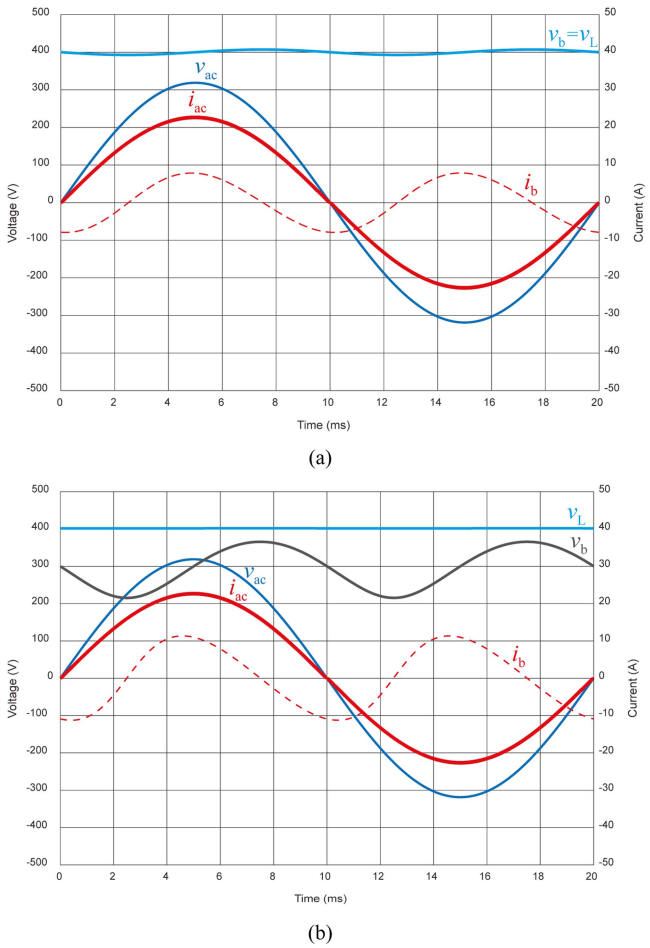

FIGURE 4. Main waveforms of a classical OBC architecture featuring a 1500 μF dc-link capacitor (a) and the proposed buck-type PPB-based architecture with 220 μF PPB capacitor (b).

3) Constant output power, P_o, defined by the converter efficiency as $P_o = \eta P_{ac}$.
4) Ideal lossless PPB converter operation.

Hypotheses (1) and (2) are valid as long as the PFC operates properly, whereas hypothesis (3) is valid for normal slow-varying battery operation and (4) is valid if the converter efficiency is high enough. Assuming this initial hypothesis, the following PPB parameters are defined, including the PPB

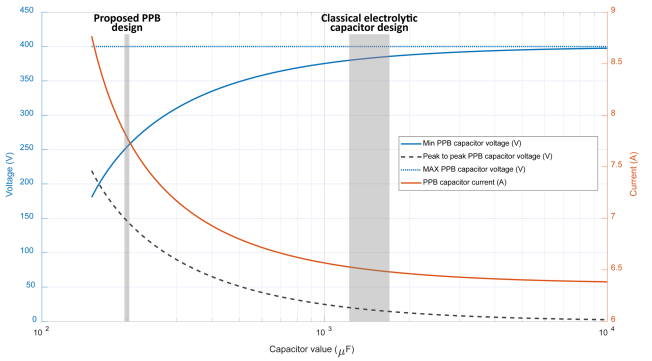

FIGURE 5. Proposed design vs classicl approach. Voltage and current vs capacitor value for 3600 W and 60 Hz.

energy storage capacitor, C_b, its voltage, v_b, and current, i_b. and the following associated values: initial pulsating capacitor voltage, V_b (0), average PPB voltage, V_b, minimum PPB voltage, $V_{b,min}$, maximum PPB voltage, $V_{b,max}$, and rms PPB voltage, $V_{b,rms}$.

Under these conditions, and using the detailed definition, the proposed PPB structure can be analyzed as follows. The sum of the output power, i.e., the consumed mains power and the processed PB power, P_b, should be zero to guarantee the energy conservation principle. Those instantaneous powers can be defined as respectively. Consequently, the power processed by the PPB is:

$$p_{ac}(t) = 2V_{ac,rms}I_{ac,rms}\sin^2(\omega_{ac}t) = 2P_{ac}\sin^2(\omega_{ac}t), \quad (1)$$

$$p_o(t) = P_o = \eta P_{ac}, \quad (2)$$

$$p_b(t) = \eta p_{ac}(t) - p_o(t) = \eta P_{ac}\left(2\sin^2(\omega_{ac}t) - 1\right). \quad (3)$$

The PB processed power can also be expressed as a function of the PBB capacitor voltage and current as

$$p_b(t) = \eta P_{ac}\left(2\sin^2(\omega_{ac}t) - 1\right) = v_b(t)\cdot i_b(t), \quad (4)$$

where the PBB capacitor current can be expressed as

$$i_b(t) = C_b\frac{dv_b(t)}{dt}. \quad (5)$$

By combining the previous equations, the PBB instantaneous power can be expressed as

$$p_b(t) = P_{ac}\left(2\sin^2(\omega_{ac}t) - \eta\right) = v_b(t)\cdot C_b\frac{dv_b(t)}{dt}. \quad (6)$$

The first order ODE of the previous expression can be solved by applying separation of variables and direct integration, yielding

$$\frac{v_b^2(t)}{2} = \frac{-\eta P_{ac}\sin(2\omega_{ac}t)}{2\omega_{ac}C_b} + c_1. \quad (7)$$

From which the PBB capacitor voltage can be expressed as

$$v_b(t) = \sqrt{2c_1 - \frac{\eta P_{ac}}{C_b\omega_{ac}}\sin(2\omega_{ac}t)}. \quad (8)$$

where only the positive solution has been considered. From this expression, the PPB capacitor rms value can be obtained, yielding,

$$V_{b,rms} = \sqrt{\frac{2\pi}{\omega_{ac}}\int_0^{\frac{2\pi}{\omega_{ac}}}(v_b(t))^2dt} = \sqrt{2c_1}, \quad (9)$$

Consequently, $c_1 = V_{b,rms}^2/2$. and, as a result, (8) can be expressed as

$$v_b(t) = \sqrt{V_{b,rms}^2 - \frac{\eta P_{ac}}{C_b\omega_{ac}}\sin(2\omega_{ac}t)}. \quad (10)$$

The average PB capacitor voltage, V_b, can be obtained by integrating the instantaneous capacitor voltage as follows

$$V_b = \frac{\omega_{ac}}{2\pi}\int_{\frac{2\pi}{\omega_{ac}}} v_b(t)dt = \frac{V_{b,rms}}{\pi}\sqrt{1-\frac{1}{\sigma_1}}\cdot \left[E\left(\frac{\pi}{4},\frac{2}{1-\sigma_1}\right) - E\left(-\frac{3\pi}{4},\frac{2}{1-\sigma_1}\right)\right],$$
$$\sigma_1 = V_{b,rms}^2\left(\frac{C_b\omega_{ac}}{\eta P_{ac}}\right), \quad (11)$$

where the elliptic integral of the second kind is required,

$$E(\phi,k) = \int_0^{\phi}\sqrt{1-k^2\sin^2(\theta)}d\theta. \quad (12)$$

From (10), the following additional parameters can be derived as a function of the dc-link voltage V_L:

$$V_b(0) = V_{b,rms}, \quad (13)$$

$$V_{b,\max} = \sqrt{V_{b,rms}^2 + \frac{\eta P_{ac}}{C_b\omega_{ac}}} < V_L, \quad (14)$$

$$V_{b,\min} = \sqrt{V_{b,rms}^2 - \frac{\eta P_{ac}}{C_b\omega_{ac}}} > 0. \quad (15)$$

It is important to note that the capacitor bus voltage must be within the ranges established in these equations. Consequently, from (14) and (15), the following constraint for the minimum required capacitor is obtained

$$C_b \geq C_{b,\min} = \frac{2\eta P_{ac}}{V_L^2 C_b\omega_{ac}}. \quad (16)$$

Finally, at this point, the current of the PPB capacitor can be easily obtained as

$$i_b(t) = C_b\frac{dv_b(t)}{dt} = -\eta P_{ac}\frac{\cos(2\omega_{ac}t)}{v_b(t)} = -\eta P_{ac}\frac{\cos(2\omega_{ac}t)}{\sqrt{V_{b,rms}^2 - \frac{\eta P_{ac}}{C_b\omega_{ac}}\sin(2\omega_{ac}t)}}. \quad (17)$$

Finally, in order to select the proper PPB inductor L_b, the following considerations are taken. It is designed to operate above the resonant frequency to operate in the inductive region under zero voltage switching conditions. Besides, the resonant frequency must be above the mains frequency that it is intended to be filtered.

In order to guarantee critical conduction mode to minimize switching losses, the maximum PPB inductor value result

$$L_{b,CrCM} \leq \min\left[\frac{V_L - v_b(t)}{2|i_b(t)|f_{sw,\min}}\frac{v_b(t)}{V_L}\right]. \quad (18)$$

In order to test the accuracy of the proposed analytical model, both Spice simulation and analytical results have been plotted in Fig. 6. In this figure, the voltage ripple in the PBB capacitor as well as the current ripple are represented. These values are used for design purposes, and clearly shows how the proposed PBB structure achieves a better usage of the energy stored in the capacitor by allowing a certain amount of voltage ripple. This figure validates the proposed analytical model, that will be later used in the converter design.

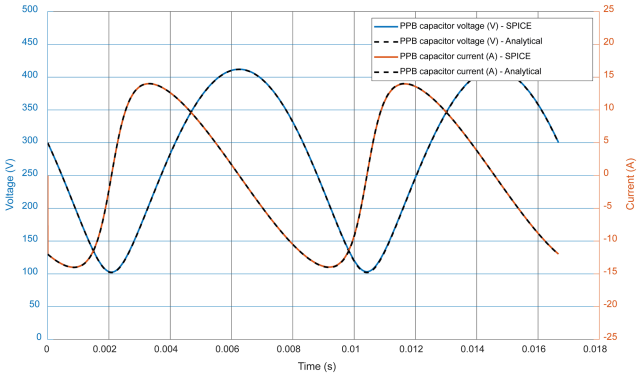

FIGURE 6. Minimum PPB capacitor as a function of the peak voltage for a 60-Hz mains grid using 120 μF, 3600 W and 60 Hz.

III. IMPLEMENTATION AND EXPERIMENTAL RESULTS

In order to prove the feasibility of the proposed PPB architecture, an experimental prototype has been designed and implemented containing the PFC, PPB and DAB converters that form the complete OBC architecture. Table 1 summarizes

TABLE 1. Prototype Main Parameters and Comparison

Parameters	Design		
	Proposed	*State of the Art 1* [26]	*State of the Art 2* [27]
Switching frequency	- AC/DC & PPB: 100-500 kHz (CrCM) - DC/DC (DAB): 100 kHz	- AC/DC: 67 kHz (CCM) - DC/DC (CLLC): 148-300 kHz	- AC/DC:70 kHz (CCM) - DC/DC (LLC): 92-250 kHz
Power devices	- AC/DC & PPB: 65HR77DS1 (77 mΩ, 650 V, Si SJ MOSFETs) - DC/DC: 65HR77DS1 (77 mΩ, 650 V, Si SJ MOSFETs)	- AC/DC: E3M0060065K (60 mΩ, 650 V, SiC MOSFETs) - DC/DC: E3M0060065K (60 mΩ, 650 V, SiC MOSFETs)	- AC/DC: SCTH35N65G2V-7AG (55 mΩ, 650 V, SiC MOSFETs) - DC/DC: STB47N60DM6AG (70 mΩ, 650 V, Si SJ MOSFETs)
PFC inductor	22 µH, PQ32 core (3C97), litz wire: 800x50µm (CrCM)	Not declared. CCM	2x514 µH (CCM)
Capacitor bank	Ceramic: 286x2.2 µF/450 V (21 cm3)	Electrolytic: 10x180 µF/450 V (105 cm3)	Electrolytic: 5x560 µF/450 V (192 cm3)
DC-DC tank	DAB. Single magnetic component: PQ50/50 (3C97).	CLLC. 2x9 µH inductor+ 20x6.8 nF resonant capacitor, PQ50/40 transformer core.	LLC. 2x16.8 µH inductor, 4x633 nF resonant cap, 2xTransformer cores (not declared).
Power density	5.4 kW/l without magnetics, 4.2 kW/l including magnetics. Power: 3.6 kW.	3.3 kW/l. Heatsink not included. Power 6.6 kW.	1.2 kW/l. Heatsink not included. Power 7.0 kW.

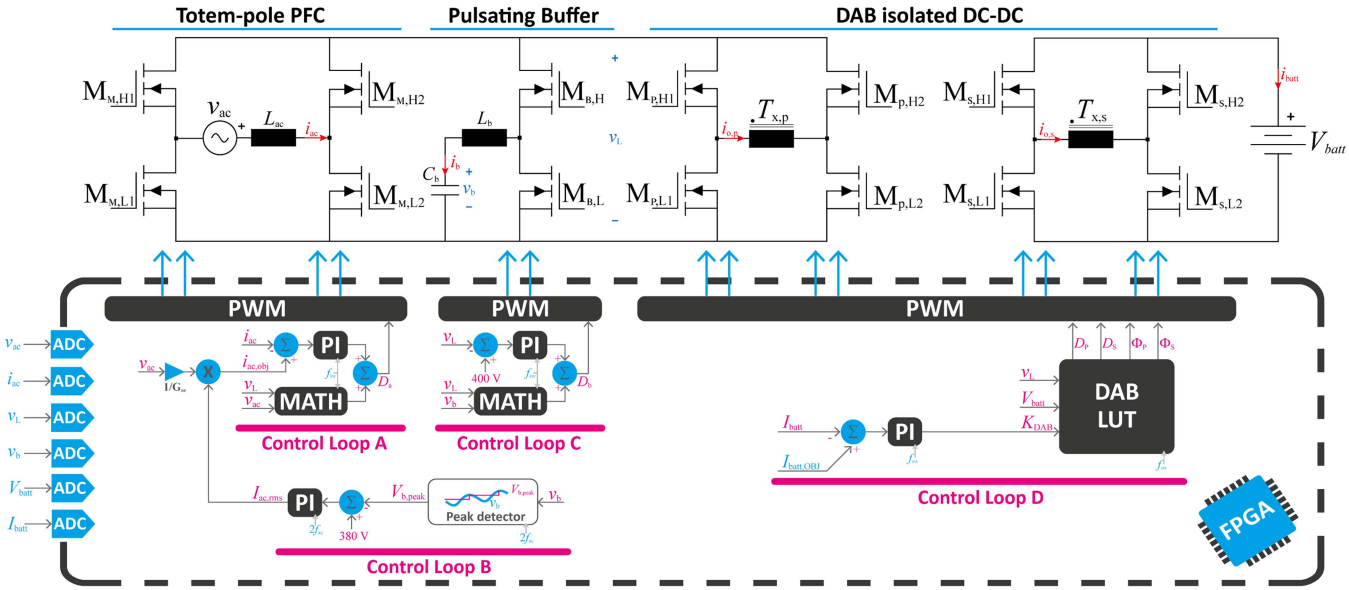

FIGURE 7. Proposed power converter control architecture.

the main prototype parameters and compares it with state-of-the-art implementations. The next lines detail the main design considerations and experimental results.

The implemented PBB-based OBC topology is shown in Fig. 7. It is based on a totem-pole PFC rectifier converter plus a dual-active-bridge dc-dc converter. The PBB replaces the classical dc-link capacitor, enabling a higher power density and lower voltage ripple implementation. It is important to remark that both PFC and PBB are operated in critical conduction mode to achieve soft-switching conditions and high efficiency operation. Besides, that allows for efficient and cost-effective operation using silicon super junction devices.

The proposed control strategy is detailed in Fig. 7, where considering a constant battery current scenario, four different control loops (A-D) are required for the proper operation of the OBC. Starting from the mains side, *Control Loop A* ensures proper mains current consumption, in phase with the mains voltage, to guarantee a power factor close to one. The required duty cycle, D_a, is the result of a simple mathematical operation and a PI controller to ensure zero steady-state current error. The magnitude of the current is determined by the required mains rms current level, $I_{ac,rms}$, which is obtained in *Control Loop B*. This current level is calculated by computing the peak PB capacitor voltage twice per mains cycle and comparing it with the required peak voltage, $V_{b,peak}$. A PI controller is employed to maintain the proper PPB peak voltage level.

To ensure the proper operation of the PB stage, *Control Loop C* uses the instantaneous PB capacitor voltage, v_b, and v_L to maintain a constant dc-link voltage level through a

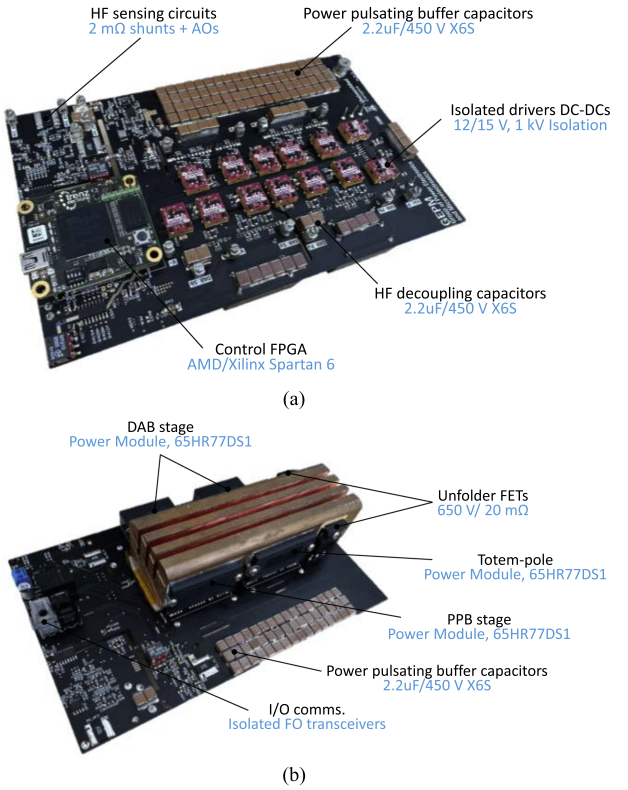

FIGURE 8. **Experimental prototype containing PFC, PPB and DAB converters: (a) top view and (b) bottom view. Dimensions 187x114x31 mm. Power density: 54 kW/l without magnetics and 42 kW/l including magnetics.**

straightforward mathematical operation and a PI controller. The output of this control loop determines the duty cycle applied to the half-bridge of the PPB stage. Lastly, to ensure a constant battery current, a dedicated PI controller is used to determine the required gain for the Look-Up Table (LUT) employed to control the DAB converter in *Control Loop D*.

Fig. 8 shows the top and bottom views of the proposed converter. It has been implemented using 65HR77DS1 power devices. 22-μH inductors are implemented using PQ32/30, 3C97 cores and 800 $\times$ 71 μm Litz wire. DAB transformer is implemented using PQ50/50 core and the same Litz wire. The designed prototype can use the three capacitor technologies using either external connectors or on-board SMD ceramic capacitors.

As it has been previously discussed along the paper, one of the key elements defining the final converter performance and reliability is the employed capacitor technology. Since the proposed architecture enables a significant reduction of the required capacitance, several capacitor technologies have been tested (Fig. 9): 200-μF electrolytic technology, 230-μF film technology, and 572-μF ceramic X6S technology. These values have been measured using a precision Keysight E4980AL LCR meter for accurate characterization. It is important to remark that the value of the ceramic capacitor has been selected to compensate its dependence with the operating voltage, since its capacitance is reduced for higher

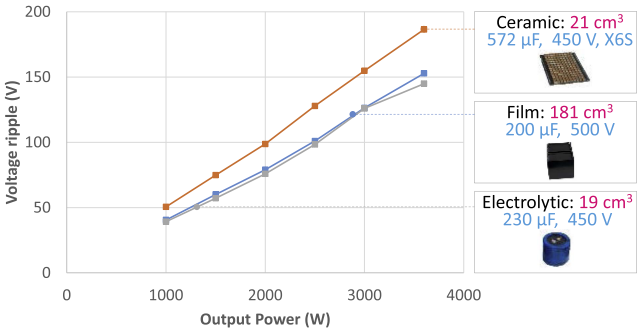

FIGURE 9. **Capacitor technology comparisson: Ceramic capacitor technology (X6S dielectric), film capacitor and electrolytic capacitor, including equivalent capacitor bank volume.**

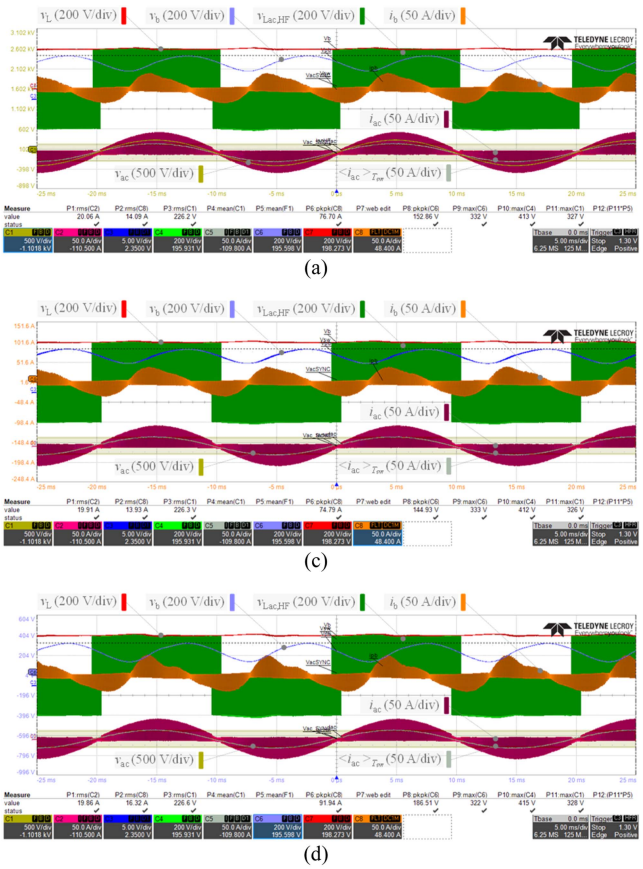

FIGURE 10. **Capacitor technology comparisson at maximum output power (3600 W), and a target peak capacitor voltage of $V_{b,peak}$=330 V. Constant dc-link voltage, V_L=400 V. Different capcitor technology performance comparisson: (a) 200 μF film capacitor, $V_{b,pp}$=152 V, (b) 230 μF electrolytic capacitor, $V_{b,pp}$=144 V, and (c) 572 μF ceramic X6S capacitor, $V_{b,pp}$=186 V. From top to bottom: Dc-link voltage (C7), pulsating buffer capacitor voltage (C6) and current (C8), mains input current (C2) and voltage (C1).**

operating voltages. Fig. 9 shows the PBB voltage ripple as a function of the output voltage, whereas Fig. 10 shows the main experimental waveforms at maximum output power for the three selected capacitor technologies. These results prove the proposer converter operation, and its ability to operate with different capacitor technologies. Besides, it is proved that electrolytic capacitors can be replaced by film capacitors

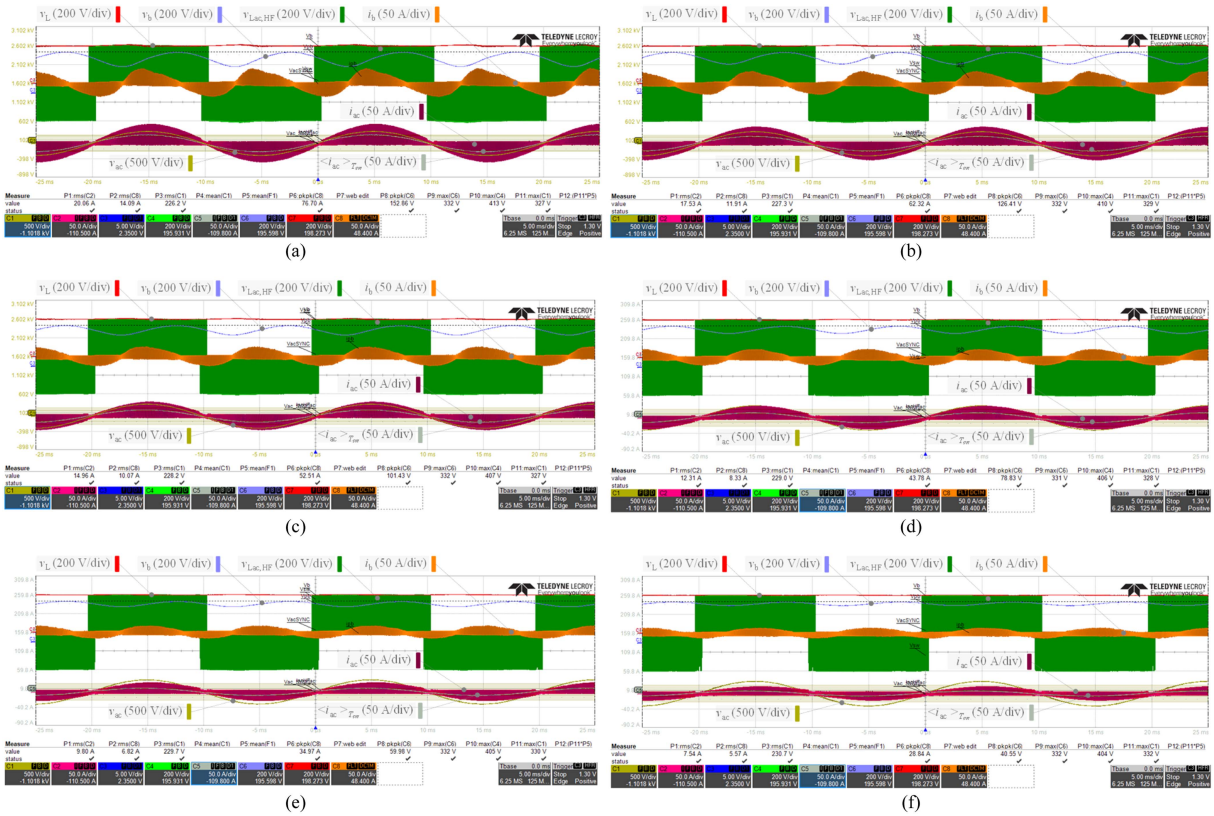

FIGURE 11. Main waveforms of the proposed converter operating at 400 V output voltage with 200 μF PBB capacitor and 330 V peak PBB capacitor voltage: (a) 3600 W, (b) 3000 W, (c) 2500 W, (d) 2000 W, (e) 1500 W, (f) 1000W. From top to bottom: Output voltage (C7), PBB capacitor voltage (C6) and current (C8), mains input current (C2) and voltage (C1).

in order to achieve a higher reliability converter. Ceramic capacitors can be implemented to obtain a higher performance and power density implementation. However, due the nature of the application in which the voltage in the PBB capacitor oscillates, it requires selecting a significantly higher value, leading to higher cost. For these reasons, film technology will be selected for the final implementation. It must be noted that considering the measured current and the power device characteristics, the efficiency penalty of the added PPB block is under 1% in the complete operating range, justifying the proposed architecture.

Finally, Fig. 11 shows the main experimental waveforms using film technology PBB capacitor in the complete output power range from 1000 W up to 3600 W. The higher the output voltage, the higher the PBB voltage ripple, which is kept in under the selected peak value. These results prove the correct converter operation under all the required output power range, proving the feasibility of the proposed converter. It is remarkable that when comparing the proposed design with state-of-the-art reference design from some of the main manufacturers (Table 1), e.g., Wolfspeed [26] or ST [27], the proposed architecture achieves a significant improvement in power density. Furthermore, the same benefit can be obtained using ceramic capacitor technology or, by keeping the similar power density, lifetime can be much increased by using film capacitors.

IV. CONCLUSION

This article has proposed an OBC charter architecture taking advantage of a power pulsating buffer stage to achieve higher performance and higher power density. The proposed converter has been analyzed, and an experimental prototype has been designed and built. The proposed converter has enabled the use of alternative capacitor technologies, enabling a significant improvement not only of power density, but also reliability and operative time. Experimental results have proved the proper converter operation, making the proposed OBC architecture a promising alternative for future higher power density EVs.

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