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Extension of the Stray Voltage Capture Short-Circuit Detection Method to a 6-Phase Fault-Tolerant Dual-Motor Drive

MUSTAPHA AL SAKKA [1,2] (Student Member, IEEE), FARZAD HOSSEINABADI [1,2] (Graduate Student Member, IEEE), THOMAS GEURY [1,2] (Member, IEEE), MOHAMED EL BAGHDADI [1,2] (Member, IEEE), MONZER AL SAKKA [3], AND OMAR HEGAZY [1,2] (Member, IEEE)

[1]MOBI-EPOWERS Research Group, ETEC Department, Vrije Universiteit Brussel, 1050 Brussels, Belgium
[2]Flanders Make, 3001 Heverlee, Belgium
[3]Tenneco Automotive Europe, 3800 Sint-Truiden, Belgium

CORRESPONDING AUTHOR: OMAR HEGAZY (e-mail: omar.hegazy@vub.be)

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ABSTRACT This article investigates and validates the applicability of the recently developed stray voltage capture (SVC) ultra-fast short-circuit (SC) detection method and its extended version (ESVC) to fault-tolerant multi-motor drives. As these methods are system-based, a fault localization algorithm is also developed. Simulation analysis of the inverter stray inductances shows additional challenges for the SVC method making it hard to achieve ultra-fast SC detection. The ESVC method is slower but overcomes these challenges. The methods are adapted for a 400 V 6-phase Silicon Carbide based inverter equipped with a 2-level turn-Off hardware protection scheme. Fault under load and hard switching fault tests are performed showing the effectiveness of the ESVC in fast (smaller than 330 ns) and reliable SC detection and protection for SiC MOSFETs. The fault localization algorithm is also validated showing a localization speed smaller than 20 μs.

INDEX TERMS Motor drives, fault tolerance, short-circuit protection, multi-motor, multiport inverters.

I. INTRODUCTION

As the trends of vehicle electrification and autonomous driving continue to grow, the use of electric motor drives in vehicles is becoming more prevalent, not only for traction, but also for braking, steering and suspension. In each application multiple motors are used either due to a distributed architecture (1 motor per corner or axle) or a modular motor design. Additionally, research advancements on multi-phase machines may increase their use in vehicular applications [1]. Multiport and multi-phase motor drives are characterized with improved cost, size, reliability, and fault-tolerance abilities compared to a conventional solution of a separate drive for each motor [2], thus, making them an attractive solution for these applications.

A crucial drawback of using electric motor drives is their high failure rate compared to mechanical systems, mainly due to the semiconductor switches faults of the power inverter [3]. While open-circuit faults are typically detected by software, short-circuit (SC) faults are more critical and must be dealt with quickly, hence, hardware SC detection and protection circuits are typically employed [4]. The most common SC detection methods are *Desaturation*, *Shunt Resistor* and *Current Mirror* [5]. The *Shunt Resistor* method directly measures the switch current; it is simple but suffers from high power loss. The *Current Mirror* method overcomes the power loss issue by scaling down the sensed current but requires expensive switches featuring a sense pin. The *Desaturation* method relies on monitoring the switch voltage and trips when the switch saturation voltage exceeds a threshold value, a blanking time is required to prevent false triggers during turn-On. It is best suited for IGBTs but for MOSFETs the desaturation circuit design is challenging due to their high transition voltage, fast switching speed and small SC withstand time [5]. Modified versions of the desaturation as well

as other types of detection methods exist but one common feature of all these methods is that they are all device-based [6], hence, each switch requires a detection circuit.

For multiport and multi-phase drives, the high number of switches equates to a high number of device-based detection circuits with multiple components each, which hinders reliability and may increase cost. Moreover, to retain the fault location, each detection circuit must communicate the fault to the controller either directly or through an encoder IC thus increasing the design complexity and size (e.g., 12 digital connections for a 6-phase drive). Therefore, a system-based approach where only 1 detection circuit is used for the whole drive is beneficial for multiport and multi-phase drives. One such method is the stray voltage capture (SVC) proposed in [7]. This method detects voltage dips in the DC link induced by a SC due to stray inductance. The method was tested on a 48 V half-bridge and proved to be quite fast and suitable for Silicon SiC MOSFET protection. However, when applied to a multi-phase drive each added inverter leg adds more inductance in the SC current path therefore the SVC behavior will depend on the fault location and tuning the circuit response becomes challenging. Although the SVC was already proposed for a 3-phase GaN drive in [8], the added inductance problem is not addressed and only simulation results for one leg are provided. Another problem for the SVC in the case of multi-phase drives is that the fault location is not inherently known, thus, a fault localization algorithm is needed, which increases the implementation effort. A flowchart of such an algorithm was given in [8], but the algorithm is risky as it requires 2 intentional SC events to localize the fault and is not simulated nor experimentally validated yet.

In this article the SVC is implemented on a 400 V 6-phase SiC-based dual-motor drive. Firstly, the effect of added inductance is investigated by simulation and experiment and the suitability of both SVC and ESVC for multiphase drives is assessed. Secondly, the fault localization algorithm is developed in detail, improved by reducing the number of intentional SC to only 1 and validated experimentally, thus, verifying the viability of the SVC method for fault-tolerance and not only protection. Additionally, a 2-level turn-Off protection scheme is implemented to reduce the voltage stress on the MOSFETs during SC events and the fault localization process. The article also covers various practical details useful for the SVC implementation and the realization of a fault-tolerant motor drive system. The article is composed of 4 main sections and structured as follows. In Section II the SVC method is reviewed and extended to a 6-phase inverter, in Section III the fault localization algorithm is detailed, Section IV illustrates the prototype and its features, finally, in Section V experimental results are provided and analyzed.

II. SVC EXTENSION TO MULTI-PHASE DRIVES

A. REVIEW OF THE SVC METHOD

The schematic of the SVC circuit as first proposed in [7] is shown in Fig. 1 (SVC frame). The circuit is placed across the

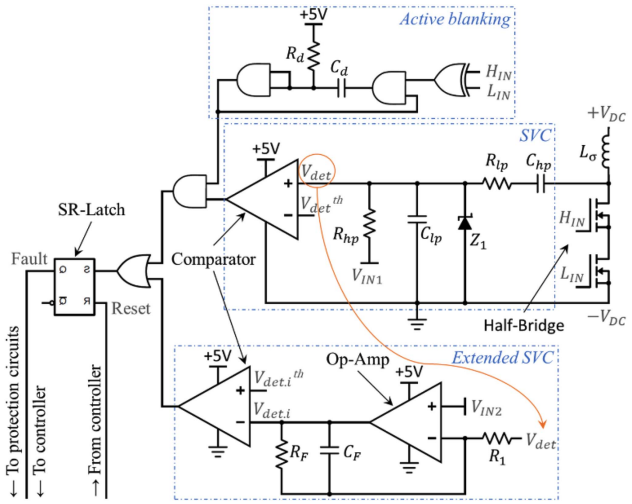

FIGURE 1. Combined SVC schematic as provided in [9].

Half-Bridge (HB) and monitors the DC link voltage minus the voltage across the stray inductance L_σ. At the initial moment of a SC, the current through a MOSFET rapidly increases in the linear region but slows down as it approaches saturation. The initial current inrush through L_σ causes voltage to rapidly develop across L_σ which is seen by the SVC as a sharp dip in the voltage and utilized for ultra-fast SC detection (<100 ns). The measured voltage is filtered by a high-pass and a low-pass filter RC network composed of (R_{hp}, C_{hp}) and (R_{lp}, C_{lp}), respectively. The RC network works somewhat like a band-pass filter where the siganl is attenuated in the frequencies between the low- and high-pass cutoff frequencies but much more attnuated outside of it. The filtering removes the DC component, thus, the filtered voltage V_{det} is biased by a voltage V_{IN1} and compared with a threshold voltge V_{det}^{th}. A Zener diode Z_1 is added to protect the circuit from overvoltage. The analysis in [7] uncovers some limitations for the SVC method; firstly, lowering the cutoff frequency of the low-pass filter results in comparator overvoltage and false triggers due to hard switching but raising the frequency increases the minimum L_σ required for detection, thus, a compromise is needed. Secondly, high values of L_σ make it hard to distinguish between SCs and hard switching transients. Finally, a reduction in the DC link voltage (e.g., when a battery discharges) reduces the amplitude of the voltage drop which may prevent the SVC from detecting SCs.

Solutions to these limitations are proposed in [7] and assessed in [9]. For false triggers an active blanking circuit shown in Fig. 1 (Active Blanking frame) is added to disable the SVC during switching transients and enable fast detection. An extended SVC (ESVC) method is also proposed as shown in Fig. 1 (Extended SVC frame), where V_{det} is integrated and the resultant voltage $V_{det.i}$ is compared with a threshold voltage $V_{det.i}^{th}$. The ESVC takes advantage of the fact that the MOSFET current keeps increasing during the first few microseconds of a SC [10], thus the voltage dip and integrator output keeps increasing while for a hard switching transient,

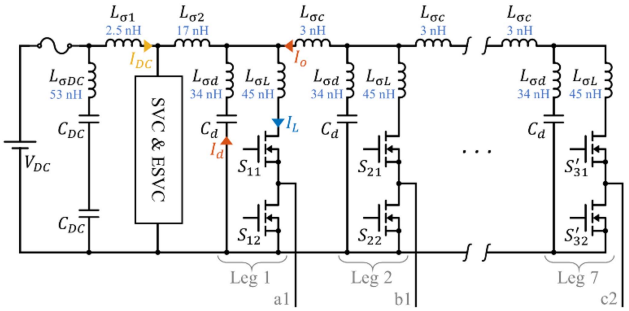

FIGURE 2. Stray inductances of the inverter prototype.

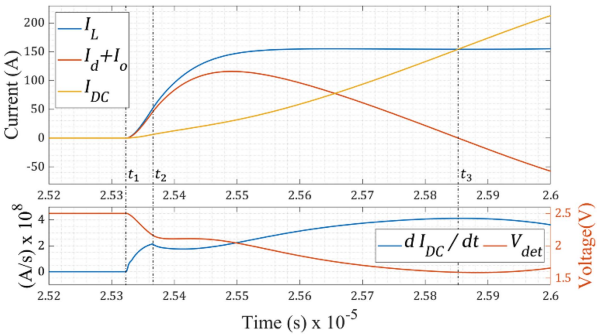

FIGURE 3. Simulated waveforms of a SC event in Leg 1.

the voltage oscillations dissipate faster. ESVC is slower than SVC but is more reliable in detecting SCs. Although not consiered in [9], ESVC may be able to deal with the reduced DC link voltage limitation as the reduced voltage drop will be integrated and eventually detected. A combination of the solutions and the original SVC can be made [9], as can be seen in Fig. 1.

It is worth noting that the original illustrations of the ESVC in [7] and [9] show the same voltage referenceV_{IN1} used to biasV_{det} in SVC and fed to the non-inverting input of the Op-Amp in the ESVC, and since V_{det} is biased by the same voltageV_{IN1} and fed into the inverting input of the Op-Amp, the Op-Amp output $V_{det.i}$ will also be equal to V_{IN1} in steady state. To remedy this, another voltage reference $V_{IN2} = V_{IN1}(R_F/(R_F + R_1))$ that gives a 0 V value at the output must be used, where R_F and R_1 are the feedback and input resistors of the integrator, respectively. Additionally, the output of the integrator must be connected to the non-inverting input of the comparator. The ESVC shown in Fig. 1 is the corrected version.

B. APPLYING SVC TO A 6-PHASE INVERTER

The application of the SVC method to a multi-phase inverter was proposed in [8] for a 48 V 3-phase GaN electric drive. Compared to SiC, GaN MOSFETS have faster switching characteristics (higher di/dt) and lower power losses, however, they have a smaller SC withstand time and suffer from higher ringing during turn-Off [8]. With higher di/dt, the SVC detection time is automatically faster. The placement and sizing of the decoupling capacitor of the inverter legs is important for minimizing the hard-switching turn-Off transients which directly influences the performance of the SV. Thus, an in-depth analysis of the effects of the decoupling capacitor's capacitance, resistance, inductance, and placement on the PCB was provided. The performance of the SVC is validated as a detection and protection method where a protection time below 100 ns is achieved. However, only simulation results are provided on an unspecified leg and the effect of added inductance of each inverter leg is not considered.

In this article, a fault-tolerance 400 V, 6 kW, 6-phase SiC drive is considered. The layout of the inverter prototype considering relevant stray inductances is shown in Fig. 2. The inverter contains 7 legs as 1 leg (in the middle) is redundant. A decoupling capacitor C_d is placed across each leg and $L_{\sigma d}$ is the inductance of that connection. $L_{\sigma L}$ is the total inductance of each leg. $L_{\sigma c}$ is the inductance between every 2 consecutive legs. $L_{\sigma d}$, $L_{\sigma L}$ and $L_{\sigma c}$ are considered equal for all legs assuming an identical, repeating, and equidistant HB structure. $L_{\sigma DC}$ is the inductance of the DC link capacitor bank. The insertion of the SVC board between the DC link and the inverter legs divides the inductance in 2 parts $L_{\sigma 1}$ and $L_{\sigma 2}$. The values of all inductances shown in Fig. 2 are estimated based on the components datasheet and PCB layout using the Saturn PCB design Toolkit V8.31 and the online inductance calculators on "*emisoftware.com*". The relatively high value of $L_{\sigma 2}$ is due to the lack of a ground plane under that PCB section and the proximity of the SVC circuit to the DC link terminals.

The SVC can be seen as measuring the voltage across $L_{\sigma 1}$ and the DC link capacitor bank. The circuit of Fig. 2 is simulated in Matlab Simscape using non-ideal MOSFET and Gate driver blocks. A SC fault in Leg 1 is simulted by turning On switch S_{12} while S_{11} was already On with the output a1 not connected. The waveforms of currents I_L (Leg current), $I_d + I_o$ (decoupling capacitors currents), and I_{DC} (DC link current) as indicated on Fig. 2 are shown in Fig. 3.V_{det} and the time derivative of I_{DC} are also shown. Between t_1 and t_2 the majority of the initial inrush current is provided through the paths with least impedance, that is the decopling capacitor across the Leg 1 and other nearby decoupling capacitors. Although only a small portion is provided through the DC link capacitor bank due to its high impedance, its rate of change is high inducing a sharp dip in V_{det} allowing for the possibility of ultra-fast SC detection (<50 ns). Between t_2 and t_3 I_{DC} keeps increasing but at a lower rate and after a short plateau V_{det} continues to decrease giving another possibility for SC detection (<500 ns). After t_3 the SC current becomes fully supported by I_{DC} which also starts recharging the decoupling capacitors.

Compared to the single HB case examined in [7] and [9], the additional legs of a multi-phase drive accentuate the SVC limitations. This is because for Leg n, an additional stray inductance (n-1)$L_{\sigma c}$ is added between the SVC and the leg. Hence, the initial current inrush is further impeded and the amplitude of the voltage developed across $L_{\sigma 1}$ is reduced. The simulation of Fig. 3 is repeated for the remaing legs and the resulting V_{det} for each leg is shown in Fig. 4. As can be seen, the amplitude and steepness of initial voltage dip in V_{det} is

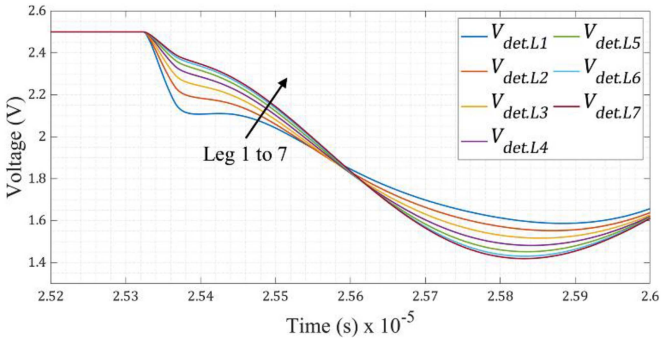

FIGURE 4. SVC response to SC in Leg 1 to 7.

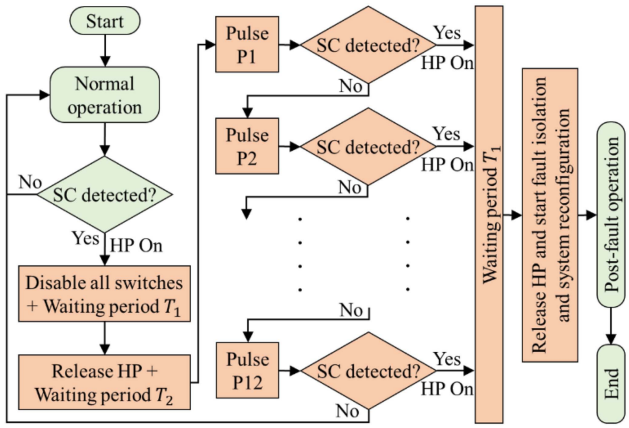

FIGURE 5. Flowchart of the fault localization algorithm.

significantly reduced with the added inductance. This hinders the ultra-fast SC detection ability of the SVC. The same effect can be expected for switching transient, thus, if V_{det}^{th} is set high enough for ultra-fast SC detection on Leg 7, it might be triggered by switching transients on Leg 1.

Eliminating false triggers due to switching tansients with a blanking circuit like that in Fig. 1 would not be suitable for a multi-phase drive since the SVC circuit would be blanked multiple times during a switching cycle and when one leg is in transient the other legs are generally not. Therefore, tuning the SVC to enable ultfa-fast SC detection in multi-phase drives is challenging and might not be possible depending on the component selection, the prototype design and PCB layout. A prototype design with circular symetry where the SVC circuit is palced at the center can solve the problem but such a design is unconventional. Fortunately, as V_{det} decreases again after the ultra-fast SC detection zone for all legs as can be seen in Fig. 4 SC can still be reliably detected. Implemeneting ESVC may accelerate the detection as $V_{det.i}$ would continue increasing in the plateau region of V_{det}, Thus ESVC is also examined in this article.

III. FAULT LOCALIZATION ALGORITHM

The SVC SC detection method is capable of fast short-circuit detection offering protection for wide bandgap semiconductor power devices. However, as it is a system-based method, the location of the faulty device is not inherently known. A complementary fault localization algorithm is needed. The original SVC authors provide a flowchart of a localization algorithm in [8], however, that algorithm is not simulated nor experimentally validated. The algorithm works as follows: after a SC is detected all switches are turned Off, then all upper switches are turned On simultaneously, if a SC is detected again, it signifies one of the lower switches is faulty. Thus, the upper switches are turned On again 1 by 1 until another SC is detected and the faulty switch is identified. If turning On the upper switches does not result in a SC, then the same process is repeated for lower switches. If no SC is detected, it signifies the fault was resolved or that it was a false trigger and normal operation is resumed. As this algorithm is unconventional and requires 2 intentional short-circuit events, a more detailed implementation and experimental validation are necessary.

In this article, using the same concept an improved fault localization algorithm is developed and experimentally validated. The simultaneous turning On of all upper or lower switches step is omitted, instead all switches are simply turned On with short pulses 1 by 1 until a SC is detected and the faulty switch is localized. The original method is seemingly faster in localizing the fault but requires 1 additional intentional SC which puts further stress on the drive. Moreover, in practice a SC occurrence and its elimination causes ripple in the DC link voltage (shown in Section V), a waiting period of a few microseconds must be reserved after each SC to prevent false triggers caused by the ripple. Hence, the additional SC of the original algorithm and the ripple it causes might eventually cost more time. Finally, as shown by simulation in [11], short differences in fault localization time are not critical for motor drive systems, thus, an algorithm with less SCs is preferable.

The flowchart of the proposed fault localization algorithm is shown in Fig. 5. When a SC occurs, hardware protection (HP) is immediately activated to safely eliminate the SC, and a fault signal is sent to the controller. The first step the controller does is turning Off all gating signals and it then waits for a period T_1 until the DC link voltage ripple settles down. Next, the HP is released and another waiting period T_2 is reserved to ensure the HP is fully released and proper operation of the gate drivers is restored. After that, pulses Pi (i from 1 to 12) of period T_p are sent to the switches 1 by 1 until a SC is detected. The HP method slowly turns Off the switch to prevent a voltage spike across it, thus the period T_p and duty cycle D_p of the pulse Pi must be set high enough to trigger a SC and to allow for the HP to be fully activated. The HP method is further detailed in Section IV. If a SC is detected again, the faulty switch is determined, and the controller waits for another period T_1 to prevent false triggers after which the HP is released, and the fault isolation and system reconfiguration process is initiated. For reconfiguration a single pole double throw (SPDT) relay for each leg is used to automatically isolate a faulty leg and connect its corresponding inverter output (motor phase) to the redundant leg. Once that is completed the system can resume operation.

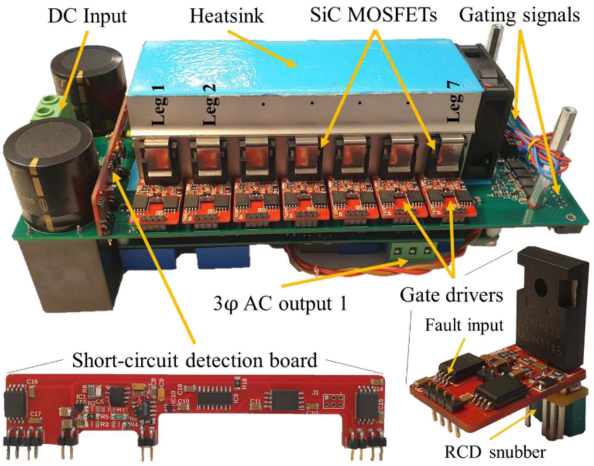

FIGURE 6. Prototype of the 400 V 6-phase fault-tolerant VSI.

The pulses are sent to the upper switches first then to the lower switches from Leg 1 to Leg 6 (not considering the redundant leg) thus faults in switches S_{12} and S'_{31} result in the minimum and maximum fault localization times of $T_1 + T_2 + T_p$ and $T_1 + T_2 + 12T_p$, respectively. The average fault localization time for leg n would then be the average time between its upper and lower switches equal to $T_1 + T_2 + (n+3)T_p$. In hindsight, sending the pulses to the lower switches in reverse order would have resulted in an equal average time for all legs equal to $T_1 + T_2 + (13/2)T_p$. The values of T_1, T_2, T_p and D_p are experimentally determined in Section V.

IV. PROTOTYPE AND TEST SETUP

A. PROTYPE DESIGN

The SVC is tested on a 400 V 6 kW 6-phase dual-output fault-tolerant inverter prototype, shown in Fig. 6 with its bottom-side view. The inverter is composed of 7 legs, where the middle leg is a redundant leg that can replace a faulty leg in either of the 2 outputs. SiC MOSFETs IMZ120R090M1H are used and are tightly integrated with custom-made gate drivers and RCD snubbers. The SVC short-circuit detection board is placed between the DC link and the first leg. The reconfiguration SPDT relays are placed on the prototype's top side (underside in the photo), on top of them lays another board equipped with line-to-line voltage and phase current sensors. It also contains the two 3-phase AC output terminals.

The gate drivers are equipped with a 2-level turn-Off protection circuit adapted from [12] and shown in Fig. 7. When switch S is short-circuited and its current rises to a high value, using R_{goff} to turn Off S quickly leads to high di/dt leading to a voltage spike across S. Selecting a high value for R_{goff} helps in reducing the voltage spike but has several drawbacks. Firstly, it reduces the switching speed and increases the switching losses. Secondly and more importantly, during a SC dv/dt across the MOSFET causes a current to flow through the gate-to-drain capacitor and gate resistor due to the Miller effect [13] which raises the gate voltage and causes failure if the

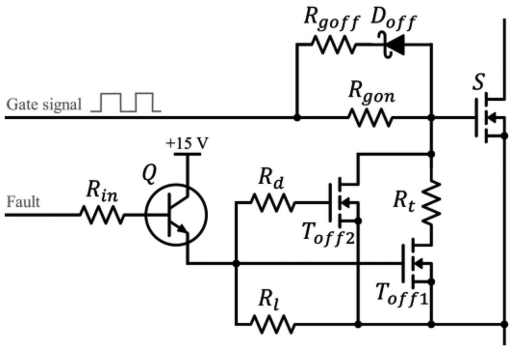

FIGURE 7. Schematic of the 2-level turn-off protection circuit.

maximum gate voltage rating is surpassed [14]. Moreover, the increased gate voltage leads to a higher SC current increasing the stress on the MOSFET and the chance of failure [15].

The 2-level turn-Off protection softly turns Off switch S to suppress the voltage spike. When the SC is detected and the fault signal is sent to the gate driver, the BJT Q is turned On which turns On MOSFET T_{off1} with minimum delay. T_{off1} creates a voltage divider between R_{gon} and R_t lowering the gate voltage V_{GS} to the first level $V_{L1} = V_{GS}\,(R_t\,/(R_t + R_{gon}))$. The delayed turn-On of T_{off2} by R_d clamps the gate terminal of S to the source terminal thus fully turning it Off (second level voltage $V_{L2} = 0$). The resistor R_l is used to limit the collector current of Q.V_{L1} is selected in a way to reduce the SC current by 5x as recommended in [16], using the MOSFET's datasheet I-V curves and considering a gate voltage of 15.5, $V_{L1} = 10.5$ V was found appropriate. The delay period should be long enough to ensure V_{GS} is clamped to V_{L1} and for the SC current to decay sufficiently, however, the delay must not surpass the SC withstand time of the MOSFET. Using simulation, a delay time of 200 ns was found sufficient, and the corresponding value of R_d can be calculated using (1) [17] where t_d is the delay time, and C_{iss} and V_{TH} are MOSFET S input capacitance and threshold voltage, respectively. Additionally, during normal switching the fast-rising voltage V_{GS} across T_{off2} induces a current through R_d and R_l due to the Miller effect which could cause a parasitic turn-On of T_{off2}. To prevent this $R = R_d + R_l$ should respect the inequality (2) [13] where C_{gd}, C_{gs} and V_{th} are the Gate-to-Drain, Gate-to-Source and minimum threshold voltage of T_{off2}, respectively. dV_{GS}/dt and T are the gate voltage rate of change and period to reach Miller plateau of switch S, respectively. The effectiveness of the 2-level turn-Off protection is verified in Section IV.

$$R_d = \frac{t_d}{C_{iss}\ln\left(V_{GS}/(V_{GS}-V_{TH})\right)} \tag{1}$$

$$RC_{gd}\frac{dV_{GS}}{dt}\left(1 - e^{-T/R\,(C_{gd}+C_{gs})}\right) < V_{th} \tag{2}$$

The SC detection board combines both the SVC and ESVC as illustrated in Fig. 1. To adapt the circuit for 400 V DC link voltage compared to the 48 V in the original SVC article,

TABLE 1. SVC, ESVC and 2-Level Turn-Off Circuit Components

SVC & ESVC SC					
C_{hp}	1 nF	R_{hp}	220 Ω	Z_1	PDZVTR5.1B
C_{lp}	0.1 nF	R_{lp}	5 kΩ	R_1	1 kΩ
C_F	0.1 nF	R_F	6.2 KΩ	V_{IN1} / V_{IN2}	2.5 V / 2.083
2-Level Turn-Off Protection					
R_{gon}	56 Ω	R_{goff}	56 Ω	Q	MMBT3904T
R_{in}	1 kΩ	R_d	1 kΩ	T_{off}	Si2304BDS
R_t	120 Ω	R_l	1 kΩ		

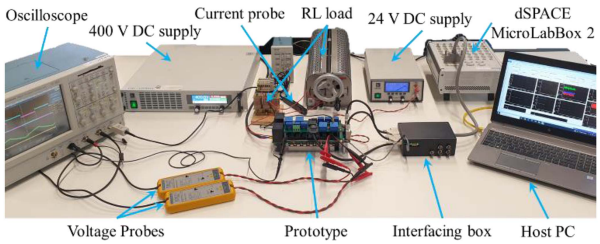

FIGURE 8. Experimental setup.

capacitor C_{hp} should be selected with an appropriate voltage rating as the voltage across it is equal to $V_{DC} - V_{IN1}$ and the resistor R_{lp} value must be high enough to limit the initial current when the DC voltage is switched On. Additionally, the ground of the low-voltage analog circuitry is connected to the DC link negative terminal. To realize galvanic isolation, the board could be connected to the filtered DC link voltage through a pulse transformer. The output of the detection circuit is sent to the controller and to the fault input of all the gate drivers through digital isolators. The values of the relevant components of the 2-level turn-Off and SC detection circuits are provided in Table 1.

B. DESCRIPTION OF THE TEST SETUP

The test setup is shown in Fig. 8. The prototype DC input is supplied from a 400 V DC source and its analog circuitry is powered by a 24 V DC supply. The output of the leg under test is connected to an RL load. The fault localization algorithm is implemented in FPGA on dSPACE MicroLabBox 2 which provides the gating signals for the MOSFET gates and relay drivers. The output current is measured using *Tektronix* current probe TCP305A. The MOSFET gate to source V_{GS} and drain to source V_{DS} voltages are measured using *Pico* differential voltage probe TA041. Other voltages are measured with *Tektronix* voltage probe TPP0101. The SC (or switch) current was not measured. All measurements are captured and recorded on the Tektronix TDS5054B Oscilloscope. Plotted data in the next section are smoothed by applying a moving average of window length 100 on the raw data records of length 2 million data points.

V. EXPERIMENTAL RESULTS

To validate the SVC for a 6-phase drive and examine the effect of added inductance a series of tests is carried out.

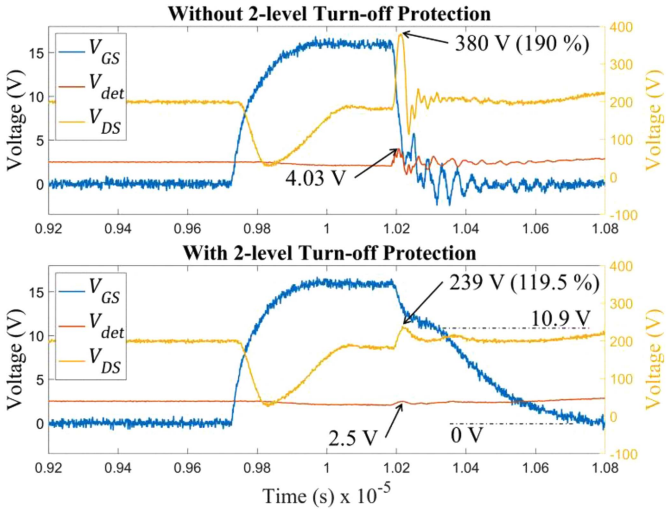

FIGURE 9. V_{DS} spike suppression with the 2-level turn-off protection.

First the effectiveness of the 2-level turn-off protection is validated. Then the response of the SVC and ESVC circuits to switching transients under load is evaluated to determine the appropriate detection thresholds for both circuits. Following, the capability of the circuit to detect faults under load (FUL) and hard switching faults (HSF) is verified. The data is also analyzed to determine parameters for the fault localization algorithm which is validated in the last experiment. As the first and last leg of the drive have the minimum and maximum stray inductance, they represent the limit cases, thus, it is only necessary to perform the tests on these 2 legs.

A. 2-LEVEL TURN-OFF PROTECTION

To demonstrate the effectiveness of the 2-level turn-Off protection scheme, the following test is carried out. The midpoint of Leg 1 is directly connected to drain of the upper MOSFET with a wire effectively bypassing it and the lower MOSFET is turned On for approximately 600 ns causing a SC, once without and once with the 2-level turn-Off protection. The test is performed at a reduced DC voltage of 200 V to avoid damage when the circuit is operated without the proper protection. The test results are shown in Fig. 9 where V_{GS}, V_{DS} and V_{det} are plotted for each case. When the MOSFET is first turned On at 9.72 μs V_{DS} drops to a low value but as the SC becomes established it starts increasing again. This increase causes V_{GS} to increase to 16 V higher than the gate voltage supply of 15.5 V due to Miller effect. V_{det} is decreasing as expected. Up until 10.19 μs the behavior in both cases is identical indicating an equal SC current. Just after that the MOSFET in the first case is turned Off by turning Off the gate signal, i.e., through the turn-Off resistance (R_{goff} //R_{gon} = 28 Ω). The quick turn-Off (25 ns) causes a spike in V_{DS} reaching 190% of the DC link voltage. After the spike, large oscillations are observed in V_{DS} and V_{GS}. When operating at higher voltage, the MOSFET could be damaged if the absolute ratings are exceeded (V_{DSmax} = 1200 V, V_{GSmin} = -7 V). A spike in V_{det} to 4 V is also observed which at higher DC

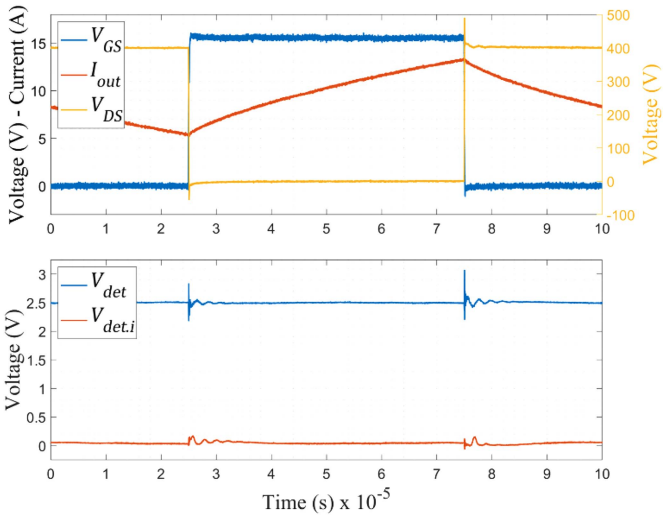

FIGURE 10. SVC and ESVC response to switching transients.

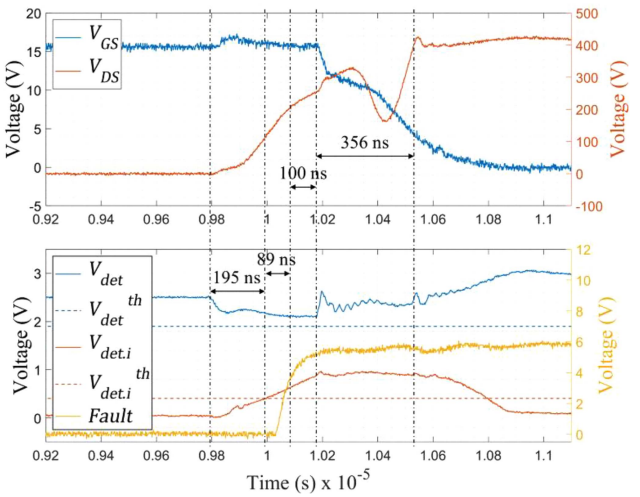

FIGURE 11. FUL waveforms for Leg 1.

TABLE 2. SVC and ESVC Transient Response Voltage Extremums

	First Leg		Last Leg	
	Lower	Upper	Lower	Upper
V_{det_min}	2.17 V	2.23 V	2.31 V	2.26 V
$V_{det.i\_max}$	0.18 V	0.19 V	0.19 V	0.2 V

voltage could damage the 5V analog circuitry of the SVC board. In the second case the MOSFET is turned Off using the 2-level turn-Off protection. First V_{GS} is brought down to the first voltage level ($V_{L1} = 16\ (120\ /(120 + 56)) = 10.91$ V) during 125 ns, this suppresses the voltage spike to only 119.5% and reduces the SC current to a lower level, V_{GS} is then reduced again slowly to reach 0 V in 450 ns. The spike in V_{det} is also suppressed and does not surpass 2.5 V.

B. SWITCHING TRANSIENT

To determine the detection thresholds V_{det}^{th} and $V_{det.i}^{th}$ for the SVC and ESVC circuits, an inverter leg is used as a buck converter and switching transients under load are measured. V_{DC} is set to 400 V, the switching frequency is set to 10 kHz with duty cycle of 50% and the load resistor is adjusted to get an input DC current of 7A (2.8 kW). The results for Leg 1 lower MOSFET are shown in Fig. 10. The test is done for the upper MOSFET as well and repeated on the last leg. The minimum of V_{det} (V_{det_min}) and the maximum of $V_{det.i}$ ($V_{det.i\_max}$) for each test are extracted and noted in Table 2. The voltage dips observed on the first leg are larger than the corresponding dips observed on the last leg, this is due to the additional parasitic inductance in the power loop of the last leg. The lowest value recorded of V_{det_min} is 2.17 V corresponding to a dip of 0.33 V and the highest value recorded of $V_{det.i\_max}$ is 0.2 V. As the prototype has 2 independent 3-phase outputs, it is possible for 2 switching instances from 1 leg in each output to coincide and the response of V_{det} and $V_{det.i}$ from each leg to add up. Therefore, appropriate values of the threshold values should be $V_{det}^{th} \leq 1.84$ V and $V_{det.i}^{th} \geq 0.4$ V. The threshold voltages are obtained with resistor voltage dividers from the voltage reference V_{IN1} with resistors available at hand. The final measured values are $V_{det}^{th} = 1.899$ V and $V_{det.i}^{th} = 0.405$ V. It is worth noting that testing 4 MOSFETs was extensive and with a proper safety margin only 1 test on the first leg (lowest inductance) is needed.

C. FAULT UNDER LOAD

For FUL test the RL load is connected between the DC link positive input and the middle point of the leg under test. The test conditions are like that in the previous test with the lower switch being the device under test. A FUL is induced by turning On the upper switch while the lower switch is already On and conducting the load current I_{Load}. The test results on Leg 1 are shown in Fig. 11. The SC occurrence is recognized by a fast dip in V_{det} to 2.16 V, but it is not enough to trigger the SVC. At the same time V_{DS} starts increasing first in the linear region of the MOSFET and accelerates once the MOSFET enters saturation. At this moment V_{det} starts decreasing again but slowly, on the other hand, $V_{det.i}$ increases at a steady pace and $V_{det.i}^{th}$ is exceeded after 195 ns. The *Fault* signal is measured at the output of a digital isolator after the SR-Latch and reaches 3.5 V (logic 1 for the digital isolator) after 89 ns, this delay is mainly from the comparator, SR-Latch and digital isolator. The turn-Off protection is activated after 100 ns of delay due to another digital isolator, the protection BJT and the MOSFET T_{off1}. As the MOSFET is turning Off, V_{DS} rises sharply but is slowed down by the first level of the turn-Off protection preventing a voltage spike across the MOSFET. However, a sudden large drop in V_{DS} is observed before it rises again as the second turn-Off level is reached and the MOSFET is fully turned Off marked by V_{GS} reaching 4.5 V (MOSFET threshold voltage) and takes 341 ns. The total SC event lasted 740 ns. Another interesting observation is the first level of the turn-Off protection lasting longer than the no load case shown in Fig. 9.

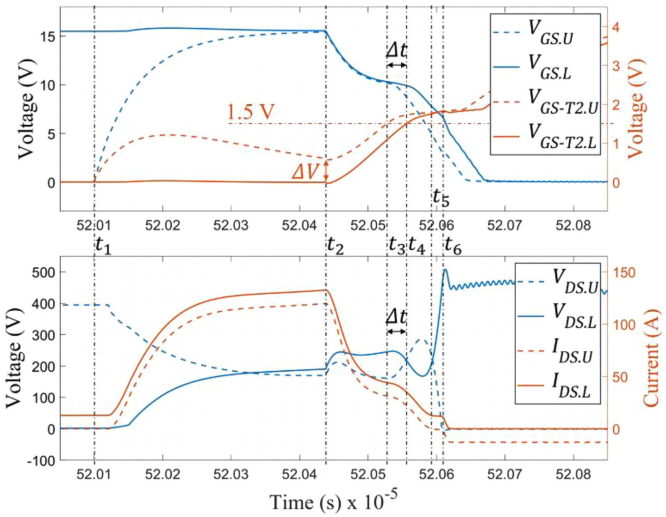

FIGURE 12. FUL simulated waveforms for Leg 1.

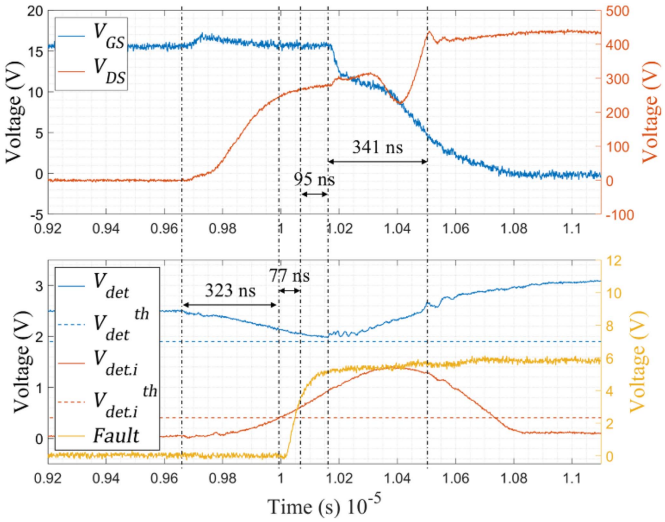

FIGURE 13. FUL waveforms for Leg 7.

Since the switch currents are not measured and due to the inaccessibility of some of the measurements, to help explain the observations the scenario is simulated in Simscape. The simulation results are shown in Fig. 12 where V_{GS}, I_{DS} and V_{DS} of the power MOSFETs and $V_{GS\text{-}T2}$ of the turn-Off MOSFETs T_{off2} are plotted. The MOSFETs of the upper and lower sides are denoted by $.U$ and $.L$, respectively. Initially, the lower MOSFET is On and carrying the load current I_{Load}, at t_1 the upper MOSFET is turned On and the SC current starts rising. The rising gate voltage of $V_{GS.U}$ induces a current in the gate of T_{off2} causing its voltage$V_{GS\text{-}T2.U}$ to rise due to Miller effect, this effect is especially significant because of the large value of R_d. The same is not observed in $V_{GS\text{-}T2.L}$ since the lower MOSFET was already On and $V_{GS.L}$ is only slightly increased. These effects are not significant on T_{off1} as it lacks a gate resistor. Hence, at t_2 when the protection is activated both $V_{GS.U}$ and $V_{GS.L}$ drop simultaneously to the first level and the SC current is reduced. The voltage across T_{off2} starts increasing and the second level is activated after a delay once it crosses the threshold voltage of 1.5 V. However, since $V_{GS\text{-}T2.U}$ had a head start of ΔV, it reaches the threshold at t_3 earlier than $V_{GS\text{-}T2.L}$ which reaches it at t_4 after a period Δt. This explains why the 2-level turn-Off protection is faster on a MOSFET that had just turned On than a MOSFET that is already on. Regarding the voltage dip in $V_{DS.L}$, between t_3 and t_4 as $V_{GS.U}$ is dropping and the SC current is reducing in both MOSFETs while $V_{GS.L}$ remains almost constant, $V_{DS.L}$ must drop while $V_{DS.U}$ rises. At t_5 the SC current is fully eliminated and only I_{Load} runs through the lower MOSFET as it is still conducting due to the delayed turn-Off. This is necessary since I_{Load} is unable to go through the body diode of the upper MOSFET yet due to reverse recovery time and if no path is available the load inductor voltage would drastically increase. The clamping of the lower switch current to I_{Load} during this period is also experimentally observed in [8]. Finally, at t_6 after the reverse recovery time has passed, the load current is diverted to the body diode of the upper MOSFET and the current of the lower MOSFET falls to zero.

The same test is repeated for Leg 7 and the results are shown in Fig. 13. The initial dip in V_{det} is almost completely gone as predicted by simulation in Fig. 13. The ESVC is again quicker than SVC in detecting the SC, however, due to the lack of the initial dip the detection time of 323 ns is significantly slower compared to that of Leg 1. The remainder of the test is similar to the test on Leg 1 with one notable difference of a smaller voltage drop in V_{DS} during the turn-Off phase. This is due to the longer fault detection time which allows $V_{GS\text{-}T2.U}$ to reduce further before the activation of the protection. Hence, ΔV and Δt are smaller and the period in which the SC current drops while $V_{GS.L}$ remains constant is smaller. The total SC event lasted 836 ns.

In both these tests ultra-fast detection with SVC was not achieved, even in the test on the first leg the voltage dip was barely larger than the dips observed during switching transients in Table 2. On the other hand, both faults are detected fast with ESVC. Thus, only the ESVC is effective for detecting FUL for this multi-phase prototype. Finally, although the timing difference of the full turn-Off between upper and lower MOSFETs was not initially considered in the design, it appears to have a significant effect and plays an important role in safely eliminating the SC current. Therefore, the values of R_t and R_d should be properly tuned, and care should be taken to prevent unintentional turn-On of T_{off2} during normal switching.

D. HARD SWITCHING FAULT

For HSF the upper switch is bypassed by connecting a wire between its drain and the middle point of the leg under test. V_{DC} is set to 400 V and an HSF is induced by turning On the lower MOSFET. Bypassing the upper MOSFET removes its resistance from the SC path compared to the FUL case, hence, a higher SC current is expected. Similarly, the parasitic

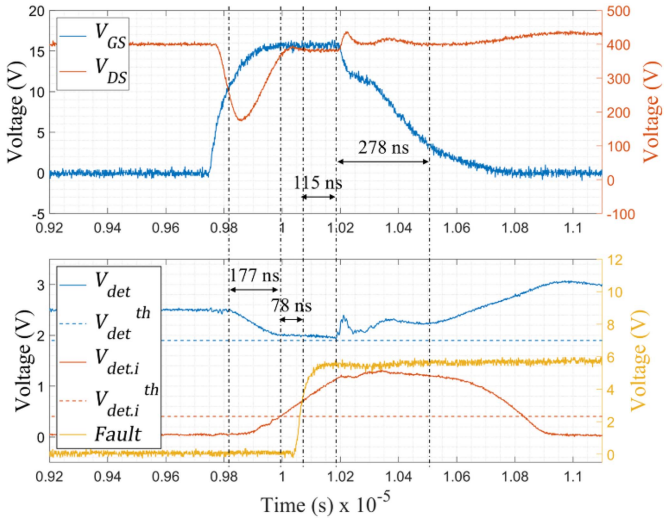

FIGURE 14. HSF waveforms for Leg 1.

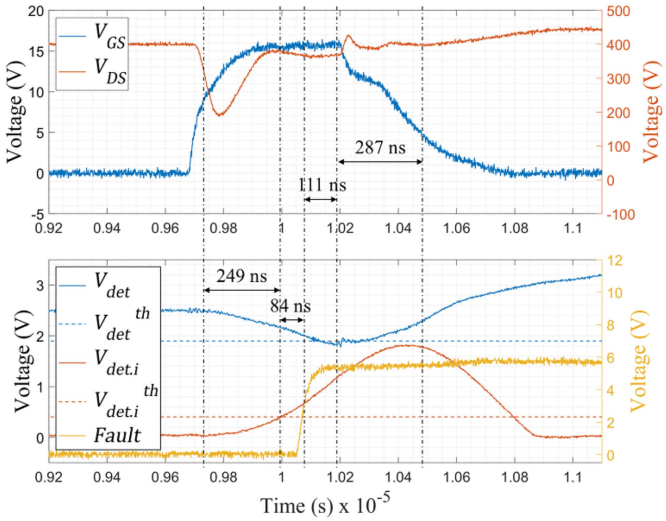

FIGURE 15. HSF waveforms for Leg 7.

inductances of the MOSFET are removed but the inductance of the added wire is higher thus in total higher inductance is expected. The test results on the first leg are shown in Fig. 14 where the same signals as in the previous test are plotted. As the MOSFET is turned on, its V_{DS} starts dropping but as the SC becomes fully established V_{DS} rises again nearly to 400 V. A less steep but longer dip in V_{det} is observed compared to FUL case due to the higher inductance, but it plateaus at 2 V just above the threshold. On the other hand, $V_{det.i}$ increases steadily leading to SC detection in 177 ns. From here on the protection is activated and the SC is eliminated in the same way as in the FUL case. As explained previously the activation of the second level of the turn-Off happens earlier compared to the FUL case leading to a faster turn-Off phase. The total SC event time is 648 ns. The same test is repeated on the last leg and the results are shown in Fig. 15. The main difference is the less steep decrease in V_{det} and increase in $V_{det.i}$, hence, the slower detection time of 249 ns compared to the first leg. The total SC event time is 731 ns.

Compared to the FUL, in the HSF case the detection time and the SC event time are shorter for each of the legs, this can be attributed to the higher SC current combined with higher inductance making the phase during which the current is rising and the voltage is dipping longer, hence, allowing the integrator output $V_{det.i}$ to rise faster. Again, the SVC was unable to capture HSF but the voltage dips where larger than in the case of FUL and if simultaneous switching can be avoided by control, the threshold for the SVC could have been set higher and potentially allowing SVC to detect HSF faster than ESVC. In any case, ESVC was fast and effective in detecting HSF. In conclusion, and for both FUL and HSF the SVC was found ineffective for the considered 6-phase prototype with a conventional structure while the ESVC was found to be effective, reliable, and fast. Therefore, the ESVC overcomes the problem of added inductance and is suitable for multiphase drives.

E. FAULT LOCALIZATION ALGORITHM

For the fault localization algorithm, the parameters T_1, T_2, T_p and D_p must be determined which further adds to the implementation effort. The longest SC event recorded in the FUL and HSF tests is 863 ns, thus localization pulse period T_p can be set to 1 μs. As a SC needs more than 500 ns to be detected and recorded by the controller, if a SC is recorder during the first half of pulse Pi it signifies pulse Pi-1 was caused the SC, hence, a waiting period between the pulses is not needed, the duty cycle and D_p is set to 90%. T_2 is the time between sending the control signal for resetting the SR-Latch and the full turn-Off of T_{off2}. It is mainly composed of the time required for the gate of T_{off2} to be discharged due to the high value of R_d, the BJT storage time of 200 ns and fall time of 50 ns and the SR-latch propagation delay time of 175 ns. The discharge time can be approximated by $3R_dC_{gs} = 685$ ns (enough to bring the voltage below the threshold of 1.5 V) where C_{gs} is the gate-to-source capacitance of T_{off2} amounting to a total delay of 1.11 μs. An additional delay is needed since the faulty MOSFET is also subject to the turn-Off protection and requires time to be fully On again. A total value of 1.85 μs for T_2 was found to be suitable. Finally, since only a small time slot of the previous experiments is plotted, the DC link voltage ripple and its effects on the detection signals was not shown, the full examination of the signals shows that a 5 μs period for T_1 is sufficient.

The test is performed at 400 V DC voltage by sending PWM signals to all MOSFETs without any load and then fixing the gate signal of one of the MOSFETs On while its complementary MOSFET is On creating a SC. The test results for the case when the upper MOSFET of the last leg (S6) is held On correspond to the longest localization time and are shown in Fig. 16. The gate voltage for S6 $V_{GS.S6}$ and its complementary switch S12 $V_{GS.S12}$, the *Fault* signal and $V_{det.i}$ are plotted, the gate voltage for the other MOSFETs could not be simultaneously captured on the same 4-channel scope,

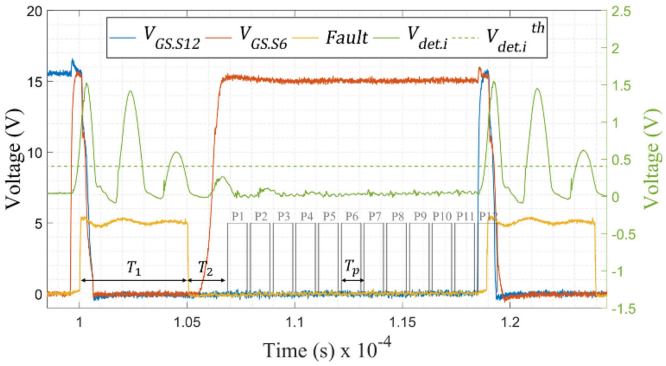

FIGURE 16. **Fault localization algorithm sequence.**

thus, the localization pulses are virtually indicated on Fig. 16 in grey color. When S6 is turned On while S12 is on, a SC occurs and the detection and turn-Off protection proceed as expected. However, soon after a few more bumps in $V_{det.i}$ occur creating false triggers, thus, the fault signal is only reset after 5 μs. Then after some delay the protection is released and S6 is On again, the localization pulses begin after 1.85 μs. Pulses are sent to all MOSFET without anything occurring until the last MOSFET S12 is reached, and a second SC occur indicating that S6 is faulty, and thus the fault is localized. The total localization time from the moment S6 is held On until the second SC is eliminated is 19.7 μs. This corresponds to the worst case, in the best case for a faulty lower MOSFET in the first leg the localization time would be $19.7 - 11T_p = 8.7$ μs. Further validation of the fault localization algorithm under load will be presented in a future publication.

VI. CONCLUSION

The SVC is a system-based, simple, and fast SC detection method suitable for protection of wide-bandgap devices. When extended to fault-tolerant multi-phase drives, it simplifies their design and could help reduce their size and cost and improve their reliability, but it requires a fault localization algorithm, additionally, tests are required to tune the detection circuit and the localization algorithm which increases the implementation effort. Simulation analysis shows that the added stray inductance of every inverter leg makes ultra-fast SC detection with the SVC challenging. Fortunately, SCs can still be detected but slower and the ESVC may accelerate the detection. Both methods are adapted for a 400V 6-phase fault-tolerant SiC based dual-motor drive featuring a 2-level turn-Off protection scheme. Experimental tests show the effectiveness of the protection scheme in suppressing voltage spikes when the SC current is eliminated. FUL and HSF tests carried out show that ultra-fast SC detection with the SVC method is not achieved for this multi-phase prototype, an optimized and dedicated design might improve its performance. On the other hand, the ESVC reliably detects SC faults in less than 330 ns and the maximum observed SC protection time was 863 ns. Thus, ultra-fast SC detection is not needed and the ESVC is fast and suitable for multi-phase SiC drives. The fault localization algorithm is also developed in detail, improved, and experimentally validated showing a maximum localization time of 19.7 μs.

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