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A Neutral Point Balancing and Voltage Error Compensation Approach for Fault-Tolerant 3-Level Inverters

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ABSTRACT Neutral point clamped inverters, such as NPC, ANPC, or T-Type inverters, have emerged as competitive solutions for specific automotive traction applications due to the increase in DC-link voltage levels up to 800 V. Besides improved harmonic performance, certain 3-level inverter structures can provide a reconfigured failure mode operation in case of a semiconductor failure by applying a permanent neutral point connection in the faulty phase leg. This feature is a vital factor in the design of traction inverters, particularly in the context of fault-tolerant autonomous vehicles. During failure mode operation, none of the neutral point balancing techniques found in current literature are practical. Addressing this issue is crucial since the neutral point stress is high in this mode of operation. Therefore, this paper investigates the impact of stationary and dynamic neutral point voltage deviations on the motor flux in electric machines and offers a compensatory strategy for these errors. Furthermore, a new neutral point control method is presented that balances stationary neutral point voltage deviations by using a phase angle dependent voltage shift in the α/β-plane. All proposed strategies are first discussed theoretically and then verified by simulation and measurements on an 800 V IPMSM machine test bench.

INDEX TERMS Error compensation, fault tolerance, multilevel inverters, space vector pulse width modulation, voltage control.

I. INTRODUCTION

Multilevel inverters are crucial components in numerous industries, including photovoltaic [1], [2] and wind power transmission [3], large industrial drives [4], [5], fast charging stations [6], and general power transmission applications [7]. Due to their superior harmonic performance, reduced semiconductor voltage stress, high power density and efficiency, the utilization of multilevel inverters is increasingly prevalent [1], [8]. Today, the relevance of multilevel inverters extends further, as discussions focus on their integration into the growing field of battery electric vehicles (BEVs) [8], [9], [10], [11], [12], [13]. This trend is being driven by the global growth in sales of BEVs, aiming for reduced emissions of carbon dioxide and pollutants in the transportation sector [8], [14]. With the increase in market share, a concurrent need for enhanced driving efficiency, cost effectiveness and fast charging times arises [9], [14]. As the traction inverter is a key component in the electric drive train, its design and further development will be essential in meeting these demands. A primary design parameter of the inverter is the level of the DC-link voltage, which has reached values of up to 800 V in certain modern BEVs in recent years [8], [9], [13]. Although a high DC-link voltage requires increased insulation efforts, it results in lower cable losses. This can be utilized to decrease cable diameters [13]. Furthermore, increasing the DC-link voltage results in shorter charging times when using fast charging stations [8], [9], [13]. With the use of multilevel inverters, a DC-link voltage of 800 V can be realized by

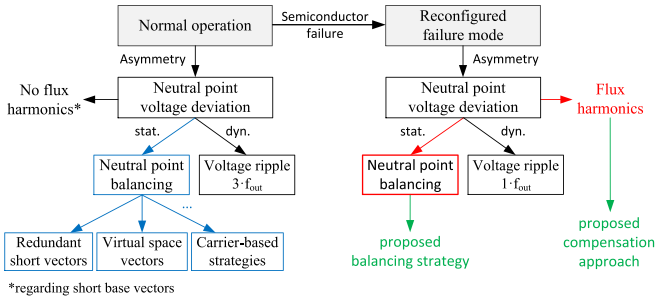

FIGURE 1. Overview of established (blue) and proposed (green) methods for treating deviations in the neutral point voltage.

applying 650 V semiconductors, such as Si-IGBTs, SiC-MOSFETs and GaN-HEMTs, which offer several design options to improve the inverter performance [15], [16]. Another advantage of multilevel inverters is the reduction in total harmonic distortion (THD) on output voltages and currents, leading to lower losses and ultimately, improved efficiency [17], [18]. Automotive traction inverters are required to handle a wider range of operating points than those in other industrial sectors. In turn, these requirements include enhanced operability throughout the full range of the power factor and modulation index, improved start-up behavior at low speeds, and distinct dynamic changes in the load. When using an inverter with a neutral point connection, any of these requirements directly affects the stability of the neutral point [19]. Thus, balancing the neutral point voltage is crucial for the proper operation of the inverter [20], [21]. Despite this, feasible solutions for controlling the neutral point voltage in certain operating conditions, such as reconfigured failure mode operation after a semiconductor fault, are not yet available in literature. Section II focuses on this topic and explains in detail why state-of-the-art methods cannot be used under fault conditions. Nevertheless, the concept of fault-tolerance has been a major topic in recent literature, especially in the field of autonomous vehicles [9], [22], but also in the context of all-electric aircraft [23], [24]. Certain multilevel inverters can provide fault-tolerant properties by using a reconfiguration of the inverter control and are therefore well suited for the afore-mentioned applications [25] [26]. In today's literature, no paper known to the authors has been published that addresses the effect of unbalanced DC-link voltages on 3-level inverters in reconfigured failure-mode under automotive conditions. This paper aims to fill that gap by exploring the effects of a DC-link voltage deviation on the motor flux and presenting a comprehensive approach to compensate for this stationary or dynamic deviation. Moreover, a new strategy is proposed to balance stationary neutral point deviations during reconfigured failure mode by using space vector modulation. Only a combination of both approaches can achieve robust and reliable operation under fault conditions. The findings of this paper prove that stable operation is possible, thus facilitating the application of fault-tolerant inverters for automotive electric power trains. Fig. 1 provides an overview of established neutral point balancing techniques in normal inverter operation and shows the different situation in reconfigured mode after a semiconductor failure. Each component depicted in Fig. 1 will be elaborated in detail in Section II.

The paper is structured in the following manner: Section II discusses fundamental operating principles of three different neutral point clamped 3-level inverters and outlines various existing neutral point balancing strategies. Moreover, this section examines an inverter reconfiguration principle for the failure mode operation of the presented inverter configurations and analyses its impact on the neutral point voltage. Section III addresses the impact of a neutral point deviation on the motor flux of electric machines driven by a (fault tolerant) neutral point clamped inverter. It comprises equations for the output voltage error in the α/β-plane and proposes a compensation strategy for this error by adjusting the switching times of certain space vectors. To counteract stationary deviations in the neutral point voltage, a control strategy for reconfigured failure mode operation is introduced in Section IV. This strategy involves manipulation of the neutral point current by injecting a control voltage vector that depends on the phase angle. The presented derivations and simulations are verified by measurements in Section V. Finally, Section VI summarizes the findings of this paper.

II. OPERATION OF FAULT-TOLERANT 3-LEVEL INVERTERS

A. 3-LEVEL INVERTERS FOR ELECTRIC VEHICLE TRACTION APPLICATIONS

Traction inverters in modern BEVs must meet severe requirements for high efficiency, power density and reliability [9], [14]. Moreover, system complexity is also a limiting factor in the design of power electronic systems. Assuming the same type of components, system cost rises as complexity and the number of components increases. In the automotive industry, system cost is a vital design parameter for enhancing new competitive inverter solutions. Hence, exclusively 3-level inverters are discussed in this paper as they are the least complex multilevel inverter structures. Literature indicates that 3-level inverters can be a competitive solution compared to 2-level inverters due to the reduced amount of harmonics and the advantage of using power semiconductors with lower blocking voltage [12].

Three distinct types of 3-level inverters are particularly well-suited for the use in traction applications [9] [27]. The most common structure is the Neutral Point Clamped (NPC) inverter [28], which features four active switches and two clamping diodes connected to the neutral point, see Fig. 2 (left) [29] [30] [31]. The NPC structure can be modified by replacing the clamping diodes with active switches, see Fig. 2 (middle). This Active Neutral Point Clamped (ANPC) inverter offers the use of different commutation loops, allowing active loss balancing [32] and other advantageous degrees of freedom in the inverter design and operation. Depending on the semiconductor type, individual switch dimensioning, and

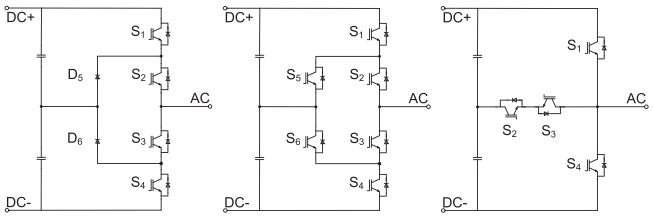

FIGURE 2. 3-level inverter structures with neutral point connection: NPC inverter (left), ANPC inverter (middle) and T-NPC inverter (right).

TABLE 1. Common ANPC Inverter Switching States

State	S_{1x}	S_{2x}	S_{3x}	S_{4x}	S_{5x}	S_{6x}
+1	1	1	0	0	0	1
0 (MS1)	0	1	0	1	1	0
0 (MS2)	1	0	1	0	0	1
0 (MS3)	0	1	1	0	1	1
-1	0	0	1	1	1	0

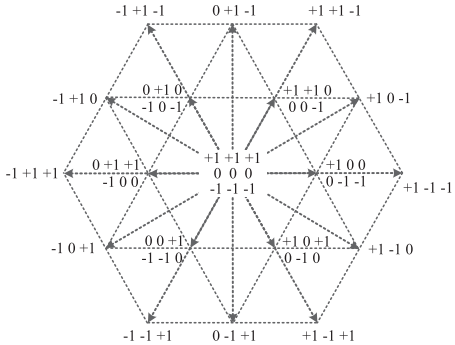

FIGURE 3. 3-level space vector diagram with small, medium and large vectors.

applied modulation scheme, it is possible to achieve an increased start-up current at low speeds [33] or reduced WLTC losses [12]. Table 1 lists the most common switching states for ANPC inverters according to [34], [35]. There are three different modulation schemes that define the current paths during the zero voltage state. Modulation scheme 1 (MS1) utilizes the upper inner path during the positive half cycle and the negative inner path during the negative half cycle, whereas modulation scheme 2 (MS2) uses the opposite paths. Modulation scheme 3 (MS3) employs both inner paths irrespective of the voltage half cycle, which in turn reduces conduction loss, particularly when SiC-MOSFETs are used [12]. The T-Type Neutral Point Clamped (T-NPC) inverter is a 3-level inverter with reduced number of power semiconductors. It is depicted in Fig. 2 (right), and achieves the neutral point connection through two anti-serial active switches. Thus, only one zero-voltage state is applicable, as seen with the NPC inverter. It is important to also consider other 3-level topologies, such as the Flying Capacitor (FC) inverter, for BEV traction applications. However, due to its demand for large DC-link capacitors, its versatility is limited [9], [36]. However, the focus of this paper is on 3-level inverters with neutral point connection because they share the need for active neutral point voltage control (see Section II-B) to protect the semiconductors from overvoltage damage [37], [38], [39], [40], [41]. One significant benefit of 3-level inverters is their (partial/full) fault tolerance against single switch failures. When the inverter control is reconfigured, each of the introduced inverter structures can be converted into a structure with two active phase legs and one permanent neutral point connection in the faulty phase leg. The operating principle is similar to the four-bridge midpoint (B4M) inverter [42] and discussed in Section II-C. Unlike the NPC and T-NPC structure, which can partially respond to some failure scenarios, the ANPC inverter control can be reconfigured to apply a permanent neutral point connection in the faulty phase without stressing the faulty switch in case of any short-circuit or open-fault [26]. This advantage facilitates the design of highly reliable BEV powertrains, but also presents some challenges in the inverter operation, which are discussed in Section II-D.

B. NEUTRAL POINT BALANCING STRATEGIES FOR 3-LEVEL INVERTERS IN NORMAL OPERATION MODE

In normal operation mode with three healthy phase legs, several neutral point control strategies are discussed in literature. An overview of the most common methods is given by [20] and [21]. One approach to prevent neutral point voltage drift is the use of hardware solutions such as balancing resistors or the use of two serial dc sources. Neither of these approaches is suitable or sufficient for automotive applications. Balancing resistors dissipate a significant amount of energy, resulting in lower inverter efficiency. Furthermore, BEVs only have a single HV battery which is not designed to provide an additional neutral point tap.

Consequently, the neutral point balancing task must be implemented in the inverter control. By using space vector modulation (SVM), certain space vectors or their corresponding switching times can be adjusted to affect the neutral point current. A positive neutral point current (defined to flow from the neutral point into the phase leg) increases (decreases) the voltage across the upper (lower) DC-link capacitor, whereas a negative neutral point current has the opposite effect. A common strategy for SVM neutral point balancing is to use redundant short vectors. As shown in Fig. 3, there are two redundant switching states for each short vector, e.g. $\{+1, +1, 0\}$ and $\{0, 0, -1\}$. Both vectors represent the same output voltage in the case of a symmetric DC-link without neutral point voltage deviation. Since $\{+1, +1, 0\}$ connects the DC+ potential to the neutral point across the load, it results in a positive neutral point current when the phase current i_c is positive. Conversely, $\{0, 0, -1\}$ results in a negative neutral point current. Fig. 4 shows both switching states and their respective current paths. The same principle applies to the other short vectors listed in Table 2. Since the output voltage is not affected by the selection of either the first or the second short vector, a defined neutral point current can be applied by setting the correct ratio of the corresponding switching times.

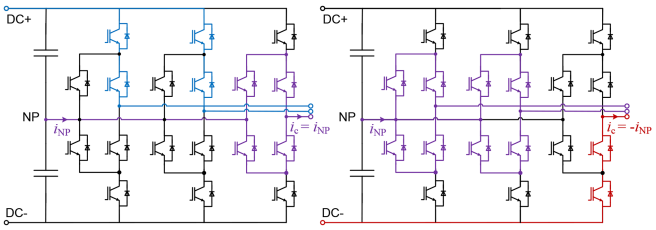

FIGURE 4. Redundant switching states {+1, +1, 0} (left) and {0, 0, −1} (right) with consequent current paths in a 3-level ANPC inverter structure.

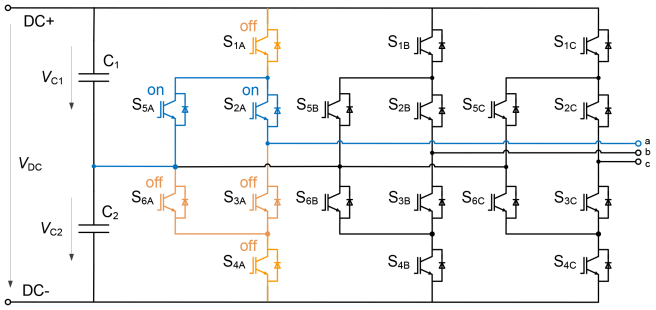

FIGURE 5. 3-level ANPC inverter with permanent neutral point connection in phase leg A.

TABLE 2. Influence of the Short Vectors on the Neutral Point Current According to [38]

State	i_{NP}	State	i_{NP}	State	i_{NP}
+1, 0, 0	$-i_a$	0, 0, +1	$-i_c$	-1, 0, -1	i_b
+1, +1, 0	i_c	+1, 0, +1	i_b	-1, 0, 0	$-i_a$
0, +1, 0	$-i_b$	0, -1, -1	i_a	-1, -1, 0	i_c
0, +1, +1	i_a	0, 0, -1	$-i_c$	0, -1, 0	$-i_b$

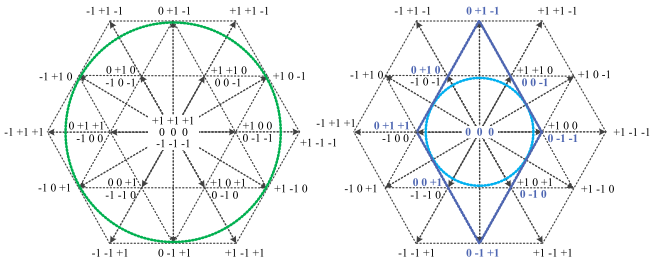

FIGURE 6. 3-level space vector diagram for normal operation (left) and reconfigured failure mode operation (right).

This approach works well for most operating points as long as the cumulative switching time for short vectors is long enough. However, it is not applicable for high modulation index and low power factor. It also requires the measurement of DC-link capacitor voltages and phase currents. [38]

Another strategy to control the neutral point voltage is the use of virtual space vectors, which are linear combinations of the existing space vectors. Each sector of the space vector diagram spanned by the large vectors is divided into five subregions by connecting the three closest virtual space vectors. By applying the correct duty cycle to each of these vectors, the desired output voltage vector is set. Since each of the virtual space vectors leads to zero neutral point current as a consequence of the chosen linear combinations, this approach is also applicable for the entire range of the modulation index and for low power factors according to [37], [43]. Other approaches replace vectors that affect the neutral point current with vectors that do not [44] or use variable dead times to control the neutral point voltage [45]. For carrier-based modulation strategies such as sinusoidal pulse width modulation (SPWM), the injection of an offset voltage to the carrier signals creates an asymmetry in the PWM pulses of both half-cycles. This asymmetry results in a shift in the mean value of the neutral point current, thus providing the ability to control the neutral point voltage. However, this method is only suited for the operation at low power factor with certain modifications. [39], [41], [46], [47]

In some operating points, a balancing effect can also be achieved by injecting even harmonics into the modulation signals in carrier-based control strategies [48], [49]. As with common mode voltage injection approaches, this method is not feasible for the wide range of operating points of an electric vehicle traction inverter.

C. OPERATION OF 3-LEVEL INVERTERS IN RECONFIGURED FAILURE MODE

In the event of a single semiconductor failure due to various potential failure mechanisms [50], [51], [52], each of the introduced 3-level inverter types offers the ability to continue operation in a reconfigured failure mode. The basic reconfiguration is done by applying a permanent neutral point connection in the faulty phase leg. Therefore, the faulty switch must be isolated either by turning off all adjacent switches or by using additional fuses. The neutral point connection is realized by keeping the inner switches permanently turned on, or by using additional bypass switches. [25], [53]

NPC and T-NPC inverters require these additional fuses and/or bypass switches to cover all possible kinds of failures. In contrast, the ANPC structure allows for reconfiguration without extra components in any failure scenario. [22], [26]

Fig. 5 shows the reconfigured structure for either an open or a short-circuit failure in S_{3A}, S_{4A} or S_{6A} by using the upper inner path for the neutral point connection. When space vector modulation is applied, failure mode operation is achieved by using a reconfigured modulator. The permanent neutral point connection of phase leg A defines its switching state to zero. This leaves only nine base vectors, including one zero vector, two medium-length vectors, and six small vectors, as shown in Fig. 6. By using only the small vectors, a symmetric quasi-2-level SVM with reduced maximum output voltage is possible. This allows the inverter to operate in a downgraded symmetric reconfigured failure mode. [19], [25], [53], [54], [55], [56]

D. RESTRICTIONS IN RECONFIGURED FAILURE MODE

Unlike the normal 3-level SVM with redundant small vectors, reconfigured failure mode operation provides only a single base vector in each direction. For a failure in phase leg A, only $\{0, 0, -1\}$ is applicable in the example of Fig. 4. Therefore, none of the introduced neutral point balancing strategies are applicable. The use of redundant small space vectors is not feasible due to the absence of redundant vectors. For the same reason, a definition of virtual space vectors is also ineffective. Especially for automotive traction inverters, SVM is the state-of-the-art modulation principle. Therefore, carrier-based balancing approaches are not applicable. This implies the need for a new neutral point balancing strategy, like indicated in Fig. 1.

Unbalanced DC-link voltages due to component scattering of the DC-link capacitors and power semiconductors, asymmetries in the modulation signals or variable signal propagation delays [28] [57] result in harmonics in the output signals. In normal operation, the voltage deviation is canceled by using the redundant small vectors, which is not feasible in the reconfigured failure mode. In addition to a potential stationary neutral point unbalance, there is a fundamental frequency voltage ripple at the neutral point. The amplitude of this voltage ripple is highly dependent on the operating point. It increases with lower fundamental frequency and higher phase current [19]. Therefore, a dynamic voltage unbalance must also be considered, which increases the harmonic content in the output signals.

Section III analyzes the effect of a neutral point voltage deviation on the flux in electric machines and proposes a strategy to compensate the resulting output voltage error. Furthermore, in Section IV, a neutral point control strategy is proposed that is specifically designed for 3-level inverters in reconfigured failure mode.

III. VOLTAGE ERROR COMPENSATION IN RECONFIGURED FAILURE MODE

Unbalanced DC-link capacitor voltages cause a shift in the neutral point potential, resulting in harmonics in the flux and consequently, in the output currents of reconfigured 3-level inverters in failure mode. This section is dedicated to examining the impact of the neutral point voltage deviation ΔV_{NP} on the output voltage vectors during this operation mode. The resultant output voltage error is derived using the Clarke transform and flux integral, and an approach to compensate for this error is presented.

A. IMPACT OF UNBALANCED DC-LINK CAPACITOR VOLTAGES ON THE INVERTER OUTPUT

The neutral point voltage deviation is defined by (1), where V_{C2} represents the voltage across the lower DC-link capacitor and V_{DC} represents the DC-link voltage (see Fig. 5).

$$\Delta V_{\mathrm{NP}} = V_{\mathrm{C2}} - \frac{1}{2} V_{\mathrm{DC}} \tag{1}$$

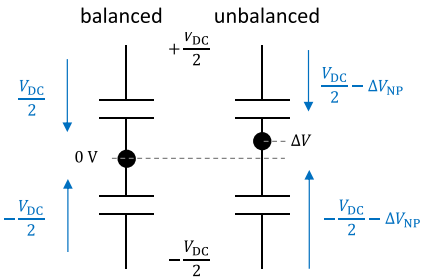

FIGURE 7. Definition of the voltage deviation ΔV_{NP} for unbalanced DC-link capacitor voltages.

Furthermore, a value of 0 V is assigned to the ideal neutral point potential. Thus, the unbalanced non-ideal capacitor voltages (each measured from outer contacts towards the neutral point) both contain an error term with a negative sign of ΔV_{NP}. Fig. 7 shows these voltage definitions for balanced and unbalanced voltage distribution. The line-to-neutral point voltages v_{x0} $(x = a, b, c)$ of an inverter with ideally balanced capacitor voltages are deduced from the DC-link voltage and the discrete switching states q_i $(i = 1, 2, 3)$ by using (2).

$$\begin{pmatrix} v_{\mathrm{a0}} \\ v_{\mathrm{b0}} \\ v_{\mathrm{c0}} \end{pmatrix} = \begin{pmatrix} 1 & 0 & 0 \\ 0 & 1 & 0 \\ 0 & 0 & 1 \end{pmatrix} \begin{pmatrix} q_1 \\ q_2 \\ q_3 \end{pmatrix} \frac{V_{\mathrm{DC}}}{2} \tag{2}$$

Subsequently, the line-to-neutral point voltages can be transformed into the α/β plane by using the Clarke Transform, as shown in (3).

$$\begin{pmatrix} v_\alpha \\ v_\beta \end{pmatrix} = \begin{pmatrix} \frac{2}{3} & -\frac{1}{3} & -\frac{1}{3} \\ 0 & \frac{\sqrt{3}}{3} & -\frac{\sqrt{3}}{3} \end{pmatrix} \begin{pmatrix} v_{\mathrm{a0}} \\ v_{\mathrm{b0}} \\ v_{\mathrm{c0}} \end{pmatrix} \tag{3}$$

$$\mathbf{D} = \begin{pmatrix} \frac{2}{3} & -\frac{1}{3} & -\frac{1}{3} \\ 0 & \frac{\sqrt{3}}{3} & -\frac{\sqrt{3}}{3} \end{pmatrix} \tag{4}$$

For simplicity, the transformation matrix is now referred to as $\mathbf{D}$. By combining the two matrix equations, the voltage vector $\vec{v}_{\alpha\beta}$ can be determined using (5).

$$\begin{pmatrix} v_\alpha \\ v_\beta \end{pmatrix} = \mathbf{D} \cdot \begin{pmatrix} q_1 \\ q_2 \\ q_3 \end{pmatrix} \frac{V_{\mathrm{DC}}}{2} \tag{5}$$

In a non-ideal inverter with neutral point shift, the equation requires the inclusion of an error voltage term. With a positive neutral point voltage deviation ΔV_{NP}, the sign of the error used in (6) is negative for each switching state $q_i \neq 0$ according to Fig. 7. This is described by the q_i^2 expression in every switching state.

$$\begin{pmatrix} v_\alpha \\ v_\beta \end{pmatrix} = \mathbf{D} \cdot \left[\begin{pmatrix} q_1 \\ q_2 \\ q_3 \end{pmatrix} \frac{V_{\mathrm{DC}}}{2} - \begin{pmatrix} q_1^2 \\ q_2^2 \\ q_3^2 \end{pmatrix} \Delta V_{\mathrm{NP}} \right] \tag{6}$$

Consequently, the voltage vector in the α/β plane comprises two components due to the linear transformation rule.

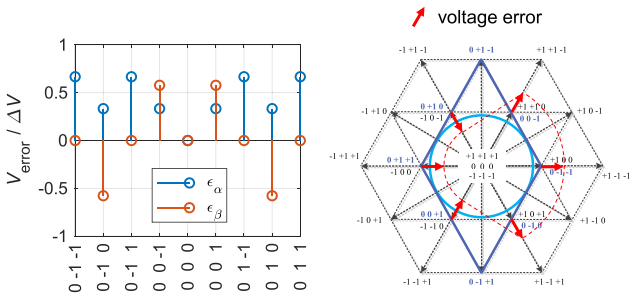

FIGURE 8. Output voltage error components in the α/β-plane for each available voltage vector with unbalanced DC-link when a permanent neutral point connection of the faulty phase leg A is applied.

One component is equivalent to $\vec{v}_{\alpha\beta}$ for a balanced DC-link (refer to (5)) which is independent from the neutral point voltage deviation. The other component is determined by (7) and relies solely on the neutral point voltage deviation and switching states.

$$\begin{pmatrix} v_{\alpha,\mathrm{err}} \\ v_{\beta,\mathrm{err}} \end{pmatrix} = \mathbf{D} \cdot \begin{pmatrix} q_1^2 \\ q_2^2 \\ q_3^2 \end{pmatrix} \Delta V_{\mathrm{NP}} \tag{7}$$

By utilizing (7), the output voltage error is defined in the α/β plane and can be represented as either α/β components or error voltage vectors as illustrated in Fig. 8. In reconfigured failure mode, only 9 out of the initial 27 switching states are available. For symmetric PWM operation, the medium vectors $\{0,-1,+1\}$ and $\{0,+1,-1\}$ are excluded. Thus, only six small vectors and one zero voltage vector remain. For a failure in phase leg A with consequent neutral point connection, the calculated voltage error components cause the voltage vectors on the left side of the hexagon to shorten while those on the right side extend. This results in phase angle-dependent output voltage deviations, which are represented by distortions in the α/β output voltage trajectory, causing harmonics in the motor flux. Besides a higher level of harmonic content, there remains an error in α direction. While all error components in β direction sum up to zero for a full rotation of 2π, the error components in α direction do not.

$$\Sigma v_{\alpha,\mathrm{err}} \neq 0 \tag{8}$$

$$\Sigma v_{\beta,\mathrm{err}} = 0 \tag{9}$$

The same principle can be applied in case of a failure in phase leg B or C. The superposition of ideal voltage vectors and error vectors results in the same diagram in any scenario, but rotated by $\frac{2}{3}\pi$ for a failure in phase B and by $\frac{4}{3}\pi$ for a failure in phase C, see Fig. 9.

B. NEUTRAL POINT VOLTAGE ERROR COMPENSATION STRATEGY

The compensation strategy outlined in this section aims to prevent the distortion of motor flux by adjusting the switching times τ_j for any of the available switching states. To meet the

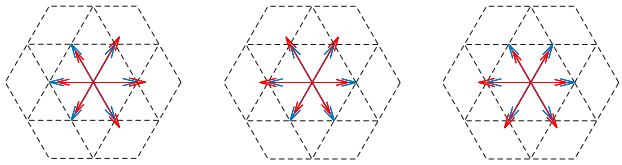

FIGURE 9. Remaining voltage vectors for balanced (blue) and unbalanced (red) DC-link voltage for a failure of phase A (left), B (middle), and C (right).

requirement of constant flux, (10) must be satisfied.

$$\Psi(t) = \int v\left(t'\right) \mathrm{d}t' = \mathrm{const.} \tag{10}$$

The discrete flux representation in the α/β plane is created by inserting the switching state dependent voltage $\vec{v}_{\alpha\beta}$ from (6) into the flux integral (10) and using τ as the discrete turn-on time interval for a given switching state.

$$\vec{\Psi}_{\alpha\beta} = \mathbf{D} \cdot \left[\begin{pmatrix} q_1 \\ q_2 \\ q_3 \end{pmatrix} \frac{V_{\mathrm{DC}}}{2} - \begin{pmatrix} q_1^2 \\ q_2^2 \\ q_3^2 \end{pmatrix} \Delta V_{\mathrm{NP}} \right] \cdot \tau \tag{11}$$

To fulfill the constant flux constraint, the flux vector must adhere to (12) at all times.

$$\vec{\Psi}_{\alpha\beta} = \vec{\Psi}_{\alpha\beta,set} \tag{12}$$

According to (11), the error caused by the neutral point voltage deviation can be eliminated by adjusting the switching times τ_j. To compensate for the voltage error, an additional time interval $\Delta\tau$ is included in (13) to satisfy (12).

$$\left[\begin{pmatrix} q_1 \\ q_2 \\ q_3 \end{pmatrix} \frac{V_{\mathrm{DC}}}{2} - \begin{pmatrix} q_1^2 \\ q_2^2 \\ q_3^2 \end{pmatrix} \Delta V_{\mathrm{NP}} \right] \cdot (\tau + \Delta\tau) = \begin{pmatrix} q_1 \\ q_2 \\ q_3 \end{pmatrix} \cdot \frac{V_{\mathrm{DC}}}{2} \cdot \tau \tag{13}$$

Each row of the vector equation can be solved independently to determine the error caused by its particular component. Since no switching states are used that include both states -1 and +1, the solution is uniquely determined by any row containing $q_i \neq 0$.

$$\left[\frac{V_{\mathrm{DC}}}{2} - \Delta V_{\mathrm{NP}} \cdot q_i \right] \cdot (\tau + \Delta\tau) = \frac{V_{\mathrm{DC}}}{2} \cdot \tau \tag{14}$$

The neutral point voltage error compensation can be achieved by solving this equation for $\Delta\tau$ or the new total switching time $\tau^* = \tau + \Delta\tau$.

$$\tau^* = \tau + \Delta\tau = \tau \cdot \frac{\frac{V_{\mathrm{DC}}}{2}}{\frac{V_{\mathrm{DC}}}{2} - q_i \cdot \Delta V_{\mathrm{NP}}} \tag{15}$$

After determining the new turn-on times for the non-zero voltage vectors, the zero-voltage time must also be adjusted

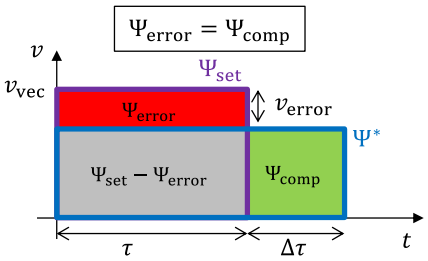

FIGURE 10. Graphical illustration of the flux compensation approach.

TABLE 3. Simulation Parameters

V_{DC}	ΔV_{NP}	$V_{LL,set}$	$C_{1,2}$	$\hat{i}_{out}$
800 V	50 V	300 V	1 mF	$\approx$ 100 A

so that the switching period is not exceeded. Fig. 10 provides a graphical illustration of the proposed compensation strategy. The output voltage vector length differs from its original amplitude v_{vec} by v_{error} due to the neutral point voltage deviation. Consequently, the required flux Ψ_{set} is either exceeded or undercut. Thus, the time interval τ is adjusted by $\Delta\tau$ to compensate for the flux error. The compensation approach is considered successful, when the equation $\Psi_{comp} = \Psi_{error}$ is met, resulting in Ψ^* being equal to Ψ_{set}.

C. EVALUATION OF THE PROPOSED NEUTRAL POINT VOLTAGE ERROR COMPENSATION STRATEGY

The proposed compensation approach is evaluated using a PLECS simulation model of an ANPC inverter. This model includes a reconfigured space vector modulator and two different realizations of the DC-link. First, simulation results with a constant deviation of the neutral point voltage are presented to validate the mathematical derivations for the compensation approach. The constant voltage deviation is achieved by utilizing ideal voltage sources in place of capacitors in the DC-link. Subsequently, the ideal voltage sources are replaced by capacitors to demonstrate the actual behavior of the neutral point. All simulations analyze a failure of phase leg A using the parameters in Table 3.

1) SIMULATION WITH IDEAL VOLTAGE SOURCES

The deviation in neutral point voltage is consistently set at a value of $\Delta V_{NP} = 50$ V. This results in a decrease of 50 V in the capacitor voltage V_{C1}, whereas V_{C2} increases by the same value. Without utilizing the proposed compensation method, the voltage deviation causes a distortion of the actual voltage vectors and thus a distortion of the output voltage trajectory, as predicted in Fig. 8, see Fig. 11 (left). By implementing the proposed compensation strategy to the reconfigured space vector modulator, this distortion is eliminated. However, the actual voltage vectors remain distorted, as shown in Fig. 11 (right). The fluctuation in the motor flux during uncompensated operation causes distorted currents, whereas the proposed compensation strategy generates undistorted

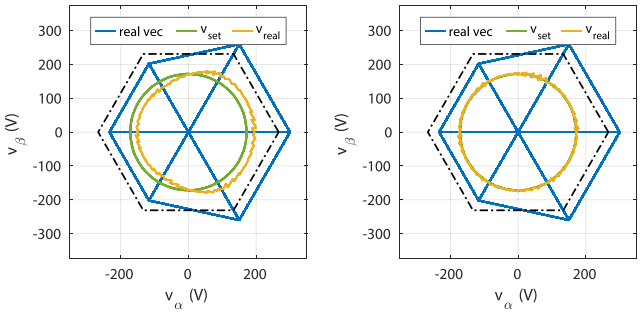

FIGURE 11. Output voltage in the α/β plane for constant neutral point voltage deviation $\Delta V_{NP} = 50$ V without (left) and with (right) voltage error compensation.

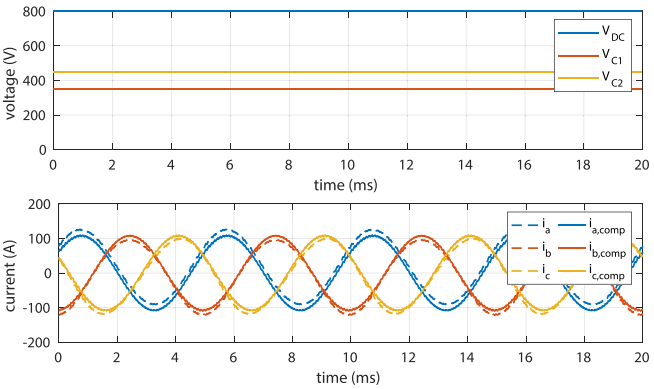

FIGURE 12. Line voltages and phase currents for constant neutral point voltage deviation $\Delta V_{NP} = 50$ V with (solid lines) and without (dashed lines) voltage error compensation.

symmetrical phase currents by maintaining constant flux, as demonstrated in Fig. 12.

2) SIMULATION WITH DC-LINK CAPACITORS

The simulation with constant voltage sources is required to validate the general functionality of the proposed compensation strategy. However, it does not describe the actual neutral point behavior in a real inverter setup. In contrast, when operating the inverter with real DC-link capacitors, the neutral point voltage can easily drift from its initial value if the DC-link capacitors are not stressed evenly. This effect is observed not only for unbalanced capacitor voltages (refer to (8)), but also when using the proposed compensation method. With the compensation approach, output voltage vectors shortened by ΔV_{NP} are assigned to longer turn-on times τ. As a result, the DC-link capacitor with reduced voltage is stressed more than in symmetrical operation. Analogously, the other DC-link capacitor is stressed less in the same scenario. This causes an offset in the neutral point current, resulting in a drift of the neutral point voltage. Fig. 14 shows an increasing gap between V_{C1} and V_{C2}, which leads to an increasing deformation of the hexagon in Fig. 13, indicated by the purple arrows. The functionality of the compensation approach is distinct, since the flux is kept constant even with increasing

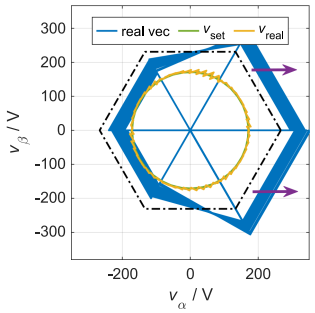

FIGURE 13. Output voltage in the α/β plane for variable neutral point voltage deviation (start: $\Delta V_{NP} = 50$ V) with voltage error compensation resulting in a neutral point voltage drift.

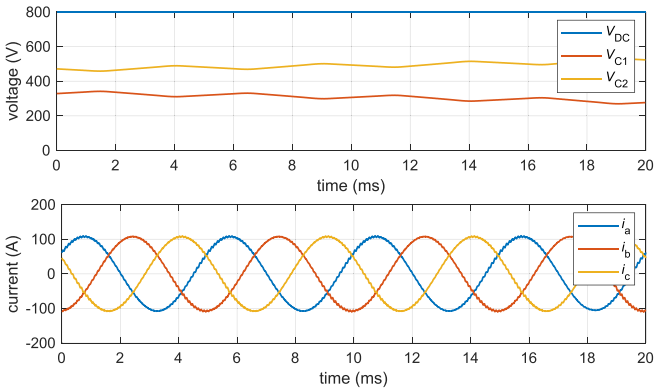

FIGURE 14. Line voltages and phase currents for variable neutral point voltage deviation (start: $\Delta V_{NP} = 50$ V) with voltage error compensation.

ΔV_{NP}. Furthermore, in addition to the dc-component, the voltage error caused by a high voltage ripple at low frequencies in reconfigured failure mode [19] is also compensated. This is accomplished by using the actual neutral point voltage to calculate $\Delta\tau$ in any switching period. However, stationary operation is impossible without an additional neutral point balancing strategy. In contrast to common neutral point balancing techniques for the normal operation of a 3-level inverter, there are no redundant vectors available to adjust the DC-link capacitor stress in reconfigured failure mode. Therefore, a new neutral point balancing approach for reconfigured 3-level inverter operation in failure mode is presented in the next section. Prior to this, the limitations of the proposed error compensation strategy are addressed.

D. LIMITATIONS OF THE PROPOSED NEUTRAL POINT VOLTAGE COMPENSATION APPROACH

The maximum feasible line voltage is limited by the length of the six voltage vectors in the space vector hexagon. In order to extend the amplitude of the available vectors in the negative half of the α/β-plane for $\Delta V_{NP} > 0$ by increasing the related switching time, a voltage reserve of ΔV_{NP} is required. Accordingly, the maximum line voltage for symmetric operation can be determined through (16).

$$\hat{v}_{set,max} = \frac{\frac{V_{DC}}{2} - |\Delta V_{NP}|}{\sqrt{3}} \tag{16}$$

A second limitation pertains to the power semiconductor's blocking capability V_{br}, which must surpass the capacitor voltages according to (17)

$$V_{br} > \frac{V_{DC}}{2} + |\Delta V_{NP}|. \tag{17}$$

Since the magnitude of in ΔV_{NP} is small in a real DC-link, none of the limitations pose significant restraints on the operation of the inverter, as long as a neutral point control mechanism is implemented. The following section presents an approach for developing a neutral point voltage controller for the reconfigured failure mode of neutral point clamped 3-level inverters.

TABLE 4. Symbols Used to Derive the Neutral Point Balancing Strategy

Symbol	Description
$f(\varphi)$	linearization function
K, A, B	coefficients in linearization function
$\Delta V_{\alpha\beta}$	voltage shift applied by the controller
$\Delta V^{*}_{\alpha\beta}$	linearized voltage shift applied by the controller
$\Delta V^{**}_{\alpha\beta}$	lin. and rotated voltage shift applied by the controller
$\overrightarrow{\Delta v}^{**}_{\alpha\beta}(t)$	voltage applied to the inverter
$i_{rel,set}$	set neutral point current ratio

IV. NEUTRAL POINT BALANCING STRATEGY IN RECONFIGURED FAILURE MODE

In reconfigured failure mode operation, the neutral point control strategies discussed in literature are no longer feasible due to the absence of redundant short vectors in the space vector diagram (see Section II-D). Therefore, this section presents a strategy, which is capable of balancing the neutral point voltage for 3-level inverters in reconfigured failure mode. The most important symbols used to describe this method are listed in Table 4.

A. NEUTRAL POINT CONTROL STRATEGY BY ADDING A PHASE ANGLE DEPENDENT DC COMPONENT

1) GENERAL CONROLLER DESIGN

The proposed neutral point control strategy is based on manipulating the neutral point current. As depicted in Figs. 13 and 14, a shift in the Clarke-transformed output voltage v_{ab} towards the α-direction affects the neutral point current, resulting in an increase in ΔV_{NP}. Now, the same mechanism is used to control the neutral point current and eliminate ΔV_{NP}. Therefore, a controller structure as shown in Fig. 15 is implemented. The proposed controller is a neutral point voltage controller with integrated neutral point current control. The neutral point voltage (which is equivalent to V_{C2}) is the input value. First, the mean value of ΔV_{NP} within a fundamental period is calculated as the control deviation. The mean value

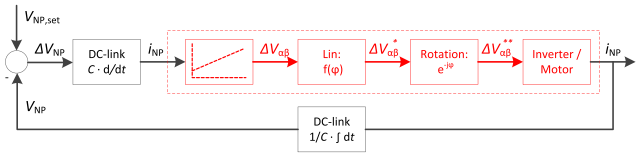

FIGURE 15. Schematic of the neutral point controller.

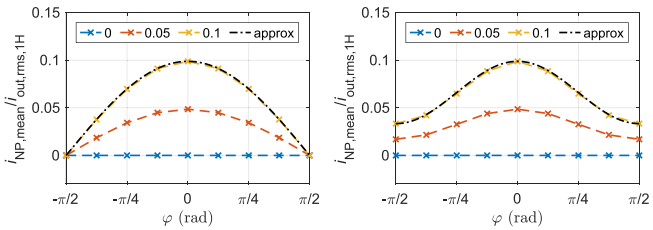

FIGURE 16. Feedforward current controller output for three different default values without (left) and with (right) vector rotation. The current ratio is determined by dividing the mean neutral point current by the rms value of the phase current's first harmonic.

is necessary for maintaining constant flux by disregarding the voltage ripple for symmetry reasons. ΔV_{NP} is converted to a neutral point current using the capacitor equation. A proportional integral (PI) current controller then calculates the voltage shift in the α/β plane $\Delta V_{\alpha\beta}$ required to compensate the previously calculated neutral point current according to (18) for a phase angle of $\varphi = 0$.

$$\Delta V_{\alpha\beta}(t) = K_{\mathrm{P}} \cdot \left(\Delta V_{\mathrm{NP}}(t) + \frac{1}{T_{\mathrm{N}}} \int_0^t \Delta V_{\mathrm{NP}}(\tau)\mathrm{d}\tau \right) \tag{18}$$

If the phase angle is not equal to zero, linearization and rotation in the α/β plane are required. Both principles are explained in more detail in this section. By applying the final voltage shift $\Delta V^{**}_{\alpha\beta}$ to the inverter, the predicted neutral point current attunes. This neutral point current results in a change in the neutral point voltage, which is measured and used to calculate the DC-link voltage deviation.

2) VECTOR ROTATION

Investigations show that the effect of $\Delta V_{\alpha\beta}$ on the neutral point current depends on the power factor. The sensitivity on the neutral point current increases as the phase angle approaches $\varphi = 0$. However, a pure shift in the α-direction in case of a failure in phase leg A is effective for most operating points but it is not applicable for phase angles close to $\varphi = \pm\frac{\pi}{2}$, see Fig. 16 (left). The problem is also present when shifting towards $\varphi_x \pm \frac{\pi}{2}$ $(x = \mathrm{a}, \mathrm{b}, \mathrm{c})$ for a failure in phase leg B ($\varphi_{\mathrm{b}} = \frac{2\pi}{3}$) or a failure in phase leg C ($\varphi_{\mathrm{c}} = \frac{4\pi}{3}$). The strategy proposed to maintaining neutral point current control at $\varphi = \pm\frac{\pi}{2}$ is the rotation of the voltage shift vector by the negative phase angle $-\varphi$ according to (19).

$$\overrightarrow{\Delta v}^{**}_{\alpha\beta}(t) = \overrightarrow{v}_{\alpha\beta}(t) + f(\varphi) \cdot \Delta V_{\alpha\beta}(t) \cdot e^{\mathrm{j}(\varphi_x - \varphi)} \tag{19}$$

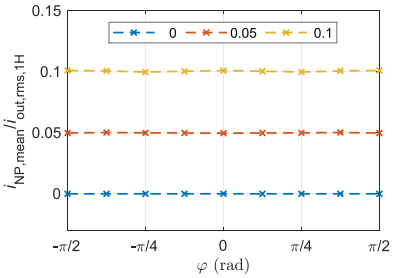

FIGURE 17. Feedforward current controller output for three different default values with vector rotation and linlinearization.

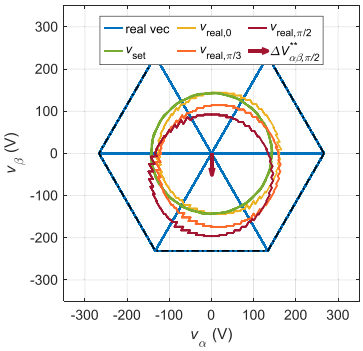

FIGURE 18. Application of the open loop neutral point control strategy for constant neutral point current at three different phase angles.

The linearization function $f(\varphi)$ is explained below. To assess the control system's behavior, first an ideally balanced DC-link with $\Delta V_{\mathrm{NP}} = 0\,\mathrm{V}$ is considered in Fig. 16. The current controller is operated in open loop mode by setting a default value for the neutral point current ratio $i_{\mathrm{NP,mean,set}}/i_{\mathrm{out,rms,1H}}$. Without the vector rotation, the nonlinearity of the neutral point current is given by $K \cdot \cos(\varphi)$ which is depicted as a dash-dotted approximation. By utilizing the vector rotation, the neutral point current ratio can be expressed as $A + B \cdot \cos^2(\varphi)$ which is also represented as a dash-dotted line in Fig. 16 (right). The constant value A enables neutral point control to be achieved at $\varphi = \pm\frac{\pi}{2}$.

3) LINEARIZATION

The non-linear behavior can be linearized by applying (20), which results in $\Delta V^{*}_{\alpha\beta} = f(\varphi) \cdot \Delta V_{\alpha\beta}$ (see Fig. 15).

$$f(\varphi) = \frac{1}{A + B \cdot \cos^2(\varphi)} \tag{20}$$

By utilizing this experimentally obtained linearization approach, a constant value for the neutral point current, independent of the phase angle, can be established in the open loop control, as demonstrated in Fig. 17. However, the absolute value of $\Delta V^{**}_{\alpha\beta} = f(\varphi) \cdot \Delta V_{\alpha\beta} \cdot e^{\mathrm{j}(\varphi_x - \varphi)}$ increases with higher values of φ for the same default neutral point current, as shown in Fig. 18. This causes limitations in the maximum control range, which will be discussed later, see Fig. 23.

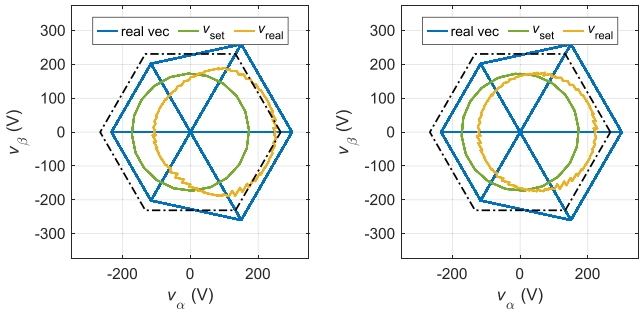

FIGURE 19. Output voltage in the α/β plane for constant neutral point voltage deviation $\Delta V_{NP} = 50\,V$ with neutral point voltage control without (left) and with (right) voltage error compensation.

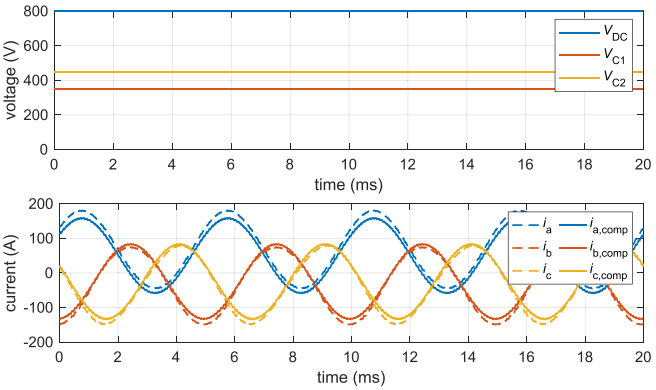

FIGURE 20. DC-link voltages and line currents for constant neutral point voltage deviation $\Delta V_{NP} = 50\,V$ with neutral point voltage control, with (solid lines) and without (dashed lines) voltage error compensation.

B. EVALUATION OF THE PROPOSED NEUTRAL POINT BALANCING STRATEGY

Now the proposed neutral point voltage control strategy can be used alongside the approach for compensating neutral point voltage deviations. A combination of both methods is required during the start-up balancing process and to compensate for the dynamic neutral point voltage ripple, which can have a significant impact on output voltages and currents at low speeds [19]. As with the evaluation of the voltage deviation compensation technique, the first simulation results are presented using constant ΔV_{NP} achieved by ideal voltage sources in the DC link. Subsequent simulations, which incorporate DC-link capacitors, demonstrate the effectiveness of the combined utilization of the proposed strategies.

1) SIMULATION WITH IDEAL VOLTAGE SOURCES

The simulations with ideal voltage sources are performed with a proportional controller by setting $\frac{K_P}{T_N} = 0$ to obtain constant controller behavior over time. The achieved results for a phase leg A failure are presented in Fig. 19. In the left figure, only the neutral point voltage control is activated which results in a constant shift of $\Delta V^*_{\alpha\beta} \cdot e^{-j0}$. The non-circular output voltage trajectory is caused by the neutral point voltage deviation ΔV_{NP}. The neutral point control adds an additional shift in α-direction. As in Fig. 11, this generates harmonics in the flux. These flux distortions are eliminated by applying the proposed voltage error compensation method, as shown in the right figure. By combining both strategies, a defined neutral point current can be set to balance the DC-link capacitor voltages without adding harmonics to the flux. The voltage offset $\Delta V^{**}_{\alpha\beta}$ has no effect on the electric machine's flux or performance. Rather, it only serves to transfer capacitor charge in the DC-link. Fig. 20 shows the DC-link voltages and output currents for the operation with neutral point control, with and without voltage error compensation. Consistent with the representation in the α/β-plane, the solid lines depicting the currents with voltage error compensation exhibit viewer harmonics.

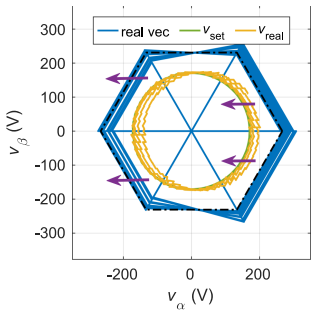

FIGURE 21. Output voltage in the α/β plane for variable neutral point voltage deviation (start: $\Delta V_{NP} = 50\,V$) with neutral point voltage control and voltage error compensation.

2) SIMULATION WITH DC-LINK CAPACITORS

The simulation model with the proportional-integral controller, as depicted in Fig. 15, is now operated with DC-link capacitors to replicate the neutral point behavior under realistic conditions. The control logic reduces the neutral point voltage deviation by shifting the output voltage trajectory in α direction, starting from a neutral point voltage deviation of $\Delta V_{NP} = 50\,V$ in Fig. 21. As ΔV_{NP} decreases, $\Delta V^{**}_{\alpha\beta}$ is also reduced until the capacitor voltages are perfectly balanced. The balancing process is indicated by purple arrows. The voltage ripple displayed in Fig. 22 does not affect the neutral point control strategy because the mean value of the neutral point voltage is used to calculate the control deviation ΔV_{NP}. Otherwise, additional harmonics would appear due to a half wave dependent distortion of the output voltage trajectory. Nevertheless, the voltage compensation method does consider the time-dependent voltage ripple and reduces harmonics by compensating $\Delta V_{NP}(t)$ at any time.

However, depending on the boundary conditions, the proposed neutral point balancing strategy can also serve the reverse objective. By utilizing the time-varying value of $\Delta V_{NP}(t)$ instead of the mean value, the voltage ripple at the neutral point can be diminished by increasing the flux harmonics. To achieve this objective, the current at the neutral point is manipulated at any given time to reduce the ripple. This

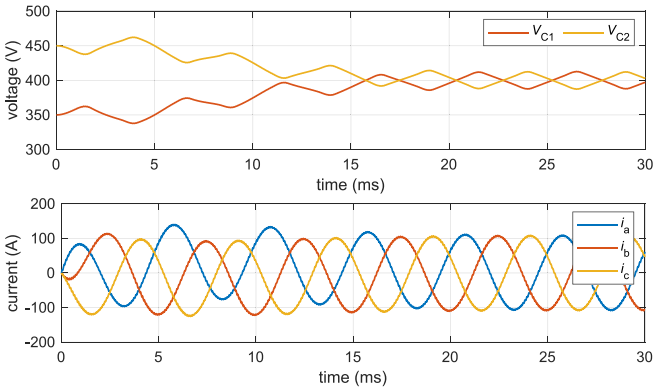

FIGURE 22. DC-link voltages and line currents for variable neutral point voltage deviation ($\Delta V_{NP,start} = 50$ V) with neutral point voltage control and voltage error compensation.

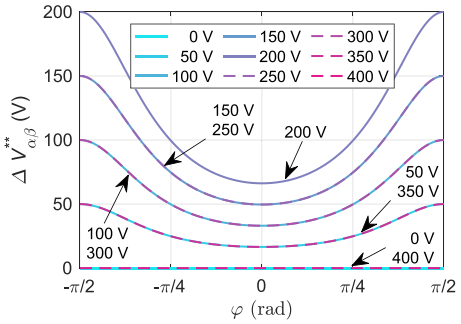

FIGURE 23. Maximum value of $\Delta V^{**}_{\alpha\beta}$ depending on the phase angle for different line-to-line voltages with the restriction of linear controller behavior.

approach may have advantages in certain operating points at low speed and high current [19] to reduce capacitor stress.

C. LIMITATIONS OF THE PROPOSED NEUTRAL POINT BALANCING APPROACH

Investigations have revealed two boundaries for the proposed neutral point balancing approach. One limit is defined by the boundaries of the space vector hexagon. According to (20), the maximum voltage shift $\Delta V^{**}_{\alpha\beta}$ is required for the phase angles $\varphi = \pm\frac{\pi}{2}$. Hence, the maximum attainable voltage shift is defined by (21). It further decreases when an imbalance ΔV_{NP} is taken into account. For high output voltages, there is a limited voltage reserve to control the neutral point current. Thus, the controller is only fully functional if $\overrightarrow{\Delta v}^{**}_{\alpha\beta}(t)$ is not limited by the boundaries of the distorted space vector hexagon. In effect, the proportional gain of the controller is limited for high line voltage magnitudes.

$$\Delta V^{**}_{\alpha\beta}\left(\varphi = \pm\frac{\pi}{2}\right) < \frac{V_{DC}}{2\sqrt{3}} - \hat{v}_{set} \tag{21}$$

The second limitation, which is defined by (22) pertains to minor output voltages. Although the control strategy is not principally limited in this case, investigations have revealed that the linearity of the neutral point current control is only achieved when the coordinate origin of the α/β-plane is within the output voltage trajectory.

$$\Delta V^{**}_{\alpha\beta}\left(\varphi = \pm\frac{\pi}{2}\right) < \hat{v}_{set} \tag{22}$$

Fig. 23 illustrates the maximum voltage shift $\Delta V^{**}_{\alpha\beta}$ for both constraints combined. Each graph represents the phase angle dependent voltage shift to be applied by the controller to achieve the maximum constant neutral point current possible. The limits specified by (21) and (22) can be taken directly from the figure at $\varphi = \pm\frac{\pi}{2}$ for different output voltages. In accordance with (20), a decrease in the absolute value of φ leads to a lower required voltage shift for maintaining a constant neutral point current.

$$\left.\frac{i_{NP,mean}}{i_{out,rms}}\right|_{\varphi=0} \approx 0.6\,\frac{\%}{V}\cdot\Delta V^{**}_{\alpha\beta}\,(\varphi = 0) \tag{23}$$

$$\left.\frac{i_{NP,mean}}{i_{out,rms}}\right|_{\varphi=\pm\frac{\pi}{2}} \approx 0.2\,\frac{\%}{V}\cdot\Delta V^{**}_{\alpha\beta}\left(\varphi = \pm\frac{\pi}{2}\right) \tag{24}$$

The control capability remaining close to the presented limits can be expressed by the sensitivity of the neutral point current to the voltage shift, which is given in (23) and (24) for the present simulation model. Therefore, even with a phase angle of $\varphi = \pm\frac{\pi}{2}$ and an applied line-to-line voltage of 10 V or 390 V, it is possible to use 2 % of the output current to control the neutral point voltage. Since the neutral point current stress increases with the magnitude of the phase current, practical inverter operation is not significantly restricted, neither at low nor at high output voltage. Another limitation arises from the inverter's maximum current capability. The proposed neutral point balancing approach is based on applying an offset to the current in the faulty phase leg. It is crucial to ensure that the current remains within the specified limits of the inverter and the machine.

V. MEASUREMENT RESULTS

In this section, measurement data is provided to validate the proposed voltage error compensation and neutral point balancing strategy. To perform these measurements, an 'Interior Permanent Magnet Synchronous Machine' (IPMSM) controlled by a 3-phase, 3-level ANPC inverter is used.

A. ANPC INVERTER AND ELECTRIC MACHINE TEST BENCH

The ANPC inverter features air-cooled 650 V TO-247 SiC-MOSFETs, allowing for DC-link voltages up to 800 V. The DC-link is mounted on the bottom of the power board. An FPGA controller integrated in a dSPACE system performs the space vector modulation and transmits the PWM signals to the inverter by using fiber-optic cables. The inverter setup is depicted in Fig. 24. The ANPC inverter drives the 800 V IPMSM shown in Fig. 25 which is coupled to another smaller electric machine. Voltage and current probes are attached to each phase on the AC-side of the inverter and to the DC-link.

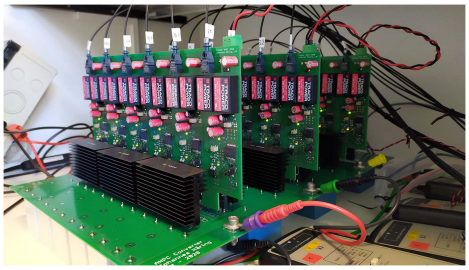

FIGURE 24. 3-phase 3-level ANPC inverter setup.

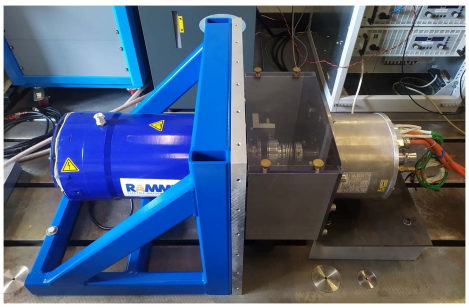

FIGURE 25. Test bench with 800 V IPMSM (left) and load machine (right).

TABLE 5. Design Parameters of the Complete Test Bench

Parameter	Symbol	Value
ANPC Inverter		
DC-link capacitance	C_{DC}	740 µF
max. DC-link voltage	$V_{\mathrm{DC,max}}$	800 V
max. phase current	$I_{\mathrm{max,rms}}$	25 A
IPMSM		
number of pole pairs	p	4
stator inductance	$L_{\mathrm{d}}/L_{\mathrm{q}}$	350/705 µH
permanent magnet flux	Ψ_{PM}	140 mVs
stator resistance	R_{s}	10 mΩ
max. line voltage	V_{max}	480 V
max. phase current	$I_{\mathrm{max,rms}}$	350 A
max. power	P_{max}	220 kW
nominal speed	n_{N}	4060 min^{-1}

The main design parameters of the entire test bench are listed in Table 5. Intentionally applying a certain voltage deviation to the DC link runs the risk of damaging the power semiconductors by overvoltage. To mitigate this risk, the DC-link voltage is limited to 400 V for all measurements. Nonetheless, the observed effects are equally applicable at higher DC-link voltages.

B. NORMAL OPERATION WITH NEUTRAL POINT VOLTAGE DEVIATION

Before discussing the proposed neutral point balancing and voltage error compensation strategies in detail, the normal 3-phase operation with 27 available space vectors is observed. With ideally balanced capacitor voltages, any of the 12 small vectors that span the inner space vector hexagon has the same length. However, when a positive constant voltage deviation $\Delta V_{\mathrm{NP}} > 0$ is applied to the DC-link by connecting a voltage supply to each of the capacitors C_1 and C_2, the vectors representing the switching states that contain -1 and 0 (e.g. $\{0, -1, -1\}$) are lengthened by ΔV_{NP}. Analogously, the vectors representing switching states with 0 and +1, such as $\{+1, 0, 0\}$), are truncated by ΔV_{NP}. This is illustrated by the Clarke-transformed measured line voltages in Fig. 26 for balanced and unbalanced operation. As depicted in Fig. 27, the voltage deviation does not affect the phase currents because the errors of shortened and elongated vectors cancel out each other during one pulse period due to equal switching times in symmetric SVM mode. Hence, there is no need to compensate for any voltage error within the inner space vector hexagon. However, further investigation showed that this is not true for the operation in the outer regions of the hexagon. Vectors of intermediate length (e.g. $\{+1, -1, 0\}$) also experience a deformation and have no counterpart to compensate for their error. Since this paper primarily addresses the operation in reconfigured failure mode, further analysis of this topic is not provided.

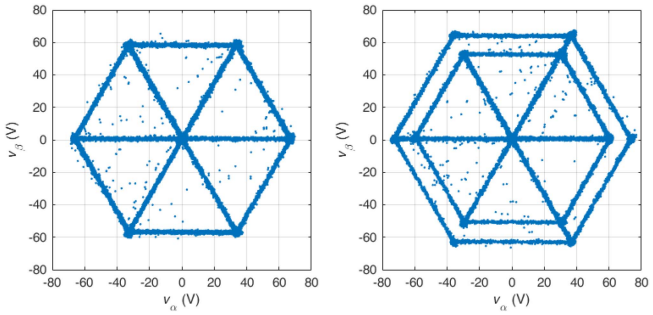

FIGURE 26. Measured line-to-neutral point voltages in the α/β-plane for normal operation with 12 short base vectors without (left) and with (right) neutral point voltage deviation of $\Delta V_{\mathrm{NP}} = 10$ V in the same operating point.

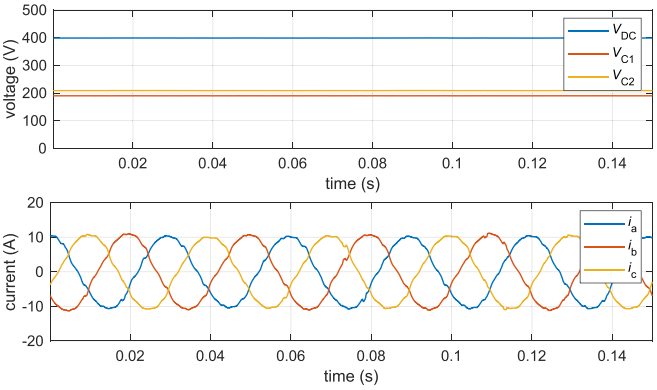

FIGURE 27. Measured DC-link voltages and phase currents in normal operation mode with a neutral point voltage deviation of $\Delta V_{\mathrm{NP}} = 10$ V without voltage error compensation.

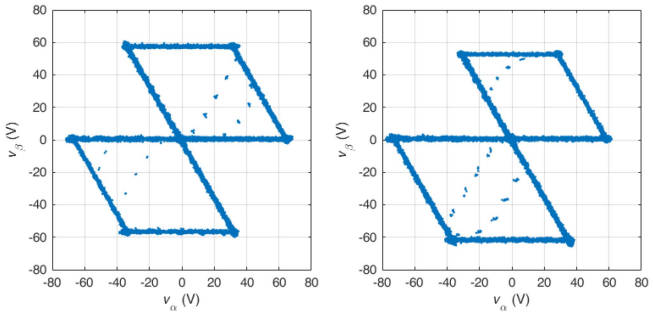

FIGURE 28. Measured line-to-neutral point voltages in the α/β-plane for reconfigured failure mode operation with 6 short base vectors without (left) and with (right) neutral point voltage deviation of $\Delta V_{NP} = 10\,V$ in the same operating point.

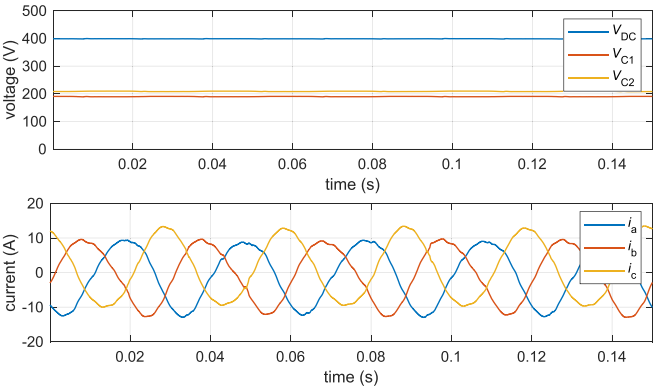

FIGURE 29. Measured DC-link voltages and phase currents in reconfigured failure mode with a neutral point voltage deviation of $\Delta V_{NP} = 10\,V$ without voltage error compensation.

C. VOLTAGE ERROR COMPENSATION IN RECONFIGURED FAILURE MODE

In reconfigured failure mode, there are six non-zero vectors available that depend on which phase leg is faulty. For any of the shown measurements, phase leg C is selected as the faulty leg. Due to the permanent neutral point connection of phase leg C, only small vectors $\{k, l, 0\}$ with $k, l \in [-1, 0, +1]$ are admissible. Fig. 28 illustrates the line-to-neutral point voltages measured and transformed into the α/β-plane for both symmetric operation and asymmetric operation, considering a neutral point deviation of $\Delta V_{NP} = 10\,V$. The measurement demonstrates that the lengths of the vectors vary due to the presence of the neutral point deviation, which is in line with the prediction made in Fig. 9 (right). This results in distorted phase currents due to an error in the applied flux, as shown in Fig. 29. Applying the proposed compensation strategy for neutral point voltage deviations restores symmetry in the three-phase AC currents, as demonstrated in Fig. 30. These results align with the simulated data presented in Section III. The measurements provided substantiate the efficacy and functionality of the proposed approach. The deviation of the voltage vectors towards the direction of phase C ($\varphi_c = \frac{4\pi}{3}$) is reflected by the distortion of line currents in the α/β-plane in the absence of compensation. In comparison, the current

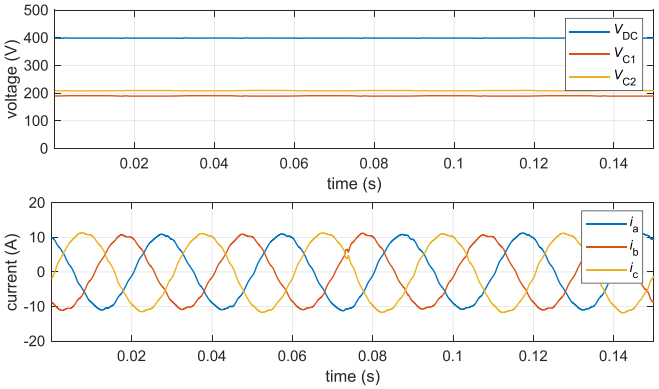

FIGURE 30. Measured DC-link voltages and phase currents in reconfigured failure mode with a neutral point voltage deviation of $\Delta V_{NP} = 10\,V$ with the proposed voltage error compensation.

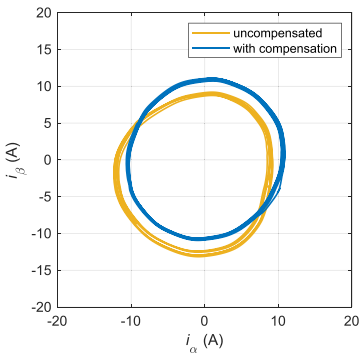

FIGURE 31. Measured phase currents in the α/β plane with and without voltage compensation for $V_{DC} = 400\,V$ and $\Delta V_{NP} = 10\,V$.

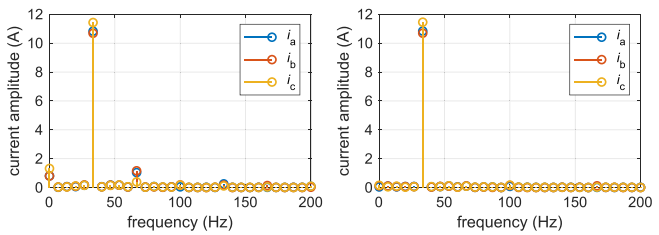

FIGURE 32. Phase current spectra for both measurements without (left) and with (right) voltage compensation for $V_{DC} = 400\,V$ and $\Delta V_{NP} = 10\,V$.

trajectory that is corrected by the flux compensation method forms a nearly perfect circle, see Fig. 31. A quantitative analysis of the reduction in harmonics is provided through the phase current spectra shown in Fig. 32. By implementing the proposed voltage compensation method, nearly all harmonics are eliminated. Without compensation, the total harmonic distortion of the phase currents is calculated to be 9.6 %. The second and fourth harmonics contribute the most to the harmonic content. Furthermore, the DC-component discussed in (8) is apparent. With compensation, THD is reduced to 4.3 %. However, without implementing an additional neutral point balancing strategy, the neutral point voltage will drift from its initial value when using the voltage error compensation

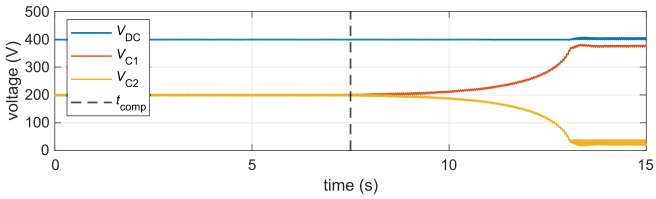

FIGURE 33. Measured DC-link voltages with activation of the voltage error compensation strategy at t_{comp} without additional neutral point control.

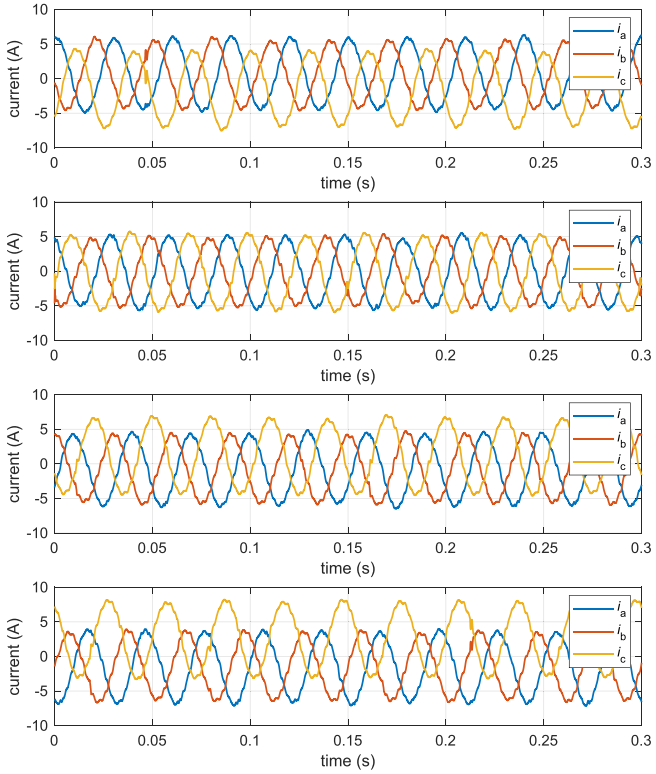

FIGURE 34. Measured phase currents for different neutral point current ratio settings $i_{rel,set} = \{-0.075, 0, +0.075, +0.15\}$ (from top to bottom).

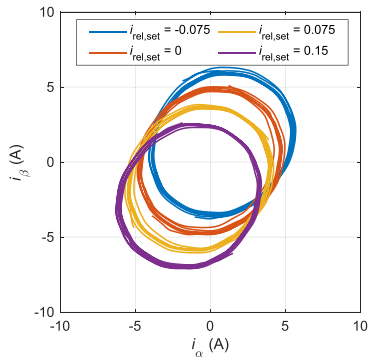

FIGURE 35. Measured phase currents in the α/β plane for different neutral point current ratio settings using feedforward control.

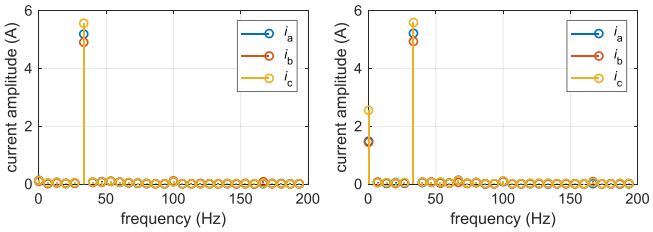

FIGURE 36. Measured phase current spectra for the neutral point current ratio settings $i_{rel,set} = 0$ (left) and $i_{rel,set} = +0.15$ (right).

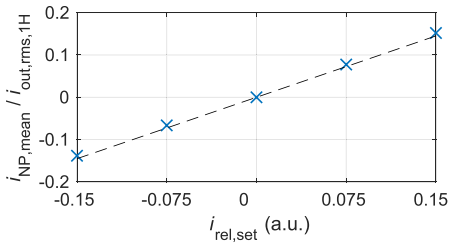

FIGURE 37. Measured values of the feedforward controlled neutral point current ratio to proof linearity regarding the set default values.

approach, as shown in Fig. 33. To address this behavior, the proposed neutral point control method is implemented in the inverter control. Measurement data is provided in the following section. The neutral point is not connected to a fixed DC potential anymore for any of the subsequent measurements. Using a single DC power supply for the DC-link facilitates imbalances in the capacitor voltages that must be eliminated.

D. NEUTRAL POINT VOLTAGE BALANCING IN RECONFIGURED FAILURE MODE

Based on the logic presented in Fig. 15, the neutral point current is controlled by adding a phase-angle dependent offset to the line voltage trajectory in the α/β plane. This voltage shift results in a constant offset in each of the AC-currents. The current flowing through the faulty phase leg, referred to as i_c, experiences the greatest offset, while the other two currents experience an offset in the opposite direction. Fig. 34 displays the line currents for four distinct settings of the neutral point current ratio $i_{rel,set}$ according to (25). All measurements are conducted in the same stationary operating point at one specific phase angle.

$$i_{rel,set} = \frac{i_{NP,mean,set}}{i_{out,rms,1H}} \tag{25}$$

Another significant finding is that the control of the neutral point has no impact on the amplitudes of the AC current. Rather, it merely adds a constant offset. This offset appears as DC-component in Fig. 36. For symmetric operation, only the fundamental frequency has a significant amplitude in the frequency spectrum. A neutral point current ratio setting of $i_{rel,set} = +0.15$ adds a DC-component to each of the phase currents but does not affect the harmonic performance. The current trajectories in the α/β-plane (see Fig. 35) show an offset in the direction of phase C, which is linearly dependent on the current ratio set by the open-loop controller. Fig. 37 displays the linear characteristics of the controller output at the

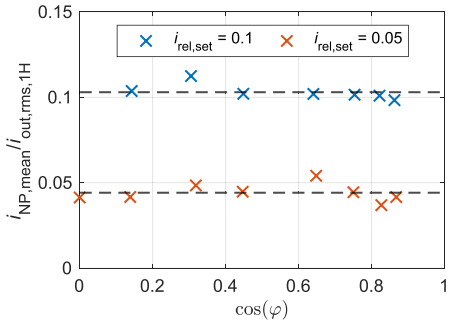

FIGURE 38. Measured neutral point current ratios for various power factors and two different default values using feedforward control.

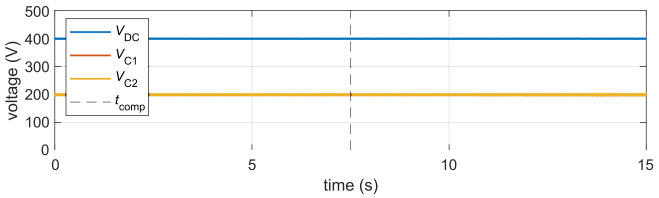

FIGURE 39. Measured DC-link voltages with activation of the voltage error compensation strategy at t_{comp} using closed-loop neutral point control.

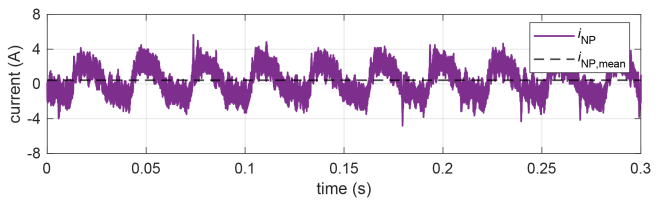

FIGURE 40. Measured neutral point current with current ratio $i_{rel,set} = 0.1$ in a stationary operating point at $i_{out} = 5\,A$, $\varphi = \frac{\pi}{5}$.

same operating points as analyzed in Figs. 34 and 35. Thus, the functionality of the controller is verified for a constant phase angle. Subsequent measurements, as demonstrated in Fig. 38, also confirm the linearity with respect to the phase angle. For the measurement, the open-loop controller was subjected to two specific default current ratio settings, each resulting in a constant measured current ratio at the neutral point despite small deviations. It should be noted that the data points were obtained in different operating points with varying phase current amplitudes ranging from 5 A to 12 A. As a result, the predicted phase current linearity has also been confirmed. In contrast to Fig. 33, by applying the voltage error compensation strategy, the neutral point voltage does not drift away when the full closed loop controller is used. This results in a stable and constant neutral point voltage, as depicted in Fig. 39. To assess the overall stability of the proposed strategy, simulations and measurements were performed in various operating points within the limits of (21) and (22). Results from all tests showed stable behavior. The neutral point current in one stationary operating point with $i_{rel,set} = 0.1$ at constant phase current and phase angle is depicted in Fig. 40. The slight positivity of the mean value inhibits an increase of the neutral point potential.

VI. CONCLUSION

Neutral point clamped 3-level inverters are now competitive solutions for the use in certain BEVs with 800 V DC-link voltage. Especially in the field of autonomous driving vehicles, fault-tolerance is becoming a key aspect in the design of electric powertrains. The treatment of single switch failures can be achieved (fully or partially) by a permanent neutral point connection of the faulty phase leg when using the NPC, ANPC or T-NPC inverter structure. Unlike normal operation, a neutral point voltage deviation entails additional harmonics on the output voltages and currents in reconfigured failure mode. Morevoer, there is currently no neutral point balancing strategy known for this mode of operation. This paper examines the impact of a neutral point voltage deviation on the flux in electric machines and offers a solution to compensate for this error. The introduced method allows to compensate the flux harmonics caused not only by stationary voltage deviations, but also by the dynamic neutral point voltage ripple. Furthermore, a neutral point voltage control strategy is proposed to enable voltage balancing in reconfigured failure mode. Theoretically derived findings are confirmed through simulations and measurements conducted at an 800 V IPMSM machine test bench with a 3-phase, 3-level ANPC inverter. The results of this paper demonstrate the feasibility of a stable dynamic operation of a 3-level neutral point clamped inverter in reconfigured failure mode without neutral point voltage drift and additional harmonics on the phase currents.

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