Novel Figures of Merit for Evaluating the Performance of the Super-Cascode Switch

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ABSTRACT The super-cascode switch (SCS) has gained significant attention in the last decade due to its ability to achieve medium-voltage ratings using low-voltage semiconductors. However, there exists a notable absence of quantitative metrics to effectively evaluate the performance of the SCS. This gap exists because the behavior of the SCS is different from that of a traditional semiconductor switch, and traditional semiconductor performance metrics are not adequate for its evaluation. The present manuscript addresses this gap by introducing new figures of merit that are designed to evaluate the unique characteristics of the SCS. The practical value of these metrics is also demonstrated through a set of experimental studies. By applying these new figures of merit to one of the best-performing SCS configurations described previously in the literature, several opportunities for improvement are revealed. The SCS prototype described in this paper is evaluated experimentally at bus voltage levels up to 3.5 kV and current levels up to 200 A, demonstrating substantial performance improvements relative to the baseline configuration from the literature. These improvements are the result of iterative refinements to the balancing network, which are selected through a process that is informed by the application of the proposed figures of merit.

INDEX TERMS JFET, medium-voltage power module, sic, super-cascode, wide bandgap semiconductors.

I. INTRODUCTION

Medium-voltage (MV) power modules are an essential building block for implementing a wide range of high-power applications, including industrial motor drives, rail traction, renewable energy conversion, and military power conversion. Wide bandgap semiconductors (WBG) hold the potential to further enhance performance in these applications. Low-voltage (LV) WBG semiconductors up to 1.7 kV are already commercialized and widely accepted by the power electronics industry. However, MV WBG semiconductors are still under development and are not yet ready for widespread deployment. Several factors contribute to this limitation, including cost considerations, manufacturability challenges, and the need for improved reliability.

An appealing alternative approach for achieving MV WBG-rated devices in the near term is the super-cascode switch (SCS). This approach utilizes a pseudo-series stack of LV Silicon Carbide (SiC) junction field effect transistors (JFETs) combined with a low voltage (LV) Silicon (Si) MOSFET to control the gating of the series string, as shown in Fig. 1. The
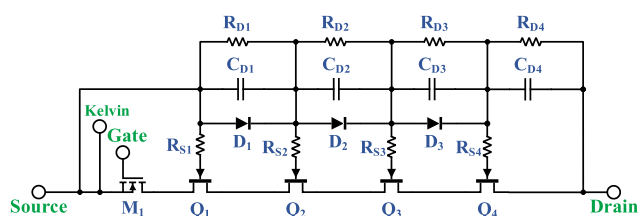

FIGURE 1. Baseline super-cascode schematic studied in this manuscript.

SCS offers a compelling solution because it bypasses many of the challenges associated with MV-rated WBG devices, which accrue from their limited maturity. Implementing an MV-capable switch using mature LV semiconductors offers many advantages, including improved cost-effectiveness, increased device availability, and reduced technical risk.

Although the SCS has been described thoroughly in the literature, somewhat less attention has been given to characterizing and evaluating the performance of this topology. The

present study aims to address this need and thereby improve the overall understanding of the SCS. The contributions of this work are as follows. First, this manuscript introduces new figures of merit that are specifically tailored to the unique characteristics of the SCS. Second, this manuscript evaluates the specific contribution of each passive element within the balancing network to the performance of the SCS. Third, by leveraging the proposed figures of merit, an improved SCS design is proposed. This improved SCS topology is similar to existing configurations described in the literature, but achieves improved performance through refinements to the balancing network. Fourth, this manuscript provides a comprehensive characterization of several variants of the SCS prototype under a wide range of operating conditions. To date, the performance of most SCS implementations has been demonstrated only for a small number of operating conditions.

This manuscript is structured as follows. Section II provides a literature review that summarizes the SCS topologies and associated characterization efforts from previous studies. Section III introduces the newly developed figures of merit, which serve as the foundation for the subsequent analysis. Section IV introduces the specific SCS topology studied in this paper, along with a set of five configuration variants that provide a means to assess the impact of the balancing network components. Section V details the SCS prototype realization and the experimental platform employed in this study, outlining its design and components. Section VI presents the experimental results for the five SCS configuration variants, highlighting their performance characteristics using the aforementioned figures of merit. Section VII provides a summary of findings derived from the analysis of the previous sections. Finally, Section VIII provides the conclusions of this work.

II. LITERATURE REVIEW

Several super-cascode topologies have been identified in the literature, each aiming to enhance the performance by strategically modifying the internal connection of the balancing elements. The first topology was proposed by Friedrich et al. in [1], and it has served as the foundational framework for all subsequent SCS implementations. In this original work, a 1.8 kV SCS was evaluated via double pulse testing (DPT), although the emphasis of the manuscript was focused on the overall operation of the circuit. No special analysis was carried out for each stage other than demonstrating the proper operation of all the semiconductors during the switching transitions. This initial topology was later improved in [2], [3], [4] to enhance the static voltage stability, improve the dynamic performance, and reduce the risk of self-sustained oscillation (SSO) [5], [6]. In [2] and [3], the authors employed a modified DPT circuit with a resistive load in lieu of an inductive load. In this case, the specific performance of each stage was not evaluated. This analysis was performed to demonstrate the faster rise and fall times of the SCS compared to an equivalent IGBT device at the same operating conditions [2].

In [7] and [8], Li et al. proposed an extension to the original topology that makes the leakage current independent of the

number of JFETs in the SCS [7], [8]. The proposed SCS was evaluated via DPT, with the goal of verifying suitable switching transitions at a specific current level. An in-depth analysis of the performance of each individual stage was not pursued in these studies. Subsequent efforts were undertaken to further improve the performance of this topology [9], [10], [11], [12], [13], [14], [15], [16]. For the studies reported in [9], [10], [11], [12], the SCS was only evaluated under a few operating conditions with no specific treatment of the individual stages. In [13], [14], [15], [16], the balancing network of the SCS was optimized to improve the dynamic performance of this topology. However, similar to previous papers, these studies mainly demonstrated the functionality of the SCS under specific operating conditions, without delving into the behavior of the individual stages.

A further enhancement of the original topology was proposed by Ni et al. in [17] to improve the static voltage distribution within the transistors in the SCS. This paper marks the first reported per-stage analysis of the SCS at sub-rated operating conditions. In this study, the authors simulated the static voltage distribution of the SCS at a handful of device current levels. This simulation highlights the balanced voltage distribution across the SCS stages under these conditions. Experimental switching losses were also calculated for the entire SCS under multiple conditions. However, an individual breakdown of per-stage switching losses was not provided. Further advancements of this topology were presented in [18] and [19]. In [18], the per-stage static and dynamic performance of the SCS were visually demonstrated via DPT under one operating condition. However, this demonstration lacked corresponding metrics to quantify the effectiveness of the implementation. This study also quantified the switching losses for the entire SCS across different voltage and current conditions, without separately evaluating the contributions of each stage.

One final topology was introduced in [20] by Gao et al. This topology attempts to improve the SCS performance by reconfiguring the balancing network of the topology described in [2]. Experimental validation of this SCS was also carried out via DPT under a select range of operating conditions. It is important to note that the performance of the individual stages within this SCS was not specifically assessed experimentally. However, via simulation, the per-stage switching losses and the static voltage balance were predicted for the SCS under resistive-load switching conditions. Further enhancements to this topology were also presented in subsequent studies [21], [22], [23], with similar limitations regarding the per-stage analysis provided. Overall, this last topology provides an attractive balance between circuit complexity, layout design, and switching speed. In consideration of these factors, this topology serves as the basis for the SCS derivative topology that is proposed and evaluated in the present paper.

Based on the literature summarized here, it is evident that researchers have identified several important challenges with the behavior of the SCS topology, but have not yet established clear figures of merit to quantify the severity of these challenges or to assess the overall SCS performance.

TABLE 1. Overview Figures of Merit

Figure of Merit	Variable	Performance Assessment	Ideal Value
Normalized Static Voltage	$\widehat{SV}$	Static	1
Normalized Voltage Margin	$\widehat{MF}$	Static/Dynamic	*
Effective Turn-On	ETO	Static/Dynamic	1
Per-Stage Switching Losses (mJ)	E_{SW}	Dynamic	0

* no ideal value, but a positive value, further from zero is preferred

FIGURE 2. Experimental static voltage distribution after turn-off for a SCS based on the topology of Fig. 1.

Additionally, a broad characterization of the SCS across a wide spectrum of operating conditions has yet to be undertaken. The present study aims to address both of these gaps through the introduction of SCS-specific figures of merit along with a comprehensive set of experimental results that serves to showcase the importance of these metrics.

III. FIGURES OF MERIT

Given the unique internal structure of the SCS, a new set of metrics is necessary to effectively evaluate both the static and dynamic performance of this switch. As will be demonstrated, it is crucial to evaluate not only the terminal characteristics of the SCS, but also the internal behavior of each stage. To achieve this comprehensive evaluation, four different figures of merit are proposed in this paper. These metrics are specifically designed to assess the static and dynamic performance of the SCS. Table 1 provides an overview of these figures of merit, along with the type of assessment accomplish by each. A detailed explanation of each figure of merit is provided next.

A. NORMALIZED STATIC VOLTAGE

The term "static voltage" refers to the voltage blocked by a transistor when it is in its off state, after the switching transients have settled. In previous literature, the static voltage distribution of the SCS is typically shown only at the rated voltage of the switch. For example, this is the case in [2], [3], [7] and [9]. While evaluating the SCS at the rated voltage confirms that the device can successfully operate at such voltage levels, this does not represent typical application behavior. In most applications, semiconductor devices are operated at one-half to two-thirds of the rated voltage.

In most super-cascode topologies, each transistor blocks a different static voltage when the voltage applied to the SCS is below the rated voltage. This phenomenon arises as a consequence of the inherent nature of the super-cascode, which involves sequential switching of the internal stages. Furthermore, the static voltage is influenced by the number of stages and the details of the balancing network. Fig. 2 presents an experimental example of the static voltage distribution for a four-stage SCS, utilizing the configuration depicted in Fig. 1. This example presents a turn-off transition conducted under a
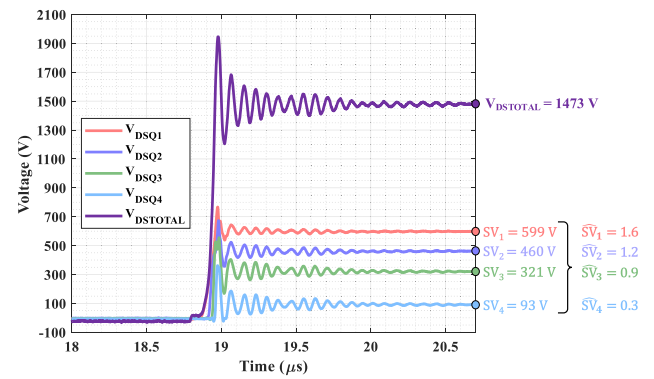
voltage bias near 1.5 kV. It is evident that each of the transistors blocks a different portion of the total voltage. In this case, transistor Q_1 provides the greatest contribution to blocking, and each subsequent transistor blocks progressively less voltage. This observation highlights a typical voltage distribution pattern across the stages of the SCS, although this operating behavior below the rated voltage is not typically shown in the literature.

The unequal distribution of static voltage among the stages of the SCS is undesirable, as it leads to differences in applied stress for each semiconductor element. To quantify the severity of this undesired behavior, the normalized static voltage metric is proposed. This figure of merit is defined in (1):

$$\widehat{SV_n} = \frac{SV_n}{(V_{DSTOTAL}\,/s)} \tag{1}$$

where SV_n corresponds to the static voltage blocked by the stage n; $V_{DSTOTAL}$ corresponds to the total voltage blocked by the SCS; and s corresponds to the total number of stages within the SCS. In an ideal scenario, the stages within the SCS would exhibit a uniform static voltage distribution, resulting in a normalized static voltage of unity for each stage. In practice, the normalized static voltage distribution within the SCS varies as a function of the operating conditions, with distinct values for each stage. In the example of Fig. 2, transistor Q_1 blocks the majority of the voltage (599 V) and therefore $\widehat{SV_1} = 1.6$. Conversely, transistor Q_4 blocks only 93 V and therefore $\widehat{SV_4} = 0.3$.

This figure of merit provides a means to evaluate the contribution of each stage relative to the "expected" balanced case, which is represented by unity. A value greater than unity means that the stage in question is blocking more than its expected share, while a value less than unity means that the stage in question is blocking less than its expected share. Due to the way the normalized static voltage is defined, the sum of the normalized voltages for a given SCS is always equal to the number of stages, as given by (2):

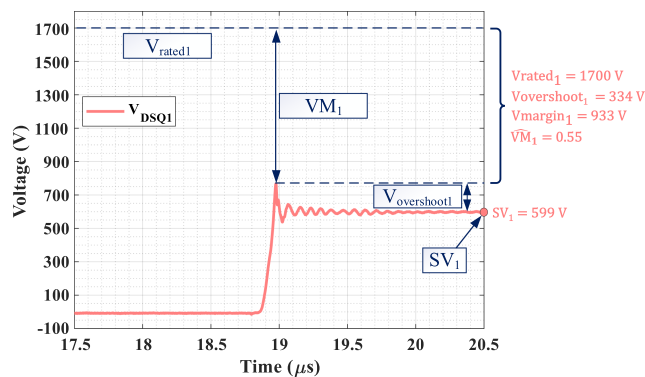$$\sum_{n=1}^{s} \widehat{SV_n} = s \tag{2}$$

FIGURE 3. Experimental turn-off event illustrating the variables necessary for the normalized voltage margin calculation.

B. NORMALIZED VOLTAGE MARGIN

During turn-off, a voltage overshoot typically appears across each stage of the SCS due to the fast edge rates of the transitions. Just like traditional power semiconductors, these transients mainly occur due to the transfer of energy from the commutation inductance to the output capacitance of the active switch. Remarkably, the occurrence of voltage transients during the switching transitions of the SCS has not been thoroughly discussed in the literature, either for the overall switch or for the individual stages. This analysis is very important, because these transients can cause the voltage ratings of the internal JFETs to be exceeded, even when the overall voltage rating of the SCS is not violated. This can lead to catastrophic failure of the SCS or to dielectric degradation of individual internal stages, which will affect the lifespan of the SCS.

Since the stages within the SCS typically block different static voltages, the consequences of voltage transients are different for each stage. For example, the risk imposed by a 300 V transient will be much greater for a JFET that is operating near its rated voltage compared to the risk for a JFET that is operating well below its rated voltage. This illustrates that the per-stage transient behavior of the SCS must be evaluated in the context of the individual per-stage static voltage distribution.

To quantify the impact of voltage transients to the individual stages within the SCS, the voltage margin metric is proposed. This metric is calculated according to (3):

$$VM_n = V_{rated_n} - V_{overshoot_n} - SV_n \qquad (3)$$

where V_{rated_n} corresponds to the rated voltage of the SiC JFET for stage n; $V_{overshoot_n}$ corresponds to the voltage overshoot of stage n; and SV_n corresponds to static voltage of stage n. This figure of merit is calculated for each stage, taking into account three essential factors: the voltage rating of the semiconductor, the magnitude of the voltage overshoot at turn-off, and the static voltage. By considering these parameters, this metric provides an estimation of the remaining margin available from the peak voltage to the rated voltage of the semiconductor. This approach quantifies the risk to each semiconductor within the SCS in a standardized way. Fig. 3 provides an

experimental example of the turn-off transition for transistor Q_1 based on the same example provided in Fig. 2. For this case, a voltage margin of 933 V is determined, which indicates that the maximum voltage expressed across this transistor is well below its rated value.

To increase the generality of this metric, the voltage margin may be normalized as given in (4):

$$\widehat{V}M_n = \frac{VM_n}{V_{rated_n}} \qquad (4)$$

where VM_n is the voltage margin for stage n and V_{rated_n} is the rated voltage of the SiC JFET in question. For the normalized voltage margin, a value approaching zero indicates that the peak voltage is nearing the rated voltage of the semiconductor. On the contrary, a value approaching unity indicates that the transistor is not actively involved in the switching transition, resulting in minimal or no voltage transient. In the case of Fig. 3, a normalized voltage margin of 0.55 is determined, which means that the peak voltage expressed across Q_1 is less than one-half of its rated voltage. While there is no universal ideal value for the normalized voltage margin, higher positive values are preferred. Negative values are undesirable, as they indicate the presence of overshoot values that exceed the rated voltage of the semiconductor elements within the SCS.

C. EFFECTIVE TURN-ON

One phenomenon that has not been detailed in the literature to date is the improper turn-on of individual stages within the SCS. It is believed that this unique behavior has remained unnoticed because it usually manifests only under high-current conditions. Notably, the majority of SCS implementations reported to date have been experimentally evaluated at current levels below 50 A. For instance, the SCS designs in [2], [7], and [18] are rated for 5 A, 23 A, and 36 A, respectively. A singular exception is the SCS developed in [20], capable of handling current levels up to 100 A. In the present study, the prototype SCS is evaluated at current levels up to 200 A. This elevated operating envelope provides the opportunity to uncover current-dependent anomalies such as the improper turn-on behavior discussed here.

Fig. 4 provides an experimental example of an improper turn-on anomaly. In this case, the voltage drop across transistor Q_3 from Fig. 1 is shown for two different current levels. At 50 A, the transistor properly turns-on and its drain-source voltage drops to the expected value of V_{DSonQ3}. However, at 200 A, the transistor fails to turn-on properly, and its drain-source voltage never drops to the expected value of V_{DSonQ3} before the turn-off event. This phenomenon occurs because the balancing network lacks sufficient charge to successfully complete the turn-on transition. This situation is undesirable and poses a significant risk to the SCS. In this case, a dissipation of approximately 71 kW occurs within Q_3 for the entire duration of the conduction interval. Proper turn-on and turn-off behavior of all transistors is essential for the reliable and safe operation of the SCS. The turn-off
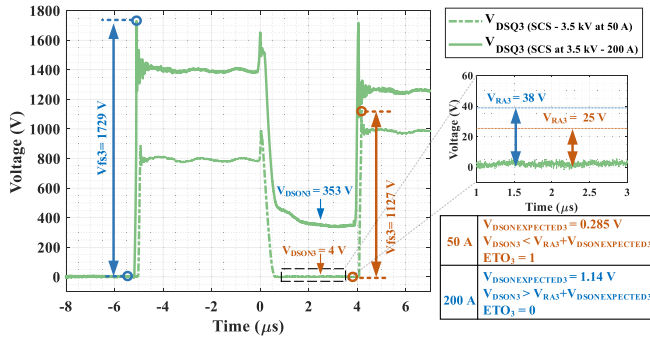
FIGURE 4. Effective turn-on representation.

behavior can be evaluated via the normalized static voltage and the normalized voltage margin, but a metric to evaluate the turn-on performance of all transistors within the SCS is also needed.

To quantify the fundamental turn-on behavior of each stage within the SCS, the effective turn-on metric is proposed. This metric is defined in (5):

$$ETO_n = \begin{cases} 0 \ if \ V_{DSon_n} \geq V_{RA_n} + V_{DSonexpected_n} \\ 1 \ if \ V_{DSon_n} < V_{RA_n} + V_{DSonexpected_n} \end{cases} \quad (5)$$

where V_{DSon_n} is the measured on-state voltage at stage n once the dynamics have settled; V_{RA_n} is the voltage reading accuracy from the metrology attached to stage n; and $V_{DSonexpected_n}$ is the expected on voltage at stage n. The effective turn-on is a binary metric that determines whether a successful turn-on has occurred. This metric must consider the practical limitations of metrology, because the on-state voltage of the semiconductors cannot be accurately assessed by high-voltage probes that are configured to measure switching dynamics [24], [25]. In response to this challenge, V_{RA} is introduced to represent the measurement uncertainty introduced by the metrology, which includes contributions from the oscilloscope and the voltage probe. The voltage reading accuracy V_{RA_n} is calculated according to (6):

$$V_{RA_n} = V_{fs_n} (a_m/100) \quad (6)$$

where V_{fs_n} is the full-scale range of the oscilloscope channel in question, and a_m is the accuracy of the metrology involved expressed as a percentage. V_{fs_n} usually varies at each operating condition, assuming that the oscilloscope vertical scale is reconfigured to maximize the vertical resolution for each switching transition. If information about the full-scale range of the oscilloscope cannot be easily retrieved for postprocessing, a good approximation is to use the peak values of the waveforms, such that $V_{fs_n} \approx V_{DSmax_n} + |V_{DSmin_n}|$. This approximation is only valid if the peak values of the switching waveforms cover the majority of the vertical scale in the oscilloscope. The accuracy of the metrology can be calculated using the root-sum-of squares (RSS) technique and the known uncertainty values of the oscilloscope and the voltage probe

[26]. The accuracy of the metrology is calculated according to (7):

$$a_m = \sqrt{a_R^2 + a_G^2 + a_{PG}^2} \quad (7)$$

where a_R is the oscilloscope resolution accuracy expressed as a percent of full-scale error; a_G is the oscilloscope DC gain accuracy; and a_{PG} is the DC gain accuracy of the voltage probe. The oscilloscope resolution accuracy can be calculated as a percentage according to the effective number of bits (ENOB) as $a_R = 100(1/2^{ENOB})/2$ [27]. Manufacturer specifications generally provide the necessary values (a_G, a_{PG} and $ENOB$) for the preceding calculations. For example, the experimental procedures described in Section V utilized a 2.5 GHz oscilloscope with 12-bit native resolution along with 6 kV differential probes. This oscilloscope offers a gain accuracy of 1% with a resolution accuracy of 0.2%, given a very conservative $ENOB$ of 7.95 [28], while the voltage probe offers a DC gain accuracy of 2% [29]. With these values, the overall metrology accuracy (a_m) is 2.245%.

The expected on-state voltage $V_{DSonexpected_n}$ is calculated according to (8):

$$V_{DSonexpected_n} = R_{DSon_n}I_D \quad (8)$$

where R_{DSon_n} is the on-state resistance of stage n and I_D corresponds to the device current. For the 50 A experiment shown in Fig. 4, the expected on-state voltage for stage three is $V_{DSonexpected_3} = 5.7 \ m\Omega*50$ A = 0.285 V. In this case, the full-scale range approximation of $V_{fs_n} \approx V_{DSmax_n} + |V_{DSmin_n}|$ may be used to estimate the voltage reading accuracy as 25 V. With the measured on-state voltage of 4 V, an ETO_3 value of unity is calculated, signifying a successful turn-on of the transistor. Conversely, for the 200 A experiment shown in Fig. 4, the expected on-state voltage for stage three is $V_{DSonexpected_3} = 5.7 \ m\Omega*200$ A = 1.14 V. The voltage reading accuracy of the metrology is approximately 38 V, while the measured on-state voltage is 353 V. In this scenario, an ETO_3 value of zero is calculated, indicating an unsuccessful turn-on of the transistor.

D. PER-STAGE AND TOTAL SWITCHING LOSSES
Switching losses play a critical role in determining the dynamic performance of any switching device. In the context of the SCS, it is essential to quantify both per-stage switching losses and total switching losses. Per-stage switching losses influence the distribution of heat generation within the module during operation. Unequal per-stage switching losses can lead to thermal imbalances and premature failure of the SCS. Total switching losses are also of significant importance for thermal design and application optimization. In the literature, the only paper that considers per-stage switching losses is [20]. In that particular manuscript, the per-stage switching losses are calculated using LTspice, but not corroborated experimentally. Generally, researchers focus on the total switching losses of the SCS, such as [9], [17], and [18].
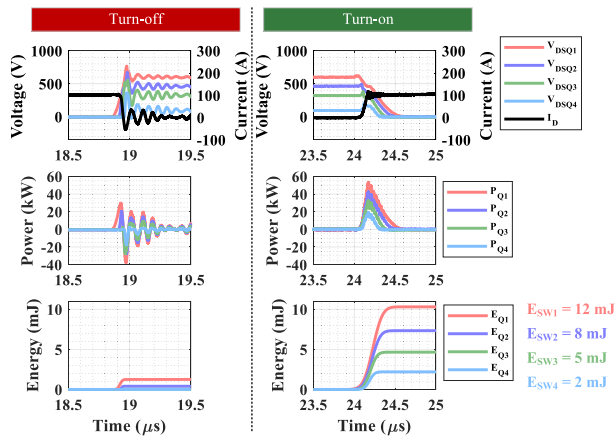
FIGURE 5. Per-stage power and energy losses during switching transitions.

Fig. 5 shows the turn-off and turn-on transitions for the same experiment presented in Fig. 2. In this figure, the instantaneous power is presented along with the accumulated switching energy loss for each stage within the SCS under consideration. A dramatic imbalance in switching loss is observed among the internal stages of the SCS, especially at turn-on. For example, the lowermost stage (Q_1) incurs approximately six times higher loss than the uppermost stage (Q_4) in this example. This imbalance has important implications for the design and implementation of SCS modules, particularly as it pertains to thermal optimization.

IV. BASELINE SUPER-CASCODE TOPOLOGY AND CONFIGURATION VARIANTS

A. BASELINE TOPOLOGY DESCRIPTION

To illustrate the value of the metrics proposed in this paper, a subject SCS topology was selected from the literature for implementation. The selected topology is an adaptation of the design originally proposed by Gao et al. in [20]. The baseline configuration, denoted as Configuration 1 in this study, incorporates a couple of fundamental changes compared to the design outlined in [20]. The primary modification corresponds to the methodology employed for calculating the values of the balancing capacitors ($C_{D1} - C_{D4}$). A first-order approximation for calculating the balancing capacitors was initially introduced in [9], followed by a further refinement for the topology under investigation in [20], [30]. However, the capacitor values produced by these methods do not provide sufficient charge for effectively switching JFETs with high input capacitance. This issue is exacerbated when the input capacitance depends strongly on the gate-source voltage bias. An initial treatment of this issue was presented by the authors in [31]. In the previous study, equations were formulated to compute values for $C_{D1} - C_{D3}$ while considering the dependence of the JFET input capacitance on gate-source voltage bias. The present paper extends the previous formulation by incorporating an additional balancing capacitor (C_{D4}) into these equations. This element was previously excluded from

the formulation in [31], as this work was following the original topology developed in [20]. While this capacitor is not a new introduction to the SCS [3], [32], it has been now incorporated into this specific SCS topology. The balancing capacitor values calculated throughout this manuscript are based on (9):

$$C_{Dn} = (s - (n - 1)) \frac{Q_G - Q_D}{V_{D_{AV}}} \tag{9}$$

where C_{Dn} is the balancing capacitor under analysis counted from the LV Si MOSFET; s is the total number of stages in the SCS; n is the stage number of the capacitor being computed; Q_G is the JFET gate charge; Q_D is the balancing diode charge; and $V_{D_{AV}}$ is the avalanche voltage of the balancing diode. The JFET gate charge and the avalanche diode junction charge can be determined according to (10) and (11), respectively:

$$Q_G = \int_0^{V_{D_{AV}} + |V_p|} C_{GD}(V_{DS}) \, dV + \int_0^{V_p} C_{GG}(V_{GS}) \, dV \tag{10}$$

$$Q_D = \int_0^{V_{D_{AV}}} C_j(V_j) \, dV \tag{11}$$

where V_p is the pinch-off voltage of the JFET; $C_{GD}(V_{DS})$ is the gate-drain capacitance of the JFET with respect to the drain-source voltage; $C_{GG}(V_{GS})$ is the input capacitance of the JFET with respect to the gate-source voltage; and $C_j(V_j)$ is the junction capacitance of the balancing diode with respect to the junction voltage.

As part of this research, we conducted a Montecarlo simulation to assess sensitivity to component tolerances. This investigation brought to light that component tolerances, particularly concerning the capacitors in the lower stages, can result in less-than-ideal static voltage balance. This concern becomes notably accentuated when operating at high voltages, as most of the stages actively engage in switching events. The fundamental issue lies in the inability to achieve sequential switching on a stage-by-stage basis. For the topology studied in this manuscript, it is advisable to select capacitors with tolerances lower than 5%. Alternatively, the balancing capacitors should be measured and screened to ensure effective sequential switching.

B. SUPER-CASCODE CONFIGURATION VARIANTS

The performance of the SCS is extremely sensitive to the configuration of the balancing network. To illustrate this sensitivity, as well as to identify the specific influence of each major component within the balancing network, an experimental study is included herein. This study evaluates the performance of five different SCS design variants, each of which differs from the baseline configuration only by a small change to the balancing network. The five configuration variants are summarized in Table 2, based on the circuit schematic of Fig. 1.

Configuration 1 corresponds to the baseline configuration, which is based on the previously proposed circuit by Gao in [20]. This initial circuit lacks the capacitor C_{D4} and the

TABLE 2. Passive Balancing Network Per Configuration

Parameter	Config. 1	Config. 2	Config. 3	Config. 4	Config. 5
R_{S1} [Ω]	3.3	3.3	3.3	3.3	10
$R_{S2} - R_{S4}$ [Ω]	3.3	3.3	3.3	10	10
C_{D1} [nF]	3.3	4.4	4.4	4.4	4.4
C_{D2} [nF]	2.2	3.3	3.3	3.3	3.3
C_{D3} [nF]	1.1	2.2	2.2	2.2	2.2
C_{D4} [nF]	-	1.1	1.1	1.1	1.1
$R_{D1} - R_{D4}$ [MΩ]	-	-	40	40	40

balancing resistors (R_{D1}-R_{D4}). Configuration 2 introduces the additional balancing capacitor (C_{D4}). The objective of introducing this capacitor is to help synchronize the switching transitions and reduce the possibility of an over-voltage on Q_4 in the case of an unsynchronized switching event. It is noted that the introduction of C_{D4} requires the recalculation of the remaining balancing capacitors to harmonize its incorporation, according to (9). Configuration 3 introduces a balancing resistor at each stage (R_{D1}-R_{D4}). The objective of introducing this resistor is to limit the peak voltage expressed across each transistor, regulating the voltage overshoot of each semiconductor at turn off. Configuration 4 evaluates the sensitivity of the SCS performance to the value of the upper stage gate resistors (R_{S2}-R_{S4}). The objective of adjusting these resistors is to investigate their influence on the dynamic performance, particularly with respect to per-stage losses. Finally, Configuration 5 explores the sensitivity of the SCS performance to the value of the lowermost gate resistor (R_{S1}). The objective of adjusting this resistor is to investigate its influence on the voltage overshoots and the per stage losses. This resistor (R_{S1}) is studied separately from the other gate resistors because it is connected to the equivalent source of the SCS, rather than to the balancing network.

Table 2 highlights the presence of two distinct sets of resistors within the analyzed SCS topology: the gate resistors and the balancing resistors. These resistor sets fulfill specific and separate purposes within the switch. Gate resistors (R_{S1}-R_{S4}) define the dynamic performance of the SCS and prevent high-frequency oscillatory behavior, while the balancing resistors (R_{D1}-R_{D4}) improve the dynamic performance while simultaneously preventing any significant increase in the power dissipation during the blocking state. This rationale requires the utilization of low values for the gate resistors and very high values for the balancing resistors.

V. SCS PROTOTYPE REALIZATION AND EXPERIMENTAL SETUP

The SCS prototype utilized for the experimental procedures described in this paper is shown in Fig. 6. This prototype is implemented on a printed circuit board (PCB) substrate
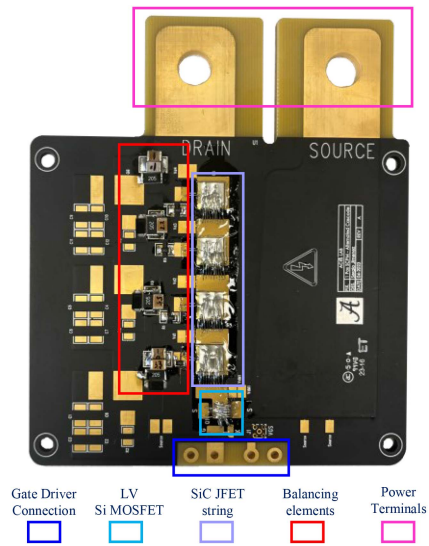
FIGURE 6. SCS prototype implementation.

TABLE 3. Semiconductors Utilized in all Super-Cascode Configurations

Description	Reference	Make	V. Rating	Package
SiC JFET ($Q_1 - Q_4$)	UF3N170006	Qorvo	1700 V	Die
LV MOSFET (M_1)	AW1060	Qorvo	35 V	Die
Av. Diode ($D_1 - D_3$)	BYG23T	Vishay	1300 V	SMD

that features electroless nickel immersion gold (ENIG) finish for easiness during wire bonding. The semiconductor devices utilized in this implementation are summarized in Table 3. As shown in this table, semiconductors in bare-die form were used to the greatest extent possible. The semiconductor chips were bonded to the substrate using TS391SNL10 solder, and top-side interconnections were implemented with 10-mil Aluminum wirebonds for the drain-source connections and 5-mil Aluminum wirebonds for the gate connections. All bond wires were ultrasonically welded using an Orthodyne M-20 manual wirebonder. To safeguard against arc formation at elevated voltage levels, a layer of 4226-55ML clear insulating varnish was applied to all die and associated MV interconnections.

All five SCS configuration variants described in the previous section were evaluated using the same PCB and the same semiconductors. The only elements changed between experiments were the specific balancing network components identified in Table 2. This approach guarantees both experiment repeatability and a consistent contribution of parasitic parameters and semiconductor characteristics for all experiments.

The static and dynamic performance characteristics of the SCS prototype were evaluated during a large number of DPT experiments performed on the testbed shown in Fig. 7. A simplified schematic of this DPT testbed is presented in Fig. 8.
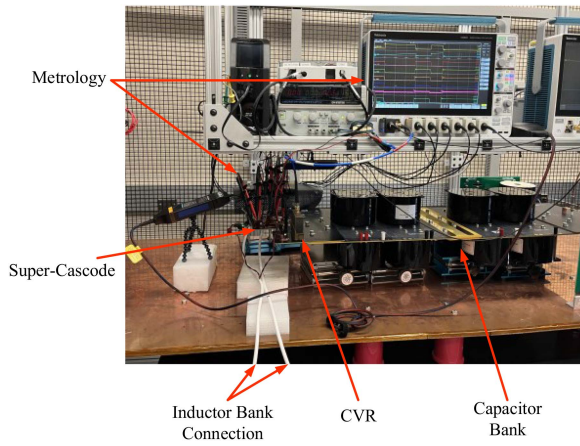
FIGURE 7. Empirical setup, DPT stand with super-cascode.
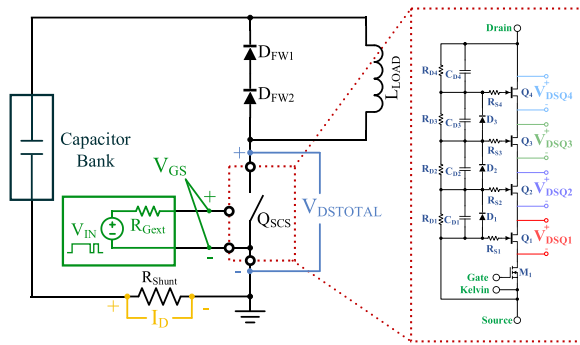
FIGURE 8. System schematic with metrology equipment disposition.

TABLE 4. Description DPT Stand Constitutive Elements

Element	Description
Capacitor Bank	186.6 µF, 7.5 kV rated
Load Inductor (L_{LOAD})	250 µH
Freewheeling Diodes (D_{FW1}, D_{FW2})	GC50MPS33H (2 in series), SiC Schottky, 3.3 kV

This figure also illustrates the attachment of the necessary metrology elements. A concise summary of the platform constitutive elements is provided in Table 4. The bulk capacitor bank is made up of 12, 140 µF, 2.5 kV film capacitors. These capacitors are interconnected in series-parallel configuration to achieve an overall voltage rating of 7.5 kV and a total capacitance of 186.6 µF. In this system, the bulk capacitor bank is charged by a DC power supply prior to each experiment utilizing the automated safety infrastructure described in [33]. Two SiC Schottky diodes rated at 3.3 kV are incorporated as the freewheeling path for the load inductor current. These diodes are connected in series to meet the voltage requirements of the system with substantial margin.

TABLE 5. Experimental Metrology

Measurement	Instrumentation	Description
V_{GS}	TIVH05 [Tektronix]	500 MHz Optically Isolated Voltage Probe
V_{DSM1}	THDP0200 [Tektronix]	200 MHz, 1.5 kV Differential Probe
V_{DSQ1} - V_{DSQ4}	THDP0100 [Tektronix]	100 MHz, 6 kV Differential Probe
$V_{DSTOTAL}$	THDP0100 [Tektronix]	100 MHz, 6 kV Differential Probe
I_D	W-2-0025-4FC [T&M Research]	400 MHz, 2.5 mΩ CVR (Shunt)
-	MSO68B [Tektronix]	2.5 GHz Oscilloscope, 8-Channel

Table 5 summarizes the metrology components utilized in this study. To minimize the influence of common mode currents, V_{GS} is instrumented with an optically isolated voltage probe. MV-rated isolated differential probes are employed to measure the drain-source voltage of each SCS stage. Experimental validations were performed to demonstrate that the voltage probes do not introduce loading to the SCS. A bar-style current viewing resistor (CVR) with high-energy rating is utilized to measure the drain current of the SCS.

VI. EXPERIMENTAL RESULTS AND ANALYSIS
As part of the present study, a standardized set of DPT experiments was performed for each of the five SCS configuration variants described previously. Every experiment was performed at 25°C, using an external gate resistor of 2 Ω. Each SCS configuration variant was evaluated using the same test matrix. The operating conditions specified by this matrix include seven bus voltage levels ranging from 500 V to 3500 V, with increments of 500 V; and four load current values from 50 A to 200 A, with increments of 50 A. The maximum bus voltage was set to approximately two-thirds of the rated voltage of the SCS (5.2 kV), for consistency with standard practices. Overall, this experimental evaluation represents one hundred and forty DPT experiments. The following subsections utilize the figures of merit proposed in this paper to provide a thorough performance comparison of the five SCS configuration variants considered here.

A. NORMALIZED STATIC VOLTAGE
The heatmaps in Fig. 9 illustrate the normalized static voltage distribution for the five configurations across all the evaluated operating conditions. It is noted that the ideal behavior would be represented in this figure by a heatmap that indicates a value of unity for all operating conditions (light blue color). Several general observations can be made from these heatmaps. First, regardless of the configuration, transistor Q_1 blocks the greatest percentage of voltage compared to the other semiconductors in the low-voltage regime, progressively blocking a smaller percentage of voltage as the applied voltage increases. Second, Since the maximum evaluated voltage
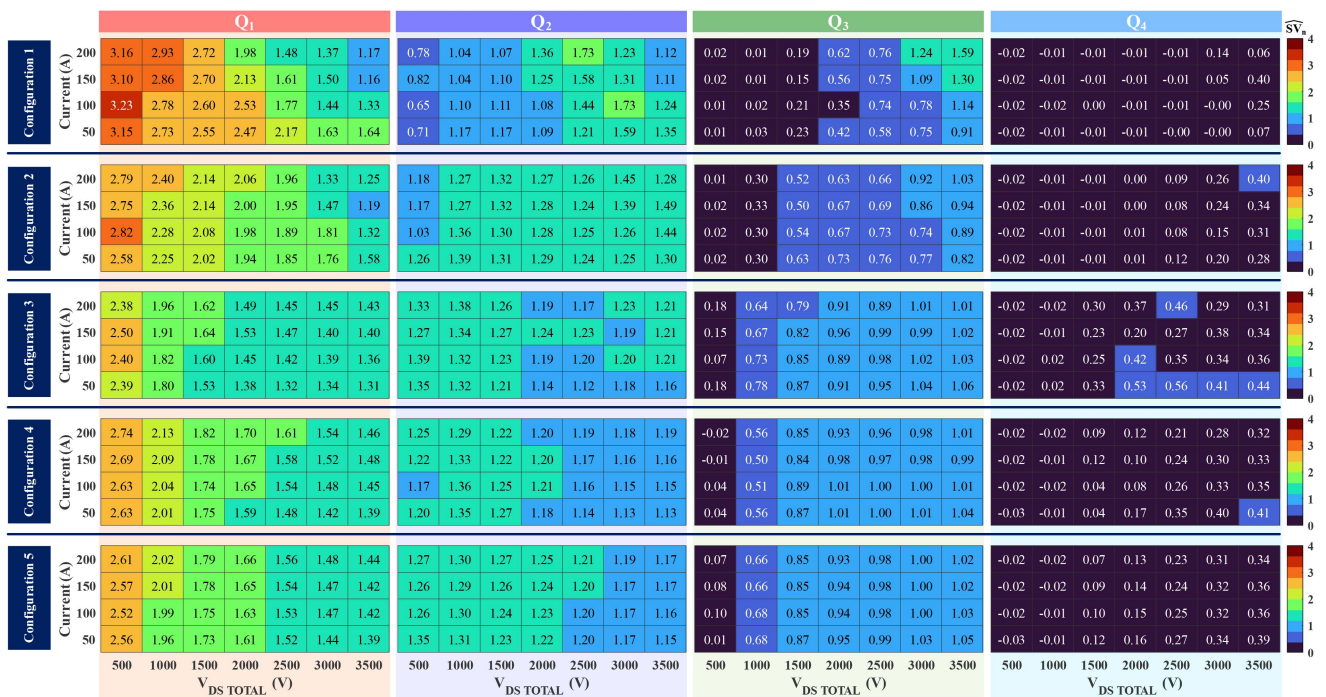
FIGURE 9. Normalized static voltage for the different super-cascode configurations.

is 3.5 kV, the uppermost JFET Q_4 does not participate in the switching events for most operating conditions. As a result, this transistor exhibits little blocking contribution. The negative values observed for this transistor are due to metrology errors, as the V_{DS-Q4} voltage is very close to zero. Third, transistor Q_3 clearly shows the effects of sequential switching. When the voltage bias is low, most of the voltage is blocked by transistors Q_1 and Q_2. As the bias voltage increases, transistor Q_3 progressively blocks more voltage. This is due to the operation of the avalanche diodes and the balancing network in the lower stages. Finally, since a four-stage configuration is studied in this manuscript, adding the normalized static voltage contribution of all the different transistors under one operating condition adds up to four, which is the upper limit of the heatmap color bar.

Among the studied configurations, Configuration 1 exhibits the poorest overall static performance due to its uneven voltage distribution. However, by adding the additional balancing capacitor (C_{D4}) and recalculating the balancing capacitor values in Configuration 2, a notable improvement in static voltage performance is achieved. As a result, the voltage stress applied to transistor Q_1 is reduced, and transistor Q_3 starts blocking at a lower voltage. This leads to a redistribution of voltage to transistors Q_2 and Q_3. Configuration 3 further enhances the static voltage distribution by introducing balancing resistors ($R_{D1} - R_{D4}$). This introduction further reduces the voltage stress on Q_1 and improves the voltage sharing among the other transistors. Consequently, Configuration 3 appears to provide the most favorable static distribution among all the evaluated configurations. Configurations 4 and 5 exhibit slightly worse static performance compared to Configuration 3. This behavior suggests that the gate resistors of the JFETs have minimal impact on the static blocking performance of the SCS.

B. NORMALIZED VOLTAGE MARGIN

The heatmaps of Fig. 10 illustrate the normalized voltage margin for the five SCS configurations across all the evaluated operating conditions. It is noted that no ideal behavior for this figure of merit exists, but large positive values are preferred. Several general observations can be made from these heatmaps. First, the normalized voltage margin is significantly influenced by both the device voltage and the device current. Notably, an increase in either operating condition produces a decrease in the normalized voltage margin across all transistors under all operating conditions, regardless of the configuration. It is noteworthy that certain configurations and operating conditions result in negative values for the normalized voltage margin. These negative values indicate that the rated voltage of the SiC JFET is exceeded, which must be avoided. Even modest violations of the semiconductor voltage rating can compromise device lifetime if repetitive switching occurs under these conditions [34], [35].

Comparing the trends of the normalized voltage margin with those of the normalized static voltage reveals notable differences. In terms of normalized static voltage, transistor Q_1 experiences the greatest percentage of voltage blocking under low voltage conditions. However, this scenario reverses when examining the normalized voltage margin. As the voltage bias increases, higher overshoot values are observed, reducing the available voltage margin. Although transistor Q_4 does not actively blocks voltage in this system, some voltage transients

Configuration 1

Q_1

Current (A)	500	1000	1500	2000	2500	3000	3500
200	0.45	0.26	0.11	0.00	-0.02	-0.04	-0.06
150	0.49	0.31	0.14	0.01	-0.02	-0.04	-0.06
100	0.56	0.40	0.20	0.05	-0.02	-0.04	-0.06
50	0.66	0.49	0.30	0.16	0.04	-0.03	-0.05

Q_2

Current (A)	500	1000	1500	2000	2500	3000	3500
200	0.72	0.67	0.59	0.46	0.09	-0.13	-0.19
150	0.74	0.68	0.61	0.55	0.24	-0.08	-0.18
100	0.77	0.69	0.65	0.56	0.39	0.04	-0.14
50	0.84	0.73	0.66	0.62	0.49	0.22	-0.06

Q_3

Current (A)	500	1000	1500	2000	2500	3000	3500
200	0.92	0.84	0.80	0.67	0.48	0.32	-0.02
150	0.96	0.85	0.81	0.76	0.55	0.44	0.14
100	0.99	0.90	0.81	0.79	0.66	0.51	0.26
50	0.99	0.98	0.87	0.80	0.75	0.62	0.48

Q_4

Current (A)	500	1000	1500	2000	2500	3000	3500
200	0.99	0.99	0.99	0.99	0.99	0.80	0.33
150	0.99	0.99	0.99	0.99	0.99	0.93	0.55
100	0.99	0.99	0.98	0.99	0.99	0.99	0.73
50	1.00	1.00	1.00	1.00	1.00	1.00	0.95

Configuration 2

Q_1

Current (A)	500	1000	1500	2000	2500	3000	3500
200	0.54	0.39	0.31	0.14	0.04	-0.02	0.02
150	0.60	0.43	0.31	0.22	0.05	-0.02	0.02
100	0.65	0.53	0.36	0.27	0.13	0.01	0.02
50	0.72	0.60	0.48	0.35	0.22	0.13	0.10

Q_2

Current (A)	500	1000	1500	2000	2500	3000	3500
200	0.71	0.58	0.49	0.43	0.32	0.23	-0.00
150	0.72	0.62	0.51	0.44	0.36	0.25	0.12
100	0.73	0.68	0.56	0.47	0.40	0.28	0.14
50	0.81	0.72	0.65	0.55	0.47	0.36	0.24

Q_3

Current (A)	500	1000	1500	2000	2500	3000	3500
200	0.79	0.73	0.67	0.60	0.56	0.45	0.33
150	0.83	0.73	0.70	0.62	0.57	0.52	0.39
100	0.91	0.77	0.71	0.66	0.58	0.54	0.46
50	0.95	0.87	0.76	0.70	0.64	0.60	0.49

Q_4

Current (A)	500	1000	1500	2000	2500	3000	3500
200	0.99	0.98	0.93	0.87	0.84	0.79	0.74
150	0.99	0.99	0.96	0.90	0.84	0.82	0.76
100	0.99	0.99	0.99	0.94	0.87	0.83	0.80
50	1.00	0.99	0.99	0.99	0.91	0.88	0.84

Configuration 3

Q_1

Current (A)	500	1000	1500	2000	2500	3000	3500
200	0.64	0.56	0.50	0.41	0.28	0.19	0.07
150	0.68	0.58	0.51	0.42	0.31	0.24	0.12
100	0.73	0.64	0.55	0.49	0.37	0.26	0.19
50	0.77	0.69	0.63	0.55	0.47	0.34	0.25

Q_2

Current (A)	500	1000	1500	2000	2500	3000	3500
200	0.72	0.61	0.53	0.47	0.37	0.26	0.17
150	0.75	0.65	0.55	0.47	0.37	0.29	0.20
100	0.77	0.70	0.60	0.52	0.42	0.31	0.23
50	0.80	0.76	0.68	0.61	0.53	0.41	0.32

Q_3

Current (A)	500	1000	1500	2000	2500	3000	3500
200	0.74	0.68	0.56	0.47	0.42	0.27	0.21
150	0.75	0.70	0.61	0.49	0.41	0.33	0.22
100	0.81	0.71	0.67	0.57	0.45	0.37	0.27
50	0.92	0.77	0.73	0.65	0.57	0.45	0.34

Q_4

Current (A)	500	1000	1500	2000	2500	3000	3500
200	0.90	0.81	0.71	0.62	0.57	0.69	0.67
150	0.94	0.82	0.76	0.75	0.73	0.68	0.68
100	0.99	0.87	0.79	0.71	0.74	0.74	0.70
50	1.00	0.96	0.85	0.77	0.73	0.77	0.73

Configuration 4

Q_1

Current (A)	500	1000	1500	2000	2500	3000	3500
200	0.60	0.48	0.40	0.29	0.19	0.11	0.04
150	0.64	0.53	0.44	0.34	0.23	0.13	0.05
100	0.66	0.59	0.52	0.39	0.30	0.20	0.09
50	0.71	0.66	0.57	0.48	0.38	0.29	0.21

Q_2

Current (A)	500	1000	1500	2000	2500	3000	3500
200	0.66	0.61	0.57	0.48	0.37	0.28	0.18
150	0.68	0.62	0.59	0.51	0.41	0.31	0.22
100	0.72	0.64	0.61	0.55	0.46	0.36	0.27
50	0.81	0.71	0.66	0.61	0.53	0.43	0.34

Q_3

Current (A)	500	1000	1500	2000	2500	3000	3500
200	0.73	0.64	0.52	0.46	0.42	0.33	0.23
150	0.80	0.66	0.53	0.47	0.43	0.36	0.27
100	0.88	0.73	0.56	0.48	0.44	0.39	0.32
50	0.96	0.82	0.69	0.59	0.54	0.47	0.38

Q_4

Current (A)	500	1000	1500	2000	2500	3000	3500
200	0.98	0.88	0.80	0.78	0.76	0.74	0.72
150	0.99	0.91	0.85	0.81	0.77	0.74	0.72
100	0.99	0.97	0.92	0.88	0.79	0.76	0.74
50	1.00	1.00	0.96	0.91	0.82	0.79	0.76

Configuration 5

Q_1

Current (A)	500	1000	1500	2000	2500	3000	3500
200	0.70	0.61	0.52	0.42	0.33	0.25	0.17
150	0.71	0.62	0.53	0.43	0.35	0.27	0.18
100	0.74	0.64	0.55	0.45	0.36	0.28	0.19
50	0.76	0.67	0.57	0.47	0.39	0.31	0.23

Q_2

Current (A)	500	1000	1500	2000	2500	3000	3500
200	0.78	0.72	0.63	0.53	0.46	0.38	0.29
150	0.79	0.73	0.64	0.55	0.47	0.39	0.31
100	0.80	0.74	0.66	0.57	0.48	0.40	0.32
50	0.82	0.76	0.69	0.59	0.51	0.43	0.35

Q_3

Current (A)	500	1000	1500	2000	2500	3000	3500
200	0.85	0.79	0.70	0.60	0.51	0.43	0.34
150	0.87	0.79	0.72	0.61	0.53	0.44	0.36
100	0.90	0.80	0.73	0.63	0.54	0.46	0.38
50	0.95	0.82	0.74	0.65	0.57	0.48	0.39

Q_4

Current (A)	500	1000	1500	2000	2500	3000	3500
200	0.99	0.93	0.89	0.88	0.83	0.79	0.75
150	0.99	0.94	0.90	0.89	0.84	0.80	0.76
100	1.00	0.96	0.91	0.90	0.86	0.81	0.77
50	1.00	0.99	0.94	0.91	0.87	0.83	0.79

$V_{DS\ TOTAL}$ (V): 500, 1000, 1500, 2000, 2500, 3000, 3500

$\widehat{VM}_n$ scale: 0 – 0.5 – 1

FIGURE 10. Normalized voltage margin for the different super-cascode configurations.

are nevertheless expressed across this device. These transients are observed across all operating conditions and configurations but become more pronounced at higher voltage and current levels.

The results of Fig. 10 indicate that Configuration 1 should be avoided, because the rated voltage of transistors Q_1, Q_2, and Q_3 is exceeded under a range of operating conditions. This poses a significant risk to the integrity and reliability of the semiconductor. Configuration 2 improves this behavior by introducing the additional balancing capacitor (C_{D4}) and reconfiguring the remaining balancing capacitors. As a result, the voltage margin is enhanced for all transistors. However, some negative margin values still appear for Q_1 and Q_2. Configuration 3 yields even better results by introducing balancing resistors ($R_{D1} - R_{D4}$). These resistors play a crucial role in balancing the dynamic voltage distribution and limiting the transient peaks. Consequently, the voltage ratings of the semiconductors are never exceeded in this setup. Configuration 4, which involves increasing the gate resistor values for Q_2-Q_4, does not show significant improvements in the normalized voltage margin for those transistors. This configuration leads to a slight degradation in the performance of Q_1, particularly under high voltage and high current conditions, when compared to Configuration 3. Finally, Configuration 5 demonstrates the best overall performance in terms of the normalized voltage margin. Similar to Configurations 3 and 4, the voltage ratings of the semiconductors in this configuration are never exceeded. Additionally, Configuration 5 offers the greatest transient headroom for all transistors. This result demonstrates the effectiveness of R_{S1} in modifying the dynamic performance of all the transistors within the SCS topology.

C. EFFECTIVE TURN-ON

The heatmaps of Fig. 11 illustrate the effective turn-on metric results for the five SCS configurations across all the evaluated operating conditions. It is noted that the ideal behavior would be represented in this figure by a heatmap that indicates a value of unity for all operating conditions (white color). Most of the evaluated operating conditions exhibit successful turn-on, except for a handful of operating conditions in Configuration 1. In this specific configuration, transistors Q_2, Q_3, and Q_4 do not achieve successful turn-on in certain cases. One key observation from Fig. 11 is that this issue is mostly observed when the transistors are switching high current levels. As previously discussed, most of the SCS experiments reported in the literature are for current levels below 100 A and usually involve only a few operating conditions. This is believed to be the reason for the lack of discussion concerning this phenomenon in the literature. Unsuccessful turn-on can be resolved by means of augmenting the balancing network, as demonstrated by Configurations 2 to 5. In this particular case, the unsuccessful turn-on was resolved by introducing the additional balancing capacitor (C_{D4}) and reconfiguring the remaining balancing capacitors. This is the primary difference that distinguishes Configuration 1 from Configuration 2 and following.

D. SWITCHING LOSSES

The heatmaps of Fig. 12 illustrate the per-stage switching losses for the five SCS configurations across all the evaluated operating conditions. It is noted that the ideal behavior would be represented in this figure by a heatmap that indicates a value of zero for all operating conditions (dark blue color).
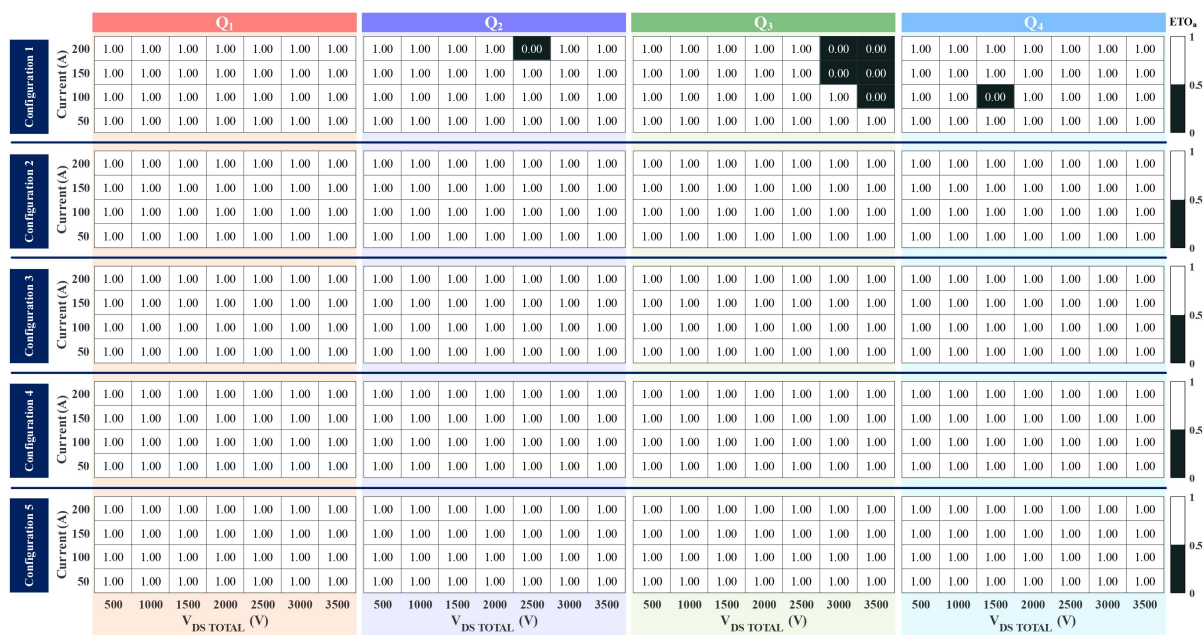
FIGURE 11. Effective turn-on for the different super-cascode configurations.

FIGURE 12. Per-stage switching losses in mJ for the different super-cascode configurations.

Of course, lossless switching is generally unattainable in a clamped-inductive-load circuit, which represents the behavior of a hard-switched converter.

The per-stage switching losses shown in Fig. 12 exhibit significant variation depending on the configuration and operating conditions. For instance, in Configuration 1, the highest switching losses occur in Q_2 and Q_3. However, these cases coincide with the conditions for which the effective turn-on criteria are not met. This correlation explains the considerable increase in switching losses for these conditions, because the drain-source voltage never reaches the expected on-state voltage. One important observation from Configuration 2 is that the switching losses in Q_1 peak at 2.5 kV when operating at high current (200 A). Above this voltage value, the highest

energy loss is exhibited by Q_2. Above 2.5 kV, Q_2 exhibits a more pronounced overlap between voltage and current waveforms, therefore, increasing its power dissipation.

In Configuration 3, adding the balancing resistors (R_{D1}-R_{D4}) shifts the voltage at which the peak switching loss occurs relative to Configuration 2. An example of this is the shift of the peak switching loss from 2.5 kV to 3.5 kV in the case of Q_1. Furthermore, Configuration 3 exhibits the lowest overall per-stage switching losses. This can be attributed to the successful achievement of effective turn-on for all transistors in all operating conditions, combined with the fact that this configuration demonstrates the best static voltage distribution and the smallest arrangement of gate resistor values.

In Configuration 4, the switching losses are very similar to those in Configuration 3. The impact of increasing gate resistors R_{S2}-R_{S4} appears to have minimal effect on the per-stage switching losses, producing only slight increases for most conditions. On the other hand, Configuration 5 reveals the dramatic influence of R_{S1} on the per-stage switching losses of the SCS. Increasing this gate resistor from 3.3 Ω to 10 Ω produces more than a twofold increase in the switching losses for most operating conditions. R_{S1} influences not only the switching losses of Q_1, but also impacts the switching losses of every stage in the SCS. From this analysis, a trade-off in terms of R_{S1} becomes evident. Employing a smaller value for this resistor reduces switching losses across all stages. This is achieved at the cost of a diminished normalized voltage margin. Conversely, opting for a higher value for this resistor significantly increases switching losses while concurrently enhancing the normalized voltage margin.

The heatmaps of Fig. 13 illustrate the switching losses for the entire SCS across all the evaluated operating conditions. These results represent the sum of the contributions from each stage as detailed in Fig. 12. In terms of the total switching losses, the performance of this prototype SCS is similar to that of a MV SiC MOSFET. The total switching losses increase with both the device voltage and the device current, as expected. Among the evaluated configuration variants, Configurations 1 and 5 demonstrate the highest total switching losses. This can be explained by the ineffective turn-on phenomenon for the case of Configuration 1, and by the high value of R_{S1} for the case of Configuration 5. Similar to the per-stage evaluation, Configuration 3 demonstrates the lowest total switching losses. Configurations 2 and 4 demonstrate only slightly higher switching losses compared to Configuration 3, which suggests that the balancing resistors and the upper-stage gate resistors (R_{S2}-R_{S4}) do not strongly influence the dissipation of the SCS during switching transients.

VII. SUMMARY OF FINDINGS

Table 6 provides a summary of the performance of each SCS configuration considered in this paper with respect to the proposed figures of merit. These results are based on the configurations outlined in Table 2 as applied to the circuit schematic depicted in Fig. 1. The baseline case (Configuration 1) shows the least favorable performance across all
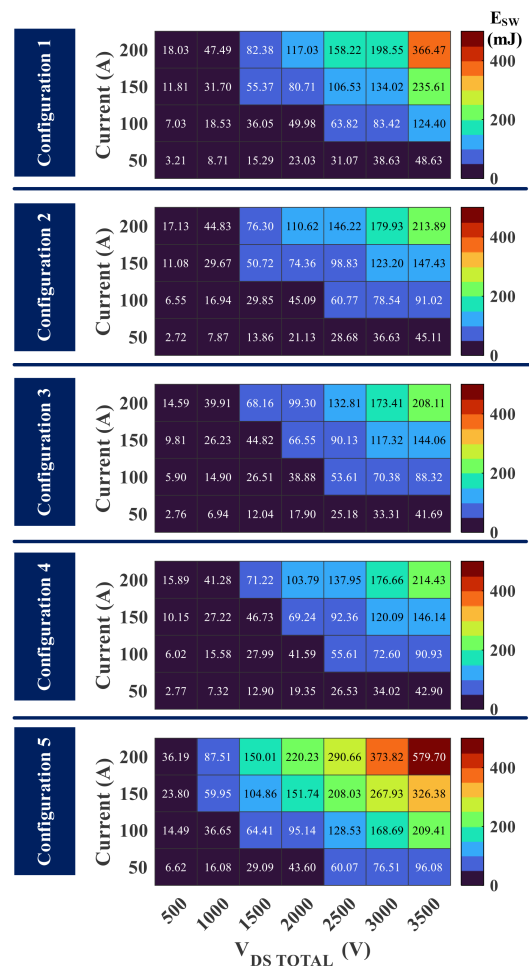
FIGURE 13. Total switching losses in mJ for the different super-cascode configurations.

TABLE 6. Summary Performance Figures of Merit Per Configuration

Figure of Merit	Config. 1	Config. 2	Config. 3	Config. 4	Config. 5
$\widehat{SV}$	↓↓	↓	↑	↑	↑
$\widehat{VM}$	↓↓	↓	↑	-	↑↑
ETO	↓↓	↑↑	↑↑	↑↑	↑↑
E_{SW}	↓	↑	↑	↑	↓↓

↑↑ = very good, ↑ = good, - = average, ↓ = bad, ↓↓ = very bad

figures of merit. Configuration 2 represents a slight improvement over the baseline, demonstrating that the introduction of balancing capacitor C_{D4} provides some benefit in terms of static voltage balance and voltage margin. These improvements are further enhanced through the introduction of balancing resistors R_{D1} - R_{D4} in Configuration 3. The similar performance of Configuration 4 indicates that the upper-stage gate resistors $R_{S2} - R_{S5}$ exert little influence over the behavior of the SCS. On the other hand, the significant increase in
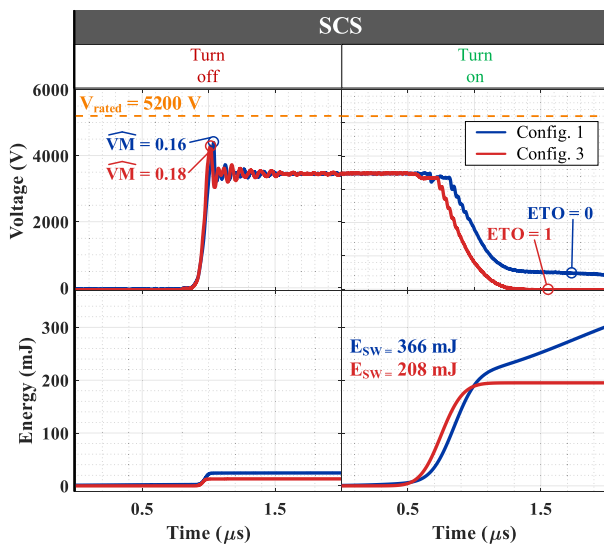
FIGURE 14. Waveform overlay for the overall SCS in Configurations 1 and 3 under 3.5 kV and 200 A.

switching loss observed for Configuration 5 indicates that the lowermost gate resistor R_{S1} does exert a big influence over the speed of SCS switching transitions. Thus, while the implementation of Configuration 5 as presented in this study is not recommended, this finding indicates that a measure of switching speed control may be available within the SCS topology through the use of this design parameter.

Additional insight regarding the performance of this topology may be obtained by comparing the overall transient behavior of the baseline case (Configuration 1) with the best-performing design obtained through this study (Configuration 3). Such a comparison is provided in Fig. 14 for a bus voltage of 3.5 kV and a load current of 200 A.

From the figures of merit developed in this manuscript, the voltage margin, the effective turn-on, and the switching losses remain calculable for the overall SCS. In terms of the voltage margin, both configurations exhibit similar performance. This stands in stark contrast to the per-stage analysis, because the rated voltage is actually exceeded for three of the five JFETs in Configuration 1 (Q_1-Q_3), as shown in Fig. 10. This underscores the importance of per-stage analysis, as it unveils internal problems that may not be observable from the SCS terminals. In terms of turn-on effectiveness, the ineffective turn-on behavior of transistor Q_3 in Configuration 1 extends to the overall behavior of the SCS, resulting in poor conduction behavior. In contrast, Configuration 3 demonstrates good conduction performance, as anticipated from the per-stage analysis. Finally, the overall switching losses for Configuration 1 are 76% higher than that of Configuration 3, due to the combination of factors that have been discussed previously. Overall, this comparison demonstrates that while some aspects of SCS performance can be understood from observing the terminal behavior of the device, the viability of a given SCS design cannot be ascertained without a detailed per-stage performance analysis.

VIII. CONCLUSION

This manuscript extensively investigates the performance characteristics of the super-cascode switch through the application of a novel set of four figures of merit. These figures of merit correspond to the normalized static voltage, the normalized voltage margin, the effective turn-on, and the per-stage switching losses. These metrics were carefully formulated to analyze the unique characteristics of the super-cascode, providing a comprehensive framework for evaluating both static and dynamic performance.

This paper also provides a comprehensive experimental evaluation of one particular SCS topology, which was selected from the literature due to its attractive performance characteristics. By applying the proposed figures of merit to the analysis of this "baseline" topology, a number of opportunities for further performance improvement were identified. The accompanying experimental study includes an evaluation of five different variants of this baseline topology, each of which reflects subtle changes to the balancing network. This analysis demonstrates that the performance of the super-cascode can be greatly improved by means of the developed figures of merit.

The final outcome of this work is a prototype super-cascode switch that demonstrates significant performance improvements over previous devices, including a 56% reduction in total switching losses compared to the baseline topology. This prototype is also experimentally demonstrated at current levels up to two times higher than previously reported super-cascode devices. Overall, these capabilities demonstrate the practical utility of the proposed figures of merit for evaluating the static and dynamic performance characteristics of the super-cascode switch.

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