

Dynamic Interactions and Stabilization of Weak Grid-Tied Parallel VSCs and Parallel CSCs Systems Considering PVG Dynamic Resistance

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ABSTRACT The parallel operation of power converters is essential to meet increased power demands. However, due to dynamic coupling, the instability in one converter can affect the stability of another. Therefore, this paper analyses the interaction and stability differences among the weak grid-tied photovoltaic (PV)-interfaced parallel voltage- and current-source converters (VSCs and CSCs) considering the PV generator (PVG) dynamics. Moreover, the impacts of the changing PVG operating points from the constant-voltage to a constant-current region (CVR to a CCR) and changing control parameters on converters' dynamic interaction are studied and compared in both cases. It is found that parallel VSCs dc-links suffer from low-frequency (<60 Hz) compared to high-frequency oscillations (>200 Hz) in parallel CSCs at the CCR with a short-circuit ratio (SCR) of 2.5. Moreover, the oscillation magnitude of injected power is higher in parallel VSCs compared to the parallel CSCs at SCR = 1.2. Therefore, a stabilization method is proposed for both systems to ensure reduced interactions and stable operation in the CVR, CCR, and maximum power regions at weak and very weak grid conditions. Finally, the proposed compensators' efficacy is validated via detailed nonlinear time-domain and real-time simulation results.

INDEX TERMS Parallel converters, PVG dynamic resistance, interaction studies, stability analysis, weak grid, stabilization.

I. INTRODUCTION

Photovoltaic generator (PVG) interfaced voltage-source converters (VSCs) are commonly used for utility grid integration due to easy implementation and lower losses [1], [2]. However, the advancement of power semiconductors and magnetic materials allows current-source converters (CSCs) to be an alternative option for PV grid integration as they offer a boost-type feature with smooth dc-current and short-circuit protection capability [3]. Moreover, its operation life is higher than VSC's and is widely used in motor drive applications and offshore wind farms [4].

The grid strength is known as the short-circuit ratio (SCR), where short-circuit capacity at the point-of-common-coupling (PCC) to the rated dc power of the interconnected converter defines SCR [2], [6]. The grid is weak with $2 \leq \text{SCR} \leq 3$ and very weak when $\text{SCR} < 2$. The converter adopts a phase-locked-loop (PLL) for the synchronization; however, in a

weak grid, it triggers low- and high-frequency instability and affects power injection capability [8]. Therefore, it has become a research interest for utility-scale PV grid-tied systems [5], [6], [7], [8], [9], [10], [11].

Under fast-changing environmental conditions, the PVG operating point moves from the right (CVR: constant voltage region) to the left (CCR: constant current region) of the maximum power point (MPP). Therefore, the forward-biased diode in a PVG equivalent model results in an operating-point-dependent dynamic resistance, which varies from low to high value when PVG moves from CVR to CCR [3], [6].

In the literature, the dynamic resistance impact on stability is carried out from a single converter point of view (either VSC or CSC) [3], [6], [11], [12], [13], [14]. The PV-CSC system suffers from high-frequency instability at the CCR [3] compared to the low- and high-frequency instability for a

weak grid-tied VSC [5]. The reduced dc-link capacitance introduces unstable poles in the control loop [11] and increases the oscillation amplitude in the CCR [12]. The dynamic resistance in the PVG reduces the MPP current by 3% [13] and affects the stability at the MPP and CCR; however, it improves with a higher resistance in the dc-link capacitance [14]. If multiple converters are connected in parallel, how the dynamic resistance (e.g., one converter in the CVR and the other in the CCR) in a weak grid impacts the control interactions and stability is still unknown; however, it must be considered to analyze the stability correctly.

The grid impedance in a weak VSC system affects the low- and high-frequency stability [2], and the current controllers' proportional gain dominates the instability [5]. Moreover, in a weak grid, the PVG at the CCR with nominal dc-capacitance induces low- and high-frequency instabilities compared to the medium-frequency oscillations with reduced dc-capacitance at the CVR [6]. The control interaction and oscillation increase under low SCR, affecting power injection capacity; however, improved control overcomes it [7]. The higher PLL bandwidth in a weak grid decreases the stability margin [8], affecting the current control negatively to lose PLL synchronization [9], and reduces the impedance magnitude at low frequencies in a weak CSC system [10]. The inner, outer, and PLL control bandwidth interactions determine the stability boundary [15]; moreover, a power control loop bandwidth dominates the oscillations and decreases the damping in a weak grid; however, the controller in [16] and a compensator in [17] reduces the VSC systems oscillation and improves damping and stability. In a weak VSC system, the ac voltage control loop introduces low-frequency oscillations [18], and the PCC voltage fluctuations introduce negative damping; however, the controller in [19] and an impedance reshaping in [20] improve it with higher damping and stability. The studies in [5], [6], [7], [8], [9], [10], [15], [16], [17], [18], [19], [20] did not analyze the stability with changing PVG dynamic resistance in a weak grid; moreover, the control interaction differences among VSC and CSC systems and damping improvement.

The studies above give insights into the stability of a single converter system; however, if the converters are connected in parallel to increase the power rating, the control interactions must be addressed in a non-stiff grid [21]. The PLL interactions in a weak grid-tied parallel VSCs system increase, resulting in instability; however, reduced PLL bandwidth [22] and an improved notch filter ensure stability [23]. In parallel VSCs, the interactions from the inner current control loop and parallel VSCs influence synchronization and stability [24]; moreover, one VSC suffers from the interaction effects of the other at the PCC [25]. In parallel VSCs, the dynamic coupling under asymmetrical fault [26] and a weak grid [27] increases interactions, decreasing damping and resulting in instability. However, the study ignored the source dynamics effect and did not report any stability improvement methods. Interaction mechanisms and stability boundary of paralleled VSCs under different current injections were carried out in [28], ignoring

the wind turbine dynamics. When parallel converters share the same ac and dc buses, a circulating current flows; therefore, a suppression method was proposed in [29]. The multiconverter interaction in a weak grid affects the synchronization stability; however, a feed-forward compensated PLL improves it [30]. Reference [31] revealed that filter and grid inductance affects the low- and high-frequency resonance in multi-VSC systems, resulting in PCC voltage fluctuations and instability; however, it did not show stability enhancement. The interactions among wind turbine-based multi-VSC systems and their impact on dc-link voltage stability under varying SCR, operating points, and control parameters were carried out in [32], ignoring the wind turbine dynamics. Moreover, it did not report any method to reduce the interactions in low SCR. The work in [21], [22], [23], [24], [25], [26], [27], [28], [29], [30], [31], [32] studied parallel VSCs interaction and stability but ignored the impacts of PVG dynamic resistance on control interactions in weak grids. Moreover, no solution was proposed to reduce the interactions and maintain stability with rated power injection. Therefore, the modeling, dynamic interactions, and stability improvements of parallel VSCs when connected to a weak grid considering changing PVG dynamic resistance are still unknown, demanding a detailed study.

Direct current control and low switching frequency in high-power CSCs offer to operate in parallel to increase the power rating; however, a few studies addressed it [33], [34], [35]. Multiple resonance modes arise (fixed high and variable low frequency) from the multi-CSCs interaction, affecting the power quality and stability; therefore, an active damper was proposed in [33] to suppress the resonance modes. However, it did not consider control interactions under changing source dynamics in a weak ac grid and no stability improvement methods. The authors in [34] reported the harmonic performance improvement of a stiff grid-tied multi-CSCs system, reducing the common-mode voltage (CMV) peak. Moreover, multilevel CSC was reported in [35] but did not develop the mathematical model to analyze the control interaction and stability in a weak grid. Reference [36] analyzed a VSC-CSC system's dc-link voltage and current interactions. However, the study did not report the impacts of changing PVG operating points (at CVR, MPP, and CCR) on frequency oscillations under changing SCR. Moreover, the study did not characterize the interactions in the following cases: 1) parallel VSCs connected to a weak grid and 2) parallel CSCs connected to a weak grid. Therefore, the mathematical modeling, dynamic control interactions, and stability improvements of weak grid-tied parallel CSCs considering PVG dynamic resistance demand a detailed study.

There is a gap in the reported parallel converters studies with the following: 1) Interaction, stability analysis, and stability improvement of PV-based parallel VSCs weak grid system considering the PVG operating point changes from the CVR to the CCR, and 2) mathematical model development, dynamic interaction, stability analysis and stabilization of parallel CSCs weak grid system considering the PVG dynamic

resistance. Therefore, to fill the gaps, considering the changing PVG dynamics, this paper develops the mathematical model of a paralleled VSCs and CSCs system to characterize the control interaction and its impact on dc-link stability for a weak grid system in each case and differentiate the instability among two systems when PVG operates at CVR, MPP, and CCR under changing SCR levels. Furthermore, compensators are proposed for both paralleled converter systems to reduce the dynamic interactions in each case and to improve stability with rated power injection under changing PVG dynamics. The contributions of this paper are:

- 1) Developing a mathematical model for a utility-scale PV-based parallel VSCs and CSCs system considering the PVG dynamic resistance, control loops interactions, and weak grid conditions,
- 2) Characterizing the interaction and stability differences among parallel VSCs and CSCs systems considering the dynamic resistance, SCR, and control parameters and
- 3) Developing parallel VSCs and CSCs weak grid systems compensation assuring dc-link stabilities, improved damping, and rated power injection at a very weak grid.

The following section first develops the parallel VSCs' mathematical model and explains PV-VSC systems control and dynamic PVG model. Section III presents parallel CSCs' mathematical model and PV-CSC control dynamics. The dynamic control interactions and stability differences among two parallel converter systems when connected to a weak grid under changing PVG dynamics and operating conditions are presented in Section IV. Section V presents the compensation methods for weak grid-tied parallel VSCs and CSCs systems to ensure stability with reduced control interactions. Finally, the time domain simulation results in Section VI and real-time simulation results in Section VII show the stability differences and verify the proposed compensators' effectiveness.

II. MODELING AND CONTROL OF PARALLEL VSCS SYSTEM

The PVG-interfaced grid-tied parallel VSCs system is shown in Fig. 1, where the PVGs are rated at 1.0 MW. The complete system and control parameters are given in Appendix A. For simplified analysis, the system and control parameters of VSC1 and VSC2 in Fig. 1 are assumed to be identical.

A. PARALLEL VSCS MODEL DYNAMICS

The capacitor (C_{dcn}) in Fig. 1 connects the PVG to the VSC, where n is the converter number (i.e., $n=1, 2$). The PV current is I_{pvn} , and the VSC's dc-side voltage and power are V_{dcn} and P_{dcvscn} , respectively. The filter reactor ($R_{fn}-L_{fn}-C_{fn}$) mitigates the harmonics of v_{in} and i_{in} , where v_{in} is the VSC terminal output voltage and i_{in} is the reactor current. The voltage at C_{fn} is v_n , and the feeder inductance (L_n) connects it to the PCC voltage (v_{pcc}) with the current i_{Ln} . The transformer ratio is N , and L_g , v_g , and i_g are the grid inductance, voltage, and currents. The VSC terminal active and reactive power is P_n and Q_n , respectively. The parallel VSCs dynamics are given

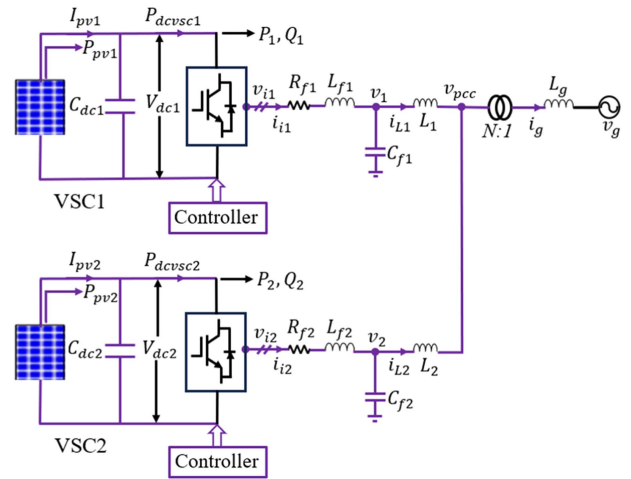


FIGURE 1. PVG-interfaced parallel VSCs system.

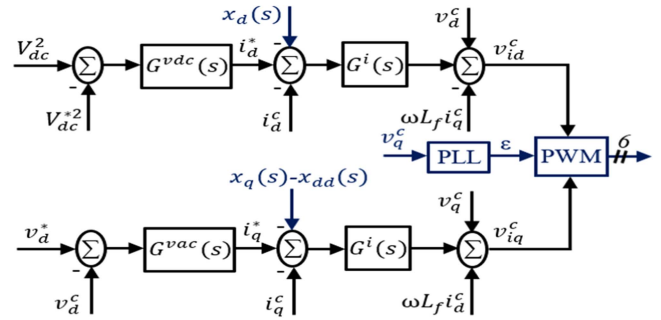


FIGURE 2. PV-VSC control system.

by

$$\vec{v}_{in} = (sL_{fn} + R_{fn} + j\omega L_{fn}) \vec{i}_n + \vec{v}_n \quad (1a)$$

$$\vec{i}_n = (sC_{fn} + j\omega C_{fn}) \vec{v}_n + \vec{i}_{Ln} \quad (1b)$$

$$\vec{v}_n = (sL_n + j\omega L_n) \vec{i}_{Ln} + \vec{v}_{pcc} \quad (1c)$$

$$N\vec{v}_{pcc} = (sL_g + j\omega L_g) \vec{i}_g + \vec{v}_g \quad (1d)$$

$$\frac{1}{2}sC_{dcn}V_{dcn}^2 = V_{dcn}I_{pvn} - P_{dcvscn} \quad (1e)$$

where $\vec{x} = x_d + jx_q$ and the d - q frame components are x_d and x_q , the angular speed is ω , and s is the Laplace operator. Considering a lossless power converter, P_{dcvscn} equals P_n ($P_n = 1.5(v_{ind}i_{nd} + v_{inq}i_{nq})$).

B. PV-VSC CONTROL SYSTEM

Fig. 2 shows the VSC control system, where $x_d(s)$, $x_q(s)$, and $x_{dd}(s)$ are the compensated signals that improve the weak VSC systems stability and it is explained in Section V. Since VSC1 and VSC2 share the same model with the same control, the same control equations represent the control dynamics.

The MPPT controller generates the reference dc-voltage V_{dc}^* , and a PI controller $G^{vdc}(s) = K_p^{vdc} + K_i^{vdc}/s$ regulates V_{dc} to V_{dc}^* via the reference d -axis current i_d^* . A PI Controller

($G^{vac}(s) = K_p^{vac} + K_i^{vac}/s$) regulates the ac-voltage and provides reference q -axis current i_q^* . The term ($\eta P_{pv}/1.5v_d^0$) in (2a) enhances dc-link voltage control robustness, where η is the feed-forward gain, and the superscript "0" is the steady-state value. In (2b), v_d^* is the reference voltage.

$$i_d^* = (V_{dc}^2 - V_{dc}^{*2}) G^{vdc}(s) + \frac{\eta P_{pv}}{1.5v_d^0} \quad (2a)$$

$$i_q^* = \frac{-1}{1.5v_d^0} (v_d^* - v_d^c) G^{vac}(s) \quad (2b)$$

The current controller ($G^i(s) = K_p^i + K_i^i/s$) regulates the current injection. The PLL generates the synchronization angle (ε) and sets the the q -component of the ac-capacitor voltage (v_q^c) to zero using the PI controller ($G^\varepsilon(s) = K_p^\varepsilon + K_i^\varepsilon/s$), and the latter transforms signals from the grid (denoted by superscript "g") to the converter frame (denoted by superscript "c") using $f_{dq}^c = e^{-j\varepsilon} f_{dq}^g$ and vice versa to model the influence of PLL on the weak grid system [12].

$$v_{idq}^c = (i_{dq}^* - i_{dq}^c) G^i(s) + j\omega L_f i_{dq}^c + v_{dq}^c \quad (2c)$$

$$\frac{d\varepsilon}{dt} = \omega = \frac{v_q^c}{v_d^0} G^\varepsilon(s) + \omega^0 \quad (2d)$$

C. WEAK GRID CHARACTERISTICS

The transmission line with a large grid impedance results in a weak grid, significantly impacting the control interactions. The SCR quantifies the strength of a power grid at the point of interconnection (POI), which is the ratio of the grid short-circuit capacity (S_{ac} in VA) at the POI to the sum of the rated power of each PV ($P_{pv\text{rated}}$) injected to the POI [5], [6].

$$SCR = \frac{S_{ac}}{P_{pv\text{rated}}} = \frac{v_g^2 / (\omega L_g)}{P_{pv\text{rated}}} \quad (3)$$

The SCR calculation for this study includes the number of parallel converters. From (3), the POI can be identified as strong ($SCR > 3$), weak ($2 \leq SCR \leq 3$), and very weak ($SCR < 2$).

D. PV SYSTEM MODEL

Fig. 3 shows a PVG equivalent circuit consisting of N_p parallel strings with N_s series modules (each module with n_s cells). The PVG current (I_{pv}) is given by [3]

$$I_{pv} = N_p I_{ph} - N_p I_{rs} \left(\exp \left\{ \frac{q(V_{pv} + (N_s/N_p) R_s I_{pv})}{N_s n_s A k T} \right\} - 1 \right) - \frac{V_{pv} + (N_s/N_p) R_s I_{pv}}{(N_s/N_p) R_{sh}} \quad (4a)$$

where, I_{ph} is the photon-generated, I_D is the diode, and I_{rs} is the diode reverse saturation current. The diode and PV voltage are V_D and V_{pv} , respectively; R_s is the series, and R_{sh} is the shunt resistance; q is the charge; k is the Boltzmann constant; T is the temperature in K; and A is the diode factor.

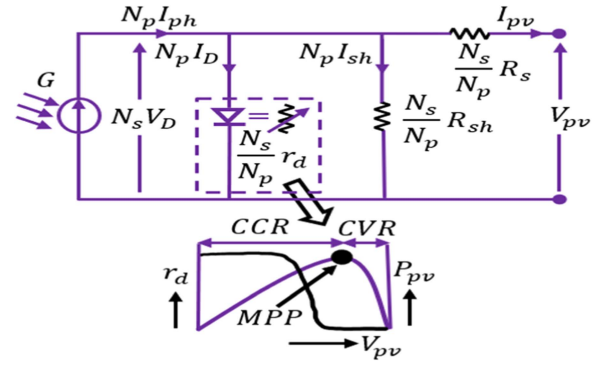


FIGURE 3. PVG equivalent model.

The P_{pv} - V_{pv} curve in Fig. 3 shows the r_d - V_{pv} characteristics due to a nonlinear I_D - V_D relationship, where r_d is the PVG dynamic resistance, which can be expressed as [3], [6]

$$r_d = - \left(\frac{dI_{pv}}{dV_{pv}} \right)^{-1} = \frac{1 + \frac{R_s}{R_{sh}} + \frac{I_{rs} \cdot q \cdot R_s}{n_s \cdot A \cdot k \cdot T} \exp \left(\frac{q(V_{pv} + (\frac{N_s}{N_p}) R_s I_{pv})}{N_s \cdot n_s \cdot A \cdot k \cdot T} \right)}{\left(\frac{1}{(\frac{N_s}{N_p}) R_s} \right) + \frac{q \cdot N_p \cdot I_{rs}}{N_s \cdot n_s \cdot A \cdot k \cdot T} \exp \left(\frac{q(V_{pv} + (\frac{N_s}{N_p}) R_s I_{pv})}{N_s \cdot n_s \cdot A \cdot k \cdot T} \right)} \quad (4b)$$

The total PVG resistance (r_D) can be expressed as

$$r_D = \frac{N_s}{N_p} [(r_d \parallel R_{sh}) + R_s] \quad (4c)$$

As shown in Fig. 3, the PVG operating regions at the left and right of the maximum power point (MPP) are the constant current region (CCR) and constant voltage region (CVR), resulting in r_d changes from a relatively large to a low value [6]. The r_d in (4b) and r_D in (4c) are connected with the VSC systems by $V_{pv} = -r_D I_{pv}$. Therefore, operating the PVG at the CCR can undesirably influence the stability of the PVG-interfaced converter systems compared to the MPP and CVR operational regions. However, the published multi-VSCs system ignored the impact of changing r_d under varying SCR on parallel VSCs control and dc- and ac-side interactions [21], [22], [23], [24], [25], [26], [27], [28], [29], [30], [31], [32]. Therefore, to investigate the control interactions and their influence on stability in weak parallel VSCs system under different PVG operating regions (at CVR, MPP, and CCR), the PVG in Fig. 3 can be modeled as a Norton equivalent circuit, where r_D , including r_d , is in parallel with a current source, and the investigation is reported later in Section IV.

III. MODELING AND CONTROL OF PARALLEL CSCS SYSTEM

Fig. 4 shows the 1.0 MW PVG interfaced grid-tied parallel CSCs system, where the control and parameters of CSC1 and CSC2 are identical and listed in Appendix A. The series diode in insulated gate bipolar transistor (IGBT) in Fig. 4 increases the reverse voltage capability.

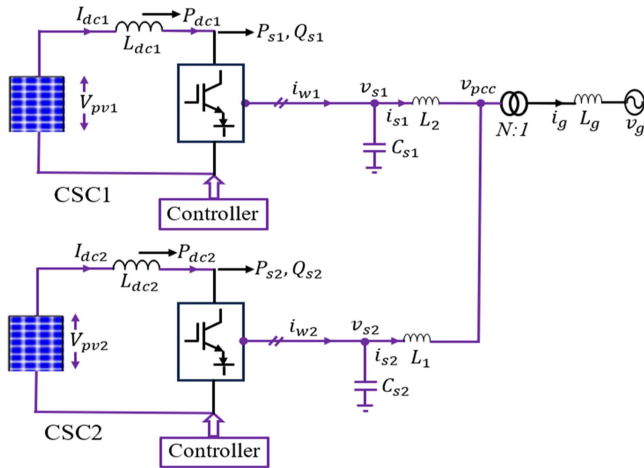


FIGURE 4. PVG-interfaced parallel CSCs system.

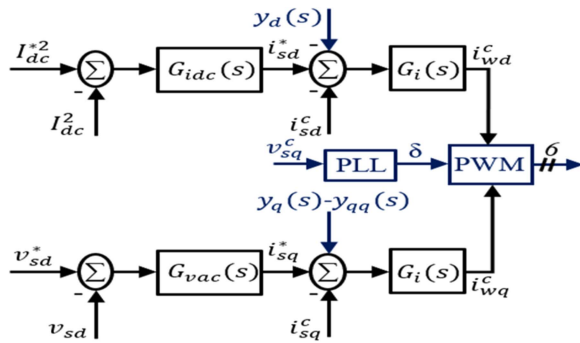


FIGURE 5. PV-CSC control system.

A. PARALLEL CSCS MODEL DYNAMICS

Fig. 4 shows that an inductor (L_{dcn}) connects the PVG to the CSC and maintains a smooth dc-link current (I_{dcn}), where n is the converter number (i.e., $n=1, 2$). The PV voltage is V_{pvn} , and the CSC's dc-side power is P_{dcn} . A capacitor (C_{sn}) with voltage v_{sn} attenuates the switching harmonics of CSC output current i_{wn} ; P_{sn} is active, and Q_{sn} is the reactive power. The feeder inductance is L_n , and the current through it is i_{sn} . The PCC voltage is v_{pcc} , and N is the transformer ratio. The parallel CSCs dynamics are given by

$$\vec{i}_{wn} = (sC_{sn} + j\omega C_{sn}) \vec{v}_{sn} + \vec{i}_{sn} \quad (5a)$$

$$\vec{v}_{sn} = (sL_n + j\omega L_n) \vec{i}_{sn} + \vec{v}_{pcc} \quad (5b)$$

$$N\vec{v}_{pcc} = (sL_g + j\omega L_g) \vec{i}_g + \vec{v}_g \quad (5c)$$

$$\frac{1}{2}sL_{dcn}I_{dcn}^2 = V_{pvn}I_{dcn} - P_{dcn} \quad (5d)$$

Considering the loss across the CSC is negligible, P_{dcn} equals P_{sn} ($P_{sn} = 1.5(v_{snd}i_{snd} + v_{snq}i_{snq})$).

B. PV-CSC CONTROL SYSTEM

Fig. 5 shows the CSC control system, where $y_d(s)$, $y_q(s)$, and $y_{qq}(s)$ are the compensated signals explained in Section V.

The same control equations represent the control dynamics in parallel CSCs as CSC1 and CSC2 share the same model.

The MPPT controller generates the reference dc-current I_{dc}^* , and a PI controller $G_{idc}(s) = K_{pidc} + K_{iadc}/s$ processes $(I_{dc}^{*2} - I_{dc}^2)$ and generates i_{sd}^* for active power balance across the CSC. A PI controller $G_{vac}(s) = K_{pvac} + K_{ivac}/s$ regulates the ac-voltage and generates the reference current i_{sq}^* .

$$i_{sd}^* = (I_{dc}^{*2} - I_{dc}^2) G_{idc}(s) \quad (6a)$$

$$i_{sq}^* = \frac{-1}{1.5v_{sd}^0} (v_{sd}^* - v_{sd}^c) G_{vac}(s) \quad (6b)$$

Furthermore, a PI current controller $G_i(s) = K_{pi} + K_{ii}/s$ regulates i_{sdq} to the reference current (i_{sdq}^*) to adjust active and reactive power injection. Finally, the PLL controller $G_\delta(s) = K_{p\delta} + K_{i\delta}/s$ synthesizes v_{sq}^c and generates the synchronization angle (δ) to synchronize the CSC to the utility grid, the latter is used for converter-grid frame transformation.

$$i_{wdq}^c = d_{dq}^c I_{dc} = (i_{sdq}^* - i_{sdq}^c) G_i(s) \quad (6c)$$

$$\frac{d\delta}{dt} = \omega = \frac{v_{sq}^c}{v_{sd}^0} G_\delta(s) + \omega^0 \quad (6d)$$

where, d_{dq}^c is the CSC control variable and v_{sd}^* is the reference voltage. Detailed design guidelines for the VSC and CSC control system can be found in [12], [36], [38].

The parallel CSCs study in [33], [34], [35] did not consider PVG dynamics to analyze how CSCs in parallel connections interact and its influence on stability when tied to a weak grid. Moreover, control interaction differences among parallel VSCs and multi-CSCs systems under different PVG operating regions (at MPP, CVR, and CCR) and grid strengths are still unknown. Therefore, the PVG dynamics in a weak ac grid system are considered in this paper to characterize the control interactions and stability of two parallel systems correctly.

IV. WEAK GRID-TIED PARALLEL VSCS AND PARALLEL CSCS SYSTEM INTERACTION ANALYSIS

This section analyzes and differentiates the weak grid-tied parallel VSCs and CSCs dc-link interactions with the changing PVG dynamic resistance and control parameters.

A. PARALLEL CONVERTERS DYNAMIC INTERACTION MECHANISM

In a converter system, the PCC voltage becomes sensitive to changing SCR and PVG dynamic resistance [32]. Operating the PVG in one converter at the CCR compared to the MPP and CVR operational regions in a weak ac grid affects dc-link stability and output power, leading to terminal voltage change, PLL operation, and PCC voltage. Furthermore, coupling affects the terminal voltage and PLL operation of the other converters, leading to output power changes and dc-link stability [36]. Therefore, under varying PVG dynamics in a weak grid, the control interactions that affect the stability of

dc-link voltage control in paralleled VSCs and dc-link current control in paralleled CSCs are investigated in this paper.

B. LINEARIZATION AND STABILITY ANALYSIS

The equations in (1a)–(4c) and (4a)–(6d) can be merged to obtain parallel VSCs and CSCs system state-space models as

$$\begin{cases} \dot{x} = f(x, u, d, r) \\ y = h(x, u, d, r) \end{cases} \quad (7a)$$

where, x is the state and y is the output vector; u , d , and r are the control, disturbance and reference input, respectively.

The steady-state d and r values define where the converters operate, known as the operating points. The PVG in Fig. 3 is highly nonlinear, resulting in the system under investigation shown in Figs. 1 and 4 are nonlinear; therefore, the model (7a) represents nonlinear differential equations. Moreover, the change in the conditions (i.e., the PVG dynamic resistance, SCR, power injection, and PLL bandwidth) changes the PVG interfaced parallel converters' system dynamic mode, and the steady-state equilibrium points (x_e), which is the steady-state value of the state x in (7a) [37]. As the model is nonlinear, the linearized state-space model in this paper is evaluated at the equilibrium point for the correct computation.

The state-space model equilibrium point is obtained using the MATLAB symbolic toolbox by setting all the differential equations in (7a) to zero. Finally, the transfer function $G_Y(s)$ of the model (7a) linearized around its x_e is computed for the frequency domain analysis and can be expressed as

$$G_Y(s) = \frac{Y(s)}{U(s)} = C(sI - A)^{-1}B \quad (7b)$$

where, A , B , and C are the state, input, and output matrices.

The following cases are considered to investigate the dc-link dynamic interactions and differences among parallel VSCs and CSCs systems.

1) EFFECT OF CHANGING SCR

The effect of changing SCR (i.e., high to low) on the frequency response of the VSC1 control variable (m_{d1}) to the d -axis terminal voltage (v_{d1}) transfer function ($G_{cv_{d1}} = \frac{v_{d1}}{m_{d1}}$) is shown in Fig. 6(a). If SCR decreases from 4 to 1.2, the magnitude of $G_{cv_{d1}}$ increases, implying increased interactions between VSC1s dc-link to the terminal voltage, affecting the PCC voltage and PLL operation. Due to coupling in parallel VSCs, the interaction with VSC2 increases, reflected by the magnitude and phase increase in the frequency response of the VSC2 control variable (m_{d2}) to the d -axis output current (i_{d2}) transfer function ($G_{ci_{d2}} = \frac{i_{d2}}{m_{d2}}$), as shown in Fig. 6(b). The i_{d2} changes affect the VSC2 active power (P_2) and dc-link voltage (V_{dc2}) control stability. For parallel CSCs, in addition to the magnitude increase, resonance peaks are observed in the CSC2 dc-link current (I_{dc2}) to the CSC1 PV voltage (V_{pv1}) transfer function ($G_{I_{dc2}V_{pv1}} = \frac{V_{pv1}}{I_{dc2}}$), as shown in Fig. 7. Moreover, the phase lags and suddenly leads with

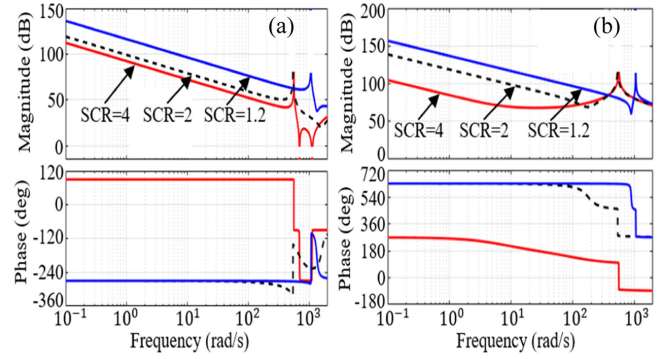


FIGURE 6. Effect of varying SCR on parallel VSCs: (a) $G_{cv_{d1}}$ and (b) $G_{ci_{d2}}$.

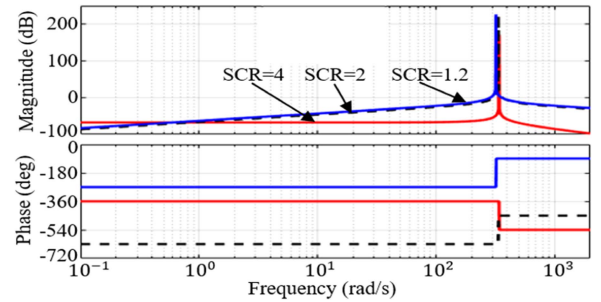


FIGURE 7. Effect of varying SCR on parallel CSCs: $G_{I_{dc2}V_{pv1}}$.

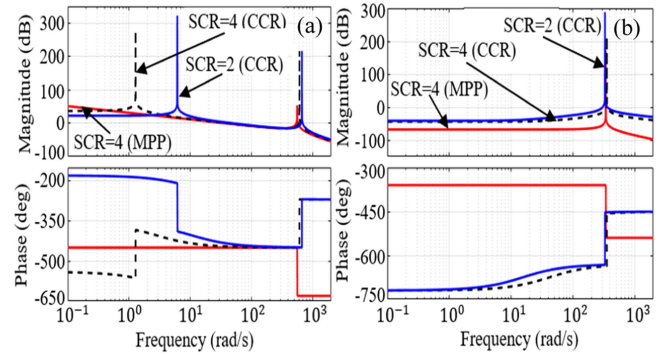


FIGURE 8. Effect of dynamic resistance: (a) Parallel VSCs and (b) parallel CSCs.

SCR=2 compared to SCR=4, further deteriorating the dc-link stability.

2) EFFECT OF PVG DYNAMIC RESISTANCE

Fig. 8 shows the effect of varying PVG dynamic resistance on parallel VSCs and CSCs systems dc-link interactions under changing grid-strength conditions. For parallel VSCs, the PVG in VSC2 at the CCR (i.e., high r_d) with SCR=4 shows a high resonant peak in the frequency response of PV2 current (I_{pv2}) to VSC1 dc-link voltage (V_{dc1}) transfer function ($G_{I_{pv2}V_{dc1}} = \frac{V_{dc1}}{I_{pv2}}$), as shown in Fig. 8(a) due to the appearance of resonant roots in $G_{I_{pv2}V_{dc1}}$ compared to the case where PVG in VSC2 operates at the MPP (i.e., low r_d). The lagging and

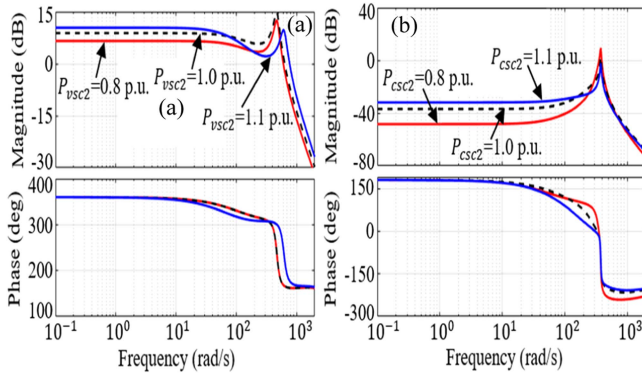


FIGURE 9. Effect of changing power injection: (a) $G_{iod2vsc}$ and (b) $G_{iod2csc}$.

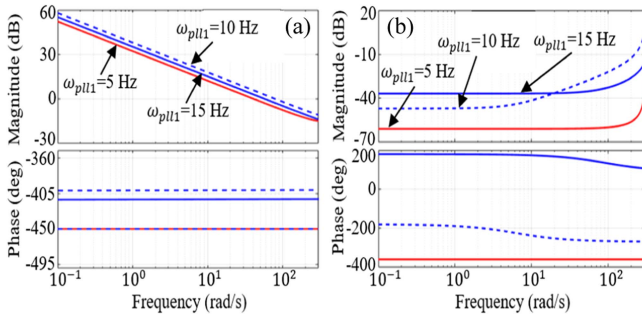


FIGURE 10. Effect of PLL bandwidth: (a) Parallel VSCs and (b) parallel CSCs.

leading phase at the CCR increases the dc-link interaction and affects stability. If SCR decreases to 2, the resonant peak further increases, affecting the damping. In the case of parallel CSCs, the $G_{Idc2Vpv1}$ magnitude highly increases when PVG in CSC2 at the CCR with SCR=4 compared to the case with PVG at the MPP, as shown in Fig. 8(b), implying higher interactions in parallel CSCs system. Moreover, the resonant peak increases considerably with SCR=2.

3) EFFECT OF CONVERTERS POWER INJECTION

Fig. 9 shows the impact of converter2's power injection on the I_{pv2} to i_{d2} transfer function ($G_{iod2vsc} = \frac{i_{d2}}{I_{pv2}}$) for parallel VSCs and I_{dc2} to the CSC2 d -axis reactor current (i_{sd2}) transfer function ($G_{iod2csc} = \frac{i_{sd2}}{I_{dc2}}$) for parallel CSCs. For rated 1.0 p.u. power injection with SCR=2, the magnitude increase is higher for $G_{iod2csc}$ than the increase in $G_{iod2vsc}$, indicating increased dc-link interactions in parallel CSCs than parallel VSCs. For $G_{iod2vsc}$, the phase remains identical; however, leading and lagging in $G_{iod2csc}$, thus affecting the terminal characteristics.

4) EFFECT OF PLL BANDWIDTH

The parallel converters' dc-link interaction with the changing PLL bandwidth of converter1 (ω_{pll1}) is shown in Fig. 10 when SCR=2 and $\omega_{pll2} = 10$ Hz. For parallel VSCs, the magnitude and phase of $G_{I_{pv2}V_{dc1}}$ increase if $\omega_{pll1} \leq \omega_{pll2}$, as shown in Fig. 10(a) but it decreases if $\omega_{pll1} > \omega_{pll2}$, resulting in stability

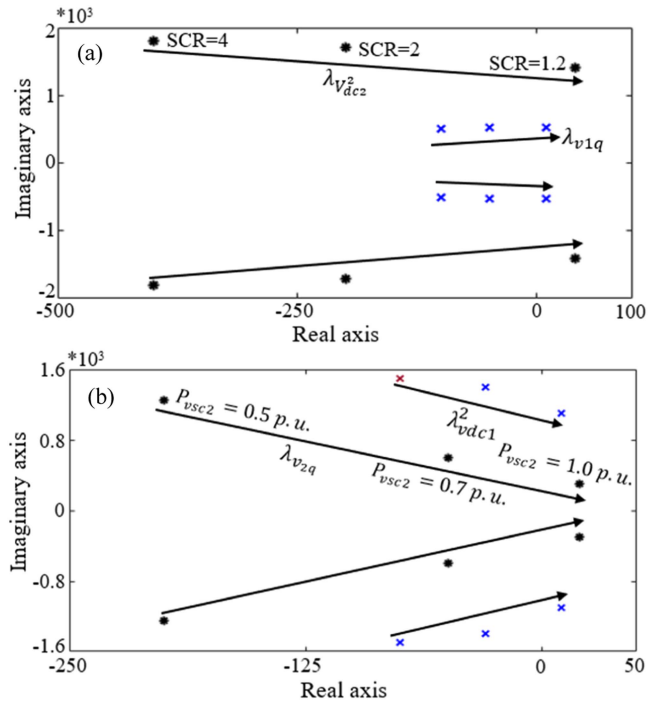


FIGURE 11. Parallel VSCs: (a) Effect of SCR and (b) active power injection.

improvements. However, for parallel CSCs, if $\omega_{pll1} \geq \omega_{pll2}$, the magnitude and phase of $G_{Idc2Vpv1}$ increase, as shown in Fig. 10(b), indicating stability degradation compared to stability improvements in parallel VSCs. It demonstrates that changing PLL bandwidth affects the dc-link stability of parallel VSCs and CSCs differently.

C. EIGENVALUE ANALYSIS

Fig. 11(a) shows that if SCR decreases from 4 to 1.2, the VSC1s terminal voltage eigenvalue (λ_{v1dq}) moves into the unstable plane, which reduces the damping ratio (ζ) from 0.196 to 0.018; therefore, the VSC2 dc-link eigenvalue (λ_{vdc2}) moves into the unstable region, verifying that the instability in VSC1 affects the dc-link voltage control stability of VSC2. The increase of P_{vsc2} from 0.5 to 1.0 p.u. for SCR = 1.2 shifts the VSC2s terminal voltage eigenvalue (λ_{v2q}) to the right side of the s -plane, which decreases ζ from 0.157 to 0.066 and the oscillation frequency (ω_n) from 201 to 47 Hz, affects the PCC voltage and the movement of λ_{vdc2} , as shown in Fig. 11(b). For parallel CSCs, if the ac grid becomes weak, the CSC2 terminal voltage eigenvalue (λ_{v_s2d}) moves toward the right, as shown in Fig. 12(a), reduces ω_n from 79.5 to 3.2 Hz, and shifting the CSC1 dc-link current eigenvalue ($\lambda_{J_{dc1}^2}$) into the unstable plane (ζ decreases from 0.164 to 0.034 and ω_n changes from 96.8 to 92.3 Hz), implying that CSC2 affects the stability of CSC1. Fig. 12(b) shows that, with r_d in the VSC2 PVG model, λ_{v_s2d} moves toward the right compared to the case without r_d , which shifts the dc-link current eigenvalue of CSC2 ($\lambda_{J_{dc2}^2}$) into the right side of the s -plane, makes the system unstable

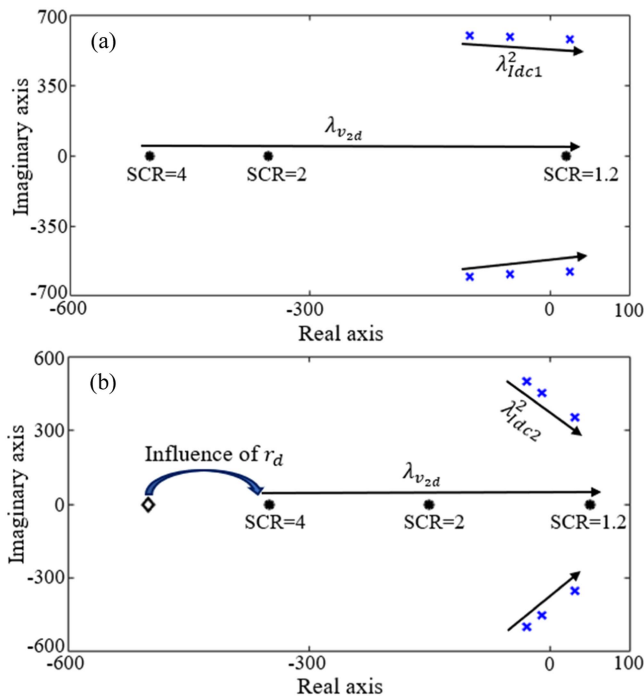


FIGURE 12. Parallel CSCs: (a) Effect of SCR and (b) dynamic resistance.

when the SCR changes from 4 to 1.2, resulting in an unstable λ_{dc1}^2 due to the direct coupling through the PCC.

V. PROPOSED COMPENSATOR OF THE PARALLEL SYSTEMS

From Section IV, the dc-link dynamic interactions between the parallel converters increase when PVG enters the CCR in a weak grid that deteriorates the dc-link stability. Moreover, the changing PLL bandwidth influences parallel VSCs' and CSCs' dc-link interactions differently. Considering the PVG dynamic resistance effect, no compensation methods were proposed in the literature to reduce the dynamic interactions maintaining the dc-link stability for weak grid-tied parallel VSCs and CSCs systems [23], [24], [25], [26], [27], [28], [29], [30], [31], [32], [33]. Therefore, a compensator is proposed to ensure reduced dc-link interactions and stability in parallel converters system when PVG moves from CVR to CCR under different operating conditions. The signals $x_d(s)$, $x_q(s)$, and $x_{dd}(s)$ in Fig. 2 and $y_d(s)$, $y_q(s)$, and $y_{qq}(s)$ in Fig. 5 are the proposed compensated signals for the VSC and CSC systems, respectively. The scaled PLL output (ω) is injected in the VSC and CSC control loop that modifies the VSC output voltage dynamics as (8a) and the CSC output current dynamics as (9a). The VSC and CSC control system injected signals have the damping ratios of ε_v and ε_c , cut-off frequencies of ω_v and ω_c , and scaling gains of K_v and K_c . Additionally, scaled v_d^c , v_q^c for the VSC and v_{sd}^c , v_{sq}^c for the CSC are injected to achieve a damped response, where, K_d , K_q , K_{dd} , and K_{qq} are the gains and ω_d , ω_q , ω_{dd} , and ω_{qq} are the cut-off frequencies. The control dynamic in (1a) is modified to (8a) and (8b), and (6c)

is modified to (9a) and (9b)

$$v_{id}^c = \left(i_d^* - i_d^c - K_v \frac{\overbrace{x_d(s)}^{x_d(s)}}{s^2 + 2\varepsilon_v \omega_v s + \omega_v^2} \omega \right) G^i(s) - \omega L_f i_q^c + v_d^c \quad (8a)$$

$$v_{iq}^c = \left(i_q^* - i_q^c + K_q \frac{\overbrace{x_q(s)}^{x_q(s)}}{s + \omega_q} v_q^c - K_d \frac{\overbrace{x_{dd}(s)}^{x_{dd}(s)}}{\omega_d} v_d^c \right) G^i(s) + \omega L_f i_d^c + v_q^c \quad (8b)$$

$$i_{wd}^c = \left(i_{sd}^* - i_{sd}^c - K_c \frac{\overbrace{y_d(s)}^{y_d(s)}}{s^2 + 2\varepsilon_c \omega_c s + \omega_c^2} \omega \right) G_i(s) \quad (9a)$$

$$i_{wq}^c = \left(i_{sq}^* - i_{sq}^c + K_{qq} \frac{\overbrace{y_{qq}(s)}^{y_{qq}(s)}}{\omega_{qq}} v_{sq}^c - K_{dd} \frac{\overbrace{y_{dd}(s)}^{y_{dd}(s)}}{\omega_{dd}} v_{sd}^c \right) G_i(s) \quad (9b)$$

A. COMPENSATED VSC SYSTEMS PARAMETERS DESIGN

The compensator adds four states to the state-space model of each VSC, and the design steps are: 1) $x_q(s)$ design, 2) $x_d(s)$ design with scaled ω and $x_q(s)$, and 3) $x_{dd}(s)$ design with $x_q(s)$ and $x_d(s)$.

I) $x_q(s)$ DESIGN

If SCR decreases from 4 to 1.2, the diamond-shaped PLL input voltage eigenvalue (λ_{vq}) becomes a complex conjugate that determines the system dynamics and moves to the unstable plane, as shown in Fig. 13(a), resulting in ζ drops from 1 to 0.045. Moreover, the q -current eigenvalue ($\lambda_{\varphi_{iq}}$) in square shape moves to the right, where ζ changes from 0.84 to 0.42. As λ_{vq} affects the VSC systems dynamics and moves to the unstable region, scaled v_q^c is considered for $x_q(s)$ design, considering the worst case of SCR = 1.2. If K_q increases from 0 to 150 with an increase of 25 for $\omega_q = 50$ rad/s, λ_{vq} moves to the left side of the stable region and relocated to $-1039.9 + j6332.6$ from $293.7 + j6436.5$, and ζ increases from 0.04 to 0.18 but negatively impacts the PLL eigenvalue (λ_ε), which moves close to the origin and tends to become unstable.

However, if ω_q changes from 50 to 10 rad/s with $K_q = 125$, λ_{vq} moves to the right side of the s -plane. Therefore, $K_q = 125$ and $\omega_q = 50$ rad/s are selected for optimal system damping. Adding $x_d(s)$ to the compensator mitigates the negative impacts on $\Delta \lambda_\varepsilon$ movement.

II) $x_d(s)$ DESIGN

To improve the stability with SCR = 1.2, in addition to $x_q(s)$, the scaled version of the PLL output (ω) is considered in this case, as λ_ε moved to the unstable plane in step (i), and its impact on the λ_ε is shown in Fig. 13(b). Fig. 13(b) shows that λ_ε relocates to $-499 + j1.785$ from $-231 + j3200$ if K_v increases from 10 to 100 with $\omega_v = 500$ rad/s. However, with $K_v = 100$, if ω_v decreases from 500 to 100 rad/s, λ_ε

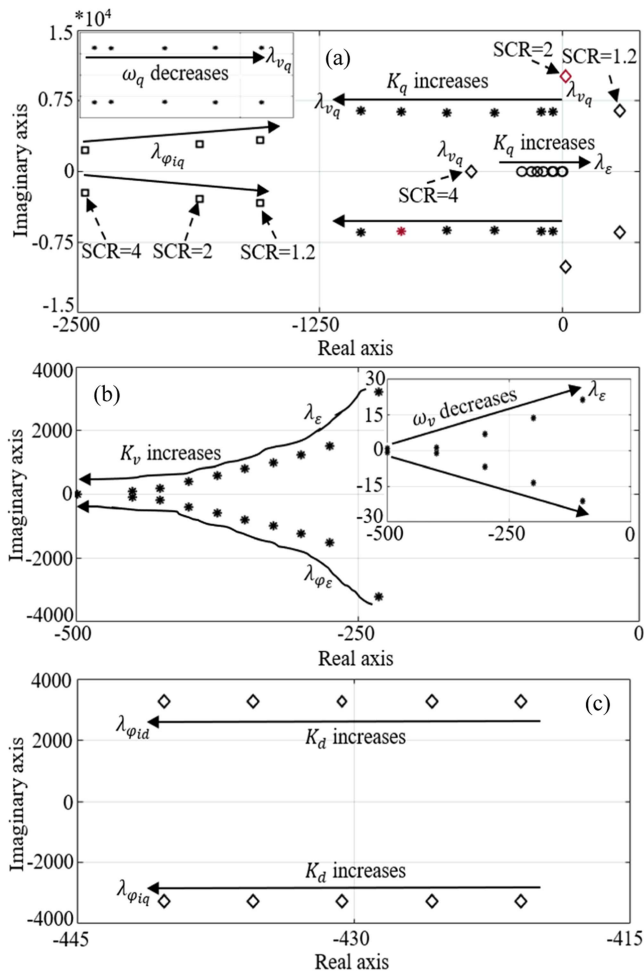


FIGURE 13. VSC systems compensator design: (a) design of $x_q(s)$, (b) $x_d(s)$ and (c) $x_{dd}(s)$.

moves toward the right side and relocates to $-99 + j1.22$ from $-499 + j1.785$. Therefore, K_v and ω_v are selected as 100 and 500 rad/s, respectively, to ensure highly damped operation.

III) $x_{dd}(s)$ DESIGN

A scaled v_d^c is injected with $x_q(s)$ and $x_d(s)$ to add additional damping and disturbance rejection. Considering, both $x_q(s)$ and $x_d(s)$, if K_d increases from 10 to 50 when $\omega_d = 50$ rad/s, the damping of d - and q -axis current eigenvalues ($\lambda_{\varphi_{id}}$ and $\lambda_{\varphi_{iq}}$) increases and moves further to the left, as shown in Fig. 13(c). However, if ω_d decreases, it moves toward the right. Therefore, for enhanced performance $K_d = 50$ and $\omega_d = 50$ rad/s are selected.

Compared to the dominant VSCs eigenvalues placement in Fig. 11, correctly selecting the compensators' gain and cut-off frequency ensures stable operation at SCR = 1.2 by placing all the eigenvalues to the left sides of the s -plane. Moreover, it demonstrates a highly damped response, which will decrease the dc-link dynamic interactions even if PVG enters the CCR from CVR at weak grid conditions.

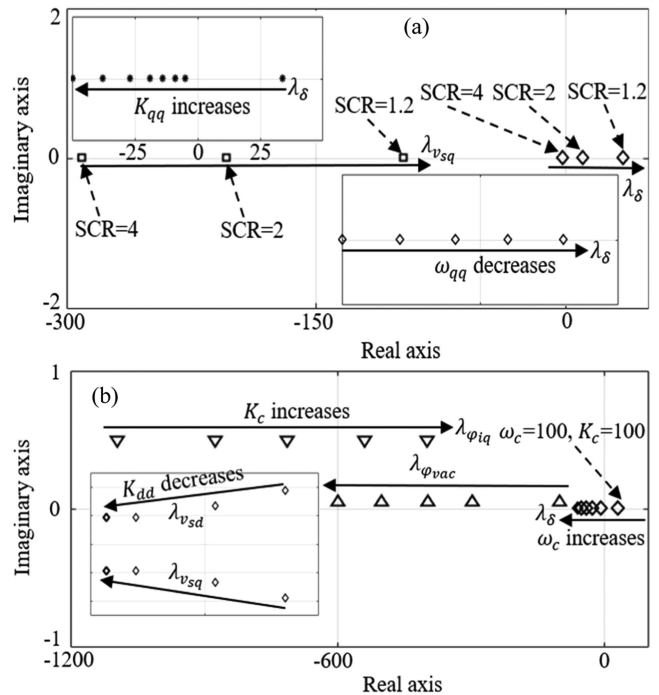


FIGURE 14. CSC systems compensator design: (a) design of $y_q(s)$ and (b) $y_d(s)$ and $y_{qq}(s)$.

B. COMPENSATED CSC SYSTEMS PARAMETERS DESIGN

The CSC compensated signals in (9a) and (9b) add four states in the state-space model, and the design steps are: 1) $y_q(s)$ design, 2) $y_d(s)$ design with scaled ω and $y_q(s)$, and 3) $y_{qq}(s)$ design with $y_q(s)$ and $y_d(s)$.

I) $y_q(s)$ DESIGN

The gain (K_{qq}) and cut-off frequency (ω_{qq}) in $y_q(s)$ are designed considering the movement of PLL and CSC terminal voltage eigenvalues (λ_δ and $\lambda_{v_{sq}}$) at worst case of SCR = 1.2. For SCR = 2 and 1.2, λ_δ enters the unstable plane; however, it remains stable with SCR = 4, as shown in Fig. 14(a). The λ_δ influences the $\lambda_{v_{sq}}$ movement and affects PCC voltage; therefore, scaled v_{sq}^c is considered in the $y_q(s)$ design to mitigate the negative impacts of $\lambda_{v_{sq}}$. Fig. 14(a) shows that if K_{qq} increases from 0 to 2 with $\omega_{qq} = 50$ rad/s, λ_δ moves to the stable plane and relocates to -49.92 from 33.97 with $K_{qq} = 1.5$. However, setting $K_{qq} = 1.5$ and decreasing ω_{qq} from 50 to 10 rad/s shifts λ_δ toward the right side of the s -plane. Therefore, $K_{qq} = 1.5$ and $\omega_{qq} = 50$ rad/s are selected to ensure CSC systems stability and high damping at SCR = 1.2 conditions.

II) $y_d(s)$ DESIGN

In this case, in addition to $y_q(s)$, $y_d(s)$ is injected, and its impact on λ_δ is shown in Fig. 14(b). If ω_c increases from 100 to 600 rad/s with $K_c = 100$, λ_δ moves from 31.57 to -61.41 ; however, it was at -49.92 without $y_d(s)$. Furthermore, the ac voltage control eigenvalue ($\lambda_{\varphi_{vac}}$) moves to the left in the s -plane. However, with $\omega_c = 600$ rad/s, if K_c increases from 0 to 100 with an increase of 25, $\lambda_{\varphi_{iq}}$ moves toward the right

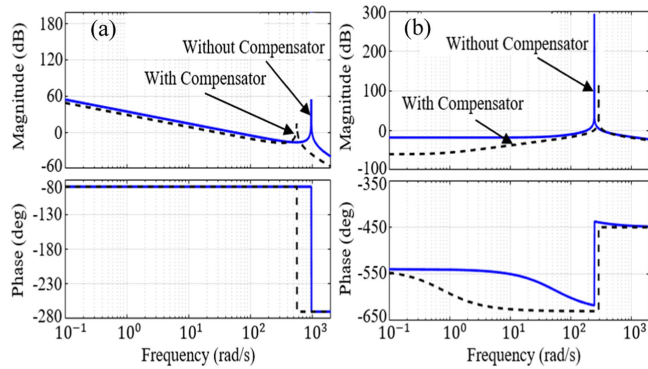


FIGURE 15. Effect of the proposed compensator: (a) $G_{I_{pv}2V_{dc1}}$ and (b) $G_{I_{dc}2V_{pv}1}$.

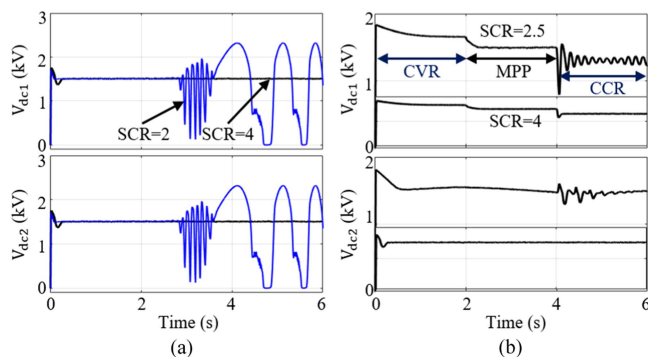


FIGURE 16. Parallel VSCs: (a) Impact of SCR and (b) PVG operating points.

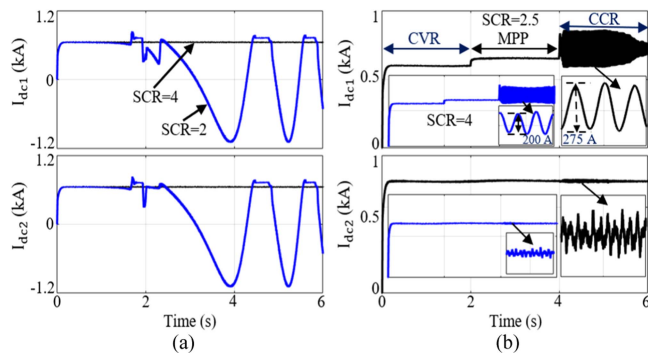


FIGURE 17. Parallel CSCs: (a) Impact of SCR and (b) PVG operating points.

and relocates to -398.7 from -1094.9 , and its locus is shown in Fig. 14(b). Therefore, $K_c = 100$ and $\omega_c = 600$ rad/s are selected, whereas $\varepsilon_c = 1.0$, ensuring rated power injection and highly damped weak CSC system's response.

III) $y_{qq}(s)$ DESIGN

Although $y_q(s)$ and $y_d(s)$ introduced damping, the $y_{qq}(s)$ injection offers disturbance rejection with increased damping. Therefore, a scaled v_{sd}^c is injected, and its effect on $\lambda_{v_{sd}}$ and $\lambda_{v_{sq}}$ is shown in Fig. 14(b), which offers a better response with $K_{dd} = 0.25$ and $\omega_d = 50$ rad/s.

Compared to the uncompensated CSC systems' eigenvalue placement in Fig. 12, the proposed compensator maintains a

stable operation when connected to a weak grid if the gain and cut-off frequencies are properly selected, which will ensure the reduced dynamic interactions in a parallel CSCs system at different operating conditions.

C. IMPACT OF THE PROPOSED COMPENSATOR

The compensated parallel VSCs system response in Fig. 15(a) shows the decreased magnitude and resonance peak of $G_{I_{pv}2V_{dc1}}$ compared to the uncompensated system, implying reduced dynamic dc-link interactions among VSC1 and VSC2. However, for parallel CSCs, the magnitude and resonant peak of $G_{I_{dc}2V_{pv}1}$ significantly decrease, as shown in Fig. 15(b). The phase decreases with the proposed compensator, reducing dc-link interactions in a weak parallel CSCs system. The frequency domain study in Fig. 15 verifies the robustness of the proposed compensator in a weak grid for the parallel VSCs and CSCs system.

VI. SIMULATION RESULTS

The dc-link dynamic interactions, stability comparisons, and the robustness of the proposed compensator of PV-interfaced weak grid-tied utility-scale parallel VSCs and CSCs systems in Figs. 1 and 4 are validated with time-domain simulation results in MATLAB/Simulink using a $20 \mu s$ sampling time. The complete system parameters are listed in Appendix A.

A. UNCOMPENSATED PARALLEL VSCS AND PARALLEL CSCS SYSTEM AT DIFFERENT SCR AND r_d CONDITIONS

The uncompensated responses of parallel VSCs (i.e., V_{dc1} and V_{dc2}) and parallel CSCs (i.e., I_{dc1} and I_{dc2}) systems at different SCR values are shown in Figs. 16(a) and 17(a), respectively, and shows stable responses with $SCR = 4$ in both cases. However, if the SCR decreases to 2, there is a low-frequency (< 60 Hz) instability followed by oscillations in V_{dc1} response compared to the overshoot, undershoot, and low-frequency instability in I_{dc1} . Moreover, the direct converters coupling through the PCC, the instability is reflected in V_{dc2} and I_{dc2} due to the fluctuations of PCC voltage, which affects the PLL synchronization operation. Next, the PVG in converter1 operates at the CVR ($t = 0-2$ s), MPP ($t = 2-4$ s), and CCR ($t = 4-6$ s), while the converter2 at the MPP and its impact is investigated. With $SCR = 4$, V_{dc1} in Fig. 16(b) is stable from CVR to CCR; however, I_{dc1} in Fig. 17(b) oscillates with high frequency (> 200 Hz) and becomes unstable when moving to CCR due to unstable resonant roots but remains stable at CVR and MPP. For $SCR = 2.5$, V_{dc1} is stable at the CVR and MPP but oscillates at CCR. This results in instability due to higher interactions from high r_d and L_g , impacting V_{dc2} , as shown in Fig. 16(b). However, when operating the PVG at the CCR, I_{dc1} oscillates with high frequency (oscillation magnitude 275 A), becomes unstable, and impacts I_{dc2} , verifying that r_d affects parallel CSCs dc-link operation differently than parallel VSCs operation. Therefore, considering r_d , weak grid-tied parallel VSCs and CSCs interaction and stability study is crucial.

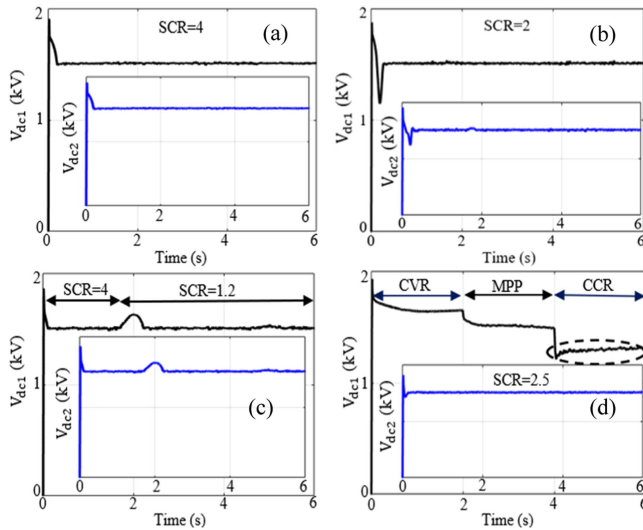


FIGURE 18. Effect of the proposed compensator on parallel VSCs operation: (a) SCR=4, (b) SCR=2, (c) changing SCR from 4 to 1.2 and (d) changing PVG operating conditions for SCR=2.5.

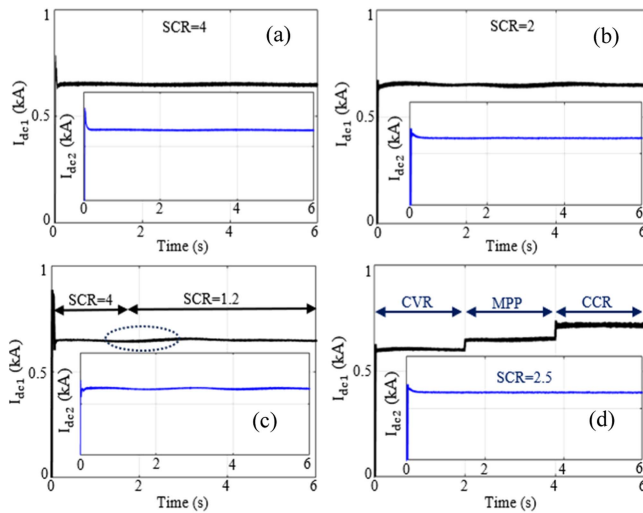


FIGURE 19. Effect of the proposed compensator on parallel CSCs operation: (a) SCR=4, (b) SCR=2, (c) changing SCR from 4 to 1.2, and (d) changing PVG operating conditions for SCR=2.5.

B. COMPENSATED PARALLEL CONVERTERS OPERATION

The proposed compensator is implemented, and its impact on parallel VSCs and CSCs operation is shown in Figs. 18 and 19, respectively. The compensated V_{dc1} and V_{dc2} in Fig. 18(a) and (b) remain stable for SCR = 4 and SCR = 2, respectively, verifying the proposed control method does not alter stability when SCR = 4. The robustness of the proposed control method is challenged by changing the grid dynamics from strong to weak (SCR varies from 4 to 1.2), and V_{dc1} and V_{dc2} in Fig. 18(c) suffer from overshoot during the SCR changes; however, the control system damps the transients quickly and maintains a highly damped stable response. Moreover, for SCR = 2.5, V_{dc1} in Fig. 18(d) remains stable from CVR to CCR, compared to the unstable response in Fig. 16(b),

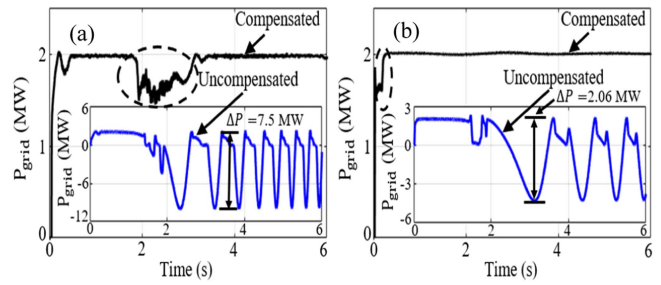


FIGURE 20. Power injection with the proposed compensator: (a) parallel VSCs and (b) parallel CSCs.

demonstrating the effectiveness of the proposed control under changing PVG dynamics in a weak grid.

The compensated I_{dc1} and I_{dc2} for the parallel CSCs in Fig. 19(a) and (b) show stable responses for SCR=4 and SCR=2, respectively, demonstrating that the proposed control does not affect the stability at SCR=4. If SCR varies from 4 to 1.2, the compensated I_{dc1} in Fig. 19(c) suffers from undershooting; however, it reaches a steady state and shows a stable response, which verifies the robustness of the proposed control under varying grid dynamics. Moreover, it ensures stable I_{dc1} and I_{dc2} from CVR to CCR with SCR=2.5 in Fig. 19(d). The uncompensated and compensated power injected into the grid response (P_{grid}) by the parallel VSCs and CSCs systems is shown in Fig. 20 when SCR=1.2. The oscillation magnitude in uncompensated P_{grid} in Fig. 20(a) for parallel VSCs is 7.5 MW, higher than 2.06 MW in parallel CSCs in Fig. 20(b). Moreover, it can not inject the rated power of 2.0 MW (1.0 MW from each converter). However, compensated parallel VSCs and CSCs systems can inject a rated power of 2.0 MW, as shown in Fig. 20. The parallel VSCs system suffers from undershooting for a shorter period. In contrast, the transient response slightly oscillates for parallel CSCs.

C. PARALLEL CONVERTERS OPERATION UNDER FAULT

A single-line-to-ground fault is applied for four cycles at the CVR, MPP, and CCR, and Fig. 21 shows its impact on parallel converters' dc-link operation. The compensated V_{dc1} in Fig. 21(a) is stable at the CVR and MPP; moreover, the overshoot undershoots difference reduces from 1165 to 450 V, providing fast fault clearance compared to the uncompensated V_{dc1} in the MPP mode. Moreover, it reduces oscillation in V_{dc1} at the CCR, ensuring stable, damped V_{dc2} operation (the magnitude decreases from 730 to 375 V), as shown in Fig. 21(b). For parallel CSCs, the compensated I_{dc1} in Fig. 21(c) offers a lower settling time and reduces the magnitude from 415 to 190 A at the fault time in the MPP regions. In addition, the compensator ensures stability by overcoming the high-frequency instability in the CCR, reducing the interaction with I_{dc2} , as shown in Fig. 21(d), reflecting a highly damped response and verifying the effectiveness of the proposed compensator under faults at different PVG operating regions.

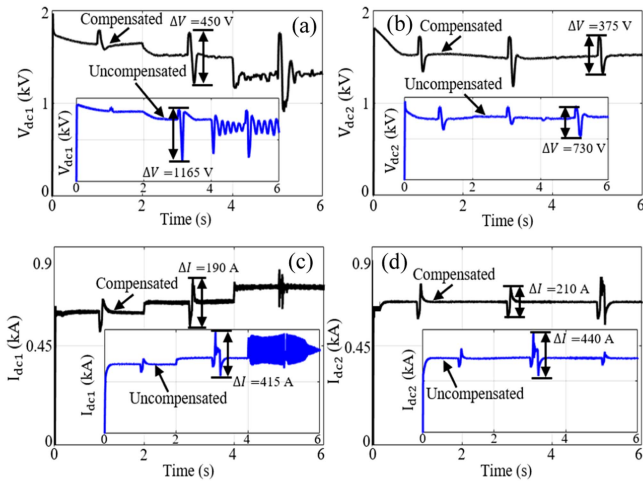


FIGURE 21. Effect of the proposed compensator under fault: (a) V_{dc1} , (b) V_{dc2} , (c) I_{dc1} and (d) I_{dc2} .

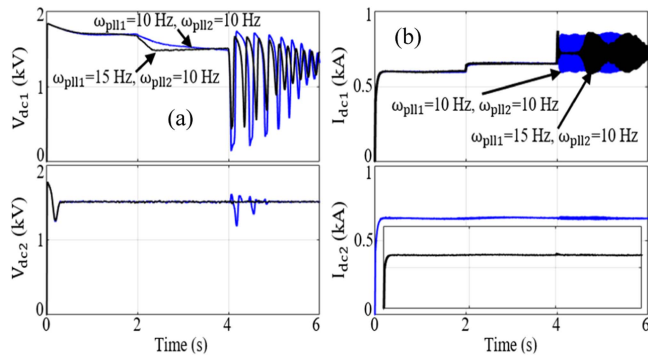


FIGURE 22. Effect of PLL bandwidth: (a) Parallel VSCs and (b) parallel CSCs.

D. EFFECT OF CHANGING PLL BANDWIDTH

For parallel VSCs, if ω_{pll1} changes from 10 to 15 Hz when $\omega_{pll2}=10$ Hz with $SCR=2.5$, V_{dc1} in Fig. 22(a) reaches a steady state faster in the MPP mode and decreased oscillations with improved stability at the CCR, resulting in highly damped V_{dc2} with reduced interactions and verifies the analysis presented in Section IV. However, under the same scenario, the stability of I_{dc1} in Fig. 22(b) deteriorates for parallel CSCs, verifying that changing ω_{pll} impacts the parallel VSCs and CSCs dc-link stability differently when PVG dynamics are considered.

VII. VALIDATION RESULTS

To validate the effectiveness of the proposed compensation method in ensuring stability and reduced dc-link dynamic interactions between the parallel converters at weak grid conditions considering PVG dynamic resistance, the OPAL-RT OP5600 setup shown in Fig. 23 has been used for real-time simulations. The setup adopts a Virtex-6 FPGA board with a step time of 290 ns, and it is fully integrated with MATLAB/Simulink. In real-time, parallel VSCs and CSCs systems are simulated with a 20 μs sampling time, and the parallel

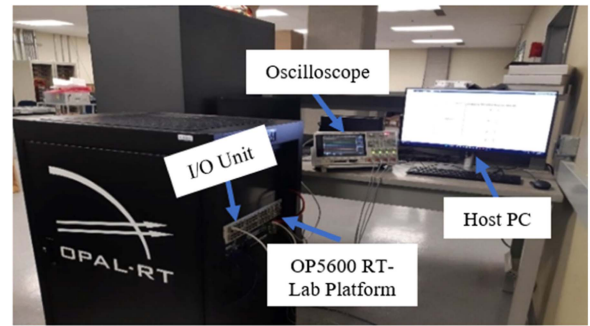


FIGURE 23. Real-time simulation setup.

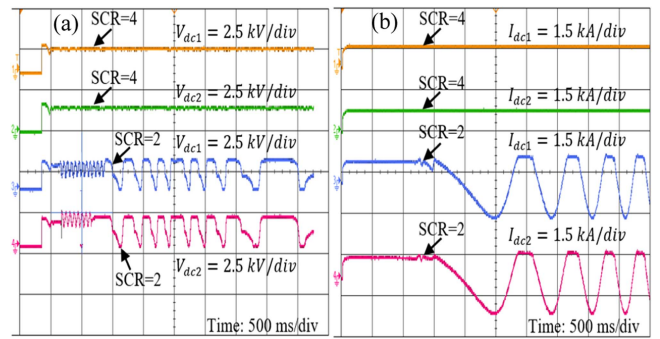


FIGURE 24. Effect of SCR: (a) Parallel VSCs and (b) parallel CSCs.

converters compensation methods are implemented to verify their real-time performance. Finally, the I/O unit accesses the results to display on a 500 MHz oscilloscope. The host PC is connected to the real-time simulator to change the input data, i.e., dynamic resistance, grid strength, and control parameters.

The uncompensated real-time simulated responses of V_{dc1} and V_{dc2} of parallel VSCs system in Fig. 24(a) are stable with $SCR=4$. However, if SCR decreases to 2, V_{dc1} oscillates and becomes unstable, which impacts the stability of V_{dc2} , implying one converter affects the dc-link stability of another converter through the coupled network. For parallel CSCs, there is an overshoot and undershoot in I_{dc1} , which oscillates with low frequency, affecting the I_{dc2} stability for $SCR=2$, as shown in Fig. 24(b). However, I_{dc1} and I_{dc2} show a damped stable response for $SCR=4$, which verifies the time-domain simulation results in Section VI.

In the following case, the PVG in converter1 operates from CVR to CCR, whereas the PVG in converter2 operates at the MPP, and the impacts of PVG dynamics on parallel VSCs and parallel CSCs dc-link responses are shown in Fig. 25 for $SCR=2.5$. The uncompensated V_{dc1} in Fig. 25(a) for parallel VSCs suffers from low-frequency instability at the CCR compared to high-frequency oscillations in I_{dc1} for parallel CSCs, as shown in Fig. 25(b), which verifies the simulation results shown in Figs. 16(b) and 17(b), respectively. The instability in V_{dc1} and I_{dc1} is reflected in V_{dc2} and I_{dc2} as the parallel converters are coupled through the PCC. It is clear that PVG

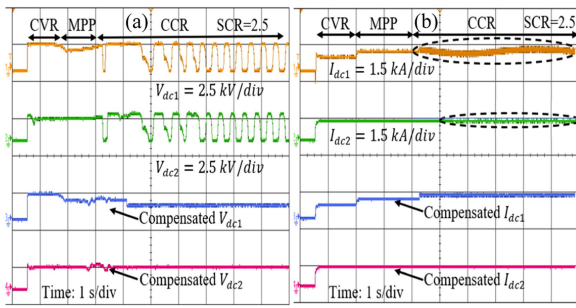


FIGURE 25. Effect of PVG dynamics: (a) Parallel VSCs and (b) parallel CSCs.

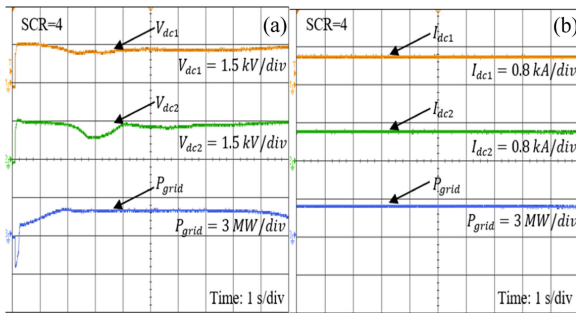


FIGURE 26. Compensated parallel converters operation with SCR=4: (a) parallel VSCs and (b) parallel CSCs.

dynamic resistance at a weak grid differently influences parallel VSCs and parallel CSCs dc-link operation; therefore, a dynamic interaction study considering the PVG dynamics is essential. However, the compensated responses remain stable from CVR to CCR at a weak grid, demonstrating the proposed compensator's robustness under changing PVG dynamics. It verifies the theoretical analysis and is an effective solution for improving parallel converters' stability.

Fig. 26(a) and (b) show the compensated responses for parallel VSCs and CSCs systems, respectively, with SCR=4. The V_{dc1} and V_{dc2} in Fig. 26(a) and I_{dc1} and I_{dc2} in Fig. 26(b) are stable, showing the proposed control method does not alter the stability of the parallel system and can inject 1.0 p.u. power to the grid, which verifies the simulation results shown in Figs. 18(a) and 19(a), respectively. If the SCR decreases to 2, the compensated V_{dc1} and V_{dc2} for parallel VSCs in Fig. 27(a) suffer from undershooting; however, they reach a steady state, remain stable, and show a highly damped response. The I_{dc1} and I_{dc2} in Fig. 27(b) are stable compared to the unstable responses shown in Fig. 24; therefore, the dynamic interactions between the parallel CSCs dc-link are reduced.

Fig. 28 shows that the uncompensated V_{dc1} and V_{dc2} for parallel VSCs and I_{dc1} and I_{dc2} responses for parallel CSCs are unstable when SCR=1.2. Since PV-VSC parameters in parallel VSCs and PV-CSC in parallel CSCs are the same, V_{dc1} and V_{dc2} in parallel VSCs and I_{dc1} and I_{dc2} responses in parallel CSCs shown in Fig. 28 are identical. Moreover, the

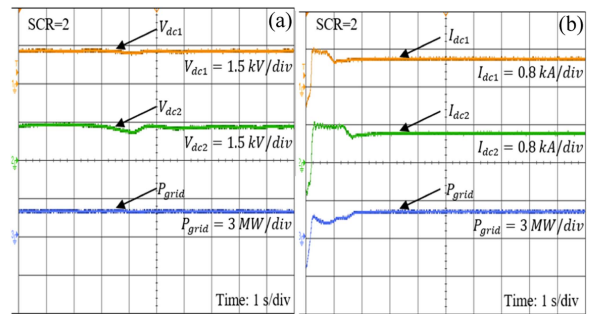


FIGURE 27. Compensated parallel converters operation with SCR=2: (a) parallel VSCs and (b) parallel CSCs.

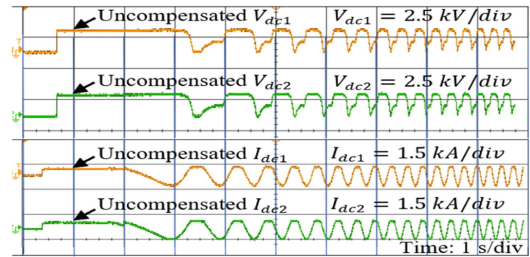


FIGURE 28. Uncompensated operation.

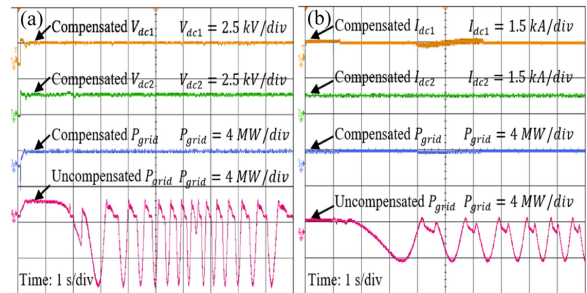


FIGURE 29. Compensated operation: (a) Parallel VSCs and (b) parallel CSCs.

dc-link instability affects power injection and uncompensated P_{grid} in Fig. 29(a) and (b) oscillate, becomes unstable, and cannot reach its rated value.

Finally, the proposed compensator is implemented in the real-time simulations, and its effectiveness is demonstrated in Fig. 29. Compared to the uncompensated V_{dc1} and V_{dc2} in Fig. 28, the proposed compensator reduces interactions between V_{dc1} and V_{dc2} . Moreover, it remains stable and injects rated 2.0 MW rated power (1.0 MW from each VSC) for parallel VSCs, as shown in Fig. 29(a). In the case of parallel CSCs, the proposed CSC compensator ensures stable I_{dc1} and I_{dc2} at SCR=1.2 and injects rated 2.0 MW power, as shown in Fig. 29(b), which validates the simulation results.

VIII. CONCLUSION

This paper investigated the dc-link interaction and stability differences among the weak grid-tied parallel VSCs and parallel CSCs systems, considering the impacts of PVG dynamic

resistance. The linearized model is developed to characterize the parallel converters' dc-link interaction and its effect on stability under PVG operating regions changing from the CVR to CCR, varying SCR, and PLL bandwidth changes. Furthermore, a stability enhancement method has been proposed for both systems to maintain stability at all PVG operating conditions (CVR, MPP, and CCR) with reduced interactions and rated power injection into the grid when tied to a very weak grid (SCR=1.2). Furthermore, the detailed nonlinear time-domain and real-time simulation results have verified the proposed stability enhancement method. The findings are:

- 1) A PVG at the CCR in a weak grid influences the low-frequency (<60 Hz) dc-link instability for parallel VSCs compared to the high-frequency (>200 Hz) instability for parallel CSCs.
- 2) The parallel VSCs dc-link suffer from low-frequency instability followed by oscillations with SCR=2 compared to the only low-frequency instability in parallel CSCs.
- 3) The oscillation magnitude of uncompensated parallel VSCs P_{grid} is higher than that in parallel CSCs at SCR=1.2 (almost four times higher in the case studied).
- 4) In a weak grid, if converter1 PLL bandwidth exceeds that of converter2 PLL, stability improves for parallel VSCs; however, it decreases for parallel CSCs.
- 5) The proposed compensator improves the stability, reduces the dc-link interactions, and injects rated power at SCR=1.2.

APPENDIX A SYSTEM PARAMETERS

A. PVG PARAMETERS (STANDARD CONDITIONS)

$S = 1.0 \text{ kW/m}^2$, $T = 298 \text{ K}$, $I_{ph} = 9.24 \text{ A}$, $I_{sc} = 9.03 \text{ A}$, $V_{oc} = 46 \text{ V}$, $R_s = 0.3 \text{ } \Omega$, $R_{sh} = 236.4 \text{ } \Omega$, $N_s = 40$, $N_p = 80$.

B. VSC PARAMETERS

VSC 1 and 2: 1.0 MVA, $f_{sw}=51*60 \text{ Hz}$, $C_{dc}=5000 \text{ } \mu\text{F}$, $L_f=100 \text{ } \mu\text{H}$, $R_f=2 \text{ m}\Omega$, $K_p^i=0.2 \text{ } \Omega$, $K_i^i=6 \text{ } \Omega\text{s}^{-1}$, $K_p^{vdc}=0.65 \text{ } \Omega^{-1}$, $K_i^{vdc}=7.2 \text{ } \Omega^{-1}\text{s}^{-1}$, $K_p^{vac}=71.5 \text{ VArV}^{-1}$, $K_i^{vac}=2 \text{ VArV}^{-1}\text{s}^{-1}$, $K_p^{pll}=0.18 \text{ V}^{-1}\text{s}^{-1}$, $K_i^{pll}=3.2 \text{ V}^{-1}\text{s}^{-2}$.

C. CSC PARAMETERS

CSC 1 and 2: 1.0 MVA, $f_{sw}=33*60 \text{ Hz}$, $C_s=300 \text{ } \mu\text{F}$, $K_{pi}=0.08$, $K_{ii}=10 \text{ s}^{-1}$, $K_{pidc}=0.2 \text{ } \Omega$, $K_{iidc}=25 \text{ } \Omega\text{s}^{-1}$, $K_{ppli}=0.18 \text{ V}^{-1}\text{s}^{-1}$, $K_{ipli}=3.2 \text{ V}^{-1}\text{s}^{-2}$, $K_{pvac}=70 \text{ VArV}^{-1}$, $K_{ivac}=2 \text{ VArV}^{-1}\text{s}^{-1}$, Transformer, $T_r=0.48/12.47 \text{ kV}$.

Strong Grid: 36 MVA (rated), 12.47 kV (ph-ph rms), 60 Hz, X/R=7.0.

APPENDIX B PARALLEL CONVERTERS LINEARIZED MODEL

– Parallel VSCs DC and AC-Side Dynamics

$$\frac{d}{dt} \begin{bmatrix} \Delta V_{dc1} \\ \Delta V_{dc2} \end{bmatrix} = \frac{-1.5}{C_{dc1}} \begin{bmatrix} I_{d1} & I_{q1} \\ 0 & 0 \end{bmatrix} \begin{bmatrix} \Delta d_{d1} \\ \Delta d_{q1} \end{bmatrix}$$

$$\begin{aligned} & + \begin{bmatrix} D_{d1} & D_{q1} \\ 0 & 0 \end{bmatrix} \begin{bmatrix} \Delta i_{d1} \\ \Delta i_{q1} \end{bmatrix} \\ & - \frac{1.5}{C_{dc2}} \begin{bmatrix} I_{d2} & I_{q2} \\ 0 & 0 \end{bmatrix} \begin{bmatrix} \Delta d_{d2} \\ \Delta d_{q2} \end{bmatrix} \\ & + \begin{bmatrix} D_{d2} & D_{q2} \\ 0 & 0 \end{bmatrix} \begin{bmatrix} \Delta i_{d2} \\ \Delta i_{q2} \end{bmatrix} \\ & + \begin{bmatrix} \frac{1}{C_{dc1}} & 0 \\ 0 & \frac{1}{C_{dc2}} \end{bmatrix} \begin{bmatrix} \Delta I_{pv1} \\ \Delta I_{pv2} \end{bmatrix} \\ \frac{d}{dt} \begin{bmatrix} \Delta i_{d1} \\ \Delta i_{q1} \end{bmatrix} & = \frac{V_{dc1}}{L_{f1}} \begin{bmatrix} \Delta d_{d1} \\ \Delta d_{q1} \end{bmatrix} + \frac{1}{L_{f1}} \begin{bmatrix} D_{d1} \\ D_{q1} \end{bmatrix} \Delta V_{dc1} \\ & - \frac{1}{L_{f1}} \begin{bmatrix} \Delta v_d \\ \Delta v_q \end{bmatrix} - \begin{bmatrix} \frac{R_{f1}}{L_{f1}} & -\omega_1 \\ \omega_1 & \frac{R_{f1}}{L_{f1}} \end{bmatrix} \begin{bmatrix} \Delta i_{d1} \\ \Delta i_{q1} \end{bmatrix} \\ \frac{d}{dt} \begin{bmatrix} \Delta i_{d2} \\ \Delta i_{q2} \end{bmatrix} & = \frac{V_{dc2}}{L_{f2}} \begin{bmatrix} \Delta d_{d2} \\ \Delta d_{q2} \end{bmatrix} + \frac{1}{L_{f2}} \begin{bmatrix} D_{d2} \\ D_{q2} \end{bmatrix} \Delta V_{dc2} \\ & - \frac{1}{L_{f2}} \begin{bmatrix} \Delta v_d \\ \Delta v_q \end{bmatrix} - \begin{bmatrix} \frac{R_{f2}}{L_{f2}} & -\omega_2 \\ \omega_2 & \frac{R_{f2}}{L_{f2}} \end{bmatrix} \\ & \times \begin{bmatrix} \Delta i_{d2} \\ \Delta i_{q2} \end{bmatrix} \\ \frac{d}{dt} \begin{bmatrix} \Delta v_d \\ \Delta v_q \end{bmatrix} & = \frac{1}{2C_{f1}} \begin{bmatrix} \Delta i_{d1} \\ \Delta i_{q1} \end{bmatrix} + \frac{1}{2C_{f2}} \begin{bmatrix} \Delta i_{d2} \\ \Delta i_{q2} \end{bmatrix} \\ & - \frac{1}{2} \begin{bmatrix} 0 & -\omega_1 - \omega_2 \\ \omega_1 + \omega_2 & 0 \end{bmatrix} \begin{bmatrix} \Delta v_d \\ \Delta v_q \end{bmatrix} \end{aligned}$$

– VSC AC, DC-Link Current, PCC Voltage and PLL Control

$$\begin{aligned} \begin{bmatrix} \Delta v_{id}^c \\ \Delta v_{iq}^c \end{bmatrix} & = \begin{bmatrix} -K_p^i & -\omega L_f \\ \omega L_f & -K_p^i \end{bmatrix} \begin{bmatrix} \Delta i_d^c \\ \Delta i_q^c \end{bmatrix} + \begin{bmatrix} \Delta \varphi_d^i \\ \Delta \varphi_q^i \end{bmatrix} \\ & + \begin{bmatrix} \Delta v_d^c \\ \Delta v_q^c \end{bmatrix} + \begin{bmatrix} K_p^i & 0 \\ 0 & K_p^i \end{bmatrix} \begin{bmatrix} \Delta i_d^* \\ \Delta i_q^* \end{bmatrix} \\ \begin{bmatrix} \Delta \dot{\varphi}_d^i \\ \Delta \dot{\varphi}_q^i \end{bmatrix} & = \begin{bmatrix} K_i^i & 0 \\ 0 & K_i^i \end{bmatrix} \begin{bmatrix} \Delta i_d^* \\ \Delta i_q^* \end{bmatrix} + \begin{bmatrix} -K_i^i & 0 \\ 0 & -K_i^i \end{bmatrix} \\ & \times \begin{bmatrix} \Delta i_d^c \\ \Delta i_q^c \end{bmatrix} \\ \begin{bmatrix} \Delta \dot{V}_{dc}^2 \\ \Delta \dot{\varphi}_v^2 \end{bmatrix} & = \begin{bmatrix} \frac{2I_{pv}^0}{C_{dc}V_{dc}^0} & 0 \\ -K_i^i & 0 \end{bmatrix} \begin{bmatrix} \Delta V_{dc}^2 \\ \Delta \varphi_v^2 \end{bmatrix} + \begin{bmatrix} \frac{2V_{dc}^0}{C_{dc}} & 0 \\ 0 & K_{ivdc} \end{bmatrix} \\ & \times \begin{bmatrix} \Delta I_{pv} \\ \Delta V_{dc}^2 \end{bmatrix} + \begin{bmatrix} \frac{-3i_d^0}{C_{dc}} & \frac{-3i_q^0}{C_{dc}} \\ 0 & 0 \end{bmatrix} \\ & + \begin{bmatrix} \frac{-3v_d^0}{C_{dc}} & \frac{-3v_q^0}{C_{dc}} \\ 0 & 0 \end{bmatrix} \begin{bmatrix} \Delta i_d \\ \Delta i_q \end{bmatrix} \\ & + \begin{bmatrix} \frac{-3i_d^0}{C_{dc}} & \frac{-3i_q^0}{C_{dc}} \\ 0 & 0 \end{bmatrix} \begin{bmatrix} \Delta v_d \\ \Delta v_q \end{bmatrix} \end{aligned}$$

$$\begin{aligned} \frac{d}{dt} [\Delta\varphi_v^{ac}] &= [-K_i^{vac} \quad 0] \begin{bmatrix} \Delta v_d^c \\ \Delta v_q^c \end{bmatrix} + [K_i^{vac}] [\Delta v_d^*] \\ &+ \begin{bmatrix} -K_{pi} & 0 \\ 0 & -K_{pi} \end{bmatrix} \begin{bmatrix} \Delta i_{sd}^c \\ \Delta i_{sq}^c \end{bmatrix} \begin{bmatrix} \Delta\dot{\varphi}_{id} \\ \Delta\dot{\varphi}_{iq} \end{bmatrix} \\ \begin{bmatrix} \Delta\dot{\varepsilon} \\ \Delta\dot{\varphi}_\varepsilon^{pll} \end{bmatrix} &= \begin{bmatrix} 0 & 1 \\ 0 & 0 \end{bmatrix} \begin{bmatrix} \Delta\varepsilon \\ \Delta\varphi_\varepsilon^{pll} \end{bmatrix} + \begin{bmatrix} 0 & \frac{K_p^{pll}}{v_d^0} \\ 0 & \frac{K_i^{pll}}{v_d^0} \end{bmatrix} \begin{bmatrix} \Delta v_d^c \\ \Delta v_q^c \end{bmatrix} \\ &= \begin{bmatrix} -K_{ii} & 0 \\ 0 & -K_{ii} \end{bmatrix} \begin{bmatrix} \Delta i_{sd}^c \\ \Delta i_{sq}^c \end{bmatrix} + \begin{bmatrix} K_{ii} & 0 \\ 0 & K_{ii} \end{bmatrix} \\ &\times \begin{bmatrix} \Delta i_{sd}^* \\ \Delta i_{sq}^* \end{bmatrix} \end{aligned}$$

– VSC Compensator Design

$$\begin{aligned} \begin{bmatrix} \Delta\dot{\delta}_1 \\ \Delta\dot{\delta}_2 \end{bmatrix} &= \begin{bmatrix} 0 & 1 \\ -\omega_v^2 & -2\varepsilon_v\omega_v \end{bmatrix} \begin{bmatrix} \Delta\delta_1 \\ \Delta\delta_2 \end{bmatrix} + \begin{bmatrix} 0 \\ 2\varepsilon_v\omega_v K_v \end{bmatrix} \\ \begin{bmatrix} \Delta\dot{\delta}_3 \\ \Delta\dot{\delta}_4 \end{bmatrix} &= \begin{bmatrix} -\omega_q & 0 \\ 0 & -\omega_d \end{bmatrix} \begin{bmatrix} \Delta\delta_3 \\ \Delta\delta_4 \end{bmatrix} + \begin{bmatrix} 0 & K_q\omega_q \\ K_d\omega_d & 0 \end{bmatrix} \\ &\times \begin{bmatrix} \Delta v_d \\ \Delta v_q \end{bmatrix} \end{aligned}$$

– Parallel CSCs DC and AC-Side Dynamics

$$\begin{aligned} \frac{d}{dt} \begin{bmatrix} \Delta V_{pv1} \\ \Delta V_{pv2} \end{bmatrix} &= \begin{bmatrix} \frac{-1}{C_{pv1}} & 0 \\ 0 & \frac{-1}{C_{pv2}} \end{bmatrix} \begin{bmatrix} \Delta I_{dc1} \\ \Delta I_{dc2} \end{bmatrix} \\ &+ \begin{bmatrix} \frac{1}{C_{pv1}} & 0 \\ 0 & \frac{1}{C_{pv2}} \end{bmatrix} \begin{bmatrix} \Delta I_{pv1} \\ \Delta I_{pv2} \end{bmatrix} \\ \frac{d}{dt} \begin{bmatrix} \Delta I_{dc1} \\ \Delta I_{dc2} \end{bmatrix} &= \begin{bmatrix} \frac{1}{L_{dc1}} & 0 \\ 0 & \frac{1}{L_{dc2}} \end{bmatrix} \begin{bmatrix} \Delta V_{pv1} \\ \Delta V_{pv2} \end{bmatrix} \\ &+ \begin{bmatrix} \frac{-3M_{d1}}{2L_{dc1}} & \frac{-3M_{q1}}{2L_{dc1}} \\ \frac{-3M_{d2}}{2L_{dc2}} & \frac{-3M_{q2}}{2L_{dc2}} \end{bmatrix} \begin{bmatrix} \Delta v_{sd} \\ \Delta v_{sq} \end{bmatrix} \\ &+ \begin{bmatrix} \frac{-3V_{sd}}{2L_{dc1}} & \frac{-3V_{sq}}{2L_{dc1}} \\ 0 & 0 \end{bmatrix} \begin{bmatrix} \Delta m_{d1} \\ \Delta m_{q1} \end{bmatrix} \\ &+ \begin{bmatrix} 0 & 0 \\ \frac{-3V_{sd}}{2L_{dc2}} & \frac{-3V_{sq}}{2L_{dc2}} \end{bmatrix} \begin{bmatrix} \Delta m_{d2} \\ \Delta m_{q2} \end{bmatrix} \\ \frac{d}{dt} \begin{bmatrix} \Delta v_{sd} \\ \Delta v_{sq} \end{bmatrix} &= \begin{bmatrix} \frac{M_{d1}}{2C_{s1}} & \frac{M_{d2}}{2C_{s2}} \\ \frac{M_{q1}}{2C_{s1}} & \frac{M_{q2}}{2C_{s2}} \end{bmatrix} \begin{bmatrix} \Delta I_{dc1} \\ \Delta I_{dc2} \end{bmatrix} \\ &+ \frac{1}{2} \begin{bmatrix} 0 & \omega_1 + \omega_2 \\ -\omega_1 - \omega_2 & 0 \end{bmatrix} \begin{bmatrix} \Delta v_{sd} \\ \Delta v_{sq} \end{bmatrix} \\ &+ \begin{bmatrix} \frac{I_{dc1}}{2C_{s1}} & 0 \\ 0 & \frac{I_{dc1}}{2C_{s1}} \end{bmatrix} \begin{bmatrix} \Delta d_{d1} \\ \Delta d_{q1} \end{bmatrix} \\ &+ \begin{bmatrix} \frac{I_{dc2}}{2C_{s2}} & 0 \\ 0 & \frac{I_{dc2}}{2C_{s2}} \end{bmatrix} \begin{bmatrix} \Delta d_{d2} \\ \Delta d_{q2} \end{bmatrix} \end{aligned}$$

– CSC AC-DC Current, PCC Voltage and PLL Control

$$\begin{bmatrix} \Delta i_{wd}^c \\ \Delta i_{wq}^c \end{bmatrix} = \begin{bmatrix} \Delta\varphi_{id} \\ \Delta\varphi_{iq} \end{bmatrix} + \begin{bmatrix} K_{pi} & 0 \\ 0 & K_{pi} \end{bmatrix} \begin{bmatrix} \Delta i_{sd}^* \\ \Delta i_{sq}^* \end{bmatrix}$$

$$\begin{aligned} \frac{d}{dt} [\Delta\varphi_v^{ac}] &= [-K_{ivac} \quad 0] \begin{bmatrix} \Delta v_{sd}^c \\ \Delta v_{sq}^c \end{bmatrix} + [K_{ivac}] [\Delta v_{sd}^*] \\ \begin{bmatrix} \Delta\dot{\delta} \\ \Delta\dot{\varphi}_\delta \end{bmatrix} &= \begin{bmatrix} 0 & 1 \\ 0 & 0 \end{bmatrix} \begin{bmatrix} \Delta\delta \\ \Delta\varphi_\delta \end{bmatrix} + \begin{bmatrix} 0 & \frac{K_{p\delta}}{v_{sd}^0} \\ 0 & \frac{K_{i\delta}}{v_{sd}^0} \end{bmatrix} \begin{bmatrix} \Delta v_{sd}^c \\ \Delta v_{sq}^c \end{bmatrix} \end{aligned}$$

– CSC Compensator Design

$$\begin{aligned} \begin{bmatrix} \Delta\dot{\delta}_{c1} \\ \Delta\dot{\delta}_{c2} \end{bmatrix} &= \begin{bmatrix} 0 & 1 \\ -\omega_c^2 & -2\varepsilon_c\omega_c \end{bmatrix} \begin{bmatrix} \Delta\delta_{c1} \\ \Delta\delta_{c2} \end{bmatrix} + \begin{bmatrix} 0 \\ 2\varepsilon_c\omega_c K_c \end{bmatrix} \\ \begin{bmatrix} \Delta\dot{\delta}_{c3} \\ \Delta\dot{\delta}_{c4} \end{bmatrix} &= \begin{bmatrix} -\omega_{qq} & 0 \\ 0 & -\omega_{dd} \end{bmatrix} \begin{bmatrix} \Delta\delta_{c3} \\ \Delta\delta_{c4} \end{bmatrix} \\ &+ \begin{bmatrix} 0 & K_{qq}\omega_{qq} \\ K_{dd}\omega_{dd} & 0 \end{bmatrix} \begin{bmatrix} \Delta v_{sd} \\ \Delta v_{sq} \end{bmatrix} \end{aligned}$$

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