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Grid-Side Current Improvement With Direct Digital Control and Capacitor Voltage Feedforward to Mitigate Distorted Grid Currents for 3Φ3W LCL Grid-Connected Inverter Under Distorted Grid Voltages

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ABSTRACT A three-phase three-wire LCL grid-connected inverter is usually used as an interface between renewable-energy sources and grid. However, grid voltage is always distorted and results in grid-current distortion when there is no control at the filter-capacitor current. This article presents the grid-current improvement with inverter-side-current direct digital control and capacitor voltage feedforward (CVF) for the grid-connected inverter under distorted grid voltages. With the inverter-side current feedback, the simple direct digital control can cover inductance variation and determine the control laws to track inverter-side inductor current, achieving robustness. A hysteresis repetitive predictor with finite impulse response low-pass filter and compensator term is introduced to the CVF loop which can stabilize the system and compensate the distorted grid current. The virtual impedance method is adopted to confirm the stability when the filter inductances drop and control parameters vary with the inductor current. Simulated and experimental results from 12 kW inverter are used to verify the theoretical analyses and discussions.

INDEX TERMS Inverter-side current control, capacitor voltage feedforward, direct digital control, finite impulse response (FIR), distorted grid voltage.

I. INTRODUCTION

Renewable energy resources are usually connected to grid through inverters. To suppress high-frequency harmonics caused by the pulse width modulation controlled inverter, low-pass filters are usually required. LCL filters are more attractive than L filters because of lower volume and better suppression capability. However, LCL filters tend to induce resonance problem without proper damping [1].

The inverters with LCL filters are controlled with inverter-side inductor current feedback or grid-side inductor current feedback [2], [3], [4], [5], [6], [7], [8], [9], [10], [11], [12], [13], [14], [15], [16], [17], [18], [19], [20], [21], [22], [23], [24], [25], [26] to solve for resonance problems while reduce harmonic currents. The grid-side current feedback (GCF) associated with capacitor voltage feedforward (CVF) is repetitively controlled to achieve zero steady-state error and to reduce harmonic currents injected to grid [2], [3], [4]. In particular, virtual impedance [5], [7], lead compensator [6], and robust control scheme [8] are used to reduce the harmonic currents and to achieve fast transient response. The inverter-side current feedback (ICF) associated with CVF is typically controlled to damp the resonant effect of the LCL filters [9], [10], [11], [12], [13], [14], [15], [16], [17], [18], [19], [20], [21], [22], [23] and can serve as overcurrent

protection [11], [12], [13]. This can also suppress grid-harmonic currents resulting from distorted and unbalanced grid voltage [12], [13], [14], [15], [16], [17], [18]. The ICF is preferred to GCF in industrial applications for its current sensors serving as overcurrent protection. Moreover, it is reported that the ICF control has inherent damping characteristic, while the GCF control needs additional damping to ensure the stability of the system under weak grid condition. Thus, this article primarily focuses on the ICF control.

For the ICF with CVF adopted, the LCL filter can be reduced to an L filter [27], [28]. The CVF can also enhance the robustness of LCL active damping against the grid impedance for the ICF control [29], [30], [31]. However, although the CVF is beneficial for the active damping of the LCL filter at the resonant frequency, it is malign to the ICF control in low-frequency range, especially under weak grids [32], [33]. It has been found that provided the voltage feedforward coefficient is too large [34], the low-frequency instability of ICF control will be induced. To resolve this problem, this article proposes to add a finite impulse response (FIR) low-pass filter (LPF) to the ICF control with CVF loop. The FIR LPF can sustain the linear phase, and pass mostly the amplitude up to the corner frequency of the LCL filter. However, with the CVF loop, the capacitor voltage lags its current which results in stability issue [3], [4]. Therefore, we have to feedforward the voltage signal certain step-ahead, and we need a hysteresis repetitive predictor [14] associated with FIR LPF.

In summary, this article presents an approach which is robust and effective, and it is not as accurate as the method in [35], but it can suppress the grid-current harmonic distortion effectively. This approach is ICF direct digital control (DDC) associated with CVF loop which includes FIR LPF, hysteresis repetitive predictor and compensator term. The control with CVF loop can track inverter-side current, take into account inductance drop, and reduce grid-side harmonic current. The application scenario includes renewable energy injection to the grid, power factor correction, active power filtering, etc. Anything connected to the grid through LCL filter and with inverter-side inductor current feedback needs this control technique.

The rest of the paper is organized as follows. Section II presents the direct digital control with CVF loop to track the inverter-side current and take into account inductance drop. The virtual impedance method for system stability analysis according to various effects is addressed in Section III, and grid-current suppression capability analysis based on compensation ratio is presented in Section IV. Simulated and experimental results from 12 kW to verify the analyses and discussions are presented in Section V.

II. ICF DIRECT DIGITAL CONTROL WITH CVF LOOP

The ICF is sensed for DDC to track the inverter-side inductor current with inductance variation, and the CVF loop is introduced to suppress the grid harmonic currents and stabilize the system. The CVF loop includes FIR LPF $Q(s)$, hysteresis repetitive predictor e^{-NsT_s} and compensator term e^{psT_s}, which

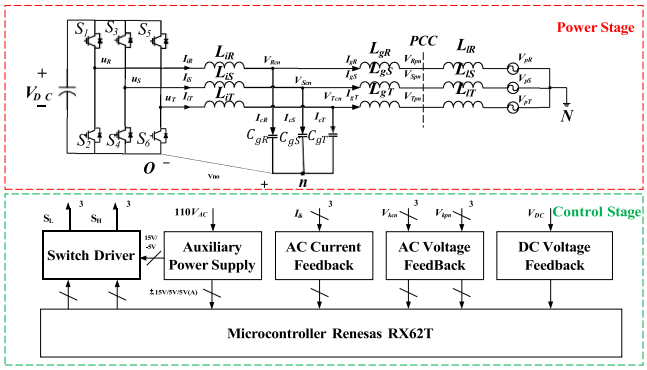


FIGURE 1. System configuration of 3Φ3W LCL inverter.

TABLE 1. System Specifications and Design Parameters

System Specifications	
DC Bus Voltage V_{DC}	380 V
Grid Voltage Frequency f_{Grid}	60 Hz
Grid Phase Voltage v_{pN}	120 V_{rms}
Rated Power P_{rated}	12 kW
Switching Frequency f_{sw}	19.2 kHz
Power Factor PF	1
DC Bus Capacitor C_{DC}	4700 μF/450 V
Power Switch	C3M0016120K
Inverter Side Inductor L_i	1500 μH ~ 450 μH
Grid Side Inductor L_g	500 μH ~ 143 μH
Filter Capacitor C_g	10 μF/350 V

play the important roles of designing a repetitive predictor. Derivation of DDC control laws and determination of $Q(s)$ and p are the kernels of this control approach.

A. DIRECT DIGITAL CONTROL

The DDC is relied on a three-phase three-wire (3Φ3W) LCL inverter, as shown in Fig. 1. The inverter consists of dc-link voltage V_{dc}, three-phase switch pairs S_1~S_6, inverter-side inductors L_{ik}, capacitors C_k, grid-side inductors L_{gk}, and line impedances L_{lk}, where k denotes R, S and T. PCC represents the point of common coupling which is located between the line impedance and grid-side inductor. Note that to have a conceptual grid system, the line impedance L_{lk} is connected in series with source voltage V_{pk}. The LCL filter design can be found from [36], in which the component values are collected in Table 1. The feedback signals include i_{ik}, v_{kcn}, and V_{DC} which are the inputs to the microcontroller *Renesas RX62T* to determine the SVPWM signals. The control laws can be derived based on the average common-mode voltage (ACMV) principle [37] as follows: Applying KVL to each phase, we have the common-mode voltage v_{nO} as

$$v_{nO} = u_{kO} - \frac{d\,(i_{ik}L_{ik})}{dt} - v_{kcn}, \tag{1}$$

where u_{kO} is a pulse output voltage of phase k with negative rail O as the reference and v_{kcn} is the capacitor voltage with neutral n as reference. Since the 3Φ KVL equations satisfy simultaneously, we can have v_{nO} with a linear combination of the 3Φ equations with non-zero real factors a_R, a_S and a_T, as shown in (2). Thus, the decoupled control laws with division-summation (D-Σ) process [38] will be derived from the 3Φ linear-combination expression of v_{nO}:

$$v_{nO} = \frac{a_R u_{RO} + a_S u_{SO} + a_T u_{TO}}{a_R + a_S + a_T} - \frac{a_R d\left(i_{iR} L_{iR}\right) + a_S d\left(i_{iS} L_{iS}\right) + a_T d\left(i_{iT} L_{iT}\right)}{\left(a_R + a_S + a_T\right) dt} - \frac{a_R v_{Rcn} + a_S v_{Scn} + a_T v_{Tcn}}{a_R + a_S + a_T}. \tag{2}$$

Based on the above linear-combination equation and assuming the inductances that keep constant over one switching period, the division process [38], with two active vectors *Vx* and *Vy* and two zero vectors *V0* and *V7*, yields the results shown in (3). Further, for the control, since v_{nO} is non-constant at different switching time intervals in one switching period, its ACMV $\overline{v_{nO}}$ needs to be determined with the summation process [38] based on the average flux over one switching period, which is shown as follows:

$$\overline{v_{nO}} = \frac{T_{V0} v_{nOV0} + T_{Vx} v_{nOVx} + T_{Vy} v_{nOVy} + T_{V7} v_{nOV7}}{T_{sw}}, \tag{3}$$

where T_{Vj} and v_{nOVj}, in which $j = 0, x, y,$ and 7, are the switching time intervals and their corresponding vectors, respectively, and T_{sw} is the switching period.

Then, based on [38], we have the ACMV as follows and the details are shown in Appendix A:

$$\overline{v_{nO}} = \frac{V_{DC}\left(a_R D_R + a_S D_S + a_T D_T\right)}{a_R + a_S + a_T} - \frac{a_R \Delta i_{iR} L_{iR} + a_S \Delta i_{iS} L_{iS} + a_T \Delta i_{iT} L_{iT}}{\left(a_R + a_S + a_T\right) T_{sw}} - \frac{a_R v_{Rcn} + a_S v_{Scn} + a_T v_{Tcn}}{a_R + a_S + a_T}, \tag{4}$$

where D_R, D_S and D_T are the control laws of the 3Φ3W inverter. The $\overline{v_{nO}}$ shown in (4) can be any arbitrary value which acts as a zero-sequence injection [37].

From the ACMV shown in (4), there is one and only one set of 3Φ decoupled forms for the control laws D_R, D_S and D_T:

$$D_R = \frac{L_{iR}\Delta i_{iR}}{V_{DC} T_{sw}} + \frac{v_{Rcn}}{V_{DC}} + \frac{\overline{v_{nO}}}{V_{DC}}, \tag{5}$$

$$D_S = \frac{L_{iS}\Delta i_{iS}}{V_{DC} T_{sw}} + \frac{v_{Scn}}{V_{DC}} + \frac{\overline{v_{nO}}}{V_{DC}}, \tag{6}$$

and

$$D_T = \frac{L_{iT}\Delta i_{iT}}{V_{DC} T_{sw}} + \frac{v_{Tcn}}{V_{DC}} + \frac{\overline{v_{nO}}}{V_{DC}}, \tag{7}$$

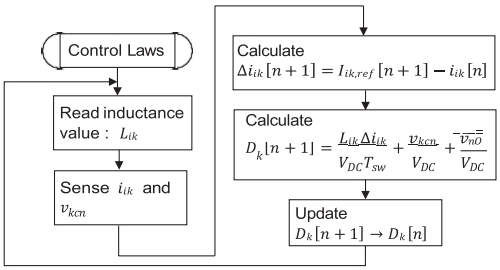


FIGURE 2. Flowchart of control-law implementation.

where $\overline{v_{nO}}/V_{DC}$ is a chosen constant, but should avoid over modulation, and Δi_{ik} denotes the inverter-side inductor current difference as

$$\Delta i_{ik}[n+1] = I_{i,ref}[n+1] - i_{ik}[n], \tag{8}$$

where $I_{i,ref}$ [n+1] is the reference value and the i_{ik}[n] is the feedback value. Note that we use $I_{i,ref}$ [n+1] instead of i_{ik}[n+1] because the one-step feedforward is used.

A flowchart to illustrate the control-law implementation is shown in Fig. 2.

From (5)–(7), we can see that if the three $\overline{v_{nO}}/V_{DC}$ terms are kept identical for the 3Φ within one switching period, the control law of each phase is only related to the parameters of its own phase. Therefore, the control laws are now totally three-phase decoupled and straightforward enough for controlling the inverter. Moreover, since they include filter inductances L_{ik}, dc-link voltage V_{DC} and capacitor voltage v_{kcn} (almost identical to the grid voltage v_{kpn} with negligible phase difference), the control laws can take into account their variations every switching period readily. Thus, we operate the system in nature frame, saving *abc-dq* frame transformations, and take into account their variations, achieving robustness.

The value of $\overline{v_{nO}}/V_{DC}$ can be any value as long as the duty ratios do not cause over modulation, which is in accordance with the concept of zero-sequence injection. For the duty ratio from 0 to 1, $\overline{v_{nO}}/V_{DC}$ is normally set as 1/2. Thus, the duty-ratio control law becomes

$$D_k[n+1] = \frac{\Delta i_{ik}[n+1] L_{ik}}{V_{DC}[n] T_{sw}} + \frac{v_{kcn}[n]}{V_{DC}[n]} + \frac{1}{2}. \tag{9}$$

To increase dc-voltage utilization, a special zero sequence can be used to replace $\overline{v_{nO}}/V_{DC}$ term. For SVPWM-type zero-sequence injection, 1/2 is replaced with 1/2+D_{SVPWM} and

$$D_{k,SVPWM}[n+1] = D_k[n+1] + D_{SVPWM}[n+1], \tag{10}$$

where $D_{k,SVPWM}$ is the control law with the SVPWM-type zero-sequence injection, and D_{SVPWM} has the following expression:

$$D_{SVPWM}[n+1] = -\frac{1}{2}\left\{\max\left(D_R^*, D_S^*, D_T^*\right) + \min\left(D_R^*, D_S^*, D_T^*\right)\right\} \tag{11}$$

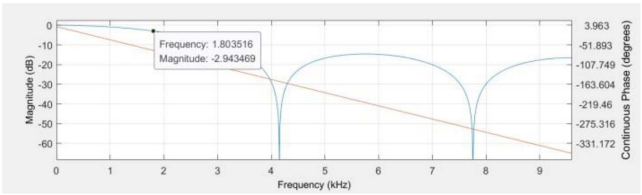


FIGURE 3. Plot of the FIR LPF Q(s).

and

$$D_k^* = \frac{\Delta i_{ik}\,[n+1]\,L_{ik}}{V_{DC}\,[n]\,T_{sw}} + \frac{v_{kcn}\,[n]}{V_{DC}\,[n]}, \tag{12}$$

where D_k^* is the duty ratio of current cycle. With the control law, the inverter-side inductor current, I_{ik}, can be tracked accurately.

B. CVF LOOP

ICF DDC control associated with CVF loop can suppress grid harmonic currents. However, without careful design of the CVF loop, it would induce stability problem [39]. Therefore, an FIR LPF, Q(s) which can sustain the linear phase, and pass mostly the amplitude up to the corner frequency of the LCL filter, is introduced into the CVF loop. The CVF loop includes hysteresis repetitive predictor and compensator term to stabilize the system. The parameters are designed as follows:

1) *Hysteresis repetitive predictor and compensator term:* For sample-period T_s as a step and in a line cycle, there are N (=320) steps totally. Owing to the periodic grid voltage, the sampled grid voltage of the former cycle can be taken as the predicted values of the current cycle, making it possible to predict the CVF term for any p ($0 \le p \le N$) steps ahead where p is a positive integer. In terms of s-domain, e^{-NsT_s} is the hysteresis repetitive predictor and e^{psT_s} is the compensator term. In a digital control system, it is easy to store the sampled grid voltage of the former cycle, making it easy to implement this hysteresis repetitive predictor.
2) *FIR LPF Q(s):* With the hysteresis repetitive predictor and compensator term only, the poles of the open-loop transfer function exist on unit circle which may lead to instability [40]. Practically, considering both control preciseness and stability, Q(s) is selected to be less than but close to unity to make the repetitive controller behave like an integrator. Additionally, to have a linear phase response, we are using FIR filter. Therefore, we select Q(s) as the FIR LPF [41] with 4th-order, corner frequency = 1.8 kHz (30th harmonic) which is high enough for filtering the harmonics, and using window method. This is designed with Matlab FilterDesign toolbox and plotted as Fig. 3 where the blue color represents the magnitude and the orange is the linear phase. Up to 1.8 kHz, the magnitude drop is only −3 dB. Note that considering computational burden, we only select Q(s) with 4th order. Higher order Q(s) would result in better filtering performances (less phase lagging and wider stability margin), but it requires heavy computational burden. Without Q(s), the system will result in instability because the on unit-circle poles. With FIR LPF Q(s), the on unit-circle poles will bring inside the unit-circle which is a stable system.

In summary, the process of deriving the parameters α_0, α_1 and α_2 are that with Matlab FilterDesign Toolbox, we first select the filter type (i.e., FIR), select the filter design method (: window method), select filter order (: 4th), set the corner frequency (: 1.8 kHz), and then we can obtain the filter parameters α_0, α_1 and α_2 through Matlab iteration which can be found from [42]. The Q(s) has been designed as follows:

$$Q\,(s) = \alpha_0 e^{2sT_s} + \alpha_1 e^{sT_s} + \alpha_2 + \alpha_1 e^{-sT_s} + \alpha_0 e^{-2sT_s} \tag{13}$$

where

$\alpha_0 = 0.174$, $\alpha_1 = 0.213$ and $\alpha_2 = 0.227$.

The overall system control block diagram for each phase is shown in Fig. 4, in which the "Power Stage" is constructed from the real components of the power stage, the "Direct Digital Control" is the proposed control with the estimated inverter-side inductor $\widetilde{L}_i$, and the "Capacitor Voltage Feedforward" is shown in the lower part of the figure. The CVF is derived with $\frac{C_g}{pT_s}(v_{ck}Q(s)e^{-(N-p)sT_s} - v_{ck})$ which forms $i_{c,com}$. Therefore, the Δi_{ik}[n+1] becomes the form as

$$\Delta i_{ik}\,[n+1] = I_{gk,ref}\,[n+1] - i_{ik}\,[n] + i_{c,com}\left[n+p-N\right], \tag{14}$$

where the $I_{g,ref}$[n+1] is the grid-side current reference and the grid current can be improved with the proposed control.

With the $i_{c,com}$, the DDC can reduce the grid-current distortion under distorted grid voltage and inductance variation readily, effectively and robustly. Thus, the harmonic current suppression can be achieved with the proposed control and CVF. To prove that the controlled system is stable, the virtual impedance method is adopted.

III. GRID CURRENT SUPPRESSION ANALYSIS

Grid current suppression analysis is to evaluate the suppression capability of distorted grid-voltage which results in distorted grid-current. The suppression capability is shown with i_g/v_{Grid}. Fig. 5 shows the bode plot of i_g/v_{Grid} with the proposed FIR LPF in the CVF loop in z-domain, in which the Tustin bilinear transform is adopted. From 1st to 7th order harmonics, the compensator has less than −40 dB attenuation, from 8th to 14th the compensator has less than −30 dB attenuation, and the attenuation rate becomes smaller and smaller when harmonic order is higher than 27th. Thus, the harmonic attenuation is high enough for the lower-order harmonics, while it becomes insignificant when the harmonic is large at high frequencies (>1.8 kHz).

When $p \ge 3$, the system is stable. But, how does it improve the grid-current THD? The plots with $p = 3 \sim 10$ versus compensation ratios are shown in Fig. 6, in which the ratios are

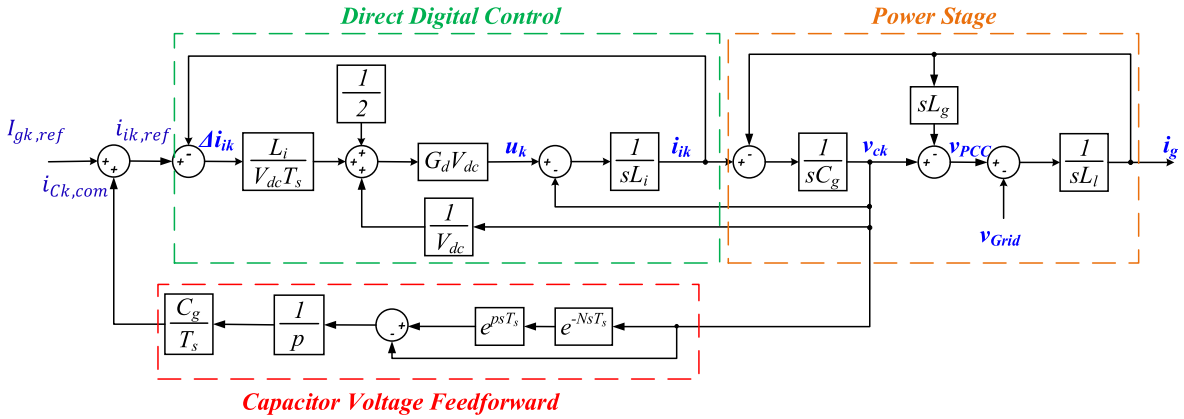


FIGURE 4. Control block diagram of each phase of 3Φ3W LCL inverter with DDC and CVF.

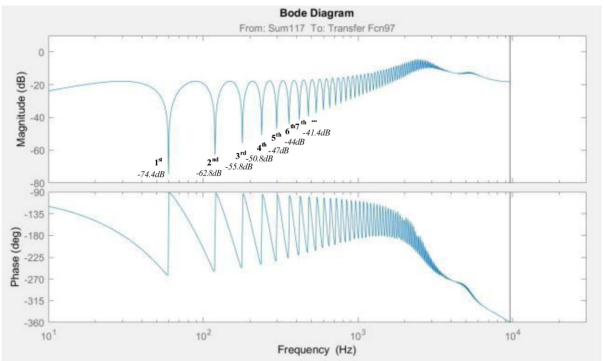


FIGURE 5. Bode plot of i_g/v_{Grid} in z-domain.

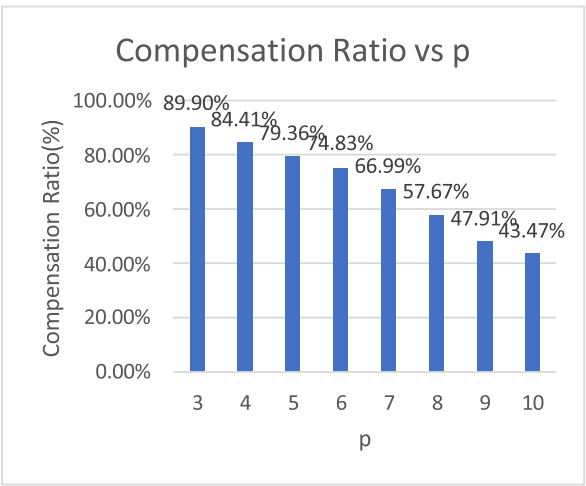


FIGURE 6. Plots of p versus compensation ratio.

defined with the following formula:

$$comp.\,ratio\% = \frac{\alpha - \beta}{\alpha}\%, \tag{15}$$

where α denotes the "before compensation" I_g THD and β represents the "after compensation" I_g THD. From the compensation-ratio plots, it can be observed that $p = 3$ results in the highest compensation ratio and $p = 10$ results in the lowest compensation ratio because $p = 3$ has the largest damping effect. Thus, we select $p = 3$ as our study. Note that the analysis is based on the parameters listed in Table 1, but the block diagram shown in Fig. 4 is represented in symbolic form and it does not lose its generality.

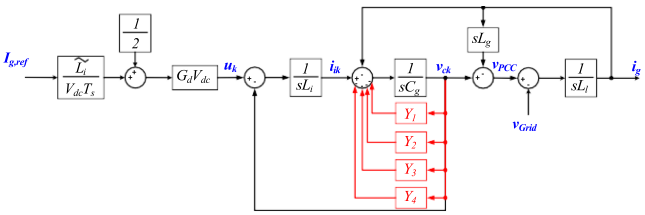


FIGURE 7. Virtual impedance model.

IV. VIRTUAL IMPEDANCE METHOD FOR SYSTEM STABILITY ANALYSIS

The underlying principle here is that the virtual resistance due to controller at the effective resonance-frequency should be positive for stability [43]. Instead of impedance-based stability analysis [44] which is more complicate in derivation, we adopt the virtual impedance and find out the virtual-impedance model first and then, investigate the effects of compensator term p and inductance drop. In addition, the inverter associated with grid strength, which is denoted as short-circuit ratio (SCR), is also discussed.

A. VIRTUAL IMPEDANCE MODEL

Now, we use the virtual impedance method to derive the virtual impedance model from Fig. 4, as shown in Fig. 7, in which

$$Y_1 = \frac{G_d}{s^2\left(L_g + L_l\right)T_s} \tag{16}$$

$$Y_2 = \frac{G_d C_g}{T_s} \tag{17}$$

$$Y_3 = -\frac{G_d}{sL_i} \tag{18}$$

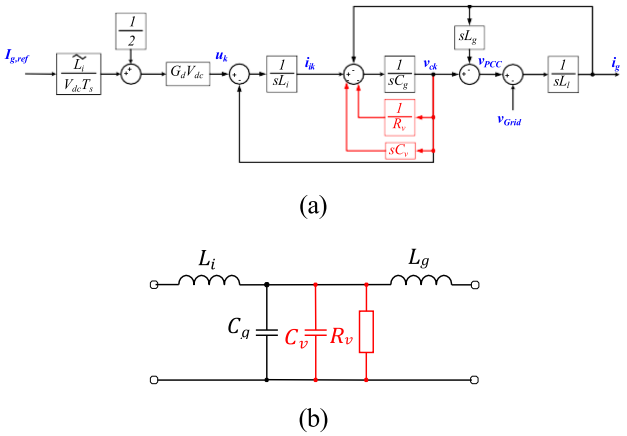


FIGURE 8. (a) Equivalent virtual impedance model and (b) an equivalent circuit of the LCL filter including virtual impedance model.

$$Y_4 = -\frac{G_d G_{comp}}{sT_s} \tag{19}$$

and

$$G_{comp} = \left(\frac{C_g}{pT_s}\right) Q(s)\, e^{-(320-p)sT_s}, \tag{20}$$

and its equivalent R_v and C_v are in parallel with the original C_g, as shown in Fig. 8. For example, Y_1 is derived as follows: we first find the $i_g/v_{ck} = 1/s(L_l+L_g)$ and find out the equivalent i_g as $(\widetilde{L_i}/V_{dc}T_s)(G_d V_{dc})(1/sL_i) = G_d/sT_s$ assuming the estimated $\widetilde{L_i} = L_i$. Then, we have $Y_1 = \frac{G_d}{s^2(L_g+L_l)T_s}$. The rest of admittances, Y_2, Y_3, and Y_4, can be derived by following the same procedure, as shown in Appendix B. As we can see, the introduced $1/R_v$ and sC_v are the equivalent virtual impedances of the control system which are defined as follows. The detailed derivation is shown in Appendix B.

$$\begin{aligned} Y_v &= Y_1 + Y_2 + Y_3 + Y_4 \\ &= \frac{1}{R_v} + sC_v. \end{aligned} \tag{21}$$

The conductance $(1/R_v)$ at the effective resonance-frequency is positive for stability [43], which means it has positive damper.

B. EFFECTS OF COMPENSATOR TERM P AND INDUCTANCE DROP

Except the DDC controller and dc gains, the CVF loop includes the most important compensator term p and FIR LPF Q(s). Without Q(s), the system appears in instability. While, with Q(s), the system appears in stability when p is properly selected. The virtual impedance plots are shown in Fig. 9, in which p is varying from 1 to 5, and they have positive dampers when $p \geq 3$. This positive damper will damp out the possible oscillation caused by the resonant frequency. In other words, the effective p must be large enough to damp out the system and it is found that $p \geq 3$ to have a stable system, and the larger the p is, the greater the stability margin will be. However,

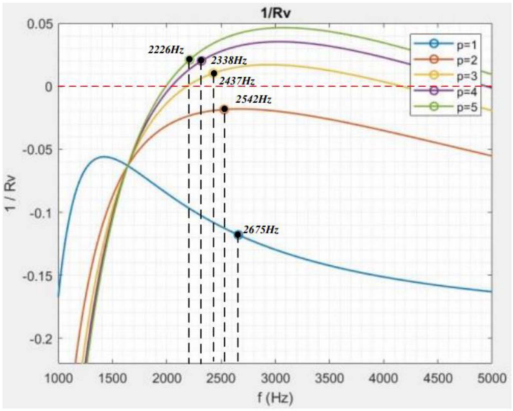


FIGURE 9. Virtual-conductance plots with p as a fitting parameter.

TABLE 2. Filtering Performance with Deviation Between L_i and $\widetilde{L_i}$

Deviation: L_i and $\widetilde{L_i}$	-20%	-10%	0%	10%	20%
THD(I_g)	0.67%	0.65%	0.63%	0.69%	0.72%

the distorted grid-current filter capability (compensation ratio) will drop with p increase, as shown in Fig. 6. In the further discussion, the trade-off between stability margin and filter capability is considered.

As shown in Fig. 9, when p = 3, it has the smallest resistance $1/R_v$. So, it has the largest compensation ratio because the $1/R_v$ may result in the largest damping effect. Thus, we use the compensation ratio to indicate the capability of i_g THD suppression. As indicated in Fig. 9 (p = 3, 4, 5) and the comp. ratio indicated in Fig. 6 (p = 3∼10), we know that p = 3 has the smallest resistance $(1/R_v)$ and therefore, the largest capability of i_g THD suppression. Thus, we use the compensation ratio to indicate the i_g THD suppression capability and we choose p = 3 for the best. Note that the frequencies marked on the plots are the resonant frequencies and they are affected by C_v.

Other stability analysis can be found from the pole-zero plot of $I_g/I_{g,ref}$ which is shown in Fig. 10 with Tustin bilinear transform. The system is with CVF, with Q and p = 3, resulting in stability. All of the poles are located inside the unit-circle, as shown in Fig. 10(a) and the I_g simulated results show a stable system, as illustrated in Fig. 10(b).

The controller of DDC is $\frac{\widetilde{L_i}}{V_{dc}T_s}$ in which V_{dc} and T_s are treated as constant, while $\widetilde{L_i}$ is the estimated value which might deviate from the hardware component L_i. The $\widetilde{L_i}$ is estimated with the inductance formula provided by the manufacturer [45]. With ±20% deviation, the filter performance of grid harmonic current I_g with DDC is almost unaffected, as collected in Table 2, in which the distorted grid voltage v_g is 7th/8% and 11th/5%. Regularly, it is ±10% deviation in the control inductance estimation. Rather, we use ±20% deviation and the results are with very minor difference. Therefore, it can be seen that the filter performance is very effective.

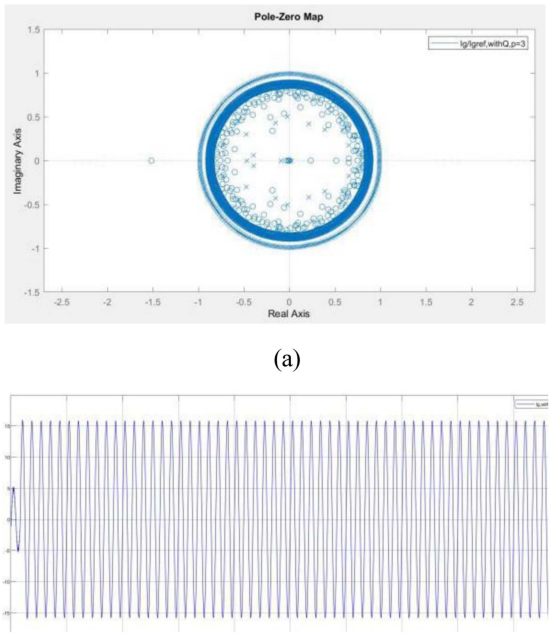


FIGURE 10. System with CVF, Q and $p = 3$: (a) stable pole-zero plot of $I_g/I_{g,ref}$, and (b) stable simulated results.

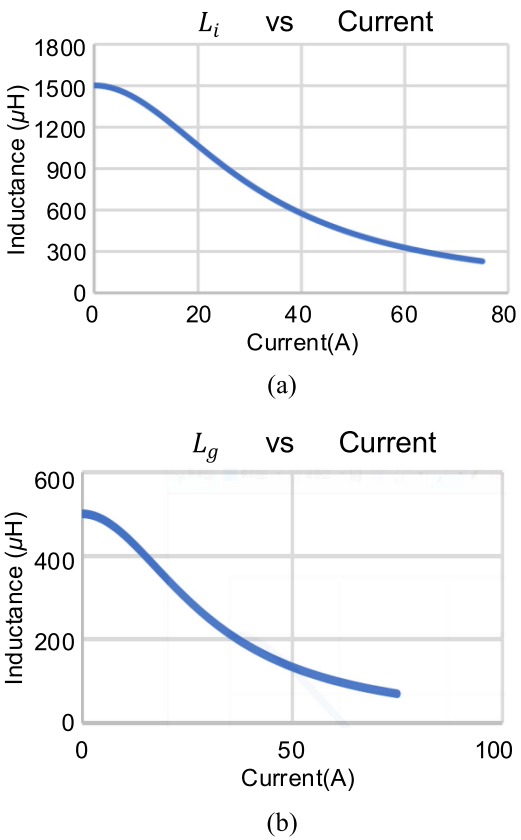


FIGURE 11. Inductance-drop with bias current increase: (a) L_i and (b) L_g.

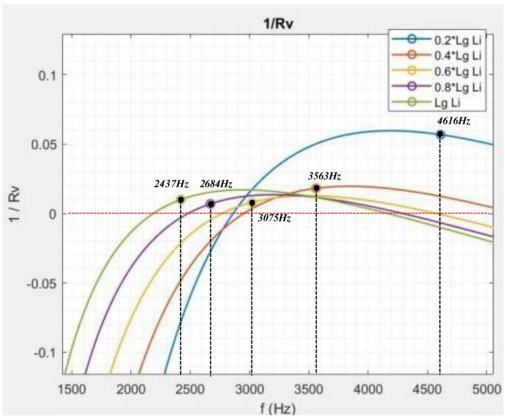


FIGURE 12. Virtual conductance plots with $L_i \cdot L_g$ as fitting parameters.

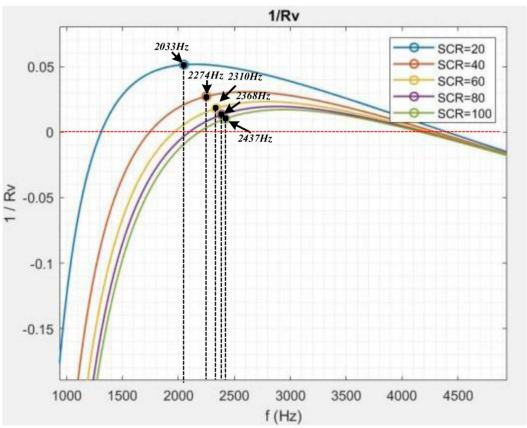


FIGURE 13. Virtual-conductance plots with SCR as a fitting parameter.

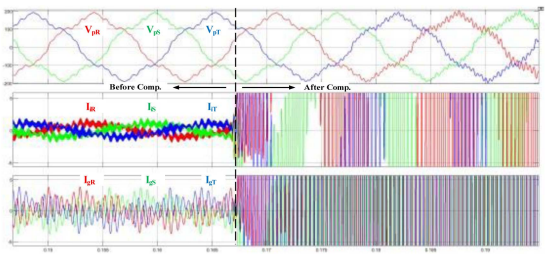


FIGURE 14. Simulated results with $p = 1$ showing unstable results "After Comp."

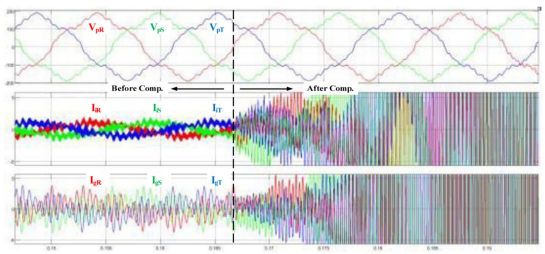


FIGURE 15. Simulated results with $p = 2$ showing unstable results with a little bit latency "After Comp."

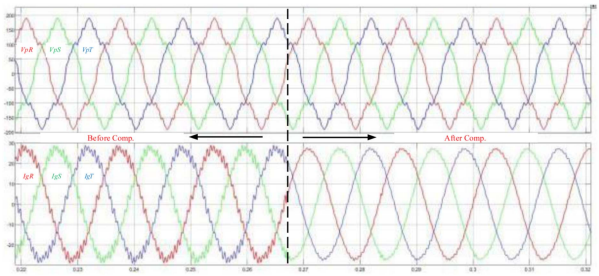


FIGURE 16. Simulated results with V_{kpn}: THD = 10.87%, "Before Comp.:" I_g THD = 7.12% and "After Comp.:" I_g THD = 1.44%.

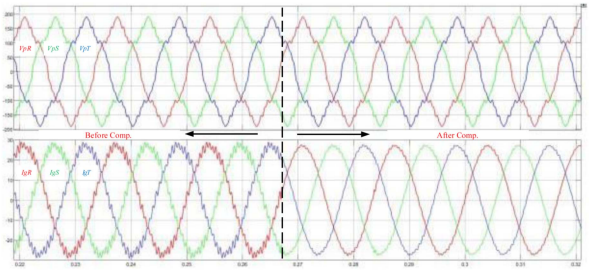


FIGURE 17. Simulated results with SCR = 65 and V_{kpn}: THD = 10.87%, Before Comp.: I_g THD = 10.82% and After Comp.: I_g THD = 1.46%.

Since the filter inductances, L_i and L_g, drop with their bias current increase, as shown in Fig. 11, we would like to see if they affect the system stability. Fig. 12 plots the virtual conductance versus frequency with $L_i \cdot L_g$ as fitting parameters when $P = 3$. From Fig. 12 and with the proposed control, it can be seen that even though the inductances drop to 20%, the worst case, all of the resonant frequencies are associated with positive conductance, proving stability. Thus, the proposed control with CVF loop is robust and effective.

C. GRID STRENGTH–SCR

SCR is the index to indicate grid strength, and it affects the system stability [12], [13], [14]. According to IEEE-519 Standard, when SCR is less than 20, it is considered weak grid, while when SCR is greater than 20, it is a strong grid. When the equivalent line impedances (i.e., SCR) are varying, the system is stable or not depending on the positive damper. Fig. 13 shows the plots of virtual conductance versus frequency with SCR as a fitting parameter when $p = 3$. All of them are showing positive dampers at resonant frequencies, proving stability. It has the trend that the lower the SCR is, the higher the positive conductance will be. Again, with the control, the system appears in robustness and effectiveness.

V. SIMULATION AND EXPERIMENT RESULTS

A. SIMULATION RESULTS

The simulated system is configured with a 3Φ3W LCL inverter as the power stage, a microcontroller to determine the SVPWM signals based on DDC control laws, feedback signals, and peripheral circuits. Fig. 14 shows the simulated results when $p = 1$, in which "Before Comp.", the system is stable but the grid current is distorted and "After Comp.", the system is diverged immediately, implying unstable. Similarly, the simulated results shown in Fig. 15 are corresponding to $p = 2$, but "After Comp.", the system is unstable with a little bit latency. This can be also observed from Fig. 9, in which $p = 2$ has higher virtual resistance than that of $p = 1$ even though both have negative virtual resistance and show unstable results. When $p = 3$, Fig. 16 shows the stable simulated results with DDC control and without/with CVF loop, in which "Before Comp.", the system shows the one without CVF loop and "After Comp.", it shows that with

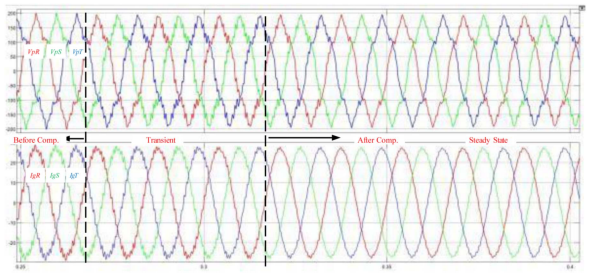
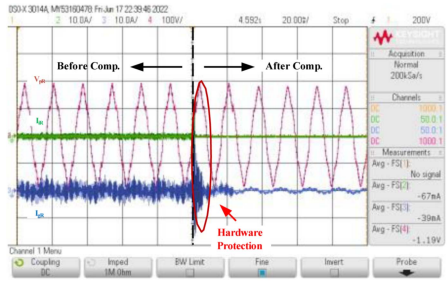


FIGURE 18. Simulated results with SCR = 10 and V_{kpn}: THD = 10.87%, "Before Comp.:" I_g THD = 6.45%:, and "After Comp.:" I_g THD = 1.62%.

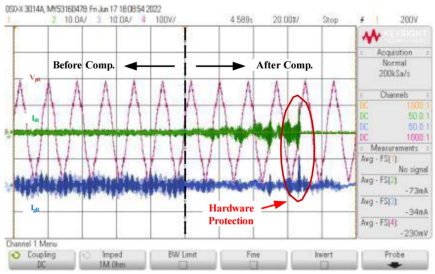
CVF loop. It can be seen that the grid current without CVF loop has THD = 7.12%, while the one with CVF loop yields the THD = 1.44%, resulting in significant and effective improvement. Note that the high frequency (>1.8 kHz) harmonic current attenuation is lower, resulting in significant harmonic components which will be shown in later measurement. Fortunately, it does not contribute much to the grid-current THD.

Similar to a proportional-integral (PI) controller, the PI gain has to be designed properly to have enough stability margin. For the system stability, the step-ahead number p needs to be chosen properly, depending on FIR LPF Q(s) design. In addition, once the LCL filter has been designed with the rules presented in [38], the step-ahead number p can be chosen to stabilize the system.

Line impedance L_l will affect the grid current suppression, which is usually expressed in terms of SCR. When SCR = 65 (L_l = 165 μH), denoting a strong grid, the simulated results of grid current is shown in Fig. 17, in which the THD "Before Comp." is 10.82% and the THD "After Comp." is 1.46%. Typically, the SCR in IEEE-519 Standard test is 20, denoting a weak grid. However, we conduct a more severe test, SCR = 10. When SCR = 10 ($L_l \approx$ 1 mH), the simulated results of grid current are shown in Fig. 18 in which the THD "Before Comp." is 6.45% and the THD "After Comp." is 1.62%. No matter what the SCR is, the I_g THD "After Comp." can meet the IEEE-519 Standard, being less than 5%. It verifies that the proposed control with CVF loop can effectively attenuate the grid current.

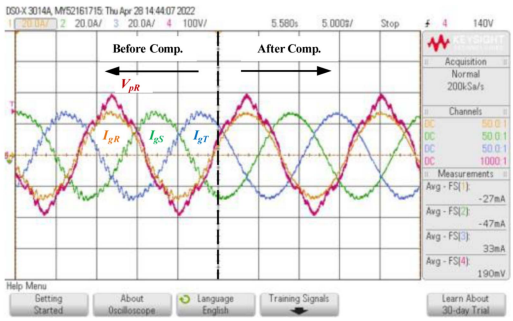


(a) $p = 1$

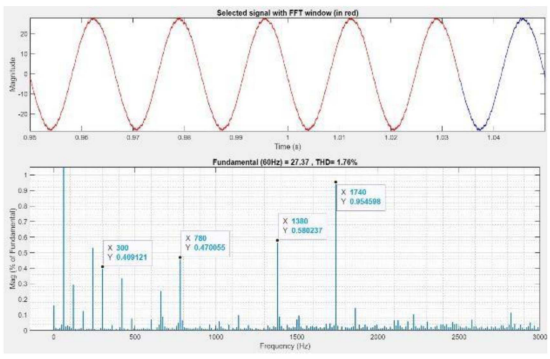


(b) $p = 2$

FIGURE 19. Hardware measurements: (a) $p = 1$, with shut down right away, and (b) $p = 2$, showing unstable results.

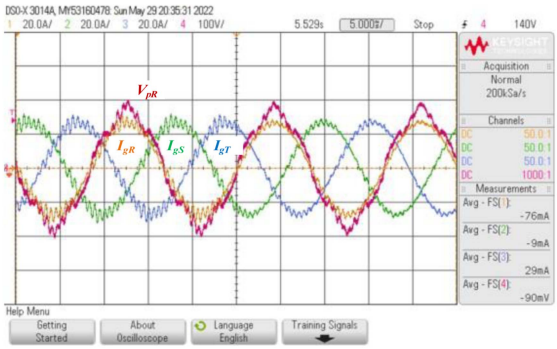


(a)

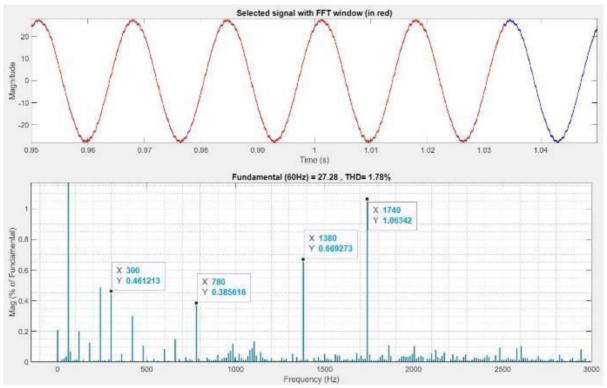


(b)

FIGURE 20. Hardware measurement: when $p = 3$ and (a)"Before Comp.," I_g THD: 6.83% and "After Comp.," I_g THD:1.76%, and (b) its spectrum.



(a)



(b)

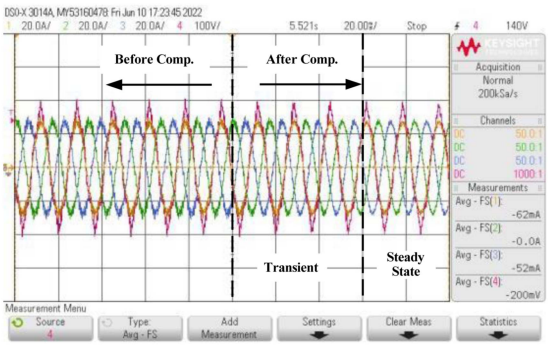
FIGURE 21. Hardware measurement: when $p = 3$ and (a) "Before Comp.," I_g THD: 11.22% and "After Comp.," I_g THD:1.78%, and (b) its spectrum.

B. HARDWARE MEASUREMENTS

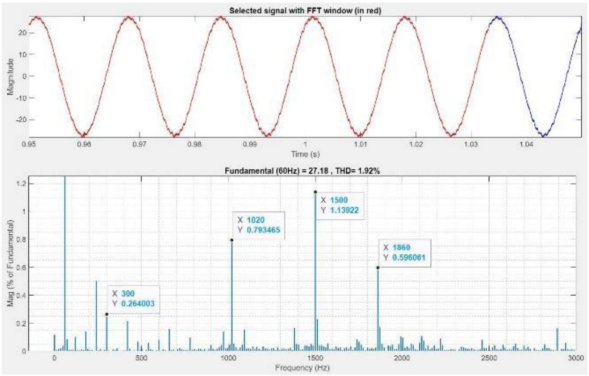
Hardware measurements were conducted under a set up for the system with the power stage, proposed control and CVF loop. They can be found from Fig. 19 in which Fig. 19(a) shows unstable results (Hardware Protection) immediately "After Comp." when $p = 1$, and Fig. 19(b) shows unstable results (Hardware Protection) "After Comp." with a little bit latency when $p = 2$. This confirms the simulated results and the virtual impedance plot shown in Fig. 9. When $p = 3$, Fig. 20(a) shows that "Before Comp." the grid-current I_g THD is 6.83% and "After Comp." the I_g THD is 1.76%, and Fig. 20(b) shows its spectrum. Note that the high frequency harmonics are still observable.

With SCR = 65 and SCR = 10, the measured results are shown in Figs. 21 and 22, respectively, when $p = 3$. Fig. 21(a) shows that the grid-current I_g THD "Before Comp." is 11.22% and the I_g THD "After Comp." is 1.78%, and Fig. 21(b) shows its spectrum. Fig. 22(a) shows that the grid-current I_g THD "Before Comp." is 7.70% and the I_g THD "After Comp." is 1.91%, and Fig. 22(b) shows its spectrum.

Both results meet the IEEE-519 Standard. Note that Fig. 21 shows that the results do not reach the steady state "After Comp." yet, while Fig. 22 shows that the results take a longer



(a)



(b)

FIGURE 22. Hardware measurement: when p = 3 and (a) "Before Comp.," I_g THD: 7.70% and "After Comp.", I_g THD:1.91%, and (b) its spectrum.

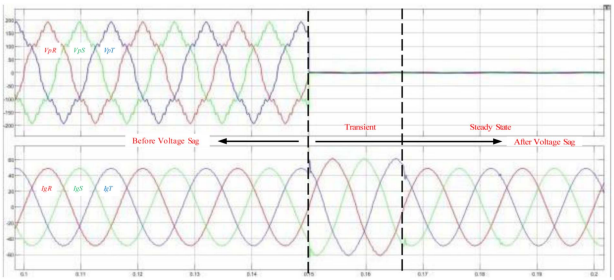


FIGURE 23. Simulated results under $I_g = 49$ A and grid voltage sagging to 0 V.

time to reach the steady state "After Comp." and they are shown in longer time division. With the repetitive control, the system has one-line-cycle lagging to reach the new state.

C. DISCUSSION

Since the hysteresis repetitive predictor is used to predict the grid voltage feedforward term by p steps ahead, it may lead to over currents of the system when the grid voltage sags [14]. Fig. 23 shows the simulated results under full load of 12 kW/49 A with grid voltage sagging down to 0 V, in which the maximum grid-current hysteresis error is 24.5%. Note that we use DDC, so that even though the voltage sags to 0 V,

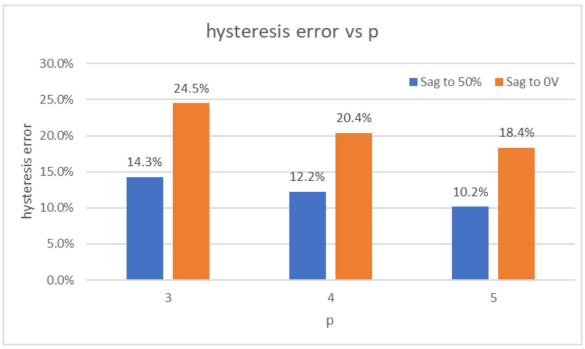


FIGURE 24. Hysteresis errors with different p's and sagging.

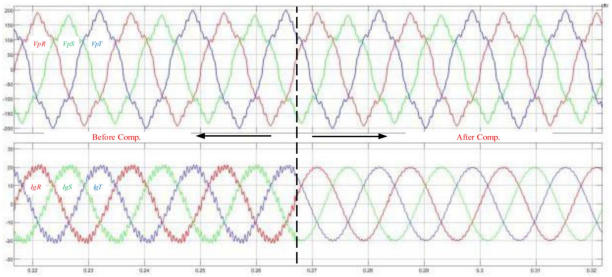


FIGURE 25. Simulated results with unbalanced voltages, showing low I_g THD (1.22%) grid current.

we still can control the current sinusoidally. The hysteresis error of the simulated results corresponding to different p's and sagging are collected in Fig. 24. The hysteresis error, because of repetitive control, is not greater than 1/4 of the rated current within one-line cycle which is considered to be acceptable for thermal issue, according to a famous power supply company [46]. A higher p will result in a lower hysteresis error, but a lower compensation ratio. Therefore, a trade-off between the hysteresis error and compensation ratio needs to make.

The DDC is insensitive to voltage imbalance which can be proved by the simulation results shown in Fig. 25, in which the voltage imbalance is $\pm 10\%$ and "After Comp.", the grid current I_g THD is 1.22%. The control is effective and robust.

When $p = 10$, the proposed control still yields stable results which are demonstrated by the simulated results shown in Fig. 26. It can be seen from Fig. 26 that "Before Comp.", the I_g THD is 8.82% and "After Comp.", the I_g THD is 3.76% which is worse than that shown in Fig. 17 because $p = 10$ results in worse compensation ratio.

As compared with [24], the proposed control scheme with CVF loop can achieve better performance as shown in Fig. 27. The performance in [24] is I_g THD = 2.12% when the 19th harmonic injected grid voltage is THD = 6.12%. The proposed can achieve I_{gR} THD = 1.96% when the 19th harmonic injected grid voltage is THD = 6.15%. The prototype of the hardware implementation with the proposed control is shown in Fig. 28.

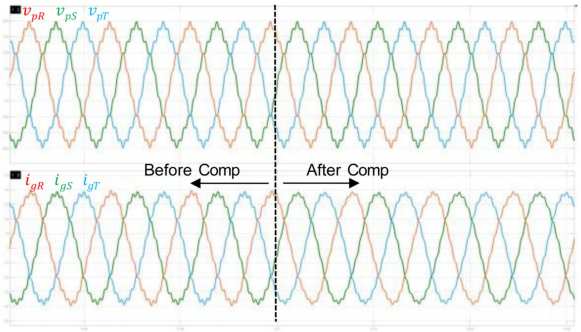


FIGURE 26. Simulated results with $p = 10$ and V_{kpn}: THD = 8.87%, "Before Comp.:" I_g THD = 8.82% and "After Comp.:" I_g THD = 3.76%.

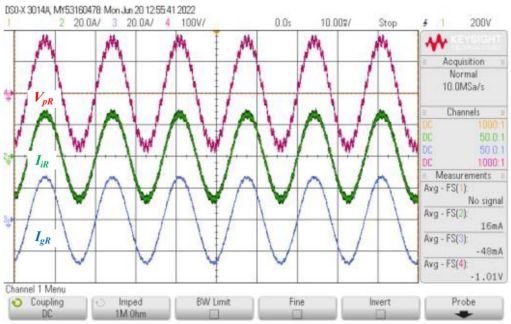


FIGURE 27. Experimental results with 19th harmonic injected grid voltage (V_{pR}) THD = 6.15% which yields injected grid current (I_{gR}) THD = 1.96%.

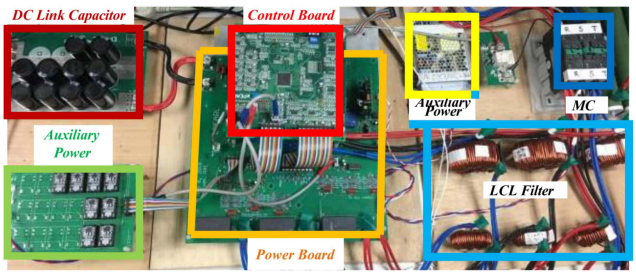


FIGURE 28. Prototype of the hardware implementation.

VI. CONCLUSION

This article has presented the 3Φ3W LCL inverter with the direct digital control and CVF loop which includes hysteresis repetitive predictor and FIR LPF to improve the injected grid current under distorted grid voltage. The algorithms of DDC and CVF loop have been presented in detail from which the control laws are derived. The virtual impedance method has been adopted to verify the stability with various inductances, L_i & L_g, and SCRs. In addition, the stability has been proved with the pole-zero plot of input-to-output transfer function $I_g/I_{g,ref}$. Moreover, the stability of step-ahead number p is proved with the virtual impedance method, which is stable when the step-ahead number ≥ 3, and the number is 3 to achieve the highest compensation ratio (89.9%), while the maximum hysteresis error is 24.5%. The step-ahead number is depending on FIR LPF $Q(s)$ for stability. The proposed direct digital control with capacitor voltage feedforward is robust and effective, which can improve grid-current distortion under distorted grid voltage. These have been confirmed with simulated and experimental results.

APPENDIX A

$$v_{nOV0} = -\frac{a_R L_{iR}\Delta i_{iRV0} + a_S L_{iS}\Delta i_{iSV0} + a_T L_{iT}\Delta i_{iTV0}}{(a_R + a_S + a_T)T_{V0}} - \frac{a_R L_{gR}\Delta i_{gRV0} + a_S L_{gS}\Delta i_{gSV0} + a_T L_{gT}\Delta i_{gTV0}}{(a_R + a_S + a_T)T_{V0}} - \frac{a_R v_{Rpn} + a_S v_{Spn} + a_T v_{Tpn}}{a_R + a_S + a_T}, \tag{A.1}$$

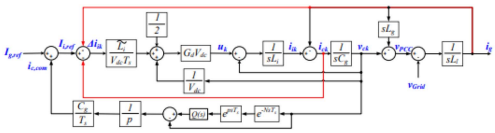
$$v_{nOVx} = \frac{u_{Vx}}{a_R + a_S + a_T} - \frac{a_R L_{iR}\Delta i_{iRVx} + a_S L_{iS}\Delta i_{iSVx} + a_T L_{iT}\Delta i_{iTVx}}{(a_R + a_S + a_T)T_{Vx}} - \frac{a_R L_{gR}\Delta i_{gRVx} + a_S L_{gS}\Delta i_{gSVx} + a_T L_{gT}\Delta i_{gTVx}}{(a_R + a_S + a_T)T_{Vx}} - \frac{a_R v_{Rpn} + a_S v_{Spn} + a_T v_{Tpn}}{a_R + a_S + a_T}, \tag{A.2}$$

$$v_{nOVy} = \frac{u_{Vy}}{a_R + a_S + a_T} - \frac{a_R L_{iR}\Delta i_{iRVy} + a_S L_{iS}\Delta i_{iSVy} + a_T L_{iT}\Delta i_{iTVy}}{(a_R + a_S + a_T)T_{Vy}} - \frac{a_R L_{gR}\Delta i_{gRVy} + a_S L_{gS}\Delta i_{gSVy} + a_T L_{gT}\Delta i_{gTVy}}{(a_R + a_S + a_T)T_{Vy}} - \frac{a_R v_{Rpn} + a_S v_{Spn} + a_T v_{Tpn}}{a_R + a_S + a_T}, \tag{A.3}$$

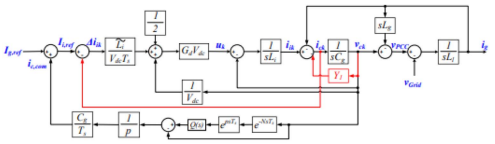
$$v_{nOV7} = V_{DC} - \frac{a_R L_{iR}\Delta i_{iRV7} + a_S L_{iS}\Delta i_{iSV7} + a_T L_{iT}\Delta i_{iTV7}}{(a_R + a_S + a_T)\,T_{V7}} - \frac{a_R L_{gR}\Delta i_{gRV7} + a_S L_{gS}\Delta i_{gSV7} + a_T L_{gT}\Delta i_{gTV7}}{(a_R + a_S + a_T)\,T_{V7}} - \frac{a_R v_{Rpn} + a_S v_{Spn} + a_T v_{Tpn}}{a_R + a_S + a_T}. \tag{A.4}$$

APPENDIX B

Derivations of Y_1, Y_2, Y_3 and Y_4 are shown as follows. First, find the equivalent i_g feedback as G_d/sT_s assuming the estimated $\widetilde{Li} = L_i$ and find $i_g/v_{ck} = 1/s(L_l+L_g)$. Then, we can find $Y_1 = G_d/s^2T_s(L_l+L_g)$, as shown in Fig. 29(b). Secondly, find the i_{ck}/v_{ck} as sC_g and find the equivalent i_{ik} as G_d/sT_s from Fig. 29(b) to determine Y_2, as shown in Fig. 29(c). Thirdly, change the v_{ck} from Fig. 29(c), the $1/V_{dc}$ path, to



(a)

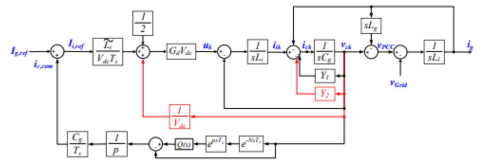


$$i_g = (v_{ck} - sL_g i_g)\cdot\frac{1}{sL_l};\ \frac{i_g}{v_{ck}} = \frac{1}{s(L_g+L_l)};$$

$$T_1' = \frac{L_i}{V_{dc}T_s}(G_d V_{dc})\frac{1}{sL_i} = \frac{G_d}{sT_s}$$

$$Y_1 = T_1'\left(\frac{i_g}{v_{ck}}\right) = \frac{G_d}{s^2(L_g+L_l)}$$

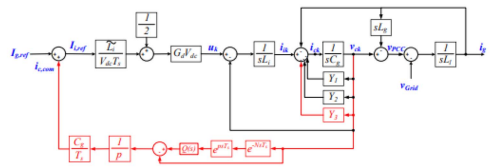
(b)



$$\frac{i_{ck}}{v_{ck}} = sC_g;\ T_2' = \frac{L_i}{V_{dc}T_s}(G_d V_{dc})\frac{1}{sL_i} = \frac{G_d}{sT_s}$$

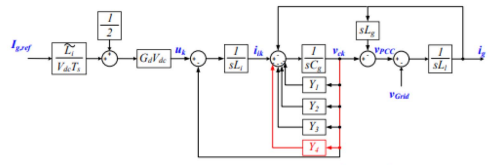
$$Y_2 = (sC_g)T_2' = \frac{C_g G_d}{T_s}$$

(c)



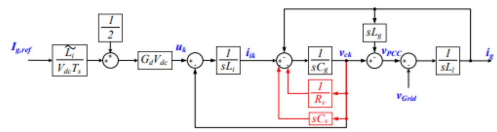
$$T_3' = \frac{-1}{V_{dc}}(G_d V_{dc})\frac{1}{sL_i};\ Y_3 = T_3' = \frac{-G_d}{sL_i}$$

(d)



$$T_4' = G_{comp}\frac{L_i}{V_{dc}T_s}(G_d V_{dc})\frac{1}{sL_i};\ Y_4 = T_{34}' = \frac{G_{comp}G_d}{sT_s}$$

(e)



$$Y_v = Y_1 + Y_2 + Y_3 + Y_4 = \frac{1}{R_v} + sC_v.$$

(f)

FIGURE 29. Derivation of Y_1, Y_2, Y_3, and Y_4, and yielding R_v and C_v.

form Y_3. Fourthly, change the CVF loop from Fig. 29(d) to form Y_4, as shown in Fig. 29(e). Finally, sum up Y_1, Y_2, Y_3, and Y_4 to find an equivalent $1/R_v$ and sC_v, as shown in Fig. 29(f).

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