IEEE Open Journal of
Power Electronics

Received 28 October 2023; accepted 12 November 2023. Date of publication 15 November 2023;
date of current version 29 November 2023. The review of this paper was arranged by Associate Editor Qiang Wei.

Digital Object Identifier 10.1109/OJPEL.2023.3333255

A Pareto Based Comparison of DC/DC Converters for Variable DC-Link Voltage in Electric Vehicles

TIMIJAN VELIĆ [1,3], YANNIK BECHER [1,2], AND NEJILA PARSPOUR [3]

[1]Dr. Ing. h.c. F. Porsche AG, 71287 Weissach, Germany
[2]Karlsruhe Institute of Technology, Institute of Electrical Engineering, 76137 Karlsruhe, Germany
[3]University of Stuttgart, Institute of Electrical Energy Conversion, 70550 Stuttgart, Germany

CORRESPONDING AUTHORS: TIMIJAN VELIĆ; YANNIK BECHER (e-mail: timijan.velic1@porsche.de; yannik.becher@porsche.de)

ABSTRACT High battery voltages increase inverter switching and harmonic losses of the electric machine. These losses dominate at low speeds in the partial load range, where the customer relevant Worldwide Harmonized Light Vehicles Test Procedure (WLTC) driving cycle is located. By installing a bidirectional DC/DC converter between the inverter and the battery, the input voltage of the inverter can be adjusted to various torque/speed conditions, thereby enhancing the efficiency and range of the electric sports car. Outside of the WLTC, the DC/DC converter is not operated and is short-circuited by a bypass. Additionally, the utilization of synchronous modulation methods, as opposed to space vector pulse width modulation (SVPWM), within the WLTC is made possible by the variable DC-Link voltage, further reducing switching and harmonic losses. In this paper, different topologies of DC/DC converters are proposed. The investigations are conducted on an 800 V system. To facilitate this, a script-based toolchain was developed based on analytic and fast calculating waveform models. The impact of the DC-Link voltage on energy efficiency during the WLTC is examined, and sensitivities are presented. A multi-objective optimization is carried out based on the WLTC driving cycle to demonstrate the maximum trade-offs between increasing the electric range and the power density of the DC/DC converter.

INDEX TERMS Automotive, buck, ĆUK, dc/dc converter, DC-Link voltage, electric drive, electric sports car, electric vehicles, mission profile, multi-objective optimization, power converters, silicon-carbide.

I. INTRODUCTION

Currently, the typical state-of-the-art electric drives consist of a three-phase (3-ϕ) synchronous machine with interior permanent magnets (iPMSM) and a 2-level voltage source inverter with a DC-Link capacitor (2LVSI), which forms the reference system for the work presented in this article. The high battery voltage in modern electric vehicles (EV), up to 800 V, offers advantages, especially in the high-load range and at high speeds. These advantages include smaller cable cross-sections, reduced DC charging currents, and the shift of the more loss-intensive field-weakening region. Currently, 800 V is the highest DC charging voltage available on the market, but in the future, there will be a trend towards higher voltages for shorter charging times [1], [2].

A higher voltage also poses challenges in the design of electrical components and systems. Higher voltages imply higher stress on the passive components and the winding insulations of the iPMSM [3], [4], [5], [6], [7], or a higher cosmic ray failure rate of the semiconductors [8], [9], which can lead to a reduced lifetime of the components. Moreover, the high battery voltage, and thus the DC-Link voltage, leads to disadvantages during the operation of the electric drive. A higher DC-Link voltage causes higher switching losses in the 2LVSI [10] and higher harmonic losses in the electric machine (EM) [11], [12], [13], [14], [15], [16], [17]. Therefore, the design and energy efficiency become increasingly critical with the trend of increasing voltages. The energy efficiency of a 3-ϕ iPMSM 800 V silicon carbide (SiC) electric drive was

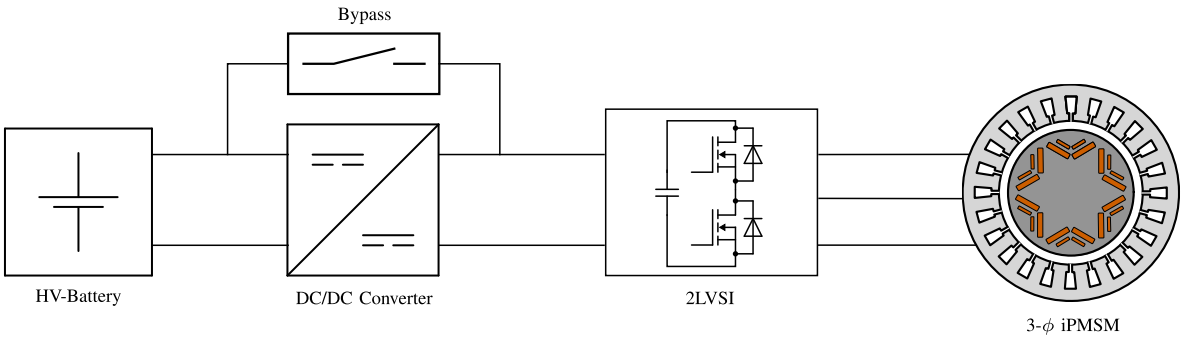

FIGURE 1. Block diagram of an electric drive with an 800 V HV-battery, an integrated DC/DC converter with a bypass circuit, a 2LVSI, and a 3-ϕ iPMSM.

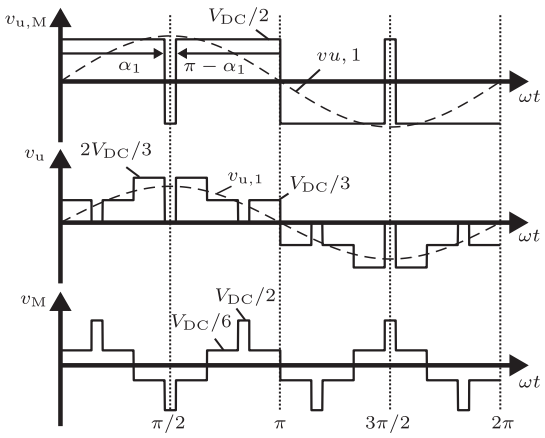

FIGURE 2. Center pulse triple clocking (CP3) with switched half-bridge voltage $v_{u,M}$, phase voltage v_u, and common-mode voltage v_M of the electrical machine in a 3-ϕ star connection, including the switching angle α, with quarter- and half-wave symmetry for controlling the fundamental amplitude.

measured in [18], which demonstrated that the DC-Link voltage has a significant impact on the energy efficiency. In [19], [20], [21], the influence of the DC-Link voltage on the losses of the inverter and the electric machine was investigated. A DC/DC converter to adjust the DC-Link voltage can be implemented between the battery and the inverter. In [21], [22], [23], [24], [25], [26], the efficiency improvement, including the losses of the installed DC/DC converter, was analyzed and demonstrated with experiments.

A variable DC-Link voltage also opens new possibilities regarding modulation and control to increase the overall system energy efficiency, which was analyzed with a 3-ϕ iPMSM 800 V Si e-drive in [27] using synchronous modulation methods [28], also known as optimal pulse pattern (OPP) or selective harmonic elimination (SHE). To adjust the DC-Link voltage, a 100-unit cascaded multilevel converter was developed. Additionally, in [29], block commutation was investigated in combination with a variable DC-Link voltage.

The DC-Link voltage, as an additional parameter of freedom, enables the use of synchronous modulation methods in the WLTC range instead of the space vector pulse-width modulation (SVPWM).

Fig. 2 shows the time characteristic of switched voltage waveforms of one phase for block commutation with an additional center pulse of opposite polarity (CP3). The pulse width of the triple clocking can be used to adjust the fundamental amplitude. On the one hand, this increases the modulation index [29], [30]. On the other hand, the iron harmonic losses can be further reduced [31].

Previous literature deals exclusively with the influence of the DC-Link voltage on the efficiency of the inverter and electric machine. No statements are made about the maximum achievable range increase based on energy efficiency. Previous studies were limited to a battery voltage in the range of 235 V to 400 V and for electric drives with very low output power that are unsuitable for an electric sports car. No statements are made about the design of the integrated DC/DC converter, such as the chip area, the total volume, or the weight. Due to the extremely high currents and power in electric sports cars, approaches to design a DC/DC converter for maximum power are not sensible, as this would require an extremely high installation space or additional weight. The use of boost and buck-boost converters is not necessary due to the gear ratio, the high power, and the non-existent field weakening operation in the customer WLTC cycle. A tradeoff between efficiency and power density always arises in the design of an optimal power electronic system. Furthermore, the calculation of losses for different electrical operating points for the WLTC cycle is necessary to make a statement about energy efficiency. This must be considered in the virtual design routine and included as a quality criterion in an optimization. For this, a script-based fast calculating tool chain is necessary. Also, no studies are made about the influence of the hardware design on the DC/DC converter when other modulation methods as SVPWM for inverter control are used. In addition, the DC/DC converter must be considered as an integrated system in the electric vehicle in order to make statements about the overall system performance, such as electric range. Fig. 1 shows a block diagram with the electric drive topology that is further investigated in this work.

To address the gaps in research and contribute from industrial research for high-performance electric sports cars, the following new questions are answered from a holistic perspective:

- Investigation of the influence and sensitivity of the DC-Link voltage on the efficiency in an 800 V system.
- Studies of the effect on energy efficiency based on the WLTC driving profile of a constant and operating point-dependent optimal DC-Link voltage.
- Virtual hardware design of the DC/DC converter with a bypass for WLTC operation only [32].
- Investigation of the maximum trade-off between power density and efficiency with multi-objective optimization.
- Comparison between optimizations for efficiency and energy efficiency with the WLTC driving cycle and the effect on the design and power density of the converter.
- Comparison between optimizations with SVPWM and CP3 inverter control and the effect on the design of the DC/DC converter.

II. VARIABLE DC-LINK VOLTAGE

In general, both low and high settings of the DC-Link voltage can offer advantages in terms of efficiency. In the high-load range, a boost converter can compensate for the voltage drop across the battery that is related to high current. Boosting the voltage is beneficial when no optimal current combination can be found using the Maximum-Torque-Per-Ampere (MTPA) method due to the inverter's voltage limit [23]. In the base speed range, forward losses, copper, and iron fundamental losses are voltage-independent, except for losses in the capacitor. However, since switching losses, current ripple, and harmonic losses increase with higher voltage, the following strategy can be derived: At each operating point, provide the minimum DC-Link voltage without the machine reaching the inverter's voltage limit and entering field-weakening mode. Otherwise, additional d-current would need to be applied, resulting in higher losses in all components. In the WLTC, therefore, reducing the voltage is the logical approach.

First, the influence of the voltage adjustment on the losses of the reference electric drive is investigated. Fig. 3 displays a normalized machine characteristic diagram over speed and torque with the loss-optimal DC-Link voltage V_{DC} for the reference system (3-ϕ iPMSM 800 V SiC electric drive). The load spectrum of the WLTC cycle is depicted in white, where the density of the points is an indicator of the dwell time of the operating point. In the base speed range, due to the voltage limit, the loss-optimal voltage has an approximate linear relation to the speed of the machine. Operating the electric drive with this voltage map reduces the losses in the WLTC by up to 30–40%.

It can also be observed from the figure that no torque/speed point in the WLTC driving cycle operates in field-weakening mode. Therefore, a DC/DC converter with the capability to increase the voltage is not beneficial. In electric sports cars, the ratio of maximum power to power in the WLTC is very high. This is evident from the maximum torque/speed curve of the iPMSM and the design point of the DC/DC converter. Due to this fact, the DC/DC converter is exclusively designed for WLTC operation, which enhances its power density. Additionally, from the perspective of extending the electric range, it only makes sense to use the converter in this range. The electrical parameters of the design point for the DC/DC converter, highlighted as a red diamond, are presented in Table 1.

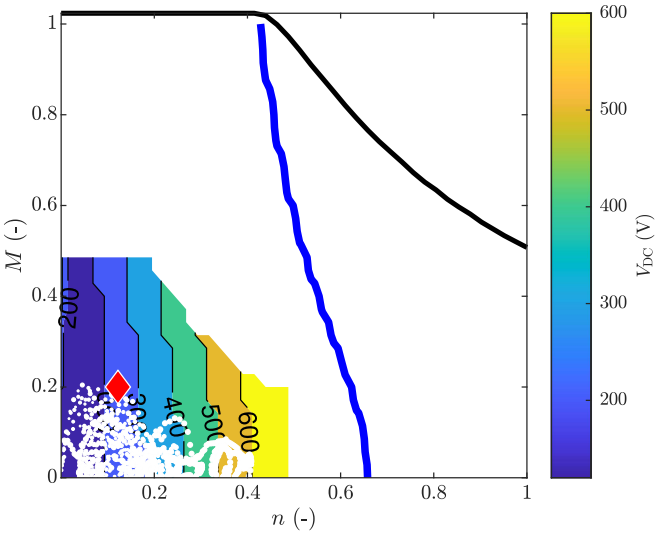

FIGURE 3. Operating point-dependent loss-optimal DC-Link voltage for the electric drive and torque/speed points of the WLTC driving cycle (white). The driving cycle displays the torque/speed tuples based on the velocity curve calculated with a vehicle model. The dwell time of the cycle is mostly located in partial load operation, where harmonic iPMSM and 2LVSI switching losses have the highest contribution to the overall e-drive losses. The blue line represents the boundary of the field-weakening mode. The hardware design point for the DC/DC converter between the battery and the inverter is highlighted (red diamond).

TABLE 1. Electrical Parameters of the Design Point of the DC/DC Converter

Parameter	Value
Normed speed n	24 %
Normed torque M	100 %
Battery voltage V_{Bat}	800 V
DC-Link voltage V_{DC}	220 V
Inverter modulation method	SVPWM
Inverter switching frequency f_{sw}	8 kHz
Mean inverter current i_{PM}	229 A
Electrical frequency f_{el}	125 Hz
Power factor $\cos(\varphi)$	0.97
Modulation index m	0.88

Fig. 4 illustrates the sensitivity of losses to voltage, considering a constant operating point. It can be observed that for the best efficiency of both the inverter and the electric motor, the lowest voltage must be set. It is also evident that the optimal voltage changes once the losses of the DC/DC converter are taken into account. Furthermore, the harmonic $P_{\mathrm{v,EM,OS}}$ and switching losses $P_{\mathrm{v,Module,Sw}}$ of the electric motor and the inverter are depicted.

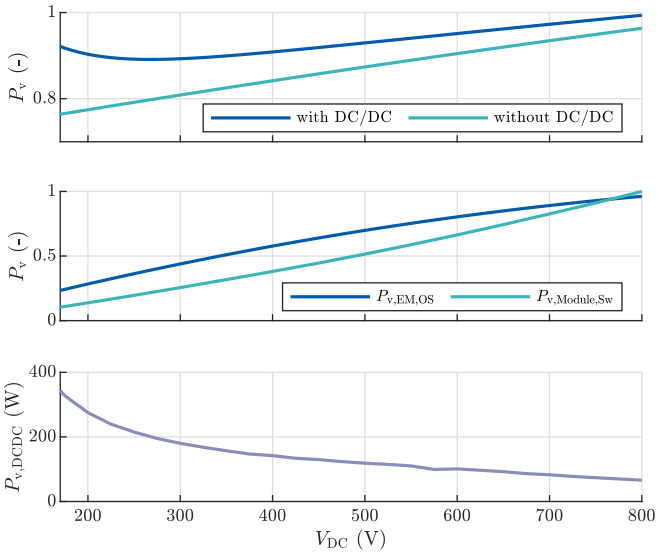

FIGURE 4. Losses dependent on the DC-Link voltage ranging from 170 V to 800 V. The upper plot depicts the losses of the electric drive with and without the DC/DC converter. The middle plot illustrates the harmonics and switching losses of the EM and the 2LVSI, while the lower plot represents the losses of the DC/DC converter. The upper and middle graphs are normalized to losses at 800 V.

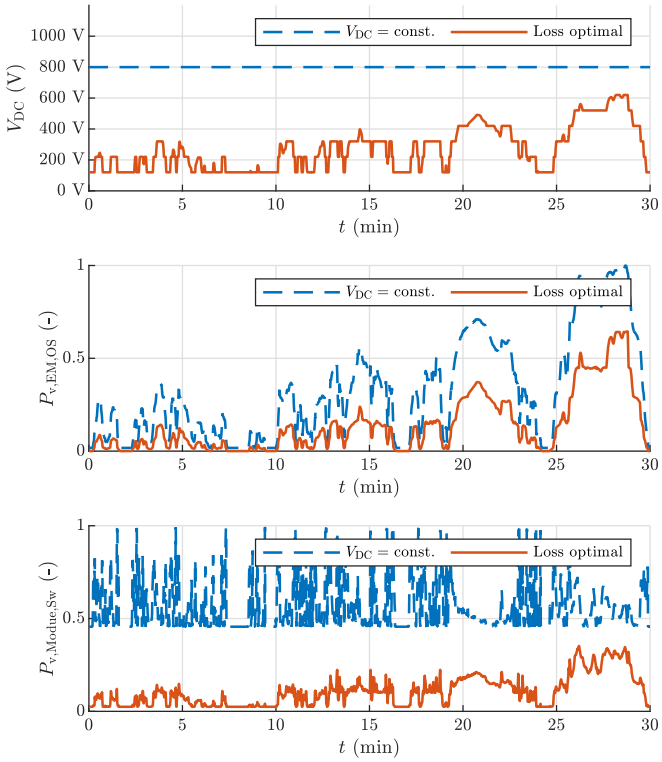

FIGURE 5. Simulation results of the WLTC driving profile. The upper representation depicts the constant DC voltage of 800 V and the loss-optimal voltage. The middle representation illustrates the harmonic losses of the electric machine. The lower graph displays the switching losses of the power module.

Based on the map in Fig. 3, a WLTC simulation was conducted using the loss-optimal voltage. The reference is the simulation with a constant voltage of 800 V. The graphs depict the harmonic losses of the motor and the switching losses of the inverter. The graphs are each normalized to the maximum occurring losses in the WLTC driving profile at 800 V. Fig. 5 illustrates the significant proportion of dynamic losses due to SVWPM in the WLTC driving profile. By reducing the voltage, both harmonic losses and switching losses are significantly reduced. The substantial reduction in switching losses is attributed to the need for a large chip area in the power module design to remain thermally compliant at maximum current. In the WLTC driving profile, very high dynamic losses occur, which are proportional to the installed chip area.

The virtual design of the DC/DC converter used for the calculations in this section is presented in Table 2. The design is carried out without optimization using the models presented here to satisfy the respective electrical and thermal constraints.

TABLE 2. Virtual Design of the DC/DC Converter With 3rd Gen. SiC MOSFET

Parameter	Value
Topology	Buck
Core Material / Type	Vitroperm 550 HF L2102-V346
Core external radius r_a	51 mm
Core internal radius r_i	38 mm
Core height h	25 mm
Air gap lenght l_d	5 mm
Number of windings w	90
Cross section copper winding A_{Cu}	20 mm^2
Inductance L_{out} @10 kHz	660 µH
# of parallel half-bridges n_{phase}	4
Switching frequency f_{sw}	10 kHz
Capacitor Type	Polypropylene Film 1000 V C4AQNEW5550M3AJ
Input capacitance C_{in}	300 µF
Output capacitance C_{out}	570 µF
Chip Area	2318 mm^2

III. TOPOLOGIES

Requirements must first be defined for the DC/DC converter. To enable recuperation, the circuit must be bidirectional. Resonant converters are discarded due to the associated greater component expense of the magnetic transformer. Galvanic isolation would not bring any further advantages for safety. To ensure that the DC/DC converter does not compensate for the loss advantage of voltage matching compared to the reference with its own losses, it must have very high efficiency at all WLTC operating points. Therefore, SiC metal-oxide-semiconductor field-effect transistors (MOSFETs) are used for the power switches. Fig. 6 shows two basic circuit topologies. The buck converter, as the basic circuit of the step-down converter, has the lowest component cost but carries a non-continuous input current. This is critical for the input voltage ripple. In contrast to the buck converter, the Ćuk converter also has an input inductance. The special feature of the topology is that the energy is transferred capacitively

from the input to the output via a fly capacitor, resulting in an inverted output voltage. Additionally, both coils can be magnetically coupled on one core. Other basic circuits with similar low component complexity, such as the Zeta or SEPIC converter, each have a pulsed input or output current. For this reason, the buck and Ćuk converters are selected for the Pareto-based comparison. Both converters can be multi-phase interleaving. n_{phase} groups, each consisting of the half-bridge switches and the inductors, are connected in parallel and recombined at the input and output, as shown in Fig. 6 as an example for the buck converter. By separately driving them out of phase with each other by $2\pi/n_{\text{phase}}$, the effective current ripple can be reduced by superposition of the individual phase currents. The following relationship applies to the current ripple of the buck converter:

$$\Delta i_{\text{Lout}} = \frac{V_{\text{Bat}}}{L_{\text{out}} f_{\text{sw}}} \cdot d_{\text{i}}(1 - n_{\text{phase}} d_{\text{i}}) \tag{1}$$

$$d_{\text{i}} = d - \frac{1}{n_{\text{phase}}} \lfloor n_{\text{phase}} d \rfloor, \tag{2}$$

where L_{out} is the output inductance, V_{Bat} battery voltage, f_{sw} switching frequency and d duty cycle [33].

IV. MODELLING

In power electronics applications, many effects must be accounted for by loss, fluid dynamic, magnetic, and waveform models to enable a holistic multi-objective optimization (MOO). For design-oriented calculations, suitable models for multi-objective optimization must be developed. A combination of analytical and semi-analytical waveform models is used to ensure the fastest possible computation time with an acceptable level of accuracy [34], [35], [36], [37].

A. WAVEFORMS

For fast design-oriented calculations, all relevant state variables of the DC/DC converter are computed using time-averaged state space models [38], [39]. Equations (4) and (5) shown at the bottom of this page, show linearized time-averaged state space models derived from the equivalent circuit diagram of a single-phase buck and Ćuk converter, as shown in Fig. 6, which also illustrates all relevant state variables. The duty cycle d is defined as the ratio of turn-on time

$$\frac{\mathrm{d}}{\mathrm{d}t}\begin{pmatrix}\Delta i_{\text{Lout}}\\ \Delta v_{\text{DC}}\\ \Delta v_{\text{Cin}}\\ \Delta i_{\text{bat}}\end{pmatrix} = \begin{pmatrix}-\frac{R_{\text{Lout}}}{L_{\text{out}}} & -\frac{1}{L_{\text{out}}} & \frac{d}{L_{\text{out}}} & 0\\ \frac{1}{C_{\text{out}}} & 0 & 0 & 0\\ -\frac{d}{C_{\text{in}}} & 0 & 0 & \frac{1}{C_{\text{in}}}\\ 0 & 0 & -\frac{1}{L_{\text{k}}} & -\frac{R_{\text{i}}}{L_{\text{k}}}\end{pmatrix}\begin{pmatrix}\Delta i_{\text{Lout}}\\ \Delta v_{\text{DC}}\\ \Delta v_{\text{Cin}}\\ \Delta i_{\text{bat}}\end{pmatrix} + \begin{pmatrix}0 & 0 & \frac{v_{\text{Cin},0}}{L_{\text{out}}}\\ 0 & -\frac{1}{C_{\text{out}}} & 0\\ 0 & 0 & -\frac{i_{\text{Lout},0}}{C_{\text{in}}}\\ \frac{1}{L_{\text{k}}} & 0 & 0\end{pmatrix}\begin{pmatrix}\Delta v_{\text{bat}}\\ \Delta i_{\text{PWR}}\\ \Delta g_{\text{T1}}\end{pmatrix} \tag{4}$$

$$i_{\text{Lout}} = i_{\text{Lout},0} + \Delta i_{\text{Lout}} \qquad v_{\text{Bat}} = v_{\text{Bat},0} + \Delta v_{\text{Bat}}$$
$$v_{\text{DC}} = v_{\text{DC},0} + \Delta v_{\text{DC}} \qquad i_{\text{PM}} = i_{\text{PM},0} + \Delta i_{\text{PM}}$$
$$v_{\text{Cin}} = v_{\text{Cin},0} + \Delta v_{\text{Cin}} \qquad g_{\text{T1}} = d + \Delta g_{\text{T1}}$$
$$i_{\text{Bat}} = i_{\text{Bat},0} + \Delta i_{\text{Bat}}$$

$$\frac{\mathrm{d}}{\mathrm{d}t}\begin{pmatrix}\Delta i_{\text{Lin}}\\ \Delta i_{\text{Lout}}\\ \Delta v_{\text{Cin}}\\ \Delta v_{\text{DC}}\\ \Delta v_{\text{Cfly}}\\ \Delta i_{\text{Bat}}\end{pmatrix} = \begin{pmatrix}-\frac{R_{\text{Lin}}}{L_{\text{in}}} & 0 & \frac{1}{L_{\text{in}}} & 0 & -\frac{1-d}{L_{\text{in}}} & 0\\ 0 & -\frac{R_{\text{Lout}}}{L_{\text{out}}} & 0 & \frac{1}{L_{\text{out}}} & \frac{d}{L_{\text{out}}} & 0\\ -\frac{1}{C_{\text{in}}} & 0 & 0 & 0 & 0 & \frac{1}{C_{\text{in}}}\\ 0 & -\frac{1}{C_{\text{out}}} & 0 & 0 & 0 & 0\\ \frac{1-d}{C_{\text{fly}}} & -\frac{d}{C_{\text{fly}}} & 0 & 0 & 0 & 0\\ 0 & 0 & -\frac{1}{L_{\text{k}}} & 0 & 0 & -\frac{R_{\text{i}}}{L_{\text{k}}}\end{pmatrix}\begin{pmatrix}\Delta i_{\text{Lin}}\\ \Delta i_{\text{Lout}}\\ \Delta v_{\text{Cin}}\\ \Delta v_{\text{DC}}\\ \Delta v_{\text{Cfly}}\\ \Delta i_{\text{Bat}}\end{pmatrix} + \begin{pmatrix}0 & \frac{v_{\text{Cfly},0}}{L_{\text{in}}} & 0\\ 0 & \frac{v_{\text{Cfly},0}}{L_{\text{out}}} & 0\\ 0 & 0 & 0\\ \frac{1}{C_{\text{out}}} & 0 & 0\\ 0 & \frac{(-i_{\text{Lout},0}-i_{\text{Lin},0})}{C_{\text{fly}}} & 0\\ 0 & 0 & \frac{1}{L_{\text{k}}}\end{pmatrix}\begin{pmatrix}\Delta i_{\text{PM}}\\ \Delta g_{\text{T1}}\\ \Delta v_{\text{Bat}}\end{pmatrix} \tag{5}$$

$$i_{\text{Lin}} = i_{\text{Lin},0} + \Delta i_{\text{Lin}} \qquad i_{\text{PM}} = i_{\text{PM},0} + \Delta i_{\text{PM}}$$
$$i_{\text{Lout}} = i_{\text{Lout},0} + \Delta i_{\text{Lout}} \qquad g_{\text{T1}} = d + \Delta g_{\text{T1}}$$
$$v_{\text{Cin}} = v_{\text{Cin},0} + \Delta v_{\text{Cin}} \qquad v_{\text{Bat}} = v_{\text{Bat},0} + \Delta v_{\text{Bat}}$$
$$v_{\text{DC}} = v_{\text{DC},0} + \Delta v_{\text{DC}}$$
$$v_{\text{Cfly}} = v_{\text{Cfly},0} + \Delta v_{\text{Cfly}}$$
$$i_{\text{Bat}} = i_{\text{Bat},0} + \Delta i_{\text{Bat}}$$

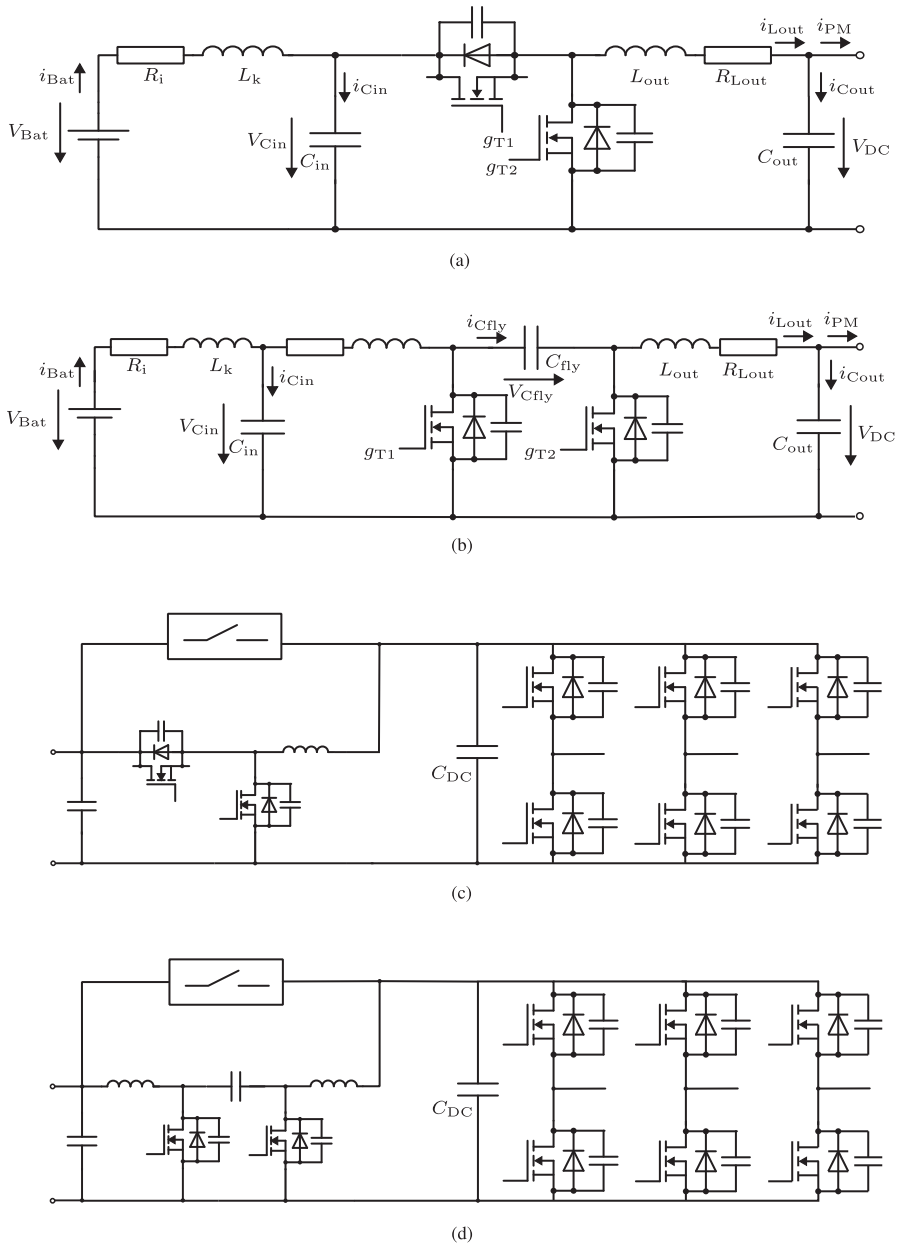

FIGURE 6. **(a) Buck Converter with HV-network and battery, (b) Ćuk Converter with HV-Network and battery, (c) Buck Converter simplified with 2LVSI, (d) Ćuk Converter simplified with 2LVSI. The HV-network and the internal resistance of the battery are modeled by R_i and L_k, which are important for the analysis of resonance effects. Both converters use the input capacitor of the 2LVSI as an output capacitor, as this provides a sufficient energy buffer for each DC/DC converter design, since it typically has a value of 500–800 μ4F due to the large phase current and low switching frequency at the corner point at maximum power of the motor map. The DC/DC converters are used in the WLTC cycle and otherwise bypassed by a suitable bypass.**

to the period of a switching cycle T_{on}/T of the gate signal g_{T1} for both topologies. The small signal approximation is only valid for small current and voltage ripples. The waveforms of one fundamental electric period calculated by the state space model are validated in a SPICE SIMetrix simulation. The calculation is performed in the frequency domain to account for frequency-dependent parameters, such as the real relative permeability of the inductor, serving as a scaling factor for each harmonic of the signal in the quasi-steady state. Due to linearity, the output variable results from the superposition of the individual transmitted input variables. An operating point with all relevant state variables, losses, and temperatures can thus be calculated in MATLAB on a standard industrial computer in less than 300 ms.

B. LOSSES

The relevant loss effects in the DC/DC converter include losses occurring in the semiconductors, the capacitors, the core, as well as the core winding. Since these effects are well-researched, this paper will only briefly touch upon them. For a more in-depth study, relevant literature is referenced. The foundation for calculating losses lies in waveform

models, which are crucial in power electronics. When combined with knowledge of component behavior and material parameters, these models allow for quick calculation of losses.

1) POWER MODULE

The losses in the power modules consist of the conduction losses $P_{\mathrm{v,Cond}}$ and the switching losses, which are further divided into v-i overlap switching losses $P_{\mathrm{v,Sw}}$ and the C_{OSS} losses due to charging and discharging the output capacitance of the semiconductors $P_{\mathrm{v,SwCoss}}$. The on-state losses are calculated using the channel resistance R_{DS} in the first and third quadrants, depending on the current direction and the junction temperature T_{J}.

$$P_{\mathrm{v,Cond}} = \sqrt{\frac{1}{T}\int_0^T \left(R_{\mathrm{DS}}(I_{\mathrm{DS}}, T_{\mathrm{J}}) \cdot i_{\mathrm{DS}}^2\right)^2 \mathrm{d}t}. \tag{3}$$

The switching energies $E_{\mathrm{sw}} = E_{\mathrm{on}} + E_{\mathrm{off}}$ and their dependencies on drain current I_{DS}, DC-Link voltage, voltage switching gradient $\mathrm{d}v/\mathrm{d}t$, and junction temperature are extracted from simulative double-pulse tests with behavioral SPICE models provided by the semiconductor manufacturer. The integration bounds of the waveforms in the double-pulse test are set based on IEC 60747-8. By accumulating the switching energies over the current waveform of a fundamental electrical period i_{DS}, the switching losses can be calculated, where n_{chip} is the number of parallel chips per topological switch. Since the current commutates to one of the two body diodes during the dead time, the reverse-conducting MOSFET enforces quasi-zero-voltage switching (ZVS). In this paper, it is assumed that complete ZVS occurs. Therefore, the switching losses can be halved [40].

$$E_{\mathrm{sw,High}} = \frac{f_{\mathrm{el}}}{f_{\mathrm{sw}}} \cdot \sum E_{\mathrm{sw}}\left(V_{\mathrm{Bat}}, i_{\mathrm{DS,HS}}, T_{\mathrm{J}}, dv/dt\right) \tag{6}$$

$$E_{\mathrm{sw,Low}} = \frac{f_{\mathrm{el}}}{f_{\mathrm{sw}}} \cdot \sum E_{\mathrm{sw}}\left(V_{\mathrm{Bat}}, i_{\mathrm{DS,HS}}, T_{\mathrm{J}}, dv/dt\right) \tag{7}$$

$$P_{\mathrm{v,Sw}} = n_{\mathrm{chip}} \cdot f_{\mathrm{sw}} \cdot (E_{\mathrm{sw,High}} + E_{\mathrm{sw,Low}}). \tag{8}$$

In addition to the v-i overlap losses, also capacitive switching losses appear

$$P_{\mathrm{v,Coss}} = n_{\mathrm{chip}} f_{\mathrm{sw}} C_{\mathrm{oss,Qq}} V_{\mathrm{DC}}^2 \tag{9}$$

due to the discharging and charging of the parasitic output capacitance C_{oss} across the channel [41], which can be calculated from the charge equivalent output capacitance [42]

$$C_{\mathrm{oss,Qq}} = \frac{\int_0^{V_{\mathrm{DC}}} C_{\mathrm{oss}}\,\mathrm{d}V}{V_{\mathrm{DC}}}. \tag{10}$$

Fig. 7 displays the relevant semiconductor properties that are pertinent for electrothermal loss calculations. As mentioned earlier, the switching energies are extracted from a SPICE behavioral model provided by the semiconductor manufacturer. This is highly advantageous when various dependencies need to be extracted. All remaining data is obtained from

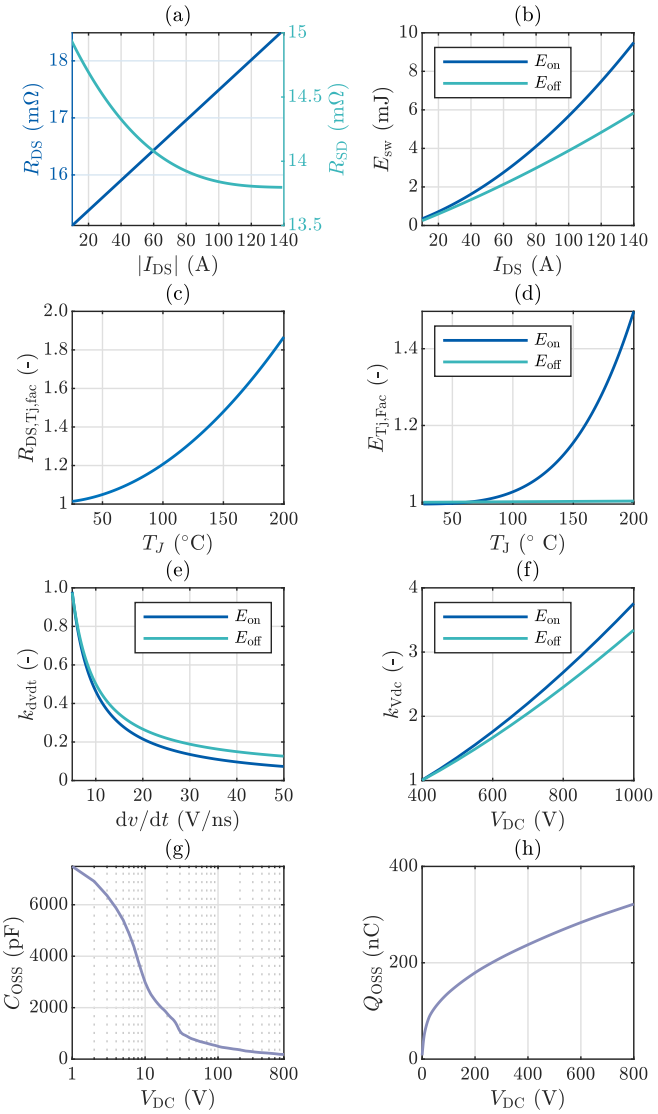

FIGURE 7. Relevant semiconductor data for the thermally coupled loss model: (a) Displays the on-state resistance in the 1st and 2nd quadrants. (b) Shows switching energies at $V_{\mathrm{DC}} = 400$ V and $dv/dt = 5$ V/ns. (c) Depicts the temperature dependence of on-state resistance as a normalized factor. (d) Illustrates the temperature dependence of switching energies as a normalized factor. (e) Shows the dependence of switching energies on the switching rate at $V_{\mathrm{DC}} = 400$, V and $I_{\mathrm{DS}} = 140$A. (f) Depicts the voltage dependence of switching energies at $I_{\mathrm{DS}} = 140$A. (g) Demonstrates the voltage-dependent output capacitance C_{OSS}. (h) Displays the stored charge in the output capacitance C_{OSS}. It should be noted that all data plotted dependent on electrical parameters are always given at a constant temperature of $T_{\mathrm{J}} = 25\,°$C. dv/dt represents the switch-off gradient (10–90)%.

static SPICE simulations or digitized from the manufacturer's datasheet. Since the component physically exists, and both the SPICE model and datasheet information are based on measurements, the confidence level in the accuracy of the loss model is very high. Fig. 8 depicts the waveform model for conduction losses. The current per semiconductor component is calculated based on PWM and current ripple. The effective on-state resistance is extracted from semiconductor data using lookup tables based on the component's average

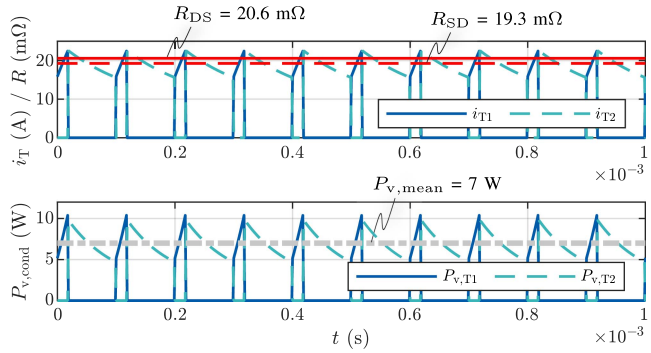

FIGURE 8. Waveform model for conduction losses. The upper representation shows the currents i_{T1} and i_{T2} in a buck converter and the corresponding resistance at mean current and $T_j = 25°C$. The lower representation shows the respective switching energies that can be extracted from semiconductor data in the form of a lookup table.

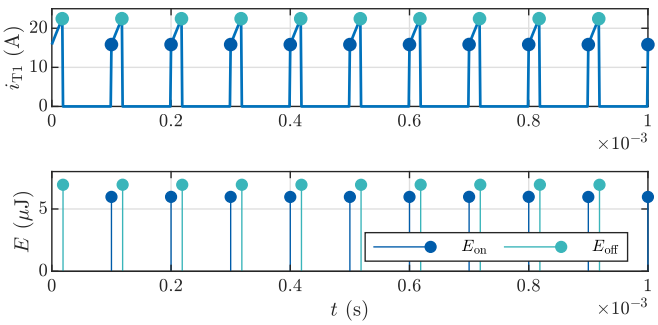

FIGURE 9. Waveform model for switching losses. The upper representation shows the current i_{T1} in a buck converter and the corresponding switching time points. The lower representation shows the respective switching energies E_{on} and E_{off}.

current, as shown in Fig. 7. Losses are calculated using (3). Thermal feedback is taken into account according to Fig. 12. Fig. 9 illustrates the waveform model of the buck converter for a high-side switch, used for calculating switching energies according to (8). Based on the current waveforms of individual switches, switching energy is extracted at the respective switching time points using a lookup table. The same procedure is applied for other switches and topologies.

2) CHOKE

In the choke coil wound with round copper wire on a nanocrystalline toroidal core, the losses are composed of the copper losses $P_{v,Cu}$ and core losses $P_{v,Core}$. In the copper losses, both the DC and AC components are considered due to the skin effect. The core losses can be calculated using the Steinmetz parameters, the magnetic flux density B in the frequency domain, and the core mass m_{Core} [43]. Fig. 10 shows the core loss model waveforms.

$$P_{v,Core} = m_{Core} \cdot k \cdot f^{\alpha} \cdot B^{\beta} \tag{11}$$

To ensure that the DC component at $f = 0$ is also considered, the Steinmetz parameters are adjusted according to

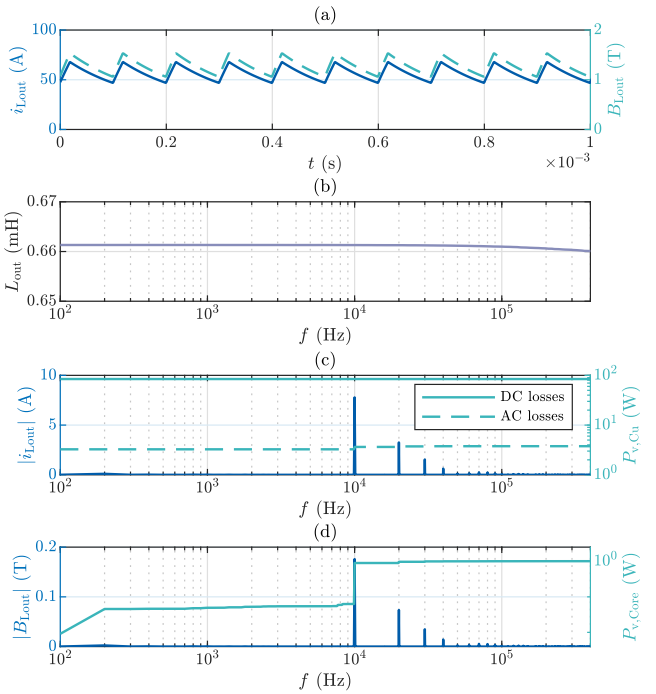

FIGURE 10. Waveform model for inductor losses. (a) Current and flux density. (b) Frequency-dependent inductance. (c) Amplitude spectrum of the current, DC losses, and accumulated AC losses. (d) Amplitude spectrum of the flux density and accumulated core losses.

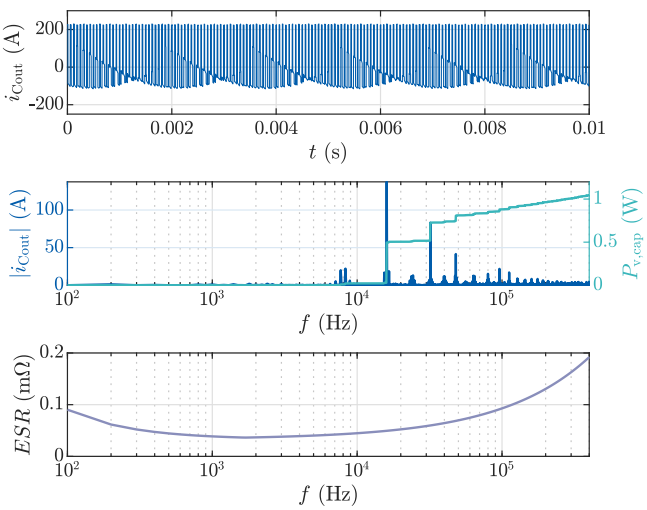

FIGURE 11. Waveform model for capacitor losses. (a) Capacitor current. (b) Amplitude spectrum of the current and accumulated resistive losses. (c) Frequency-dependent ESR.

the DC bias [44]. Linearization of the hysteresis loop up to the saturation flux density B_{sat} provides a sufficiently good approximation in the context of multi-objective optimization [46].

3) CAPACITORS

The polypropylene film capacitors at the input and output use the DC-Link capacitor C_{DC} connected in parallel via the

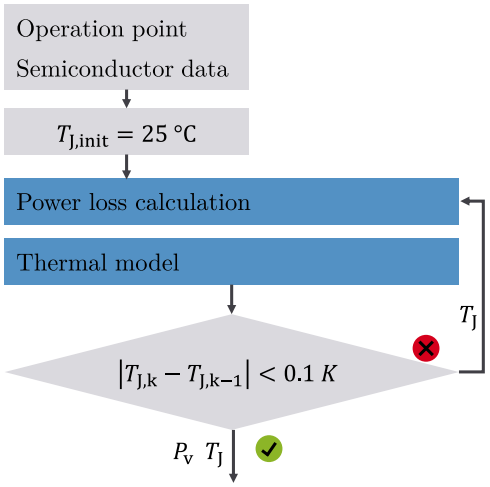

FIGURE 12. Thermal feedback routine for temperature-dependent power loss calculation.

bypass. Since these capacitors only carry the alternating components of the current, the losses can be determined by the capacitor current i_C and the frequency-dependent equivalent series resistance (ESR) in the frequency domain. The ESR is extracted from the manufacturer's K-SIM online design analysis tool for a single capacitor. The ESR is scaled according to the number of paralleled capacitors ESR/n_{cap} to achieve the overall required capacitance.

$$P_{v,Cap} = \frac{1}{2 \cdot n_{cap}} \sum_f ESR(f) \cdot \mathrm{FFT}\{i_C\}^2(f). \qquad (12)$$

Fig. 11 shows the capacitor loss model waveforms.

C. THERMAL

The thermal models are needed, on the one hand, to provide feedback to the electrical loss model in order to adjust temperature-dependent parameters accordingly [45]. Fig. 12 shows the implemented electrothermal model, which is realized by a for-loop in Matlab. On the other hand, maximum temperatures of individual components form the boundary conditions for the design. For the polypropylene film/foil capacitors used, the static thermal resistance is taken from the online library of various capacitor manufacturers. For polypropylene material, the thermal coefficient for the ESR is negative; therefore, the thermal feedback can be neglected. With the nanocrystalline core material Vitroperm 500 F/550 HF from Vacuumschmelze, the thermal feedback can also be disregarded in an initial design to keep the model complexity low [47]. The parameters of the used semiconductors show a strong dependence on the junction temperature; therefore, a feedback model is necessary. Fig. 13 shows the one-dimensional stack structure of a chip with a copper heat sink and direct water cooling. The steady-state junction temperature is calculated based on the fluid temperature T_{fluid} and the losses per chip $P_{v,Chip}$.

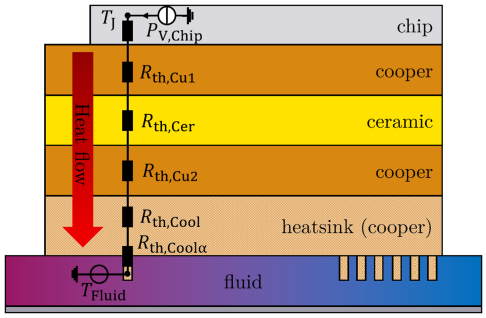

FIGURE 13. Equivalent thermal circuit diagram of one-dimensional heat sink with water cooling.

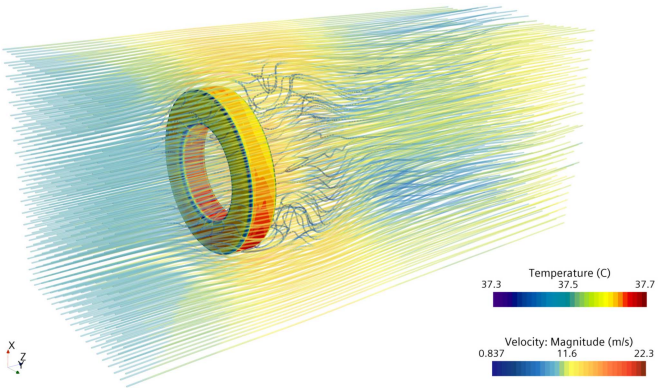

FIGURE 14. CFD simulation of a simplified choke where the core losses are distributed homogeneously over the volume, and thus, no local saturation effects are taken into account.

$$T_J = T_{fluid} + P_{v,Chip} \cdot \sum_i R_{th,i}, \qquad (13)$$

where $R_{th,i}$ is the thermal resistance of each layer. The thermal transfer coefficient $\alpha = 15000\,\mathrm{W}/(mK^2)$ is validated by a computational fluid dynamics (CFD) simulation and is a typical value for automotive power modules cooled with a 50/50 water/glycol mix at volume flow rates from 6 l/min to 12 l/min, depending on the cooling structure. The choke with a core and copper winding is modeled in an analogous way with a homogeneous copper layer. For forced air convection with a fluid velocity of 10 m/s, the CFD simulation provides a thermal transition coefficient $\alpha = 100\,\mathrm{W}/(mK^2)$. This extracted heat transfer coefficient is used for an analytical lumped RC thermal model. The results for one operating point are shown in Fig. 14. Fig. 15 displays a pie chart with the percentages of the loss mechanisms of an exemplary four-phase buck converter at the high-load point at $V_{DC} = 170\,\mathrm{V}$. The bar chart compares the total losses of the e-drive with the reference. This shows that the DC/DC converter compensates for half of the loss advantage in the drive with its own losses.

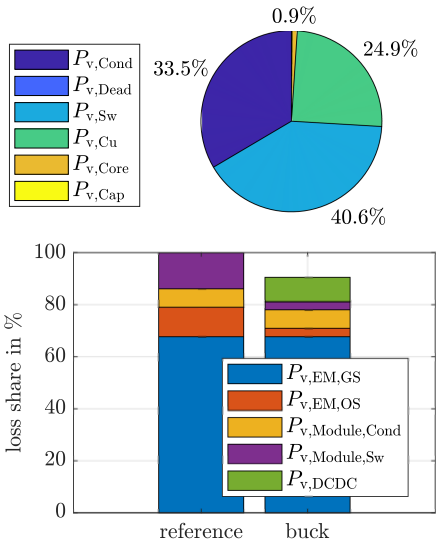

FIGURE 15. Loss distribution of the DC/DC converter (pie chart) and comparison of e-drive losses to reference (bar chart). It can be observed that using the DC/DC converter at a reference point reduces the losses in the inverter and the electric machine. The losses of the DC/DC converter do not offset the savings, resulting in an overall increase in the system's efficiency.

TABLE 3. Specifications, Degrees of Freedom and Design-Relevant Constraints

Specifications	
Topology	Buck or Ćuk converter
Cooling power module	water cooling
Cooling inductor	air convection
Modulation method	8 kHz-SVPWM or CP3
Core external radius r_a	51 mm
Core internal radius r_i	38 mm
Core height h	25 mm
Core material	Vitroperm 550 HF
Degrees of freedom	
# of parallel half-bridges $n_{phase} \in \mathbb{N}$	1...6
Switching frequency f_{sw}	5...30 kHz
Maximum current ripple $\Delta i_{Lout} = \Delta i_{Lin}$	0...100 A
Winding number $w \in \mathbb{N}$	10...100
Air gab length l_d	0, 1...20 mm
Coil cross section A_{Cu}	10...30 mm^2
# of chips per topological switch n_{chip}	5...30
Critical constraints	
Equal DC-Link capacitance	$C_{DC} = C_{in} + C_{out}$
Saturation flux density B_{sat}	1.27 T
Blocking voltage of MOSFETs $V_{DS,max}$	1200 V
Blocking voltage of capacitors $V_{DC,cap}$	1000 V
Maximum DC-Link voltage ripple Δv_{DC}	50 V
Maximim Input voltage ripple Δv_{Cin}	50 V
Possibly fly voltage ripple Δv_{Cfly}	120 V
Maximum junction temperature T_J	175 °C
Maximum capacitor temperature T_{Cap}	105 °C
Maximum core temperature T_{Core}	120 °C
Maximum coil temperature T_{Cu}	100 °C

V. DESIGN

For the hardware design, there are a total of seven degrees of freedom, consisting of six hardware design parameters and the global switching frequency of the converter. Both converter topologies, the core geometry with core material, and the modulation method are available as specifications. Geometric, magnetic, electrical, and thermal constraints are imposed on the DC/DC converter [48], and these are listed along with all degrees of freedom and specifications in Table 3. In order to make the best use of the seven degrees of freedom, it is advisable to design the DC/DC converter using MOO techniques [49] to meet the requirements of the WLTC. In this process, the design space is transformed into the performance space, considering quality criteria such as efficiency η_{DCDC} at the high load point, mass, volume, power density ρ_{DCDC}, chip area A_{Chip}, material costs of the converter, and energy efficiency, or the WLTC range gain $\Delta\eta_{WLTC}$ of the EV in the WLTC cycle. MOO not only aims to find the optimal design that balances several objective functions but also facilitates a fair comparison between different topologies using appropriate objective variables. It highlights sensitivities and trade-offs during the design process, contributing significantly to technology understanding.

For integrating the loss and design models in Matlab, a genetic optimizer is a suitable choice. In principle, in a model-based design, each individual component can be iteratively designed for electrical, magnetic, and thermal boundary constraints independently. However, since all components of the DC/DC converter are interconnected via individual variables such as the choke current, an independent iterative design is only possible when certain degrees of freedom are fixed. This approach may lead to a loss of performance.

Therefore, a brute-force approach is chosen here, which restricts the design space only by nonlinear boundary conditions as well as upper and lower bounds. Fig. 16 illustrates the schematic structure of the design routine, implemented in Matlab. The *gamultiobj* genetic algorithm, a variant of NSGA-II, is used for MOO. Constraints are evaluated based on the degrees of freedom and specifications from Table 3. Once all constraints are satisfied, quality criteria (e.g., Efficiency, WLTC consumption) are assessed using a fitness function. In cases where constraints are not met, the optimizer adjusts the degrees of freedom independently until compliance is achieved.

To simplify the optimization problem and reduce its complexity, the capacitors are designed iteratively within the optimization process. Capacitor losses have a minimal impact on efficiency. Therefore, designing for the minimum possible capacitance at the design switching frequency while satisfying the constraint consistently leads to maximum power density. Also, the DC/DC converter utilizes the inverter's DC-link capacitor as its output capacitance, and the constraint that the

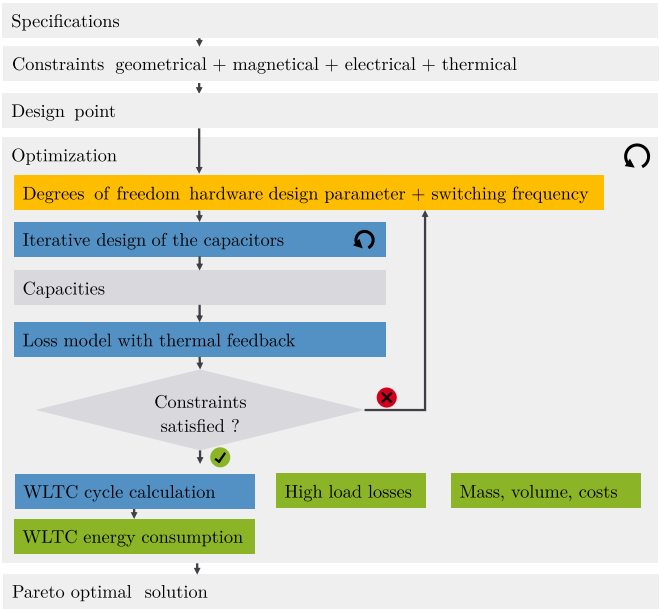

FIGURE 16. Simplified MOO mission profile based design routine for a DC/DC converter.

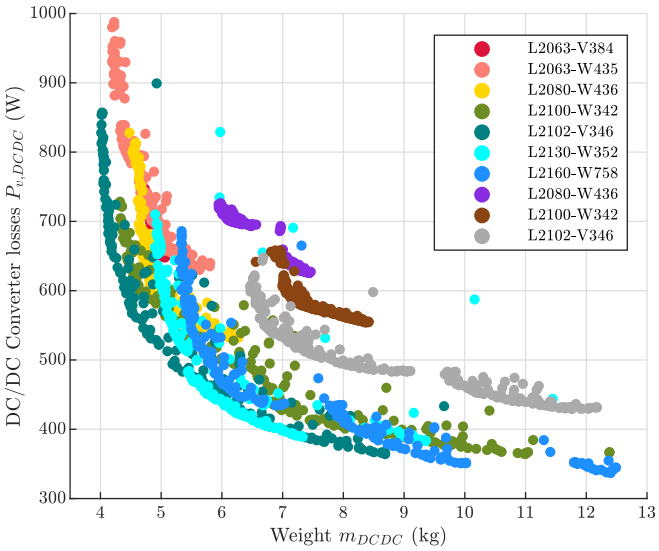

FIGURE 17. 2D Pareto front of DC/DC converter losses $P_{v,DCDC}$ vs. converter weight m_{DCDC} for the buck converter with different core geometries using nanocrystalline Vitroperm 550 HF material from Vacuumschmelze.

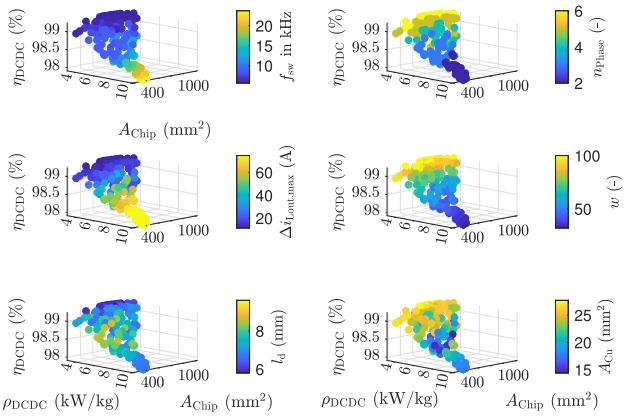

FIGURE 18. 3D η-ρ-A_{Chip} Pareto front of the buck converter with 8 kHz SVPWM inverter control and L2102-V346 core considering high-load efficiency. The relevant parameters of the DC/DC converter design are shown in the colormap.

DC/DC output capacitance must be less than or equal to the DC-link capacitance must be met. The input capacitance is designed based on the constraint of maximum voltage ripple. Because of this constraints, the design of the capacitor in the DC/DC converter is limited by the design of the 2LVSI DC-Link capacitor. The design point is a worst-case point in terms of power losses, electrical waveforms and maximum steady-state temperatures. This design point corresponds to the high load point of the WLTC with a maximum mean choke current of $I_L = 230$ A. The output power in the WLTC is at its maximum, reaching $P_{mech} = 62$ kW at this operating point. For the worst-case scenario, a maximum current ripple, independent of the output level, is assumed.

VI. COMPARISON

A. CORE GEOMETRY

First, an optimal core geometry with material is selected for both topologies. In this process, ten nanocrystalline core geometries from the manufacturer Vacuumschmelze [50] are multi-objectively optimized for minimum high-load DC/DC converter losses $P_{v,DCDC}$ and weight m_{DCDC}. The Pareto fronts for the buck converter are shown in Fig. 17. This indicates that the L2102-V346 Vitroperm 550 HF core exhibits the highest performance for the buck converter and is used for further optimization.

B. TRADE-OFF HIGH LOAD VS. WLTC EFFICIENCY

Fig. 18 shows a 3D Pareto front of the buck converter with 8 kHz-SVPWM inverter control, with each design parameter shown in a separate color. The chip area is chosen as the third target parameter, which predominantly determines the material costs. As is typical in power electronics, the power density increases with increasing switching frequency, whereas the high load efficiency decreases. The six-phase converter achieves the highest efficiency. Despite the larger DC copper resistance, a high number of windings is more efficient in the overall optimization, which is due to the lower current ripple. The air gap to be sawed into varies only slightly but ensures the right balance between saturation current and inductance of the coil. Fig. 19 shows the same MOO with the high load efficiency replaced by the WLTC efficiency. In contrast to high load efficiency, WLTC efficiency optimisation requires the chip area to be reduced to the minimum thermally permissible area in order to achieve the highest range gain. This can be justified by the fact that the switching losses dominate on average in the WLTC cycle, which behave linearly to the chip area in a simple approximation.

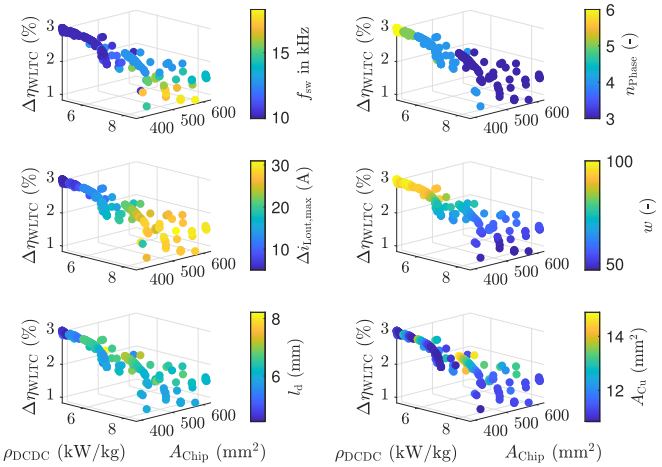

FIGURE 19. 3D $\Delta\eta_{WLTC}$-ρ-A_{Chip} Pareto front of the buck converter with 8 kHz SVPWM inverter control and L2102-V346 core considering WLTC energy efficiency of the overall e-drive with the buck converter. The relevant parameters of the DC/DC converter design are shown in the colormap.

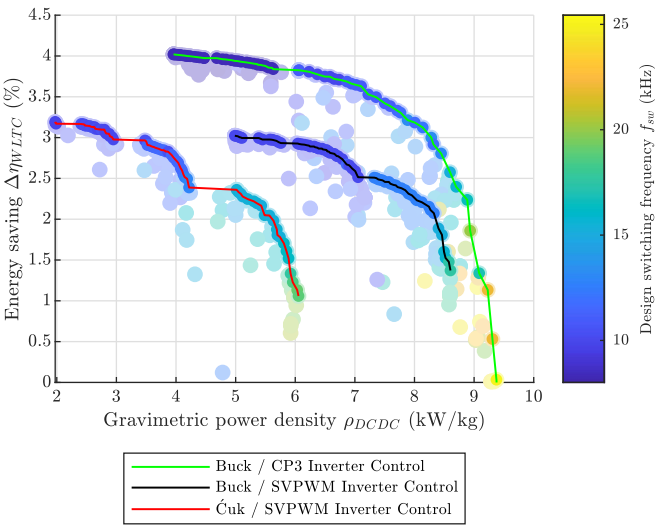

FIGURE 20. 2D Pareto-based comparison of the Buck and Ćuk converters with the L2102-V346 core. For the Buck converter, the two Pareto-optimal designs are shown for 8 kHz-SVPWM and CP3 inverter control.

C. TOPOLOGY AND MODULATION METHOD

For the comparative analysis, both DC/DC converter topologies are optimized for maximal WLTC efficiency, power density, and minimal chip area using 8 kHz SVPWM inverter control. Fig. 20 shows that the buck converter clearly outperforms the Ćuk converter in all three performance parameters. The efficiency disadvantage of the Ćuk topology is due to the necessary serial connection of two 1200 V MOSFETs in series to block the high fly capacitor voltage $V_{Cfly} = V_{Bat} + |V_{DC}|$. When combined with the buck converter with CP3, the WLTC range can be increased by up to 4 % compared to the reference. However, using this modulation method can result in very low switching frequency in the WLTC range, which may affect the stability or dynamics of the current controller and

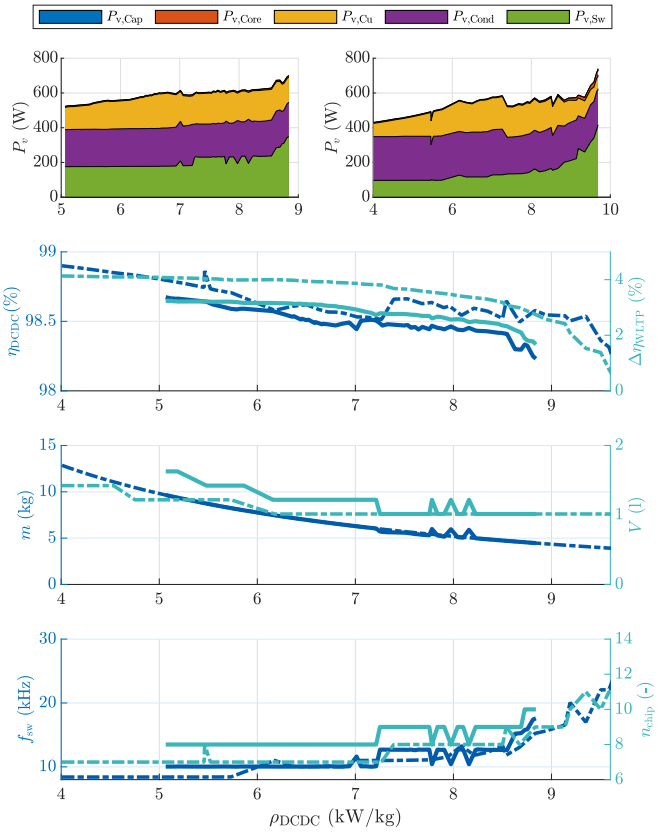

FIGURE 21. Parameterized trajectory of the Pareto front of the Buck converter with 8 kHz-SVPWM inverter (solid line) and CP3 control (dashed line), both with the L2102-V346 core. The upper-left representation shows the losses for the Buck converter with 8 kHz-SVPWM inverter, and the upper-right shows losses for CP3 control.

lead to abnormalities in the acoustics of the electric drive. Therefore, the use of higher-order modulation methods such as quintuple clocking or more may be necessary. For a detailed analysis of the buck converter with 8 kHz-SVPWM and CP3 inverter control, the design points on the Pareto front are shown as a parameterized trajectory in Fig. 20 and Fig. 20, inspired by the representation in [35], [36]. The x-axis corresponds to the Pareto points from left to right, with decreasing WLTC efficiency. While the copper T_{Cu} and core T_{Core} steady-state temperatures at the high-load point are not critical, the semiconductor chips are designed to the thermal limit.

VII. CONCLUSION

This paper presents efficiency optimization using a variable DC-Link voltage for an 800 V system. It is shown that in modern electric sports cars, only lowering the voltage causes an increase in efficiency. The gear ratio is designed such that no field weakening operation occurs in the WLTC cycle. The effect of the operating point efficiency-optimal DC-Link voltage is investigated based on the WLTC cycle. Two DC/DC converter topologies are virtually designed to provide the variable voltage. Based on a requirements analysis, the DC/DC converter is designed for customer-oriented operation only. With multi-objective optimization, it is shown that a range

increase of up to 3% is possible with SVPWM inverter control for the Buck converter at a power density of 5 kW/kg. For the Ćuk converter, a range increase of 3% is possible at a power density of 3 kW/kg. This paper shows that optimizing the converter to one efficiency point does not lead to the optimal design for a converter used for variable-speed drives. Therefore, for the optimizations, the complete cycle must always be calculated for a virtual design to obtain energy efficiency. The application of other modulation methods in the inverter also leads to a change in the performance space of the designed DC/DC converter. With CP3 modulation, a DC/DC converter is designed, which results in a range increase of 3% at a power density of approximately 8.3 kW/kg.

REFERENCES

[1] K. Zhou, Y. Wu, X. Wu, Y. Sun, D. Teng, and Y. Liu, "Research and development review of power converter topologies and control technology for electric vehicle fast-charging systems," *Electronics*, vol. 12, no. 7, Mar. 2023, Art. no. 1581, doi: 10.3390/electronics12071581.

[2] H. Tu, H. Feng, S. Srdic, and S. Lukic, "Extreme fast charging of electric vehicles: A technology overview," *IEEE Trans. Transp. Electrific.*, vol. 5, no. 4, pp. 861–878, Dec. 2019, doi: 10.1109/TTE.2019.2958709.

[3] T. Petri, M. Keller, and N. Parspour, "The insulation resilience of inverter-fed low voltage traction machines: Review, challenges, and opportunities," *IEEE Access*, vol. 10, pp. 104023–104049, 2022, doi: 10.1109/ACCESS.2022.3210348.

[4] M. Keller, M. Maier, T. Petri, and N. Parspour, "Modelling the dynamic voltage distribution in electric traction motor windings," in *Proc. IEEE Int. Symp. Power Electron., Elect. Drives, Automat. Motion*, 2022, pp. 599–604, doi: 10.1109/SPEEDAM53979.2022.9842170.

[5] O. Magdun and A. Binder, "High-frequency induction machine modeling for common mode current and bearing voltage calculation," *IEEE Trans. Ind. Appl.*, vol. 50, no. 3, pp. 1780–1790, May/ Jun. 2014, doi: 10.1109/TIA.2013.2284301.

[6] K. Hameyer, A. Ruf, and F. Pauli, "Influence of fast switching semiconductors on the winding insulation system of electrical machines," in *Proc. IEEE Int. Power Electron. Conf.*, 2018, pp. 740–745, doi: 10.23919/IPEC.2018.8507972.

[7] C. He, M. Beltle, S. Tenbohlen, T. Hubert, S. Schmidt, and J. Schneider, "Partial discharge characteristic of hairpin windings for inverter-fed motors," in *Proc. IEEE 4th Int. Conf. Dielectrics*, 2022, pp. 49–52, doi: 10.1109/ICD53806.2022.9863473.

[8] R. A. Prado and C. N. L. Gajo, "Power semiconductor failures due to cosmic rays," in *Proc. Braz. Power Electron. Conf.*, 2017, pp. 1–6, doi: 10.1109/COBEP.2017.8257437.

[9] T. Oda, T. Arai, T. Furukawa, M. Shiraishi, and Y. Sasajima, "Electric-field-Dependence mechanism for cosmic ray failure in power semiconductor devices," *IEEE Trans. Electron Devices*, vol. 68, no. 7, pp. 3505–3512, Jul. 2021, doi: 10.1109/TED.2021.3077208.

[10] T. Velic, M. Barkow, and N. Parspour, "Loss model for SiC MOSFET based power modules using synchronous rectification," in *Proc. IEEE Int. Symp. Power Electron., Elect. Drives, Automat. Motion*, 2022, pp. 503–510, doi: 10.1109/SPEEDAM53979.2022.9842103.

[11] D. Cittanti, V. Mallemaci, F. Mandrile, S. Rubino, R. Bojoi, and A. Boglietti, "PWM-Induced losses in electrical machines: An impedance-based estimation method," in *Proc. IEEE 24th Int. Conf. Elect. Mach. Syst.*, 2021, pp. 548–553, doi: 10.23919/ICEMS52562.2021.9634438.

[12] T. Velic et al., "Efficiency optimization of electric drives with full variable switching frequency and optimal modulation methods," in *Proc. IEEE 17th Conf. Elect. Mach., Drives Power Syst.*, 2021, pp. 1–6, doi: 10.1109/ELMA52514.2021.9503056.

[13] R. Krüger, P. P. Durán, T. Gerhard, and K. Hameyer, "Current displacement effects on copper losses in PWM supplied permanent magnet excited electrical machines," in *Proc. IEEE Int. Conf. Elect. Mach.*, 2022, pp. 1437–1443, doi: 10.1109/ICEM51905.2022.9910762.

[14] R. Krüger, S. Singh, P. P. Durán, and K. Hameyer, "Inverter control and its effect on copper losses in electrical machines equipped with hairpin winding," in *Proc. IEEE 12th Int. Electric Drives Prod. Conf.*, 2022, pp. 01–07, doi: 10.1109/EDPC56367.2022.10019753.

[15] D. Cittanti, "System level efficiency optimization of an electric vehicle traction drive," Ph.D. dissertation, Politecnico di Torino, Turin, Italy, 2018.

[16] M. Schweizer, T. Friedli, and J. W. Kolar, "Comparative evaluation of advanced three-phase three-level inverter/converter topologies against two-level systems," *IEEE Trans. Ind. Electron.*, vol. 60, no. 12, pp. 5515–5527, Dec. 2013, doi: 10.1109/TIE.2012.2233698.

[17] M. Schweizer, "System-oriented efficiency optimization of variable speed drives," Ph.D. dissertation, ETH Zurich, Zurich, Switzerland, 2012.

[18] A. Carlsson, V. Josefsson, F. Furufors, S. Nategh, D. Ekholm, and N. Kleen, "An investigation on DC-Link voltage influence on E-drive efficiency for e-mobility application," in *Proc. IEEE Workshop Elect. Mach. Des., Control Diagnosis*, 2023, pp. 1–6, doi: 10.1109/WEMDCD55819.2023.10110942.

[19] C. -Y. Yu, J. Tamura, and R. D. Lorenz, "Optimum DC bus voltage analysis and calculation method for inverters/motors with variable DC bus voltage," *IEEE Trans. Ind. Appl.*, vol. 49, no. 6, pp. 2619–2627, Nov./Dec. 2013, doi: 10.1109/TIA.2013.2265873.

[20] J. Lemmens, J. Driesen, and P. Vanassche, "Dynamic DC-link voltage adaptation for thermal management of traction drives," in *Proc. IEEE Energy Convers. Congr. Expo.*, 2013, pp. 180–187, doi: 10.1109/ECCE.2013.6646698.

[21] C. -Y. Yu, J. Tamura, and R. D. Lorenz, "Control method for calculating optimum DC bus voltage to improve drive system efficiency in variable DC bus drive systems," in *Proc. IEEE Energy Convers. Congr. Expo.*, 2012, pp. 2992–2999, doi: 10.1109/ECCE.2012.6342361.

[22] T. Schoenen, M. S. Kunter, M. D. Hennen, and R. W. De Doncker, "Advantages of a variable DC-Link voltage by using a DC-DC converter in hybrid-electric vehicles," in *Proc. IEEE Veh. Power Propulsion Conf.*, 2010, pp. 1–5, doi: 10.1109/VPPC.2010.5729003.

[23] C. Klöffer, "Reichweitenverlängerung von elektrofahrzeugen durch optimierung des elektrischen antriebsstranges," Ph.D. dissertation., Karlsruher Institut für Technologie, Karlsruhe, Germany, 2015.

[24] A. Najmabadi, K. Humphries, and B. Boulet, "Implementation of a bidirectional DC-DC in electric powertrains for drive cycles used by medium duty delivery trucks," in *Proc. IEEE Energy Convers. Congr. Expo.*, 2015, pp. 1338–1345, doi: 10.1109/ECCE.2015.7309848.

[25] S. Tenner, S. Gimther, and W. Hofmann, "Loss minimization of electric drive systems using a DC/DC converter and an optimized battery voltage in automotive applications," in *Proc. IEEE Veh. Power Propulsion Conf.*, 2011, pp. 1–7, doi: 10.1109/VPPC.2011.6043024.

[26] K. K. Prabhakar, M. Ramesh, A. Dalal, C. U. Reddy, A. K. Singh, and P. Kumar, "Efficiency investigation for electric vehicle powertrain with variable DC-link bus voltage," in *Proc. IEEE 42nd Annu. Conf. Ind. Electron. Soc.*, 2016, pp. 1796–1801, doi: 10.1109/IECON.2016.7793714.

[27] L. Liu et al., "Loss minimization of traction systems in battery electric vehicles using variable DC-Link voltage technique – experimental study," in *Proc. IEEE 22nd Eur. Conf. Power Electron. Appl.*, 2020, pp. P. 1–P. 8, doi: 10.23919/EPE20ECCEEurope43536.2020.9215904.

[28] T. Zeltwanger, H. Sprenger, M. Damson, and N. M. Gupta, "The six-step mode: Unwanted or rather the ideal voltage modulation method," in *Proc. 19. Internationales Stuttgarter Symp.*, 2019, pp. 290–304.

[29] I. Ralev, T. Lange, and R. W. De Doncker, "Wide speed range six-step mode operation of IPMSM drives with adjustable DC-Link voltage," in *Proc. IEEE 17th Int. Conf. Elect. Machines Syst.*, 2014, pp. 2987–2993, doi: 10.1109/ICEMS.2014.7014008.

[30] J. Poon, M. Sinha, S. V. Dhople, and J. Rivas-Davila, "Real-time selective harmonic minimization using a hybrid analog/digital computing method," *IEEE Trans. Power Electron.*, vol. 37, no. 5, pp. 5078–5088, May 2022, doi: 10.1109/TPEL.2021.3126678.

[31] A. Boglietti, P. Ferraris, M. Lazzari, and F. Profumo, "Iron losses in magnetic materials with six-step and PWM inverter supply (induction motors)," *IEEE Trans. Mag.*, vol. 27, no. 6, pp. 5334–5336, Nov. 1991, doi: 10.1109/20.278830.

[32] M. Dr Brüll, "Fahrzeugbordnetz und verfahren zum betreiben eines fahrzeugbordnetzes," Patent DE 10 2017 221 982 A1, Continental Automotive GmbH, 30165 Hannover, 06.06. 2019. [Online]. Available: https://register.dpma.de/DPMAregister/pat/register?AKZ=1020172219823

[33] G. Tsolaridis, "A High Power Dynamic Arbitrary Current Source With a Modular Design," Ph.D. dissertation, ETH Zürich, Zürich, Switzerland, 2021.
[34] J. W. Kolar, J. Biela, and J. Miniböck, "Exploring the pareto front of multi-objective single-phase PFC rectifier design optimization - 99.2 percent Efficiency vs. 7 kW/dm3 power density," in *Proc. IEEE Int. Power Electron. Motion Control Conf.*, 2009, pp. 1–21.
[35] R. M. Burkart and J. W. Kolar, "Comparative life cycle cost analysis of Si and SiC PV converter systems based on advanced $\eta - \rho\sigma$ multiobjective optimization techniques," *IEEE Trans. Power Electron.*, vol. 32, no. 6, pp. 4344–4358, Jun. 2017.
[36] R. Burkart, "Advanced modeling and multi-objective optimization of power electronic converter systems," Ph.D. dissertation, ETH Zürich, Zürich, Switzerland, 2016.
[37] T. Guillod, P. Papamanolis, and J. W. Kolar, "Artificial neural network (ANN) based fast and accurate inductor modeling and design," *IEEE Open J. Power Electron.*, vol. 1, pp. 284–299, 2020, doi: 10.1109/OJPEL.2020.3012777.
[38] R. D. Middlebrook and S. Ćuk, "A general unified approach to modelling switching converter power stages," in *Proc. IEEE Power Electron. Specialists Conf.*, 1976, pp. 18–34.
[39] D. Maksimović and S. Ćuk, "General properties and synthesis of PWM DC-to-DC converters," in *Proc. IEEE 20th Annu. Power Electron. Specialists Conf.*, 1989, pp. 515–5 25, doi: 10.1109/PESC.1989.48529.
[40] A. Acquaviva, A. Rodionov, A. Kersten, T. Thiringer, and Y. Liu, "Analytical conduction loss calculation of a MOSFET three-phase inverter accounting for the reverse conduction and the blanking time," *IEEE Trans. Ind. Electron.*, vol. 68, no. 8, pp. 6682–6691, Aug. 2021, doi: 10.1109/TIE.2020.3003586.
[41] J. A. Anderson, "Ultra-high efficiency isolated/non-isolated three-phase multi-level PWM converter," Ph.D. dissertation, ETH Zurich, Zürich, Switzerland, 2020.
[42] M. Kasper, R. M. Burkart, G. Deboy, and J. W. Kolar, "ZVS of power MOSFETs revisited," *IEEE Trans. Power Electron.*, vol. 31, no. 12, pp. 8063–8067, Dec. 2016, doi: 10.1109/TPEL.2016.2574998.
[43] J. Mühlethaler, J. Biela, J. W. Kolar, and A. Ecklebe, "Improved core-loss calculation for magnetic components employed in power electronic systems," *IEEE Trans. Power Electron.*, vol. 27, no. 2, pp. 964–973, Feb. 2012, doi: 10.1109/TPEL.2011.2162252.
[44] J. Mühlethaler, J. Biela, J. W. Kolar, and A. Ecklebe, "Core losses under DC bias condition based on steinmetz parameters," in *Proc. IEEE Int. Power Electron. Conf.*, 2010, pp. 2430–2437, doi: 10.1109/IPEC.2010.5542385.
[45] Y. Wu et al., "Electrothermal-control co-design of an all silicon carbide 2×250 kW dual inverter for heavy-duty traction applications," *IEEE Trans. Ind. Appl.*, vol. 58, no. 1, pp. 505–516, Jan./Feb. 2022, doi: 10.1109/TIA.2021.3127144.
[46] B. Zwang, "Modellierung und hocheffiziente berechnung der lastabhängigen eisenverluste in permanentmagneterregten synchronmaschinen," Ph.D. dissertation, Karlsruhe Institut of Technology, Karlsruhe, Germany, 2019.
[47] K. Reichert, "Nanocrystalline materials for power transformers in switched-mode power supplies".
[48] D. Zhang, M. Guacci, M. Haider, D. Bortis, J. W. Kolar, and J. Everts, "Three-phase bidirectional buck-boost current dc-link EV battery charger featuring a wide output voltage range of 200 to 1000 V," in *Proc. IEEE Energy Convers. Congr. Expo.*, 2020, pp. 4555–4562, doi: 10.1109/ECCE44975.2020.9235868.
[49] J. W. Kolar, "Multi-objective optimization in power electronics," in *Proc. Plenary Presentation Southern Power Electron. Conf.*, 2016, pp. 28–33.
[50] VITROPERM 550 HF, Vacuumschmelze. [Online]. Available: https://vacuumschmelze.de/03_Documents/Brochures/Flyer%20VITROPERM%20550%20HF.pdf

TIMIJAN VELIĆ received the B.Eng. degree in electrical engineering with the Hochschule Esslingen University of applied Sciences, Esslingen, Germany, in 2019, and the M.Sc. degree in mechatronics from Reutlingen University, Reutlingen, Germany, in 2020. He is currently working toward the Ph.D. degree with Dr. Ing. h.c. F. Porsche AG, Departement of Drive System Predevelopment in cooperation, Institute of Electrical Energy Conversion, University of Stuttgart, Stuttgart, Germany. From 2018 to 2020, he was a bachelors candidate and working student with Robert Bosch GmbH in the field of voltage modulation and eDrive control for traction inverters. His research interest focuses on holistic multi-objective-optimization of traction inverters.

YANNIK BECHER is currently working toward the M.Sc. degree in electrical engineering with focus on electric drives and power electronics with the Karlsruhe Institut of Technology, Karlsruhe, Germany.

He wrote his bachelor's thesis at Porsche on the topic Investigation on DC/DC converters in the DC-Link for the application in high-performance electric drives after an internship with Dr. Ing. h.c. F. Porsche AG, Departement of Drive System Predevelopment, where he is currently a working student.

NEJILA PARSPOUR received the master's degree in electrical engineering and the Ph.D. degree from Technical University of Berlin, Berlin, Germany, in 1991 and 1995. She is currently a Professor of electrical energy conversion with the University of Stuttgart, Stuttgart, Germany, and the Director of the Institute of Electrical Energy Conversion, Stuttgart.

She has 5 years of industrial experience with Philips and 6 years of scientific experience with the University of Bremen, Bremen, Germany. Her research and teaching interests include field of electrical machines and drives with a focus on machine design and in the field of contactless energy transfer with a focus on inductive charging systems.