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A New Class of Modular Multilevel Converter for Direct AC-AC Conversion

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ABSTRACT This article introduces the modular multilevel ac/ac converter (M2AC) which capitalizes on a new partial power processing mechanism (P3M) to achieve direct voltage transformation in single frequency power systems. The proposed P3M allows direct voltage transformation using only half-bridge submodules (HBSM) by harnessing internally circulating dc currents to achieve the charge balance of the submodule capacitors. The M2AC represents a new class of modular multilevel converter (MMC) where, unlike with the classical back-to-back MMC, all submodules contribute to net ac power transfer. When contrasting this single-stage ac/ac conversion process with the ac/dc-dc/ac conversion process for the back-to-back MMC, the M2AC is shown to have a significantly lower semiconductor effort requirement. The article begins by using the classical dc-ac MMC structure to motivate the derivation of the M2AC. A detailed analysis of the M2AC's fundamental working principle is conducted with emphasis on the P3M. A dynamic controller is proposed that incorporates key functionalities such as output voltage regulation and submodule capacitor voltage balancing controls. The M2AC's principle of operation and the proposed controls are validated by simulation studies, and experimental tests performed on a laboratory-scale 250 Vpk, 1.25 kW prototype further confirm the efficacy of the novel P3M. The M2AC offers a new approach to voltage conversion in ac power systems that may be an attractive solution for certain distribution and transmission level applications, primarily where voltage regulation and power flow control are core objectives.

INDEX TERMS Modular multilevel converter, direct ac/ac conversion, partial power processing.

I. INTRODUCTION

The rapidly escalating penetration levels of distributed generation (DG) with renewable energy-based sources and unpredictable loads like electric vehicle (EV) charging stations are imposing formidable challenges on the conventional ac grid. These challenges include overloading, power flow imbalances, feeder hosting capacity limitations, and excessive voltage fluctuations and unbalances [1], [2]. Traditional solutions like on-load tap changers [3] and phase shifting transformers [4] have limited effectiveness in systems with high variability due to the extensive proliferation of DG and EV technologies. As a result, advanced voltage/power control devices such as dynamic voltage restorers [5], flexible ac transmission systems (FACTS) [6] and custom power flow controllers [7], solid-state transformers (SST) [8], [9] and soft-open points [10], [11] have gained the interest of grid operators to overcome challenges with active voltage and power control. Power electronic ac/ac converters are fundamental enablers of many of these concepts. The modular multilevel converter (MMC) technology, originally developed for high voltage direct current (HVDC) conversion [12], [13], has earned widespread industry acceptance and is now being increasingly considered for ac/ac conversion in medium-to-high voltage and power applications. This is due to its salient features such as high degrees of modularity and scalability, operational redundancy, control flexibility, and high power quality combined with relatively low power losses.

MMC-based ac/ac converters can be broadly categorized into two subgroups: (i) direct ac/ac converters such as modular multilevel matrix converters (M3Cs) [14], [15], [16] and hexverters [17], and (ii) indirect ac/ac converters including back-to-back MMC (BTB-MMC) [18], [19], [20], [21] and MMC based solid-state transformer (MMC-SST) [22], [23], [24]. The direct ac/ac MMCs typically use full-bridge submodules to support power conversion directly between two different ac frequencies, without a main dc link. In contrast, the indirect ac/ac MMCs interface two ac systems operating at different or similar frequencies by using cascaded dc-ac MMCs with half-bridge submodules (HBSM); here, the ac systems are decoupled via an intermediate dc link. The MMC-SST further utilizes a high frequency internal ac transformer stage. A shared trait of direct and indirect ac/ac MMCs is that they process all of the incoming ac power.

The M3C and BTB-MMC are the most extensively researched and widely utilized direct and indirect ac/ac MMCs, respectively [25]. While the M3C holds great promise for different frequency applications such as fractional frequency transmission systems, variable frequency motor drives, and grid integration of wind turbines, it faces challenges related to excessively large capacitor voltage ripples when operating the input and output ac ports at the same frequency. While some methods to mitigate this issue have been proposed, e.g. through injecting circulating currents [26] or absorbing reactive power at the input side [27], these solutions often lead to complex control strategies, increased valve current stresses, and reduced power quality. Additionally, the M3C's use of full-bridge submodules limits potential savings in the required semiconductors. In comparison, the BTB-MMC avoids the capacitor voltage ripple issue for same frequency operation due to the use of separate dc-ac stages. But this two-stage conversion underpins its main drawbacks of larger size and weight, and higher losses [10]. Modified versions of BTB-MMCs to reduce the total number of semiconductors have been proposed such as in [28] but the potential reduction in semiconductors is limited due to the full-power processing involved, while a more complex per phase implementation is required relative to the conventional MMC (3 versus 2 arms, per phase leg).

Indirect ac/ac MMCs with separate input/output stages offer high operational flexibility but, in some applications, such a high degree of flexibility is not always essential. For example, the limited voltage control range typically required in distribution grids makes it difficult to justify indirect ac/ac converters with multiple full-rated power conversion stages [8]. Other more competitive options exist such as power electronic assisted tap-changing transformers [29], [30] or hybrid transformers [8], however, these are not fully power electronic solutions. Ultimately, apart from the established direct and indirect type MMCs, there are few alternative choices for ac/ac voltage conversion. Especially for fully power electronic (i.e., transformerless) converter solutions that are not obliged to process all of the incoming ac power.

Motivated by the aforementioned gap, this work presents a new method of ac/ac power conversion that leverages a novel partial power processing mechanism (P3M) to achieve direct voltage transformation in single frequency power systems. The proposed modular multilevel ac/ac converter (M2AC), first disclosed in [31], represents a new class of ac/ac MMC that, unlike existing direct and indirect ac/c MMCs, is rated to handle only a portion of the input power. The M2AC allies the direct power conversion characteristic (no main dc link needed) of direct ac/ac MMCs with the simpler structure of indirect ac/ac MMCs (only HBSMs needed). It is somewhat analogous to a power electronic autotransformer that can adjust both ac grid voltage magnitude and phase. When contrasting the M2AC with its closest counterpart, the BTB-MMC, it is shown that substantial savings in semiconductor effort can be realized, which points to the promise of potential reductions in converter footprint, losses and capital cost. Potential applications of the M2AC include smart transformers, line voltage regulators, soft open points in distribution systems and deployment as part of power flow controllers.

The main contributions of this article are detailed analysis of the M2AC and its novel P3M, the development of a dynamic controller with output voltage regulation and internal arm energy balancing controls, validation of M2AC operation and controls by PLECS simulation, and extensive experimental testing on a laboratory scale 1.25 kW prototype considering different ac voltage ratios.

II. PROPOSED MODULAR MULTILEVEL AC-AC CONVERTER (M2AC)

A. MOTIVATION

A single phase leg of the conventional dc/ac MMC with n cascaded HBSMs per arm is shown in Fig. 1(a), along with its ideal dc and fundamental frequency ac arm currents and voltages. The diode symbols correspond to the anti-parallel diodes across the switches and are shown to denote the physical orientation of the HBSMs. The associated internal (arm level) power transfer mechanisms are illustrated in Fig. 1(b) [32], [33]. The upper (U) and lower (L) arms must carry both ac and dc currents; the dc current is common to both arms while the output ac current is evenly split between the arms. Each arm processes half of the power being transferred between dc and ac ports. Therefore, collectively, the arms must satisfy $P_{ac} = P_{dc}$ to ensure the steady-state charge balance of the submodule capacitors. Two dc/ac MMCs are connected in a back-to-back fashion to form the BTB-MMC for ac/dc-dc/ac power conversion (indirect class of ac/ac MMC).

Steady-state arm energy balance is necessary for the proper operation of any MMC topology and is achieved by leveraging the orthogonality of power flow at different frequencies [34]. The dc-ac MMC with HBSMs in Fig. 1(a) and (b) utilizes internal dc currents to generate an average power component orthogonal to the fundamental frequency average ac power. But for the BTB-MMC, this translates to double power processing, i.e., each dc-ac MMC stage must process the same

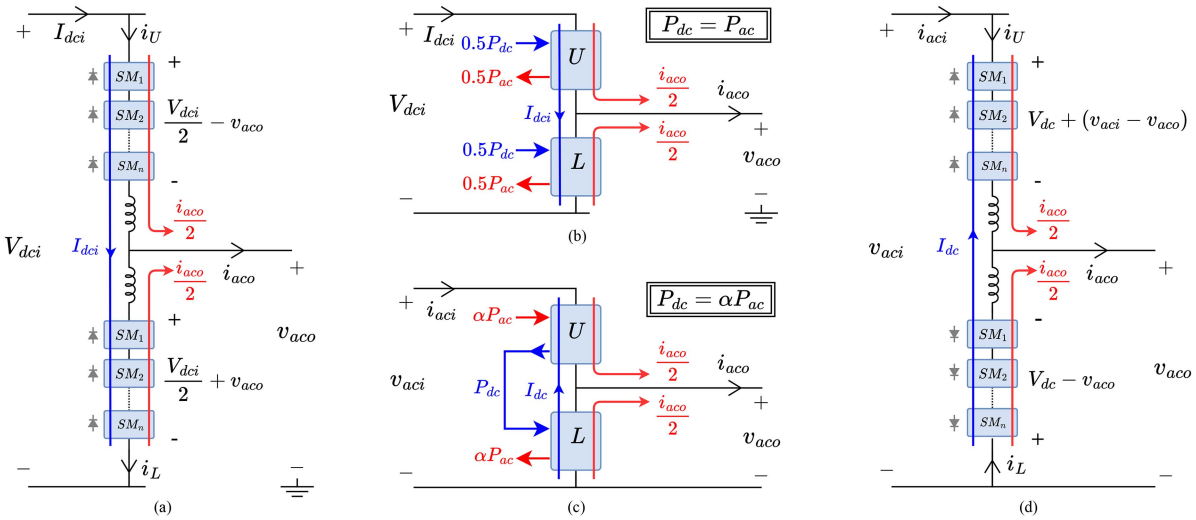

FIGURE 1. Derivation process for proposed ac/ac MMC (a) Single phase leg model of the conventional dc/ac MMC (b) Submodule power processing mechanism of dc/ac MMC phase leg (c) Postulated partial power processing mechanism for direct ac/ac MMC phase leg and (d) Practical realization of direct ac/ac MMC phase leg.

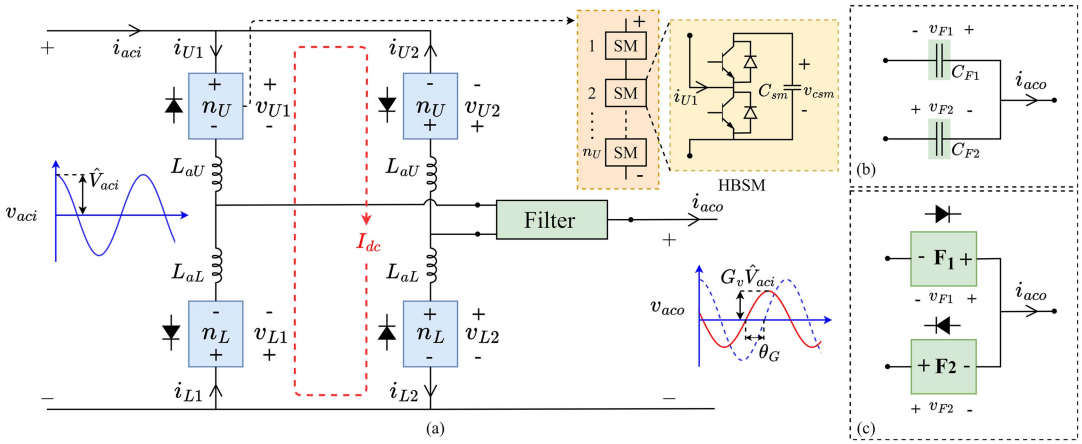

FIGURE 2. (a) Overview of the proposed M2AC topology, (b) Example passive filter implementation, (c) Active filter implementation using submodules.

input power. Therefore, the authors were motivated to seek an alternative MMC structure that adopts a partial-power processing mechanism (P3M) to perform direct ac-ac conversion, while utilizing only dc and fundamental frequency ac quantities for the arms. Fig. 1(c) postulates how such a P3M could be achieved using a single MMC phase leg. Here, the orthogonality of power flow at different frequencies now requires the *exchange* of dc power between arms to facilitate direct conversion between ac input and output. Consequently, steady-state arm power balance dictates the proposed P3M requires only α per-unit (p.u.) of P_{ac} to be processed as dc power exchange between arms.[1]

Considering the flow of I_{dc} in Fig. 1(c), the U and L arms must inject opposite polarity dc voltages to ensure the requisite dc power exchange. Therefore, considering the use of HBSMs, the practical realization of the postulated P3M can be achieved using the MMC phase leg structure of Fig. 1(d). A key difference from Fig. 1(a) is the opposite orientation of the submodules in the L arm (denoted by diode symbols), which is to accommodate the inter-arm P_{dc} exchange in Fig. 1(c). Note the dc voltages injected by the arms cancel at the input terminals, ensuring v_{aci} sees no net dc voltage. The lower arm supports the ac output voltage while the upper arm supports the difference between ac input and output voltages. Interestingly, Fig. 1(d) is somewhat analogous to an autotransformer where a lower output voltage is tapped off from a higher input voltage.

B. M2AC ARCHITECTURE

Fig. 2(a) depicts the proposed M2AC topology where two MMC phase legs of Fig. 1(d) are utilized along with an output filter. Two phase legs are employed to ensure I_{dc} circulates within the M2AC without affecting input or output ac systems. Accordingly, the orientation of the arms within the two-phase

[1]The P3M including quantification of α is studied in Section II-D.

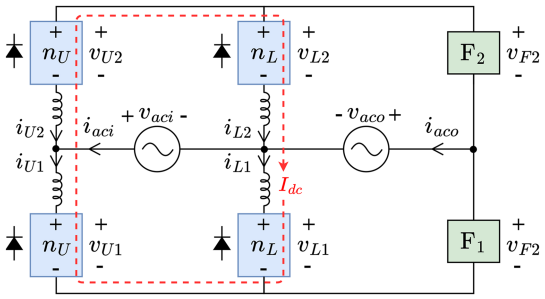

FIGURE 3. Alternative representation of the proposed M2AC topology.

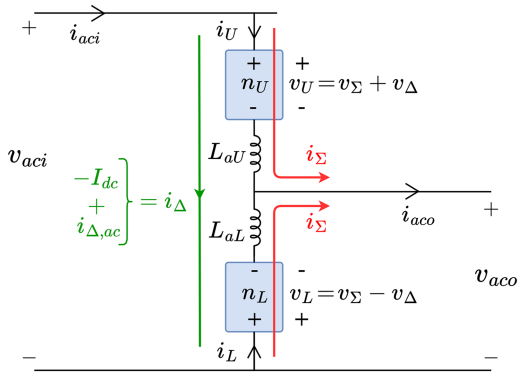

FIGURE 4. Single phase leg model of M2AC including $\Sigma - \Delta$ parameters.

legs is different from each other. The U and L phase arms have n_U and n_L HBSMs, respectively. Variables G_v and θ_G denote the output-to-input ac voltage magnitude ratio and ac voltage phase shift, respectively. The proposed M2AC is a single-phase topology. Three-phase ac/ac conversion can be accommodated by deploying an M2AC in each phase.

The output-side *Filter* in Fig. 2(a) is needed to block a dc voltage bias between the phase legs midpoints, to ensure dc current does not infiltrate the output. The filter should also present a relatively low impedance to the fundamental frequency ac output current. Fig. 2(b) shows the most basic passive filter implementation employing capacitors. However, higher-order filters can also be used, e.g., series LC. Active filter implementation with submodules is also possible, as shown in Fig. 2(c), which allows the use of many smaller and lower voltage capacitors (as opposed to one large capacitor). But this comes with the caveat of increased semiconductor requirement and control complexity. In this work, the simple capacitive filter of Fig. 2(b) is adopted as i) it is the most basic implementation fulfilling all filter objectives, allowing the study focus to be on the M2AC's main operating principle and P3M, and ii) it yields the minimum semiconductor burden and simplest overall control complexity for ease of analysis.

The M2AC is redrawn in Fig. 3 to show an alternative but electrically equivalent representation of the M2AC, where all arms are oriented in the same direction (see diode symbols). This convention is standard practice for MMC circuits. The roles of the converter arms and filter blocks now become clearer. This new perspective reveals that v_{aci} is applied between two MMC phase legs while an output port v_{aco} is created by allowing fundamental frequency current to flow through the midpoint connection of the filter blocks.

C. OPERATING PRINCIPLE OF M2AC

In Fig. 2(a), both phase legs operate in a similar fashion and contribute to the overall ac power transfer. That is, unlike in the BTB-MMC, each M2AC phase leg contributes to net ac power transfer. Therefore, to simplify the analysis, the single-phase leg model in Fig. 4 is adopted. Here, time-averaged voltages and currents are expressed as common-mode (Σ) and differential-mode (Δ) quantities, where

$$v_\Sigma = (v_U + v_L)/2 \qquad v_\Delta = (v_U - v_L)/2 \tag{1}$$

$$i_\Sigma = (i_U + i_L)/2 \qquad i_\Delta = (i_U - i_L)/2. \tag{2}$$

The following modeling assumptions are made to simplify the proceeding analysis:

1) Steady-state voltages and currents are ideal and consist of dc and fundamental frequency components;
2) Power conversion is lossless;
3) Voltage drops across internal passive elements including the arm inductors and filter capacitors are assumed small (by design) and thus are neglected.

M2AC input voltage is denoted by $v_{aci} = \hat{V}_{aci}\cos(\omega t)$ and a complex-valued steady-state voltage conversion ratio is defined as $\overline{G}_v = G_v \angle \theta_G$. Therefore, the output-to-input voltage magnitude gain is $G_v = \hat{V}_{aco}/\hat{V}_{aci} \in [0, 1]$ and output-to-input voltage phase shift is $\theta_G \in [-\pi, \pi]$. The output voltage is thus given by $v_{aco} = G_v \hat{V}_{aci}\cos(\omega t + \theta_G)$.

In Fig. 4, the lower arm must support output voltage v_{aco}. Concurrently, to comply with the HBSMs' incapability to synthesize negative arm voltages, a dc voltage V_{dc} also has to be injected. Thus, the lower arm voltage is

$$v_L = V_{dc} + v_{aco} = V_{dc} + G_v \hat{V}_{aci}\cos(\omega t + \theta_G). \tag{3}$$

The P3M illustrated in Fig. 1(d) requires the upper and lower arms to have equal dc voltage components. This also ensures no net dc voltage is imposed across the ac input terminals. The ac voltage of the upper arm should also compensate for the difference between the input and output ac voltages. Therefore, the upper arm voltage can be expressed as

$$v_U = V_{dc} + \hat{V}_{aci}\cos(\omega t) - G_v \hat{V}_{aci}\cos(\omega t + \theta_G) \tag{4}$$

$$v_U = V_{dc} + v_{U,ac} = V_{dc} + \hat{V}_{U,ac}\cos(\omega t - \theta_U), \tag{5}$$

where $\hat{V}_{U,ac} = (\sqrt{1 - 2G_v\cos(\theta_G) + G_v^2})\hat{V}_{aci}$ and $\theta_U = \tan^{-1}((G_v \sin(\theta_G))/(1 - G_v\cos(\theta_G)))$. Note that if $\theta_G = 0$, v_U in (5) simplifies to $V_{dc} + (1 - G_v)\hat{V}_{aci}\cos(\omega t)$.

Considering the use of HBSMs, V_{dc} in (3) and (5) must always be greater than or equal to the magnitude of arms' ac voltage component to ensure positive voltage injection. Hence, the following criteria must be satisfied,

$$V_{dc} \geq \begin{cases} G_v \hat{V}_{aci} & ; \quad \text{if} \quad G_v\cos(\theta_G) \leq 0.5 \\ \hat{V}_{U,ac} & ; \quad \text{if} \quad G_v\cos(\theta_G) > 0.5. \end{cases} \tag{6}$$

Recalling the variable transformations in (1), the arm voltages in (3) and (5) can be represented as $\Sigma-\Delta$ quantities

$$v_\Sigma = V_{dc} + v_{\Sigma,ac} = V_{dc} + \hat{V}_{\Sigma,ac}\cos(\omega t + \theta_\Sigma) \tag{7}$$

$$v_\Delta = \frac{1}{2}\hat{V}_{aci}\cos(\omega t), \tag{8}$$

where $\hat{V}_{\Sigma,ac} = (\sqrt{4G_v^2 - 4G_v\cos(\theta_G)+1})\hat{V}_{aci}$ and $\theta_\Sigma = \tan^{-1}((2G_v\sin(\theta_G))/(1-2G_v\cos(\theta_G)))$. Observe that v_Δ has only a fundamental frequency component while v_Σ can have both dc and fundamental frequency components. However, v_Σ becomes purely dc valued for the special case $\overline{G}_v = 0.5\angle 0^\circ$. That is, the frequency content of the arms' voltages becomes perfectly decoupled when $v_{aci} = 2v_{aco}$. This decoupling aspect will be exploited for control design.

In Fig. 4, the input and output side ac currents are generalized as $i_{aci} = \hat{I}_{aci}\cos(\omega t + \phi_{aci})$ and $i_{aco} = \hat{I}_{aco}\cos(\omega t + \theta_G + \phi_{aco})$. To simplify analysis while focusing on converter active power transfer characteristics, this work assumes the output-side reactive power demand is zero and thus $\phi_{aco} = 0$ hereinafter. The average ac power transferred to the output is $P_{aco} = \hat{V}_{aco}\hat{I}_{aco}/2$ while the active and reactive powers at the input side are respectively $P_{aci} = \hat{V}_{aci}\hat{I}_{aci}\cos(\phi_{aci})/2$ and $Q_{aci} = \hat{V}_{aci}\hat{I}_{aci}\sin(\phi_{aci})/2$. Hence, i_{aci} is related to i_{aco} as follows.

$$i_{aci} = \frac{\hat{I}_{aco}G_v}{\cos(\phi_{aci})}\cos(\omega t + \phi_{aci}). \tag{9}$$

The upper arm carries input ac current i_{aci} along with I_{dc}, per Fig. 4. Thus, the upper arm current can be expressed as

$$i_U = -I_{dc} + i_{aci} = -I_{dc} + \hat{I}_{aci}\cos(\omega t + \phi_{aci}). \tag{10}$$

The lower arm must support circulating I_{dc} along with the difference between input and output ac currents. Therefore, the lower arm current can be expressed as

$$i_L = I_{dc} + \hat{I}_{aco}\cos(\omega t + \theta_G) - \hat{I}_{aci}\cos(\omega t + \phi_{aci}) \tag{11}$$

$$i_L = I_{dc} + i_{L,ac} = I_{dc} + \hat{I}_{L,ac}\cos(\omega t + \phi_L), \tag{12}$$

where $\hat{I}_{L,ac} = (\sqrt{1 - 2G_v\cos(\theta_G) + G_v^2})\hat{I}_{aci}/G_v$ and $\phi_L = \tan^{-1}((\sin(\theta_G))/(\cos(\theta_G) - G_v))$. Utilizing the relationships in (2), the arm currents in (10) and (12) can be represented as $\Sigma-\Delta$ quantities

$$i_\Sigma = \frac{1}{2}\hat{I}_{aco}\cos(\omega t + \theta_G) \tag{13}$$

$$i_\Delta = -I_{dc} + i_{\Delta,ac} = -I_{dc} + \hat{I}_{\Delta,ac}\cos(\omega t + \phi_\Delta), \tag{14}$$

where $\hat{I}_{\Delta,ac} = (\sqrt{4G_v^2 - 4G_v\cos(\theta_G) + 1})\hat{I}_{aci}/(2G_v)$ and $\phi_\Delta = \tan^{-1}((\sin(\theta_G))/(2G_v - \cos(\theta_G)))$. Similar to the arm voltages in (7) and (8), perfect frequency content decoupling occurs for the $\Sigma-\Delta$ arm currents at voltage ratio $\overline{G}_v = 0.5\angle 0^\circ$. That is, i_Δ in Fig. 4 is purely dc valued for the special case $v_{aci} = 2v_{aco}$.

Another important implication of (13)–(14) is that the input current can be decomposed as $i_{aci} = i_\Sigma + i_{\Delta,ac}$. This indicates the flexibility to adjust i_{aci} by controlling the ac component of i_Δ. Therefore, input current phase angle ϕ_{aci} can be independently controlled without disturbing i_{aco}. Hereinafter, to simplify the P3M analysis, it is assumed $\phi_{aci} = 0$ via suitable control action. This ability will be confirmed in both simulation and experiment.

D. PARTIAL POWER PROCESSING MECHANISM (P3M)

The M2AC practices P3M and thus only a portion of the input ac power is processed to keep the arms' energy balance. The steady-state average power absorbed by the upper arm, $\langle P_U\rangle$, is

$$\langle P_U\rangle = \frac{1}{T}\int_0^T \left((V_{dc} + v_{U,ac})(-I_{dc} + i_{aci})\right) dt \tag{15}$$

$$\langle P_U\rangle = -I_{dc}V_{dc} + \frac{1}{2}(1 - G_v\cos(\theta_G))\hat{V}_{aci}\hat{I}_{aci}. \tag{16}$$

Because $\hat{V}_{aci}\hat{I}_{aci}/2$ is equal to the input ac power, P_{ac}, and $V_{dc}I_{dc}$ is the dc power exchanged between arms, P_{dc}, the upper arm average power absorption can be re-expressed as

$$\langle P_U\rangle = -P_{dc} + (1 - G_v\cos(\theta_G))P_{ac}. \tag{17}$$

Similarly, the steady-state average power absorbed by the lower arm, $\langle P_L\rangle$, is given by (18) and simplified through (19)–(21)

$$\langle P_L\rangle = \frac{1}{T}\int_0^T \left((V_{dc} - v_{aco})(I_{dc} + i_{L,ac})\right) dt \tag{18}$$

$$\langle P_L\rangle = I_{dc}V_{dc} - G_vV_{in}\left(\hat{I}_{aco} - \hat{I}_{aci}\cos(\theta_G)\right)/2 \tag{19}$$

$$\langle P_L\rangle = I_{dc}V_{dc} - (1 - G_v\cos(\theta_G))\hat{V}_{aci}\hat{I}_{aci}/2 \tag{20}$$

$$\langle P_L\rangle = P_{dc} - (1 - G_v\cos(\theta_G))P_{ac}. \tag{21}$$

To achieve arm energy balance, the average powers absorbed by each arm must be zero at steady-state, i.e., $\langle P_U\rangle = \langle P_L\rangle = 0$. Therefore, (17) and (21) quantify the P3M inherent to the M2AC:

$$P_{dc} = (1 - G_v\cos(\theta_G))P_{ac}. \tag{22}$$

The M2AC needs only to process $(1 - G_v\cos(\theta_G))$ p.u. of P_{ac} in the form of internally circulating dc power.[2] That is, $G_v\cos(\theta_G)$ p.u. of P_{ac} is unprocessed. P_{dc} is shuttled between the upper arm and lower arm with the aid of I_{dc} to satisfy the charge balance of the HBSM capacitors, see Fig. 1(c). If the M2AC provides only ac voltage magnitude adjustment, i.e., $\theta_G = 0$, then $(1 - G_v)$ p.u. of P_{ac} is processed.

The M2AC's P3M requirement is graphically illustrated in Fig. 5 considering four different G_v values and $\theta_G \in [-120^\circ, 120^\circ]$. The normalized P_{dc}/P_{ac} curves elucidate that achieving P3M is possible only within the range $\theta_G \in [-90^\circ, 90^\circ]$. To achieve $|\theta_G|$ of more than 90°, the converter has to process more than 1 p.u. of the ac power being transferred which inevitably leads to reduced efficiency. For any value of G_v, the corresponding P_{dc}/P_{ac} becomes minimum as θ_G approaches zero. Fig. 5 indicates the M2AC is best suited

[2] Comparing (22) and Fig. 1(c) reveals that $\alpha = (1 - G_v\cos(\theta_G))$.

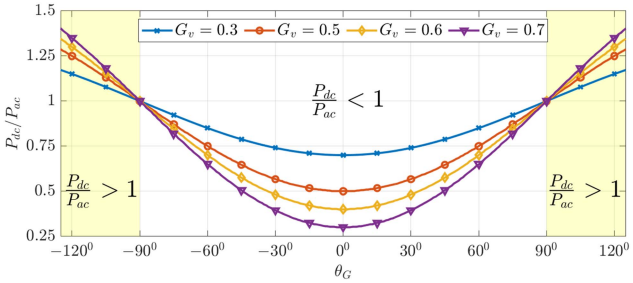

FIGURE 5. Variation of power processing requirement with θ_G and G_v.

for applications with moderate output-to-input voltage gains, e.g. around 0.3 or greater, and modest output-to-input voltage phase shifts, e.g. up to around ±45°. Ultimately, the lower arms of the M2AC support the output voltage and the upper arms must support the difference between input and output voltages (see Fig. 2), and so the required upper arm voltage injection can become excessive if the designed θ_G becomes too large. The BTB-MMC does not have any such limitation on θ_G since the input and output sides use separate dc-ac MMC stages.

The required circulating current, I_{dc}, is determined by the amount of dc power being processed within the converter and the imposed V_{dc}. Based on (16) and (20), and considering the minimum possible V_{dc} value given in (6), the ratio $I_{dc}/\hat{I}_{aci}$ can be determined

$$\frac{I_{dc}}{\hat{I}_{aci}} = \begin{cases} \frac{1-G_v\cos(\theta_G)}{2\sqrt{1-2G_v\cos(\theta_G)+G_v^2}} & ;\text{ if } G_v\cos(\theta_G) \le 0.5 \\ \frac{1-G_v\cos(\theta_G)}{2G_v} & ;\text{ if } G_v\cos(\theta_G) > 0.5. \end{cases} \quad (23)$$

E. IMPLEMENTATION ASPECTS AND M2AC FILTER DESIGN GUIDELINES

The peak voltage requirement of the upper and lower arms is $V_{peak,U} = V_{dc} + \hat{V}_{U,ac}$ and $V_{peak,L} = V_{dc} + G_v\hat{V}_{aci}$, respectively, which dictates the total amount of submodule capacitor voltage needed in the arms. Similarly, the peak current stress for the upper and lower arms is $I_{peak,U} = I_{dc} + \hat{I}_{aci}$ and $I_{peak,L} = I_{dc} + \hat{I}_{L,ac}$, respectively, which gives an indication of the required ampacity ratings for the semiconductor switches in the submodules.[3] Fig. 6 plots the per-unitized peak voltage and peak current stresses that must be supported by the arms, as a function of G_v. Representative curves are shown for $\theta_G \in \{0°, \pm30°, \pm45°\}$. Observe the voltage and current stresses in Fig. 6 are minimum for $\theta_G = 0°$ and trend upward as θ_G increases. The required number of SMs in each arm and their ratings for a chosen operating point are decided based on these peak voltage and current stresses. Section VI will use the results of Fig. 6 to assess the overall semiconductor requirements for the M2AC.

The M2AC filter in Fig. 2(a) can be realized using passive components (see Fig. 2(b)) or additional submodules (see Fig. 2(c)). The former is chosen as the study emphasis of this work, as justified in Section II-B. General filter design guidelines and considerations are summarized below:

1) The filter capacitors must each support the average voltage component injected by the arms, V_{dc}, which depends on the designed $\overline{G}_v$ according to (6). This determines the nominal dc voltage rating of the filter;
2) The filter capacitors must also support a fundamental frequency voltage ripple due to the flow of i_{aco}. Capacitance C_F directly impacts the ripple size. Since the amount of fundamental frequency ripple impacts the internal voltage drop of the M2AC, C_F can be chosen based on the allowed internal voltage drop at rated power transfer.[4] Alternatively, another approach is to choose C_F such that the peak fundamental frequency voltage ripple is similar (on p.u. terms) to the peak ripple on the submodule arms capacitor voltages. Likely a detailed optimization study would need to be carried out in practice to select C_F that minimizes cost and size for a specific converter design;
3) It should be confirmed the chosen C_F avoids potential resonances with the arm inductors and submodule capacitors;
4) Simulation studies should be performed to verify acceptable voltage ripple, the avoidance of any resonance issues and satisfactory converter dynamic performance.

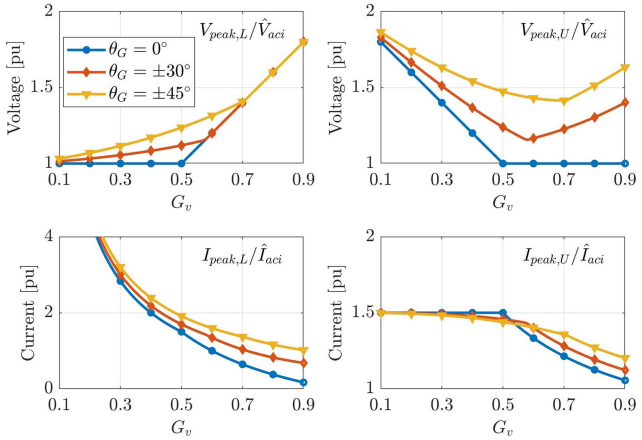

FIGURE 6. Peak arm voltage and current stresses for the single phase leg M2AC in Fig. 4.

III. MATHEMATICAL MODELLING AND DYNAMIC CONTROLLERS

The $\Sigma - \Delta$ convention introduced in Fig. 4 can be applied to each phase leg of the M2AC (Fig. 2(a)) to decouple internal state dynamics. The dynamics of the common mode current in the two phase legs are

$$L_a\frac{d}{dt}i_{\Sigma 1} + R_a i_{\Sigma 1} + \frac{2}{C_F}\int i_{\Sigma 1}dt = -v_{\Sigma 1} + \frac{v_{aci}}{2} - v_{aco} \quad (24)$$

[3] Note, these equations assume the M2AC comprises a single phase leg, and thus $\hat{I}_{aci}$ here denotes the total ac current carried by the upper arm.

[4] One approach is to assume the M2AC should offer a fundamental frequency voltage drop comparable (on p.u. terms) to the internal voltage drop of a power transformer.

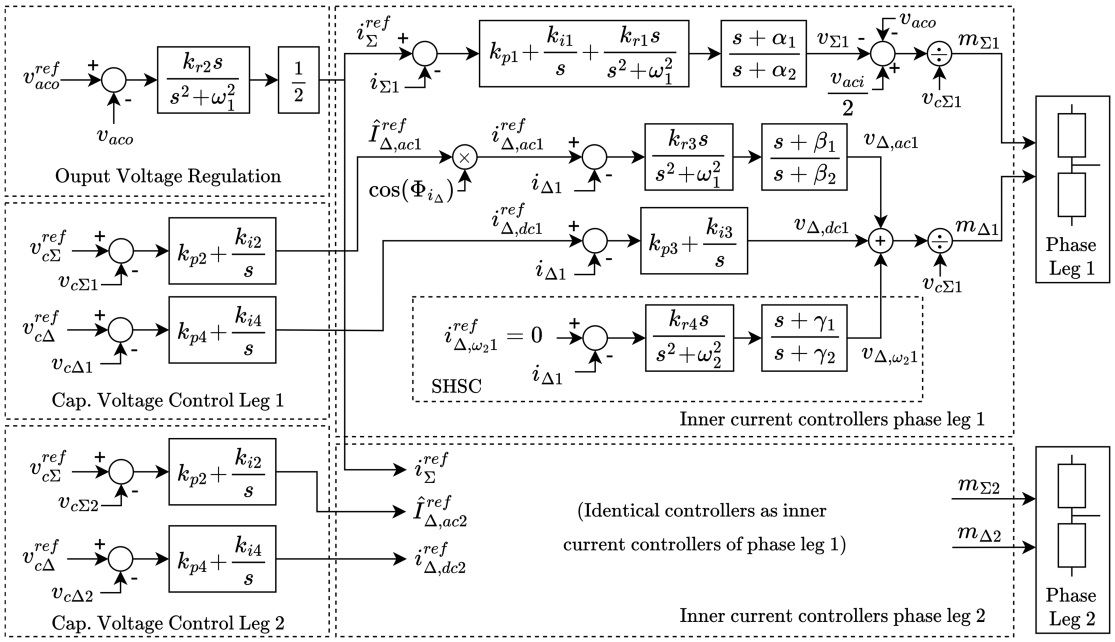

FIGURE 7. Proposed dynamic Control Scheme.

TABLE 1. Control Objectives of Internal Currents

Current	Component	Control Objective
$i_{\Sigma 1}, i_{\Sigma 2}$	ac fundamental	v_{aco} control
$i_{\Delta 1}, i_{\Delta 2}$	ac fundamental phase	ϕ_{aci} control
	ac fundamental magnitude	$v_{c\Sigma}$ control
	dc	$v_{c\Delta}$ control
	ac 2^{nd} harmonic	suppress 2^{nd} harmonic

$$L_a\frac{d}{dt}i_{\Sigma 2}+R_a i_{\Sigma 2}+\frac{2}{C_F}\int i_{\Sigma 2}dt = v_{\Sigma 2}+\frac{v_{aci}}{2}-v_{aco}, \tag{25}$$

where subscripts 1 and 2 denote the first and second phase legs, respectively. Further, it has been assumed that for both phase legs, $L_{aU} = L_{aL} = L_a$ and R_a is the internal resistance of each inductor. Similarly, dynamic equations for the differential mode currents of two phase legs are

$$L_a\frac{d}{dt}i_{\Delta 1} + R_a i_{\Delta 1} = -v_{\Delta 1} + \frac{v_{aci}}{2} \tag{26}$$

$$L_a\frac{d}{dt}i_{\Delta 2} + R_a i_{\Delta 2} = v_{\Delta 2} + \frac{v_{aci}}{2}. \tag{27}$$

Equations (24)–(27) reveal that arm voltages [$v_{\Sigma 1}$ $v_{\Sigma 2}$ $v_{\Delta 1}$ $v_{\Delta 2}$] enable controls over the respective arm currents [$i_{\Sigma 1}$ $i_{\Sigma 2}$ $i_{\Delta 1}$ $i_{\Delta 2}$], e.g., $v_{\Sigma 1}$ drives $i_{\Sigma 1}$. These current components can be utilized for different control objectives as summarized in Table 1, by leveraging their distinct frequency bands and implementing controllers with proper control bandwidths. Common-mode currents $i_{\Sigma 1}, i_{\Sigma 2}$ are utilized as the inner loop control parameter for v_{aco} regulation. The fundamental frequency phase of differential-mode currents $i_{\Delta 1}, i_{\Delta 2}$ can be adjusted to achieve a desired input current phase (and hence power factor), while the fundamental frequency magnitude of $i_{\Delta 1}, i_{\Delta 2}$ can be controlled to regulate the (total sum) common-mode arm capacitor voltage, $v_{c\Sigma}$. The dc component of $i_{\Delta 1}, i_{\Delta 2}$ can be utilized as a mechanism to regulate the (total sum) differential arm capacitor voltage, $v_{c\Delta}$. The second harmonic components of $i_{\Delta 1}, i_{\Delta 2}$ are suppressed to minimize the losses and rms current stresses in the arms.

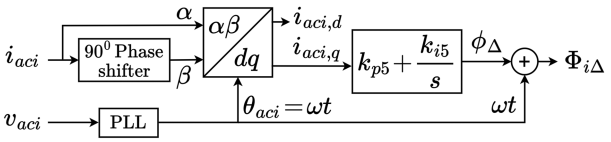

FIGURE 8. Input current phase correction controller.

Based on Table 1, a closed-loop dynamic control scheme is proposed in Fig. 7 that comprises an output voltage regulator, SM capacitor voltage balancing controls, and second harmonic suppression controllers (SHSC). Resonant compensators are used to regulate fundamental frequency quantities and proportional-integral (PI) compensators are adopted to regulate dc quantities. Disturbance terms in the plant model are decoupled using feed-forward control theory. v_{aco}^{ref} is the desired fundamental frequency output voltage which is equal to $G_v\hat{V}_{aci}\cos(\omega t+\theta_G)$. The SM (total sum) arm capacitor voltage references $v_{c\Sigma}^{ref}$ and $v_{c\Delta}^{ref}$ are equal to $0.5(n_U+n_L)V_c^{ref}$ and $0.5(n_U-n_L)V_c^{ref}$, respectively, where V_c^{ref} is the nominal voltage of a SM capacitor. To regulate input current phase ϕ_{aci} to zero, the phase of $i_{\Delta,ac}$ (i.e., ϕ_Δ) is set by the controller illustrated in Fig. 8. The single-phase dq-theory is employed to control the q component of i_{aci} which enables the regulation of ϕ_{aci} [35].

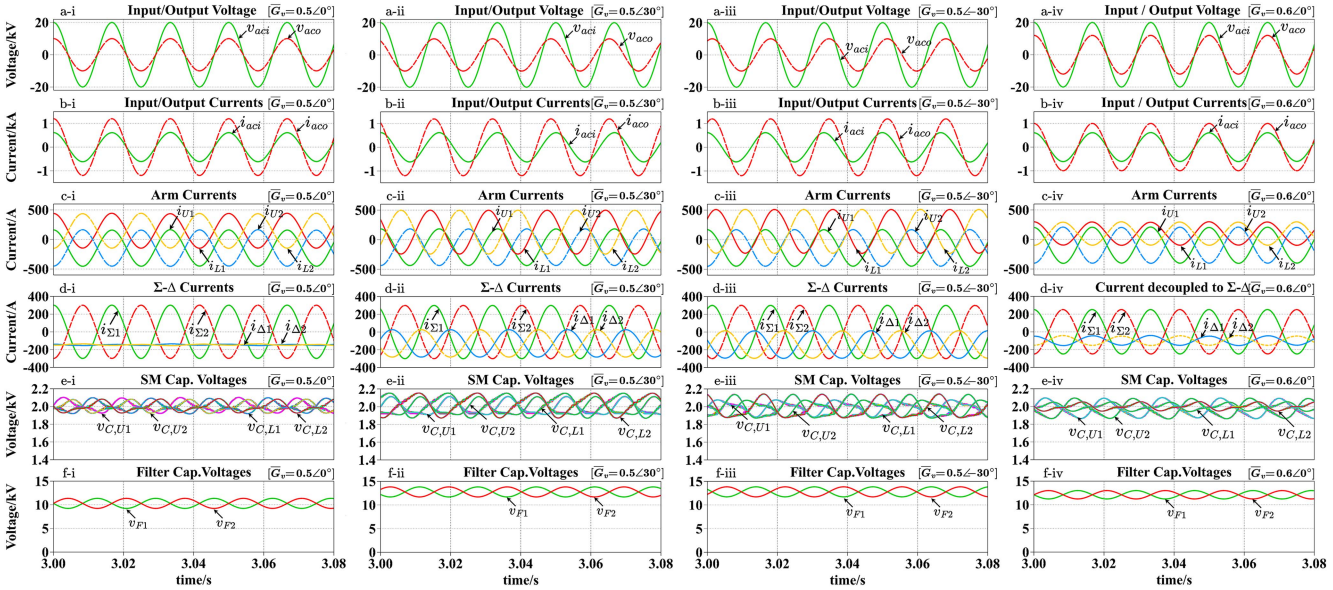

FIGURE 9. Steady-state simulation waveforms: (a) Input/output voltage, (b) Input/output current, (c) Arm currents, (d) Arm currents decoupled into $\Sigma-\Delta$, (e) SM cap. voltage and (f) Filter cap. voltage for the operating points of $\overline{G}_v = 0.5\angle 0°$, $\overline{G}_v = 0.5\angle +30°$, $\overline{G}_v = 0.5\angle -30°$, $\overline{G}_v = 0.6\angle 0°$.

TABLE 2. Simulation Parameters

Converter parameter	Value		
Power Rating, S_{in}	6 MVA		
Input voltage peak, $\hat{V}_{aci}$	20 kV		
SM Cap. voltage, V_c^{ref}	2 kV		
Conversion ratio, $\overline{G}_v$	$0.5\angle 0°$	$0.5\angle \pm 30°$	$0.6\angle 0°$
Output voltage mag., $\hat{V}_{aco}$	10 kV	10 kV	12 kV
SMs in upper arm, n_U	10	13	13
SMs in lower arm, n_L	10	12	12
Arm inductance, L_a	26 mH		
SM capacitance, C_{SM}	3 mF		
Filter capacitance, C_F	1500 μF		
Control parameter	**Value**		
$k_{r2}, k_{p1}, k_{i1}, k_{r1}, \alpha_1, \alpha_2$	$290, 22, 1650, 1320, 1077, 527$		
$k_{p2}, k_{i2}, k_{r3}, \beta_1, \beta_2$	$0.045, 0.1, 600, 91, 1840$		
$k_{p4}, k_{i4}, k_{p3}, k_{i3}$	$0.1, 5, 0.4, 1.4$		
$k_{r4}, \gamma_1, \gamma_2$	$610, 350, 3600$		
k_{p5}, k_{i5}	$0.1, 1.5$		

IV. SIMULATIONS

The operation and performance of the M2AC and the proposed dynamics controls are validated through extensive simulations using a detailed switched model in PLECS. Four different test cases are considered, each representing a distinct voltage conversion ratio $\overline{G}_v$: case i) $0.5\angle 0°$, case ii) $0.5\angle +30°$, case iii) $0.5\angle -30°$, and case iv) $0.6\angle 0°$. The converter design and controller parameters are given in Table 2. The sort and selection algorithm is used for balancing individual capacitor voltages within each arm.

A. STEADY-STATE PERFORMANCE

Steady-state simulation results for the four different voltage conversion ratios are presented in Fig. 9. The results demonstrate successful tracking of the desired output ac voltage magnitude and phase. In all cases, the arm currents consist of dc and fundamental frequency components and the input ac current has a zero phase relative to the input ac voltage, confirming input-side unity power factor operation. Capacitor voltages remain balanced at all times.

Common-mode arm currents $i_{\Sigma 1}$ and $i_{\Sigma 2}$ contain only a fundamental component, as expected given its relation to i_{aco} per (13). Differential-mode arm currents $i_{\Delta 1}$ and $i_{\Delta 2}$ contain mainly the circulating dc component (I_{dc}) superimposed with a fundamental frequency component depending on the designed $\overline{G}_v$. Specifically, $i_{\Delta 1}$ and $i_{\Delta 2}$ are purely dc valued at $\overline{G}_v = 0.5\angle 0°$ while an additional fundamental frequency component appears at $\overline{G}_v = 0.5\angle \pm 30°$ and $\overline{G}_v = 0.6\angle 0°$. This is consistent with (14). It is interesting to note that peak arm currents for the upper arms, i.e., $I_{peak,U}$, are 1.5, 1.46, 1.48 and 1.34 in p.u.[5] for cases i, ii, iii and iv, respectively. These are in good agreement with the expected values of 1.5, 1.46, 1.46. and 1.34 in p.u.[6] Similarly, $I_{peak,L}$ are 1.5, 1.66, 1.68 and 1 in p.u. for the four cases and are in line with expected values of 1.5, 1.66, 1.66 and 1 p.u.

In all four cases, the individual SM cap voltages are regulated to 2 kV but exhibit different peak-to-peak ripples depending on the designed $\overline{G}_v$. The filter capacitor voltages v_{F1} and v_{F2} contain both dc and fundamental frequency ripple

[5]Per-unitized with respect to $\hat{I}_{aci}/2 = 300\ A$ for $S_{in} = 6$ MVA, as i_{aci} is evenly distributed between the two phase legs.

[6]As per the theoretical analysis in Section II.

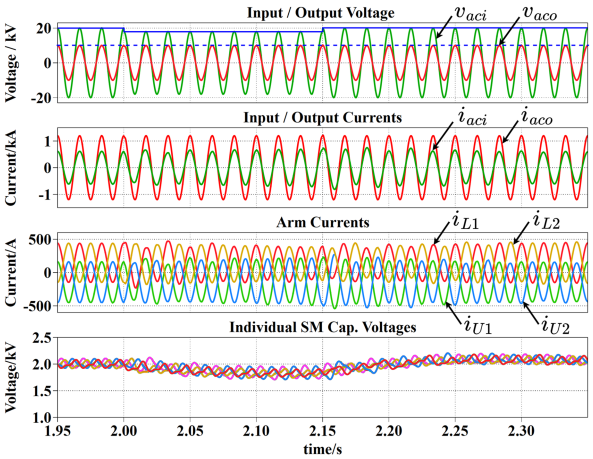

FIGURE 10. Simulation waveforms for 10% drop in $\hat{V}_{aci}$ when $\overline{G}_v = 0.5\angle 0°$.

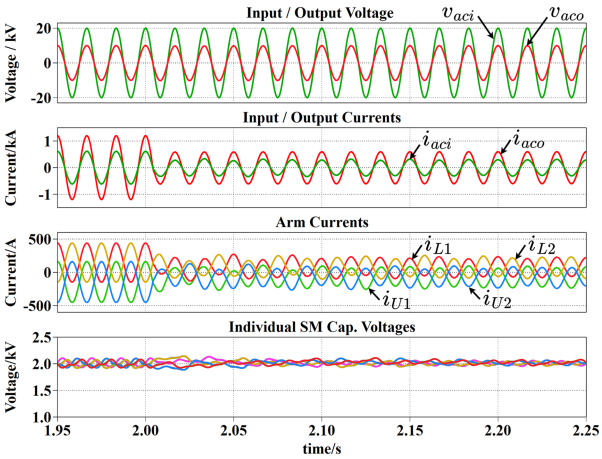

FIGURE 12. Simulation waveforms for 50% reduction in power transfer when $\overline{G}_v = 0.5\angle 0°$.

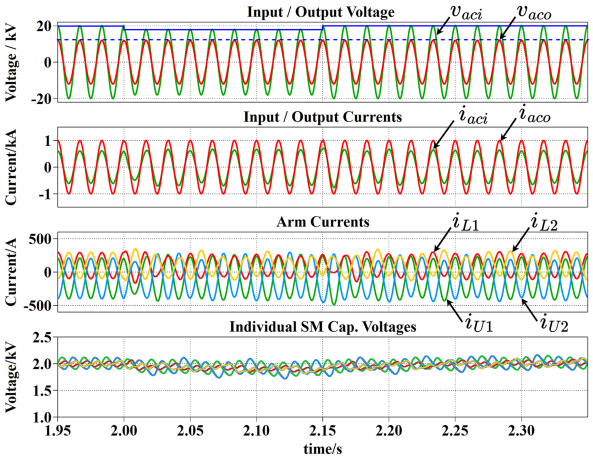

FIGURE 11. Simulation waveforms for 10% drop in $\hat{V}_{aci}$ when $\overline{G}_v = 0.6\angle 0°$.

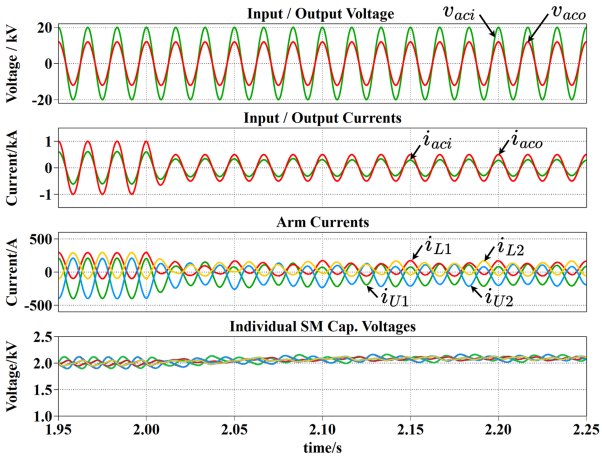

FIGURE 13. Simulation waveforms for 50% reduction in power transfer when $\overline{G}_v = 0.6\angle 0°$.

components as expected. These voltages are inherently balanced such that the dc component is equal to the dc voltage injected by the arms, V_{dc}, which varies with the designed $\overline{G}_v$. The ripple component depends on the load current. Overall, the steady-state waveforms in Fig. 9 confirm the M2AC with P3M can achieve single-stage ac/ac voltage conversion, including both voltage magnitude and phase changes. Moreover, the input and output ac terminals do not contain any unwanted dc components.

B. TRANSIENT PERFORMANCE

To assess the transient performance of the M2AC and the proposed control scheme, the following two scenarios are examined for the operating points of $\overline{G}_v = 0.5\angle 0^\circ$ and $\overline{G}_v = 0.6\angle 0^\circ$:

1) 10% step change reduction in v_{aci} while regulating v_{aco} constant, i.e., response to input voltage sag;
2) 50% step change reduction in power transfer, i.e., response to sudden load change.

Figs. 10 and 11 show the M2AC waveforms for a 10% drop in v_{aci} from $t = 2$ to $t = 2.15$ s for operating points $\overline{G}_v = 0.5\angle 0^\circ$ and $\overline{G}_v = 0.6\angle 0^\circ$, respectively. Despite the sudden supply voltage sag, in both cases, the M2AC successfully maintains the desired ac output voltage. These results confirm the proposed control strategy can counteract rapid variations in the ac line voltage. This is something not possible with traditional tap-changing transformers or shunt capacitor banks.

Figs. 12 and 13 show the M2AC waveforms for a 50% reduction in ac power transfer, initiated at $t = 2$ s, for operating points $\overline{G}_v = 0.5\angle 0^\circ$ and $\overline{G}_v = 0.6\angle 0^\circ$, respectively. Since the output voltage is regulated to be constant, the change in power flow is achieved by imposing a step change in load resistance. Consequently, in both cases, the input and output ac currents decrease by half, aligning with the decrease in delivered power. During this transient, the arm currents are also adjusted accordingly via control action, i.e., $i_{\Sigma 1}$ and $i_{\Sigma 2}$ are halved due to the reduction in load current, and the dc components of $i_{\Delta 1}$ and $i_{\Delta 2}$ are also halved as the internal power processing is halved according to (22).

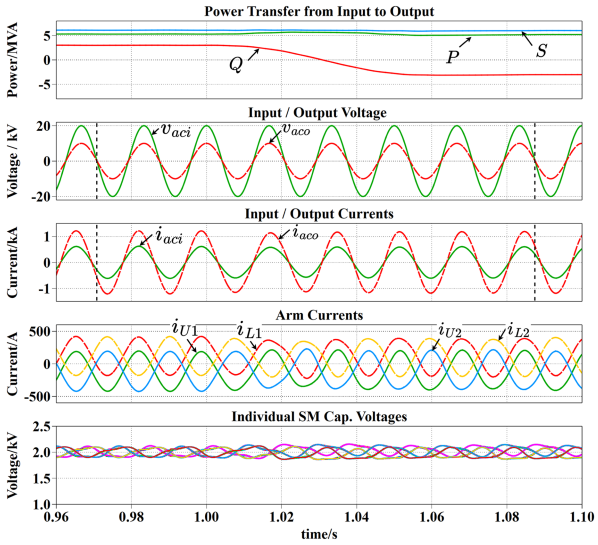

FIGURE 14. Positive active power transfer (input to output) with reactive power transfer changed from positive (load consuming reactive power) to negative (load injecting reactive power).

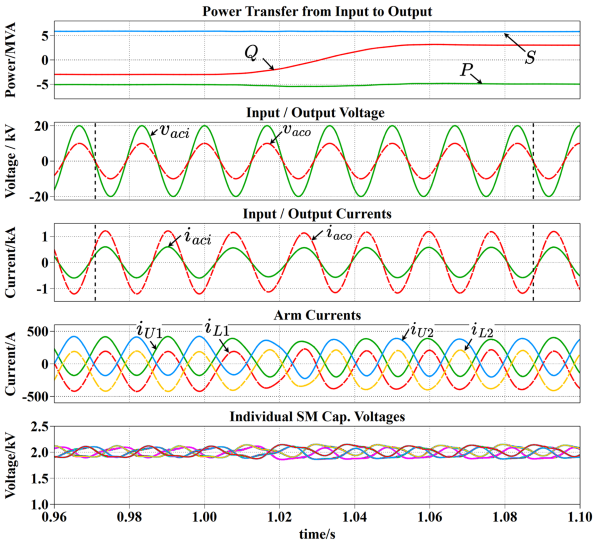

FIGURE 15. Negative active power transfer (output to input) with reactive power transfer changed from negative (load injecting reactive power) to positive (load consuming reactive power).

C. VALIDATION OF FOUR-QUADRANT POWER FLOW OPERATION

The earlier analyses and preceding simulations concentrated on the active power transfer capabilities of the M2AC to retain focus on key M2AC power transfer mechanisms while also simplifying the converter analysis. However, the proposed M2AC is indeed capable of four-quadrant operation given that it is an MMC-based structure employing standard HBSMs. To verify the M2AC's ability to operate in all four quadrants of the PQ-plane, this section presents simulation results for the operating point $\overline{G}_v = 0.5\angle 0^\circ$ where changes in direction of both active and reactive power transfers are imposed. The resistive load at the output is therefore replaced with an ac source. Note, that this requires deactivation of the input current phase correction controller in Fig. 8 so that the input and output terminals operate at the same power factor.

Fig. 14 illustrates a scenario in which 5.2 MW of active power (P) is transferred to the output. Simultaneously, the reactive power (Q) transfer shifts from 3 MVar (load consumes reactive power) to -3 MVar (load injects reactive power), while maintaining a power factor of 0.866 and a total apparent power (S) of 6 MVA. In a similar manner, Fig. 15 illustrates a scenario in which 5.2 MVA of active power is transferred from the output to the input (reverse), and the reactive power transferred from the input to the output changes from -3 MVar to 3 MVar, confirming the four-quadrant operational capability of M2AC.

V. EXPERIMENTS

To confirm the practical efficacy of the M2AC in Fig. 2(a) and its novel P3M, several experimental tests are conducted on a laboratory scale 1.25 kW, 250 V_{pk} prototype. The experimental setup is shown in Fig. 16, adopting the passive filter of Fig. 2(b). Experimental parameters are given in Table 3. For consistency with the simulation study, the same four M2AC design cases are considered: $\overline{G}_v = [0.5\angle 0^\circ, 0.5\angle +30^\circ, 0.5\angle -30^\circ, 0.6\angle 0^\circ]$. Four HBSMs from Imperix are used per arm (total of 16 HBSMs). The nominal capacitor voltage in the experiment varies depending on the designed $\overline{G}_v$. This is a slightly different design strategy from simulation, where, due to the much larger number of HBSMs, the nominal capacitor voltage was instead kept the same and the number of HBSMs was varied depending on $\overline{G}_v$. The controls in Fig. 7 are implemented on the Imperix boom-box real-time controller platform, using the control gains listed in Table 3. An NHR 9410-12 grid simulator served as the input voltage source and the output is connected to a resistive load bank.

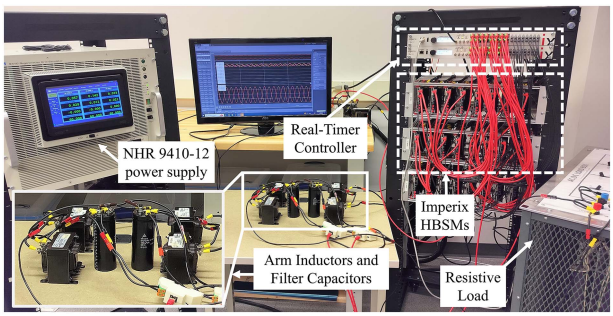

FIGURE 16. Experimental Setup.

A. STEADY-STATE PERFORMANCE

Fig. 17 plots the steady-state experimental waveforms obtained for all four voltage conversion ratios. The output voltages are regulated as desired in each case while maintaining the unity power factor at the input terminals. These

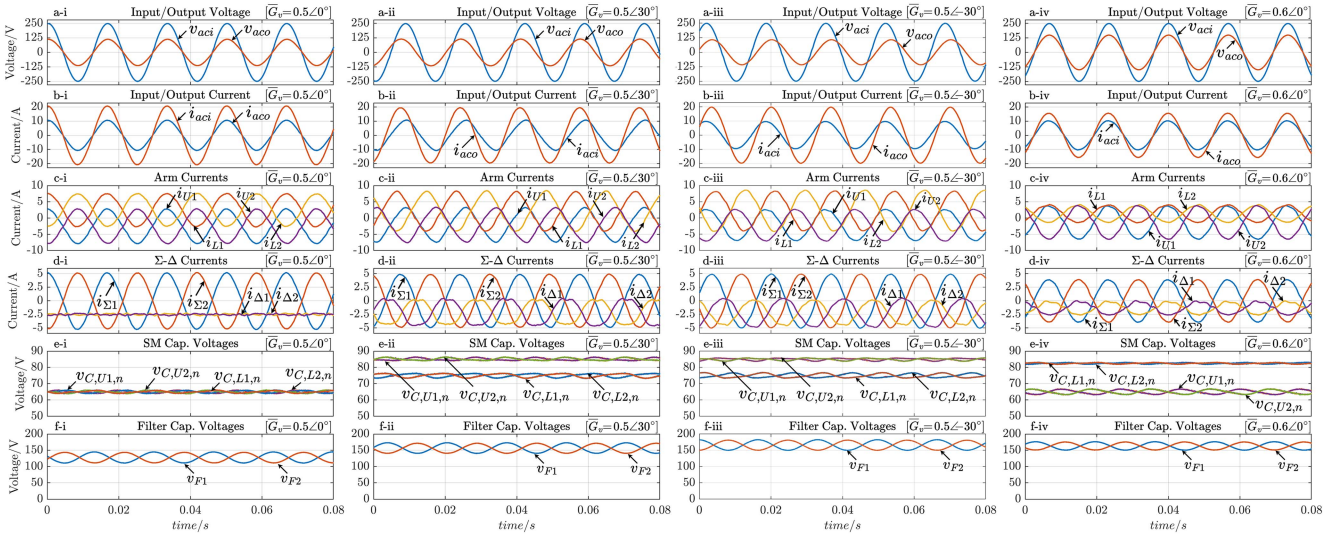

FIGURE 17. Steady-state experimental waveforms: (a) Input/output voltage, (b) Input/output Current, (c) Arm currents, (d) Arm currents decoupled into $\Sigma - \Delta$, (e) SM cap. voltage and (f) Filter cap. voltage for the operating points of $\overline{G}_v = 0.5\angle 0°$, $\overline{G}_v = 0.5\angle +30°$, $\overline{G}_v = 0.5\angle -30°$, $\overline{G}_v = 0.6\angle 0°$.

TABLE 3. Experimental Parameters

Converter parameter	Value		
Power Rating, S_{in}	6 MVA		
Input voltage peak, $\hat{V}_{aci}$	20 kV		
SM Cap. voltage, V_c^{ref}	2 kV		
Conversion ratio, $\overline{G}_v$	$0.5\angle 0°$	$0.5\angle \pm 30°$	$0.6\angle 0°$
Output voltage mag., $\hat{V}_{aco}$	10 kV	10 kV	12 kV
SMs in upper arm, n_U	10	13	13
SMs in lower arm, n_L	10	12	12
Arm inductance, L_a	26 mH		
SM capacitance, C_{SM}	3 mF		
Filter capacitance, C_F	1500 μF		
Control parameter	**Value**		
$k_{r2}, k_{p1}, k_{i1}, k_{r1}, \alpha_1, \alpha_2$	$290, 22, 1650, 1320, 1077, 527$		
$k_{p2}, k_{i2}, k_{r3}, \beta_1, \beta_2$	$0.045, 0.1, 600, 91, 1840$		
$k_{p4}, k_{i4}, k_{p3}, k_{i3}$	$0.1, 5, 0.4, 1.4$		
$k_{r4}, \gamma_1, \gamma_2$	$610, 350, 3600$		
k_{p5}, k_{i5}	$0.1, 1.5$		

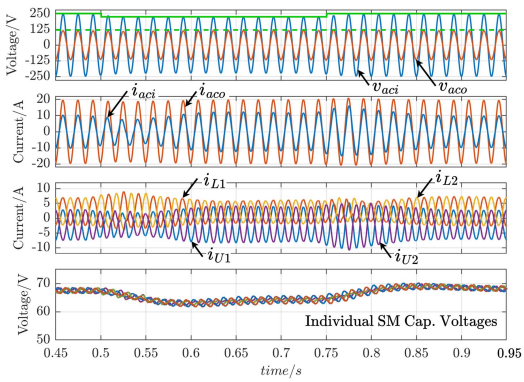

FIGURE 18. Experimental waveforms for 10% drop in $\hat{V}_{aci}$ when $\overline{G}_v = 0.5\angle 0°$.

waveforms show close agreement with their simulated (distribution level) counterparts in Fig. 9.

At all the operating points, arm currents predominantly carry a fundamental component and a dc current. Decoupled $\Sigma - \Delta$ currents clearly show that the currents $i_{\Sigma 1}, i_{\Sigma 2}$ carry one-fourth of the output current while $i_{\Delta 1}, i_{\Delta 2}$ contains the circulating dc current I_{dc} and a fundamental ac component that depends on $\overline{G}_v$. All these currents are well aligned with the simulations and the theoretical analysis when compared on the p.u. basis. Additionally, for all four voltage conversion ratios, the SM capacitor voltages of the upper and lower arms in Fig. 17 are maintained balanced at their respective nominal average values (see Table 3). Furthermore, as expected, the filter capacitors were inherently balanced corresponding to the dc component of arm voltage. Additionally, an ac ripple is present, with its magnitude dependent on the load current.

B. TRANSIENT PERFORMANCE

The two transient scenarios considered in the simulation study for $\overline{G}_v = 0.5\angle 0°$ are also replicated in the experiments to assess the practical dynamic performance of the M2AC. Fig. 18 shows experimental waveforms for the scenario where v_{aci} amplitude is suddenly reduced by 10% at t = 0.5 s and restored after 250 ms. Observe output voltage v_{aco} is unaffected. During this input voltage sag, the individual SM capacitor voltages momentarily decrease but the controllers quickly bring them back to their nominal values. Fig. 19 shows the experimental M2AC response when the ac power transfer is abruptly reduced by 50% via a step-change in load resistance at $t = 0.5$ s. In both scenarios, the proposed dynamic controls

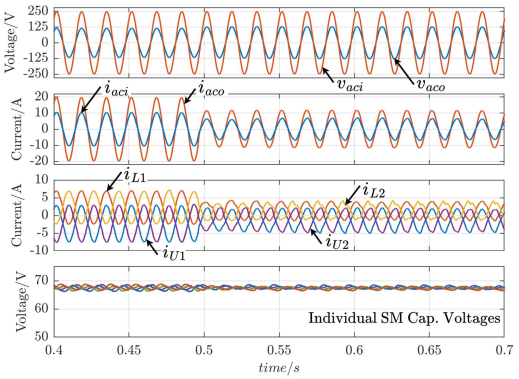

FIGURE 19. Experimental waveforms for 50% reduction in power transfer when $\overline{G}_v = 0.5\angle 0°$.

successfully maintain a fixed ac output voltage despite the input and load side disturbances. These experimental tests closely match the general response of their simulated counterparts in Figs. 10 and 12.

VI. CONTRAST WITH THE BACK-TO-BACK MMC

The M2AC represents a new class of ac/ac MMC that, unlike existing direct and indirect ac/c MMCs, employs a P3M to render input-to-output ac voltage transformation. It is somewhat analogous to a power electronic autotransformer that can adjust both ac grid voltage magnitude and phase. The closest counterpart to the M2AC is the conventional BTB-MMC, given they both use only HBSMs and are naturally suited for single frequency power system applications. This stems from the structural similarities in their basic building blocks, see Fig. 1(a) and (d).

A. THEORETICAL COMPARISON

This section contrasts the M2AC in Fig. 2(a) (and Fig. 3) with a single-phase version of the BTB-MMC, shown in Fig. 20 [21], as a benchmark for comparison. Both topologies employ a total of 4 phase arms (two phase legs) for transferring power between input and output. The emphasis is on transformerless voltage conversion. The minimum semiconductor requirements of both converters are determined based on the measure of semiconductor effort, λ, which assesses the collective effect of the peak voltage and current stresses in all the arms. This metric quantifies the total sum of all semiconductors' power ratings on a p.u. basis, normalized by the peak input power

$$\lambda = N_S * \sum_{n=1}^{n=N_{arms}} \left[\frac{V_{peak,n}\, I_{peak,n}}{\hat{V}_{aci}\, \hat{I}_{aci}} \right], \tag{28}$$

where N_S is the number of semiconductors in a single SM, e.g., 2 IGBTs in an HBSM, and N_{arms} is the total number of arms. Peak arm voltages (i.e., $V_{peak,U}$ and $V_{peak,L}$) and peak arm current stresses (i.e., $I_{peak,U}$ and $I_{peak,L}$) of the M2AC were previously discussed in Section II-E they depend on $\overline{G}_v$.

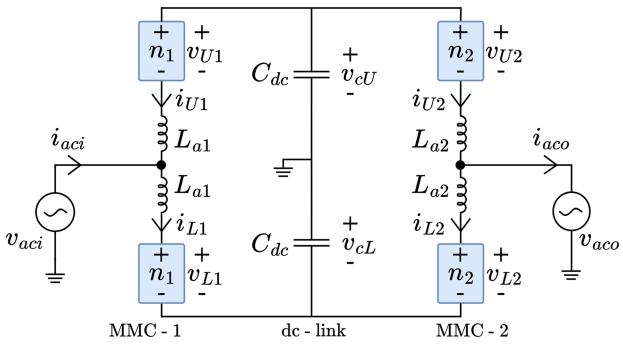

FIGURE 20. Single phase BTB-MMC topology used for the comparison.

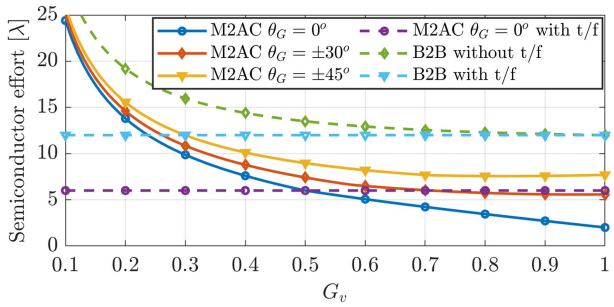

FIGURE 21. Semiconductor efforts of M2AC and the BTB-MMC.

For the BTB-MMC in Fig. 20, the arm voltages and currents of the input-side phase leg do not change with $\overline{G}_v$, as the input side voltage and power are fixed. However, the arm voltages and currents of the output-side phase leg vary depending on the desired ac voltage at the output.

The p.u. semiconductor efforts of the M2AC (λ_{M2AC}) and BTB-MMC (λ_{BTB}) as functions of G_v are illustrated in Fig. 21. The BTB-MMC results do not depend on output voltage phase shift θ_G. However, as seen in Fig. 5, the operating θ_G impacts the M2AC arms' voltages and currents. Therefore, θ_G values up to ±45° are considered for the M2AC, which is sufficient for applications requiring control of ac line power flows. The results show the M2AC possesses a significantly lower λ value when compared to the BTB-MMC for the considered operating points. This is due to the P3M employed by the M2AC. For transformerless operation at $G_v = 0.5$, λ_{M2AC} is 6, 7.4 & 9 p.u for a θ_G of 0, ±30 & ±45°, respectively, as compared to λ_{BTB} of 13.5 p.u. for the BTB-MMC. This represents a considerable reduction in semiconductor effort. Furthermore, potentially significant savings in associated operating losses can also be realized.

Fig. 21 also plots the total semiconductor effort assuming the BTB-MMC and M2AC employ ac transformers at their outputs with nominal turns ratios of $1 : G_v$ and $1 : 2G_v$, respectively. That is, the converters are designed with constant output-to-input voltage ratios of 0.5 for M2AC and 1 for BTB-MMC. These are given by the dotted light blue and purple lines. Considering this transformer assisted voltage

TABLE 4. Summary of Transformerless Voltage and Frequency Conversion Capabilities Between M2AC and BTB-MMC

Parameter	M2AC	BTB-MMC
Voltage ratio, $\lvert\overline{G}_v\rvert$	down to around 0.3	around 1
Voltage phase-shift, θ_G	0 to around $\pm 45°$ at $\lvert\overline{G}_v\rvert = 0.3$	any
Frequency at input/output	same	same or different

conversion, the M2AC has a 50% lower λ across all possible step ratios for $\theta_G = 0°$ (6 compared to 12 p.u).

The BTB-MMC can operate with any phase shift θ_G between input and output ac terminal voltages. It does not impact the required total semiconductor effort. This is an advantage of using two full-rated dc-ac MMCs decoupled via a dc link. However, due to its autotransformer type structure, the M2AC's semiconductor effort goes up as the designed range of θ_G increases. This is apparent from Fig. 21. The M2AC always has lower semiconductor effort compared to the BTB-MMC. The relative reduction is more pronounced as $\lvert\overline{G}_v\rvert$ approaches unity. In Fig. 21, the M2AC's semiconductor effort at $\overline{G}_v = 0.3\angle\pm 45°$ is approximately equal to the minimum semiconductor effort for the BTB-MMC that occurs at $\lvert\overline{G}_v\rvert = 1$. Therefore, for transformerless voltage conversion, the M2AC is best suited (or more cost-effective) for output-to-input voltage ratios down to around 0.3 while the BTB-MMC quickly becomes cost-prohibitive as the voltage ratio starts to drop below 1. It should be noted that while θ_G is practically limited to around $\pm 45°$ at $\lvert\overline{G}_v\rvert = 0.3$ for the M2AC to be cost-effective, this limit will increase somewhat as $\lvert\overline{G}_v\rvert$ increases. In other words, for $\lvert\overline{G}_v\rvert >> 0.3$, θ_G can cost-effectively be designed to be greater than $\pm 45°$. It is also important to point out that while the BTB-MMC can accommodate different or same frequency operation between input and output terminals, the M2AC is intended for same frequency operation only. This is a consequence of the P3M described in Section II-D.

Based on the above discussion, a summary of the voltage and frequency conversion capabilities of the M2AC and BTB-MMC is provided in Table 4.

B. SIMULATION STUDY OF BTB-MMC

A simulation study of the BTB-MMC is carried out here to substantiate the analyses in the preceding section. It also permits the study of other case study specific features such as capacitor voltage ripple variation and total capacitive energy storage requirements for comparison with the M2AC. A detailed switched model of the single-phase BTB-MMC in Fig. 20 was developed and simulated in PLECs for two different operating points: $\overline{G}_v = 1\angle 0°$ and $\overline{G}_v = 0.5\angle 0°$. Table 5 lists the parameters for the BTB-MMC model, which are chosen to be consistent with the M2AC design for $\overline{G}_v = 0.5\angle 0°$ in Table 2. The BTB-MMC for $\overline{G}_v = 1\angle 0°$ uses identically rated SMs as compared to the M2AC design for $\overline{G}_v = 0.5\angle 0°$, however, the BTB-MMC design for $\overline{G}_v = 0.5\angle 0°$ requires the SM capacitance of MMC-2 to be twice that of MMC-1

TABLE 5. Simulation Parameters of Single-Phase BTB-MMC

Converter parameter	Value	
Power rating, S_{in}	6 MVA	
Input voltage peak, $\hat{V}_{aci}$	20 kV	
SM Cap. voltage, V_c^{ref}	2 kV	
Conversion ratio, $\lvert\overline{G}_v\rvert$	$G_v = 1$	$G_v = 0.5$
Output voltage mag., $\hat{V}_{aco}$	20 kV	10 kV
SMs in an arm of MMC 1, n_1	20	20
SMs in an arm of MMC 2, n_2	20	15
SM capacitance in MMC-1	3 mF	3 mF
SM capacitance in MMC-2	3 mF	6 mF
Arm inductance in MMC-1, L_{a1}	26 mH	26 mH
Arm inductance in MMC-2, L_{a2}	26 mH	13 mH
DC-link capacitance, C_{dc}	375 μF	

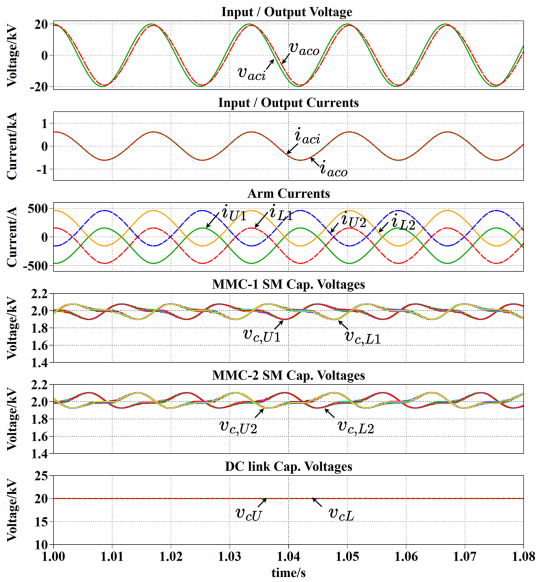

FIGURE 22. Steady-state simulation waveforms of BTB-MMC for the operating point $\overline{G}_v = 1\angle 0°$.

to maintain the same p.u. ac voltage ripple. This is because the ac current at MMC-2 is doubled (relative to MMC-1) due to the voltage ratio $\lvert\overline{G}_v\rvert = 0.5$. Also for this reason, the arm choke inductance for MMC-2 is reduced by half to yield the same p.u. ac voltage drop. The SM capacitances in Table 5 impose the same p.u. ac voltage ripple as the M2AC simulations, thus ensuring a fair and equitable comparison. Also, the dc-link capacitance C_{dc} for the BTB-MMC is picked to yield the same total capacitive energy storage as the M2AC filter capacitance C_F in Table 2.

Simulation results of the single-phase BTB-MMC designed for $\overline{G}_v = 1\angle 0°$ are illustrated in Fig. 22. The waveforms for both MMC-1 and MMC-2 are identical to their counterparts in the M2AC that was designed for $\overline{G}_v = 0.5\angle 0°$, Fig. 9. Specifically, all arm currents have the same dc and fundamental frequency components and all SM capacitor voltages have the same p.u. ac voltage ripple. The only difference is the dc link

TABLE 6. Comparison of Capacitive Energy Storage Requirements for M2AC and BTB-MMC

	M2AC	BTB-MMC	
	$\overline{G}_v = 0.5\angle 0°$	$\overline{G}_v = 1\angle 0°$	$\overline{G}_v = 0.5\angle 0°$
E_{arm}	**1 p.u.**	2 p.u.	**2.5 p.u.**
E_{filter}	**1.5 p.u.**	—	—
$E_{dc\text{-}link}$	—	—	**1.5 p.u.**
Total	**2.5 p.u.**	2 p.u.	**4 p.u.**

The bold entities indicates better emphasis.

capacitors for the BTB-MMC do not carry any fundamental frequency current, since $i_{aci} = i_{aco}$ at $\overline{G}_v = 1\angle 0°$, while the M2AC filter capacitors must always carry i_{aco}. C_F for the M2AC is sized to maintain the same p.u. ac voltage ripple as in the SM capacitors. It is important to point out that for the same 6 MW of power transfer, the BTB-MMC at $\overline{G}_v = 1\angle 0°$ requires twice the number of identically rated SMs per arm relative to the M2AC at $\overline{G}_v = 0.5\angle 0°$ (20 vs. 10). Therefore, at these operating points, the total semiconductor effort for the BTB-MMC is twice that of the M2AC, which aligns with Fig. 21 (12 vs. 6 p.u.). Moreover, since both topologies have equal arm current stresses and have equal SM capacitor voltage ripples, it can be concluded that: i) the BTB-MMC requires twice the total installed SM capacitive energy storage and ii) the BTB-MMC has twice the total switching and conduction losses associated with the semiconductors, and is therefore less efficient. However, the M2AC filter capacitors require 1.5 p.u. of energy storage to maintain a voltage ripple equivalent to that of the SM capacitors. The relative energy storage requirements between BTB-MMC and M2AC for these different voltage conversion ratios are summarized in Table 6 (see first 2 columns).

It is more useful to compare the M2AC and BTB-MMC for the same ac voltage conversion ratio. Therefore, Fig. 23 shows simulation results for the single-phase BTB-MMC designed for $\overline{G}_v = 0.5\angle 0°$. These waveforms can be directly compared to their M2AC counterparts in Fig. 9 (first column of subplots) that are for the same voltage ratio. The arm currents and SM capacitor voltages in the M2AC and MMC-1 of the BTB-MMC are identical. However, the ac component of the arm currents in MMC-2 is now doubled, resulting in overall higher arm current stresses. This results in even lower efficiency than the $\overline{G}_v = 1\angle 0°$ case discussed above. The required number of SMs in MMC-2 is 25% less since the peak arm voltage stress is 25% less. However, since the capacitance of SMs in MMC-2 is twice as much as MMC-1, the total capacitive energy storage of the SMs in the BTB-MMC is equal to 2.5 p.u. Moreover, at this operating point, the BTB-MMC requires the inclusion of dc-link capacitors to accommodate the difference in fundamental frequency current between input and output. To maintain a ripple on these dc-link capacitors equivalent to that of the SMs, an additional 1.5 p.u. of energy storage is needed, resulting in a total of 4 p.u. capacitive energy storage. These energy storage requirements are summarized in Table 6

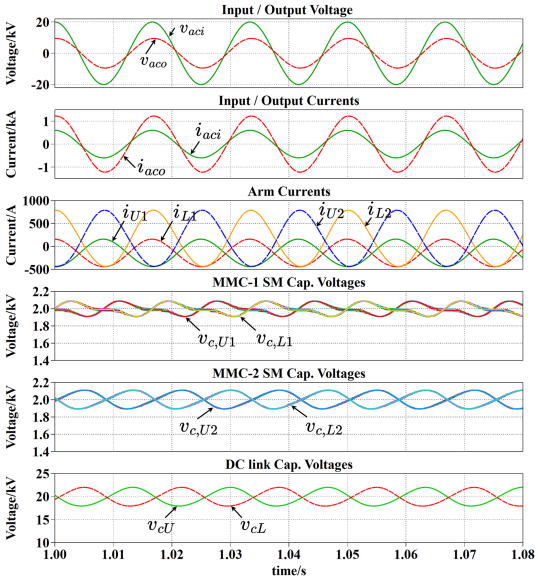

FIGURE 23. Steady-state simulation waveforms of BTB-MMC for the operating point $\overline{G}_v = 0.5\angle 0°$.

(see third column). Comparing the first and third columns in Table 6 indicates the single-phase M2AC has lower total capacitive energy storage requirements relative to the single-phase BTB-MMC. This implies the total volume occupied by the SM capacitors and filter capacitors in the M2AC would be commensurately less than the total volume occupied by the SM capacitors and dc-link capacitors in the BTB-MMC. It should be noted the BTB-MMC in Fig. 20 could potentially eliminate the need for dc-link capacitors by using two phase legs for each MMC, however, this would require a more complex structure with double the number of phase legs.

VII. CONCLUSION

This article presents a new class of MMC, the M2AC, which allows direct ac/ac voltage conversion by capitalizing on internally circulating dc currents to satisfy the charge balance of its half-bridge submodule capacitors. This novel P3M can achieve output voltage magnitude and phase shifting in single frequency power systems without using a transformer or multiple conversion stages. Contrasting the M2AC with the established BTB-MMC, its closest counterpart, indicates that substantial savings in semiconductor effort can be realized for output-to-input voltage ratios down to around 0.3 at $\pm 45°$ phase shift. Therefore, the M2AC offers an alternative approach to ac voltage conversion that may be attractive for certain distribution and transmission applications, primarily where power flow control and voltage regulation are key objectives. The M2AC structure and P3M are analyzed and modeling results are used to develop a dynamic control scheme. PLECS simulation studies and extensive experimental tests conducted on a 1.25 kW prototype confirm the practical efficacy of the M2AC and its P3M. Suggested future works include exploring active filtering at the output and extending the M2AC analysis to three-phase study systems.

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