Multi-Pulse Si-MOSFET Gate Driving Utilizing Gate Loop Inductance

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ABSTRACT   Gatedriving circuits are a crucial part of the safety, compliance, and performance of switched-mode power converters. Traditionally, these circuits use a single pulse and employ a gate resistor to control silicon (Si) MOSFETs. Unfortunately, the performance of this approach is limited by parasitic inductances, which can cause excessive oscillations, voltage stress, and catastrophic false turn-ON failures. As a result, power conversion applications typically sacrifice performance with respect to increased transient times and switching losses to maintain safe operation. This work proposes a simple multi-pulse (MP) driving sequence that enables reduced transient times and switching losses while keeping oscillations and voltage stress low. With this, the performance can be increased while upholding safety margins of the switched-mode power converter. The concepts and derived equations are verified by circuit simulations and experiments showcasing up to 25% loss reduction in the driver-stage, up to .2% efficiency improvement in the power-stage, and up to 18X oscillation amplitude reduction compared to the conventional approach. Moreover, the proposed sequence and driving circuit achieve reliable operation in extreme slew-rate conditions beyond the capabilities of the traditional approach, resulting in voltage stress reduction and false turn-ON failure mitigation.

INDEX TERMS   Converters, gate drivers, MOSFET, power conversion, power electronics, power transistors, power semiconductor switches, power semiconductor devices, printed circuits, parasitics, semiconductor device modeling.

I. INTRODUCTION

Gate driving circuits are an essential component in switched-mode power converters. These circuits control the power semiconductor switching transition slew-rates, which tremendously influences most figures of merit in hard-switched applications, including efficiency, electromagnetic compatibility (EMC), and electromagnetic interference (EMI). Conventional gate driving (CGD) circuits for silicon (Si) MOSFETs utilize a single pulse with a gate resistor (R_G) to control turn-ON and turn-OFF slew-rates and transients of the power switch. One drawback of this approach is the slew-rate limitation through parasitic inductances (L_{Par}), as the single pulse and L_{Par} can cause significant oscillations and voltage stress in the gate commutation loop, which may result in catastrophic false turn-ON failures. Thus, R_G needs to provide minimum damping to ensure safe operation by maintaining reasonable levels of voltage stress and oscillations. This minimum

damping requirement typically results in performance degradation as transient times and consequently efficiency is reduced. With respect to the ongoing demand in high efficiency for hard-switched applications, it is paramount to explore driving solutions that improve efficiency while ensuring safe operation.

Various gate-driving contributions have been proposed to improve the performance and safety of power switches in hard-switched applications with respect to efficiency, voltage stress, and oscillations. A common approach to improve performance and safety is the minimization of L_{Par} [1], [2], [3], which is effective but limited by thermal, mechanical, and cost constraints. Another promising approach to overcome the minimum damping requirement and improve performance of CGD are active gate drivers (AGD), which are able to generate non-linear driving signals by adjusting either their internal resistance [4], [5], [6], or gate voltage [7], [8], [9], or gate

current [10], [11], [12]. However, a common problem with AGDs is the added complexity through either multiple stages [4], [5], [6], [7], [8], [9], external components to form a resonant circuit [10], [11], [12], or both. Other approaches focus on improving the efficiency and safety of the hard-switched application by actively suppressing false turn-ON failures via clamping circuits [13], [14], [15], with the draw-back of added complexity. Overall, numerous gate-driving contributions address performance and safe operation of the power switch in hard-switched applications. Yet, a simple driving solution that allows swift transient times and low switching losses while simultaneously providing reduced oscillations in the gate circuitry, resulting in increased safety margins with respect to false turn-ON failures is lacking in the literature.

In this paper, a simple multi-pulse (MP) driving sequence is proposed, which enables various benefits for Si-MOSFETs. The benefits of the proposed method include a simple driving sequence employed by a fundamental half-bridge topology, which enables high slew-rate operation with the consequent improvements in efficiency while maintaining low voltage stress and oscillations in the gate circuitry. In particular, the proposed MP-Sequence consists of a simple switching pattern described by two pulses, namely the A-pulse (t_A), the B-pulse (t_B), which create a specific charge and discharge of the resonant tank formed by the input capacitance (C_{iss}) and the parasitic inductances participating in the gate commutation, represented by the gate loop inductance (L_G). Fig. 1 depicts the proposed approach and the traditional approach including the driving voltage (v_{DR}), the power switch (S), the driving switches of the half-bridge (Q_1 and Q_2), the drain current (i_D), the drain-source voltage (v_{DS}), the gate-source voltage (v_{GS}), the gate current (i_G), switching losses (P_{SW}), t_A, t_B, C_{iss}, R_G, and L_{Par}. It can be seen in Fig. 1(a) that the traditional turn-ON and turn-OFF approach applies a single pulse to v_{DR} and R_G to charge and discharge C_{iss}, with the consequent under- or overdamped responses in v_{GS} for low and high values of R_G respectively. On the one hand, the underdamped response results in a fast commutation with low switching losses at the cost of significant voltage stress and oscillations in v_{GS}, which leads to a turn-ON failure in i_D and v_{DS}. On the other hand, the overdamped response results in a slow commutation with large switching losses, with the benefit of reduced voltage stress and oscillations in v_{GS}. Further, Fig. 1(b) illustrates the proposed method, including the multi-pulse (MP) driving sequence applied to v_{DR} described by t_A and t_B, which in contrast to the traditional approach achieves reduced voltage stress and oscillations in v_{GS} while operating at high slew-rates of v_{DS} and i_D with consequent low switching losses. Overall, the proposed MP-Sequence utilizes a fundamental driver architecture and simple switching pattern, which achieves fast transient times while providing reduced voltage stress and less oscillations in the gate circuitry. The main advantages of the proposed MP driving sequence are summed up as:
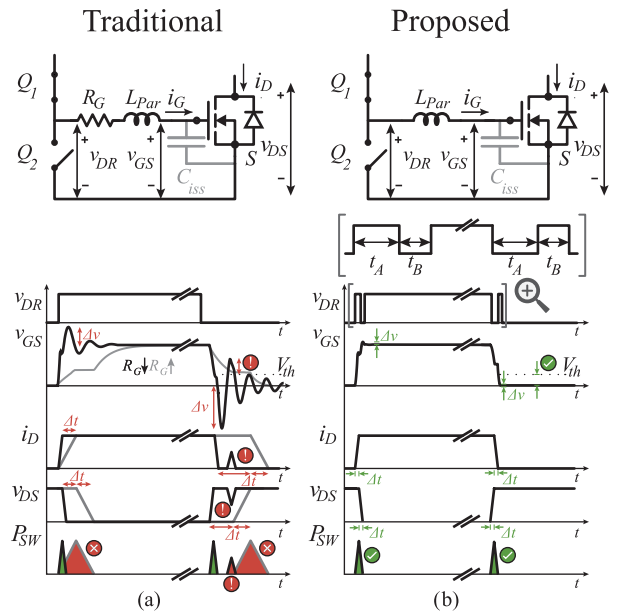- Reduced oscillations in gate circuitry

FIGURE 1. Gate driving strategies: (a) Traditional driving with gate resistor (R_G) and single pulse operation of v_{DR} with over- and underdamped transient responses and consequent oscillations in v_{GS}, false turn-ON failure, and slow switching speeds in i_D and v_{DS}, and switching losses (P_{SW}) for the over- and underdamped case respectively; (b) Proposed approach utilizing parasitic inductance L_{par} with the multi-pulse sequence applied to v_{DR} resulting in minimal oscillations in v_{GS} and rapid commutation times of i_D and v_{DS} while mitigating false turn-ON failures with the consequent low switching losses (P_{SW}).

- Capability of extreme slew-rate operation
- Increased efficiency of power- and driving stage
- Simple driving circuit architecture

The rest of the paper is structured as follows: In Section II the operating principle of the MP-Sequence is described in detail and the necessary steps to determine t_A and t_B are elaborated. Section III provides implementation guidance and investigates the influence of parameter tolerances. Section IV presents the experimental verification of the proposed method. Finally, Section V concludes the paper, highlighting the key contributions of this work.

II. MULTI-PULSE DRIVING SEQUENCE
In this section, the proposed Multi-Pulse (MP) driving sequence is described with the consequent pulse timings that charges and discharges L_G effectively, allowing v_{GS} to reach the target voltage swiftly, which results in reduced commutation times and oscillations in the gate circuitry as well as enhanced efficiency of the power stage. The determination of these timings is obtained with the aid of normalization, which allows for general solutions and simple graphical representation in the state plane.

In order to describe the MP-Sequence, which enables high slew-rates and efficiency with low oscillations and reduced voltage stress in the gate circuitry, the operating principle is illustrated Fig. 2. In particular, Fig. 2(a) displays the gate-drive circuit of the MP-Sequence, which operates at six given
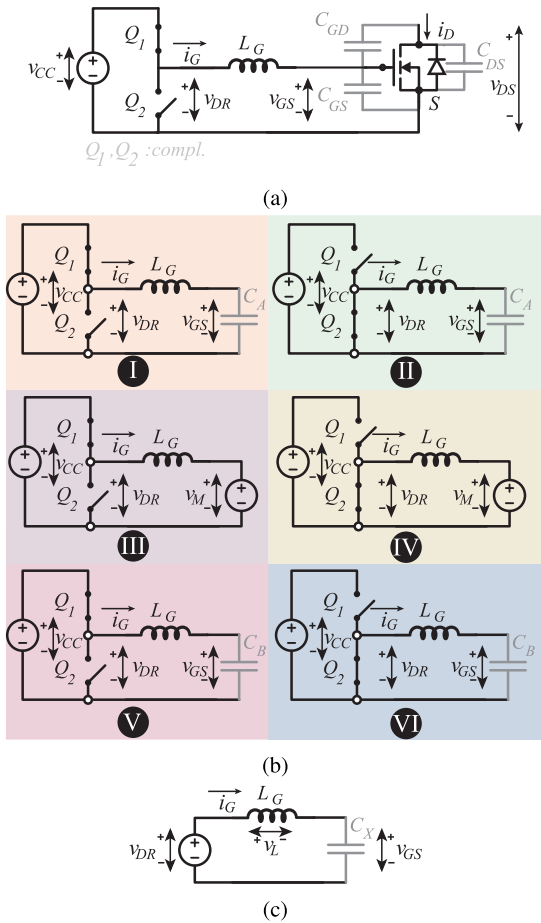
(a)

(b)

(c)

FIGURE 2. Operating principle of the proposed MP-Sequence: (a) Gate drive circuit; (b) Transient modes of the MP-Sequence: ON-A Ⓘ, OFF-A ⒾⒾ, ON-M ⒶⒶ, OFF-M ⒶⒶ, ON-B Ⓥ, OFF-B ⓋⒶ; (c) Equivalent circuit.

states depicted in Fig. 2(b). These states are labeled ON-A Ⓘ, OFF-A Ⓘ, ON-M Ⓘ, OFF-M Ⓘ, ON-B Ⓥ, and OFF-B Ⓥ. Each of these states can be represented with the equivalent circuit illustrated in Fig. 2(c), with corresponding values for v_{DR} and the equivalent capacitance (C_X) for each state described by

$$V_{DR} = \begin{cases} 0, & \text{Ⓘ, Ⓘ, Ⓥ;} \\ V_{CC}, & \text{Ⓘ, Ⓘ, Ⓥ;} \end{cases}$$

$$C_X = \begin{cases} C_A = C_{iss}, & \text{Ⓘ, Ⓘ;} \\ \infty, & \text{Ⓘ, Ⓘ;} \\ C_B = \frac{Q_T}{V_{CC}}, & \text{Ⓥ, Ⓥ;} \end{cases} \quad (1)$$

where Q_T is the total gate charge of the device, which can be obtained via the datasheet of the device, and V_{CC} is the supply voltage of the driver. According to the Kirchhoff voltage law the equivalent circuit can be represented by

$$v_L + v_{GS} = v_{DR} \quad (2)$$

which can be extended through the differential equations for v_L and v_{GS} to represent the dynamic behavior as

$$L_G \frac{di_G}{dt} + \frac{1}{C_X} \int i_G dt = v_{DR} \quad (3)$$

In order to obtain generality and simple representation of the dynamic behavior in the state plane, the time (t), voltages (v_x), currents (i_x), and charges (q_x) are normalized

$$t_{xn} = \frac{t_x}{T_{0x}}; \; v_{xn} = \frac{v_x}{v_{norm}}; \; i_{xn} = \frac{i_x}{i_{norm}}; \; q_{xn} = \frac{q_x}{q_{norm}} \quad (4)$$

where n indicates that the variables are normalized, and x is a placeholder for the corresponding variable. For instance, v_{GSn} represents the normalized gate-source voltage. The base quantities of the employed resonant tank are described by

$$T_{0X} = 2\pi \sqrt{L_G C_X}; \; Z_{0X} = \sqrt{\frac{L_G}{C_X}}; \; \omega_X = \frac{1}{\sqrt{L_G C_X}} \quad (5)$$

where T_{0X} is the period, Z_{0X} is the characteristic impedance, and ω_X the angular speed of the employed resonant tank respectively. The normalizing voltage, current, and charge are

$$v_{norm} = V_{CC}; \; i_{norm_X} = \frac{v_{norm}}{Z_{0X}}; \; q_{norm} = v_{norm} C_X \quad (6)$$

With the normalization and the relationships between q_n, i_{Gn} and v_{GSn} via

$$i_{Gn} = \frac{dq_n}{dt_n}; \; v_{GSn} = \frac{q_n}{C_X} \quad (7)$$

(3) can be rewritten as

$$\frac{d^2 q_n(t_n)}{dt_n^2} + \frac{q_n(t_n)}{L_G C_X} = \frac{v_{DRn}}{L_G} \quad (8)$$

Solving the general differential (8), results into the particular time-domain equations for v_{GSn} via (7) as

$$v_{GSn}(t_n) = A Z_{0X} sin(\omega_X t_n) + B cos(\omega_X t_n) + v_{DRn} \quad (9)$$

and for i_{Gn} via (7) as

$$i_{Gn}(t_n) = A cos(\omega_X t_n) - \frac{B}{Z_{0X}} sin(\omega_X t_n) \quad (10)$$

With $A = i_{Gn(0)}$, $B = v_{GSn(0)} - v_{DRn}$, where $v_{GSn(0)}$ is the initial voltage for v_{GSn}, and $i_{Gn(0)}$ is the initial current for i_{Gn}. Combining both equations to eliminate the time variable results in a circular state plane described by

$$i_{Gn}^2 + (v_{GSn} - v_{DR_n})^2 = i_{Gn(0)}^2 + (v_{GSn(0)} - v_{DR_n})^2 \quad (11)$$

With this, the transient behavior of all six MP-Sequence states (Ⓘ–Ⓥ) can be described via (9), (10) in the time domain and (11) in the state space.

A. MP TIMING INTERVALS

In this section, the timing of the MP-Sequence, which results in a swift commutation, high efficiency, and reduced oscillations in the gate circuitry is described. In particular, t_A and t_B are determined with the aid of the theoretical waveforms presented in Fig. 3. Through the use of symmetry, t_A and t_B
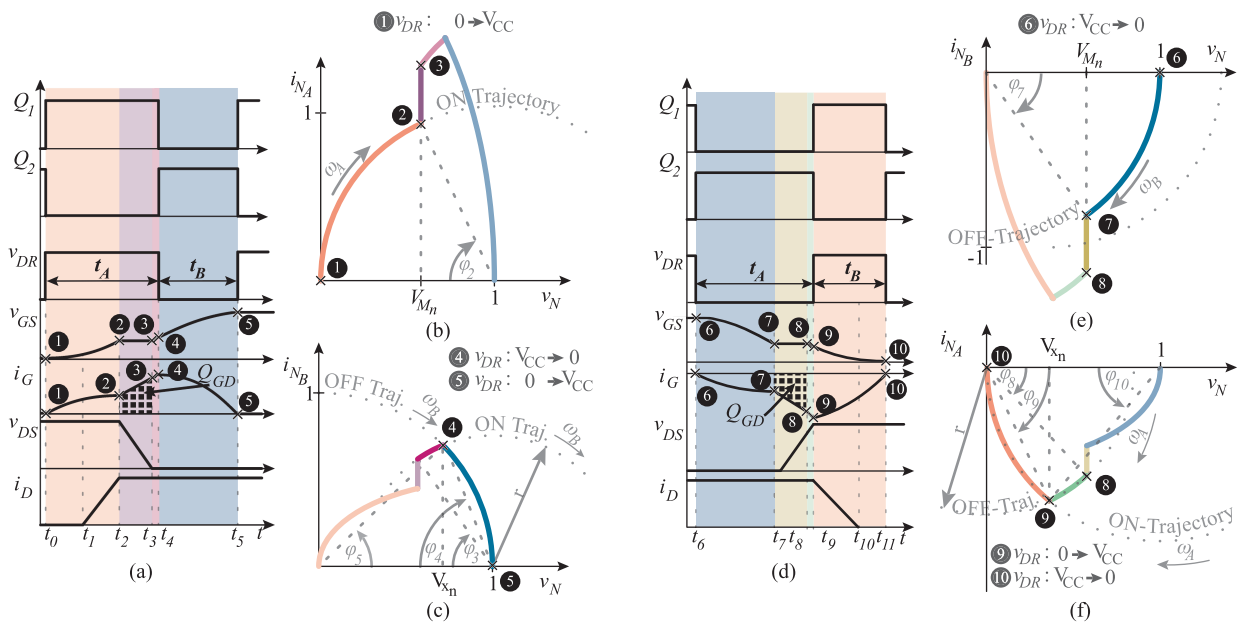
FIGURE 3. Theoretical waveforms and state planes of the proposed MP-Sequence: (a) waveforms of the turn-ON with turn-ON starting point ❶, Miller plateau entry point ❷, Miller plateau exit point ❸, turn-OFF point ❹, and turn-ON target point ❺; (b) turn-ON state plane normalized to i_{N_A}; (c) turn-ON state plane normalized to i_{N_B}; (d) turn-OFF time domain waveforms with turn-OFF start point ❺, Miller plateau entry point ❼, Miller plateau exit point ❽, turn-ON point ❾ and turn-OFF target point ❿; (e) turn-OFF state plane normalized to i_{N_B}; (f) turn-OFF state plane normalized to i_{N_A}.

are equivalent for turn-ON (see Fig. 3(a)) and turn-OFF (see Fig. 3(d)) as

$$t_A = t_{0-2} + t_{2-3} + t_{3-4} = t_{6-7} + t_{7-8} + t_{8-9}$$
$$t_B = t_{4-5} = t_{9-11} \tag{12}$$

What follows are the descriptions of the time intervals to determine t_A and t_B via the turn-ON Sequence, which is analog to the turn-OFF sequence as described in (12).

1) INTERVAL t_{0-2}

Prior to this interval, $V_{DR} = 0$ is applied to keep the device OFF. The interval begins at ❶ with $i_{Gn(0)} = 0$, and $v_{GSn(0)} = 0$ and uses stage **I**. This interval ends at ❷, where V_{GS} meets the Miller voltage (V_M), which is described by

$$V_M = V_{th} + \frac{i_D}{g_m} \tag{13}$$

at

$$t_{0-2} = \frac{acos(1 - V_{M_n})}{\omega_A} \tag{14}$$

where ω_A is the angular speed of the resonant tank with $C_X = C_A$, V_{th} is the threshold voltage, and g_m is the transconductance of the power switch.

2) INTERVAL t_{2-3}

This interval utilizes stage **III** and begins at ❷, with $i_{Gn(0)} = i_{Gn(t_2)}$, and $v_{GSn(0)} = V_{M_n}$. The initial current in this interval is given by

$$i_{Gn}(t_2) = i_{norm_A} sin(\omega_A t_{0-2}) \tag{15}$$

where i_{norm_A} is the normalized current considering the resonant tank with $C_X = C_A$. This interval ends at ❸ when the gate-drain charge (Q_{GD}) of the gate-drain capacitance is delivered by i_G via

$$Q_{GD} = \int_{t_2}^{t_3} i_G \, dt = i_G(t_2)t_{2-3} + 0.5t_{2-3}\Delta i_{23} \tag{16}$$

where

$$\Delta i_{23} \approx t_{2-3} \frac{V_{DR} - V_M}{L_G} \tag{17}$$

Consequently, (16) can then be rewritten, with (17) and the shorthand $M = (V_{DR} - V_M)/L_G$, as

$$Q_{GD} \approx I_g(t_2)t_{2-3} + 0.5t_{2-3}^2 M \tag{18}$$

resulting in

$$t_{2-3} \approx -i_G(t_2)/M + \sqrt{(i_G(t_2)/M)^2 + 2Q_{GD}/M} \tag{19}$$

3) INTERVAL t_{3-4}

This interval utilizes stage **V** and begins at ❸, with $i_{Gn(0)} = i_{Gn(t_3)}$, and $v_{GSn(0)} = V_{M_n}$. The initial current in this interval is determined by

$$i_{Gn}(t_3) = i_{Gn}(t_2) + \frac{\Delta i_{23}}{i_{norm_B}} \tag{20}$$

This interval ends at ❹, where the ON-Trajectory intersects with the desired OFF-Trajectory, that intersects with the target point. This OFF-Trajectory can be described via (11) as

$$i_{Gn}^2 + v_{GSn}^2 = 1 \tag{21}$$

TABLE 1. Simulation Parameter

Circuit Param.	Value	Device Param.	Value
V_{DS}	480 V	Q_T	45 nC
I_D	11 A	Q_{GD}	22 nC
V_{CC}	10 V	C_{iss}	1.2 nF

whereas the ON-Trajectory is described via (11) as

$$i_{Gn}^2 + (v_{GSn} - v_{DRn})^2 = i_{Gn(t_3)}^2 + (V_{M_n} - v_{DRn})^2 \quad (22)$$

The normalized intersecting voltage (V_{x_n}) can be found when combining (21) and (22) to

$$V_{x_n} = 1 - 0.5r^2 \quad (23)$$

where

$$r = \sqrt{i_{Gn(t_3)}^2 + (V_{M_n} - v_{DRn})^2} \quad (24)$$

With V_{x_n} determined, the length of this interval can be defined via the angular difference of the voltage vectors $v_{GSn}(t_3)$ and $v_{GSn}(t_4)$ (see Fig. 3(c)) through

$$t_{3-4} = \frac{\phi_4 - \phi_3}{\omega_B} = \frac{acos(\frac{1-V_{M_n}}{r}) - acos(\frac{1-V_{x_n}}{r})}{\omega_B} \quad (25)$$

where ω_B is the angular speed of the resonant tank with $C_X = C_B$.

4) INTERVAL t_{4-5}

This interval utilizes stage **VI** and begins at **❹**, with $i_{Gn(0)} = i_{Gn(t_4)}$, and $v_{GSn(0)} = V_{x_n}$. The initial current in this interval is determined by

$$i_{Gn}(t_4) = i_{Gn}(t_3) + i_{norm_B}sin(t_{3-4}\omega_B) \quad (26)$$

This interval ends at **❺**, where the target point for v_{GS_n} and i_{G_n} is reached. The time for this is determined by

$$t_{4-5} = \frac{acos(V_{x_n})}{\omega_B} \quad (27)$$

At the end of this interval, $V_{DR} = V_{CC}$ is applied to keep the device ON, which concludes the MP-Sequence, that enables rapid commutation times while maintaining low voltage stress and reduced oscillations in the gate circuitry, for the turn-ON. As described earlier, the turn-OFF is analog to the turn-ON described by (12) and thus the turn-OFF description is omitted for readability.

III. IMPLEMENTATION & SENSITIVITY ANALYSIS

In this section, the implementation as well as the operation and sensitivity to parameter variations of the previously developed MP-Sequence, which provides swift commutation times, low voltage stress, and reduced oscillations in I_{GS} and V_{GS}, is discussed. The following simulations are performed with LTSpice, a non-ideal power switch (SPP11N60C3XKSA1), and the parameters found in Table 1.
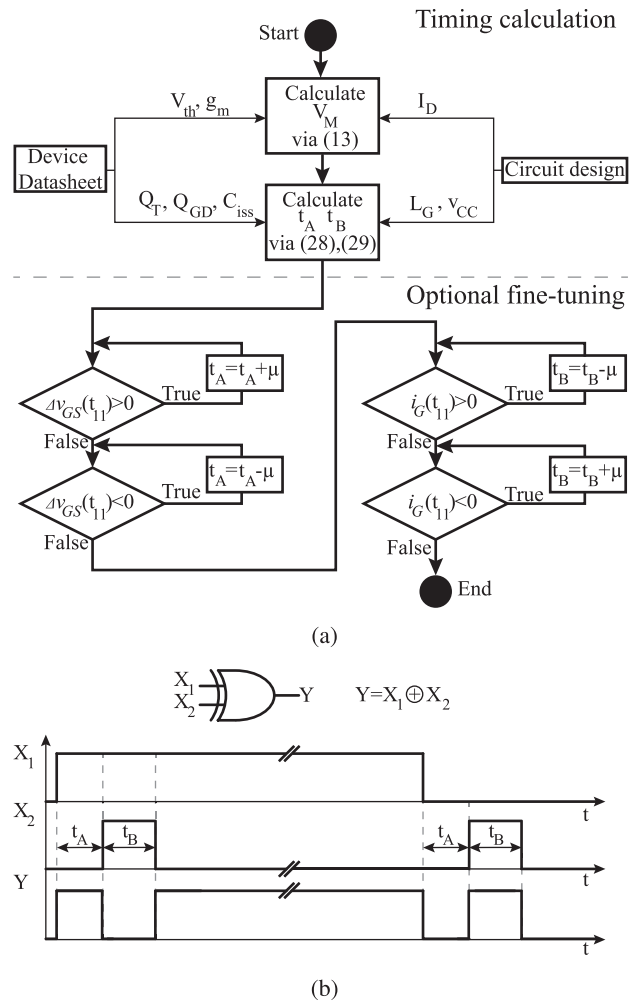

FIGURE 4. Implementation of the MP-Sequence: (a) Timing calculation flow chart with optional fine-tuning via incremental time adjustment (μ); (b) Signal diagram with simple Boolean algebra.

A. MULTI-PULSE IMPLEMENTATION

The MP-Sequence requires the determination of t_A and t_B as described by the equations in the previous section. For practicality, these equations can be simplified to the following approximations

$$t_A \approx \sqrt{L_G C_{iss}} \left(acos(1 - V_{Mn}) - \frac{\sqrt{2V_{Mn} - V_{Mn}^2}}{1 - V_{Mn}} \right)$$

$$+ \sqrt{\frac{2 L_G Q_{GD}}{V_{CC} - V_M} - \frac{L_G C_{iss} V_{CC}^2 (V_{Mn}^2 - 2V_{Mn})}{(V_{CC} - V_M)^2}} \quad (28)$$

$$t_B \approx \sqrt{L_G \frac{Q_T}{V_{CC}}} acos(V_{M_n}) \quad (29)$$

which allows for a simple implementation. With the help of these approximations, and (13) the implementation can be performed as illustrated in Fig. 4(a). As shown, the required parameters to estimate t_A and t_B can be extracted from
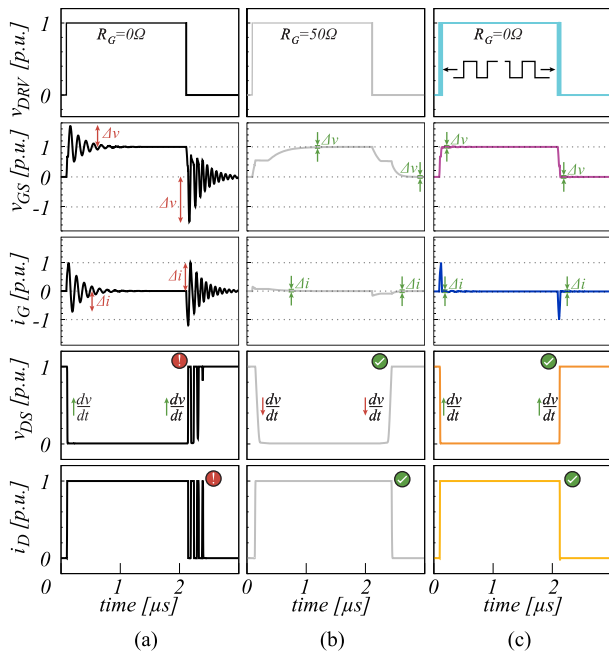
FIGURE 5. Comparison of the approaches with $L_G = 100nH$: (a) traditional underdamped approach resulting in significant oscillations in v_{GS} and i_G leading to catastrophic false turn-ON failures in v_{DS} and i_D during turn-OFF; (b) traditional overdamped approach leading to slow transients in v_{DS} and i_D; (c) proposed MP-Sequence with minimal oscillations in v_{GS} and i_G as well as safe operation while maintaining fast transients in v_{DS} and i_D.
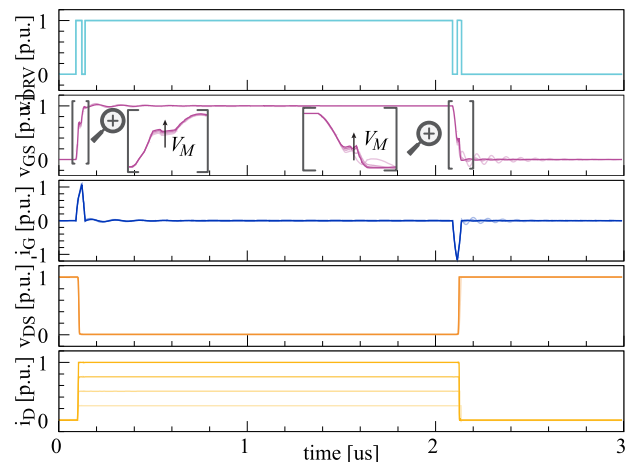

FIGURE 6. MP-Sequence with $L_G = 100nH$ under load variation: Maintaining stable operation across the whole loading range as the change in V_M with respect to i_D is incorporated into the MP-Sequence analysis.

the device datasheet and the circuit design. Moreover, the flowchart reflects how to fine-tune the timing with the help of the turn-OFF transient. In particular, t_A and t_B can be tuned via incremental time adjustments (μ) based on v_{GS} and i_G during the turn-OFF (see t_{11} in Fig. 3(d)). It is worthwhile mentioning, that the optional fine-tuning is performed offline, as the MP-Sequence operating with consistent timing achieves good performance across a wide operating range, which is demonstrated in the experimental section later on. Due to the simplicity of the MP-Sequence, it can be easily implemented in the logic unit of the application. Fig. 4 b depicts the implementation of the proposed MP-Sequence with one simple XOR gate combining the drive signal (X_1) with a defined signal (X_2) resulting to the desired MP-Sequence.

B. COMPARATIVE ANALYSIS
For comparison, the traditional approach and the proposed MP-Sequence have been simulated with $L_G = 100nH$.

Fig. 5 depicts the simulated waveforms of the proposed MP-Sequence, which enables swift commutation times while maintaining low voltage stress and reduced oscillations in the gate circuitry, in contrast to the traditional under- and overdamped responses. On the one hand it can be seen that the traditional underdamped response results in swift commutation times but suffers from excessive voltage stress and large oscillations, which lead to multiple false turn-ON failures as seen in v_{DS} and i_D. On the other hand, the traditional overdamped response results in slow transients

with reduced voltage stress and oscillations, mitigating false turn-ON failures. However, this approach suffers from significantly reduced slew-rates with the consequent penalty in efficiency. In contrast to the traditional approach, the proposed MP-Sequence achieves swift commutation times while maintaining low voltage stress and oscillations, which effectively mitigates false turn-ON failures.

C. SENSITIVITY ANALYSIS
In this section, the sensitivity of the proposed MP-Sequence with respect to parameter variations is analyzed.

Fig. 6 illustrates the proposed MP-Sequence with fine-tuned timings for $L_G = 100nH$ and load variations from 20 % to 100 % of the rated device current. It can be seen that the proposed MP-Sequence achieves good timings with respect to the changes in I_D and consequent V_M according to (13), resulting in reduced voltage stress and oscillations across the whole loading range of the device.

Fig. 7 illustrates the time domain simulation results of the sensitivity analysis of the proposed method with $L_G = 100nH$ and a $\pm 5\%$ variation of timing-related parameters (L_G, V_{th}, g_m, Q_T, Q_{GD}), which result in a $\pm 10\%$ timing error of t_A and t_B. It can be seen that the timing error has an impact on the transient behavior, leading to timings close to the target conditions. Yet, the deviation from the target conditions causes oscillations and voltage stress of about $\pm 20\%$ for the turn-ON and about $\pm 40\%$ for the turn-OFF transient. Fortunately, these oscillations are dampened by the internal gate resistance of the power switch, which leads the transient to converge to the ON- and OFF- state before the next switching cycle. Although these oscillations are undesired, it is worthwhile pointing out that the MP-Sequence achieves a significant improvement in contrast to the traditional underdamped transient indicated in grey. Moreover, these timing errors can easily be addressed in a practical setting via proper fine-tuning of the pulses to a given application.
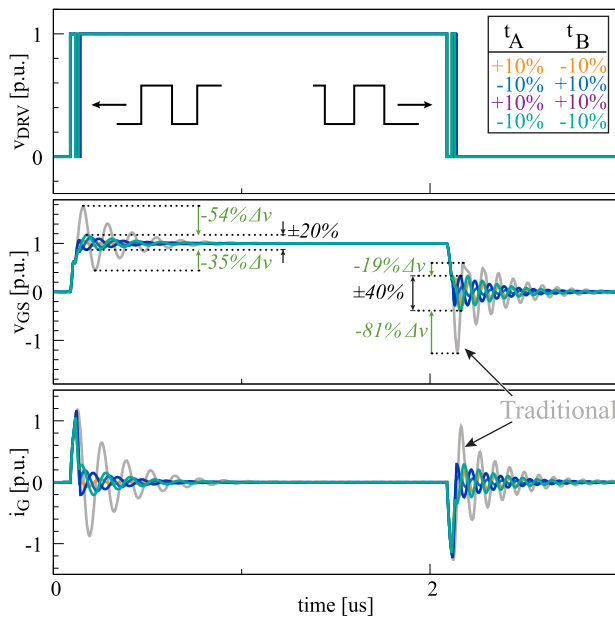
FIGURE 7. Sensitivity analysis with $L_G = 100nH$ of the proposed MP-Sequence (colored) with $\pm 10\%$ for t_A and t_B with consequent timing error vs. traditional approach (grey).

TABLE 2. Operating Conditions

Circuit Param.	Value
v_{in}	200 V
v_{out}	440 V
i_{out}	1 A
f_{sw}	100 kHz
v_{DR}	0-10 V
L_{Boost}	980 µH
C	12 µF

IV. EXPERIMENTAL VERIFICATION

In this section, the proposed MP-Sequence, which enables a simple driver circuit architecture that provides reduced transient times, switching losses, and oscillations in the gate circuitry during extreme slew-rates, is employed for experimental verification. In particular, the MP-Sequence is implemented within an asynchronous boost topology with the previously introduced power switch and the operating point described in Table 2. Moreover, the half-bridge to drive the power switch is implemented with an off-the-shelve driver (UCC5304DWV), as it implements the half-bridge internally. Fig. 8 shows the experimental verification configuration with the asynchronous boost topology (see Fig. 8(a)) and the setup (see Fig. 8(b)), including the power stage, the pulse-generating board, and the high-precision power analyzer.

A. OPERATIONAL VERIFICATION

Fig. 9 depicts the experimental captures of the proposed MP-Sequence scheme with $L_G = 15\,\mu H$ to showcase the proof of concept. It is worthwhile mentioning that the benefits of the
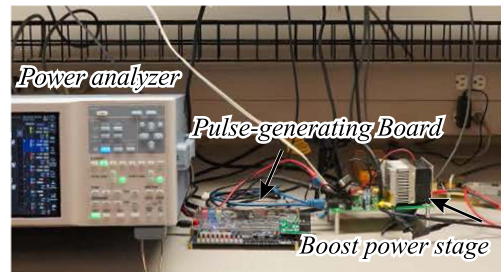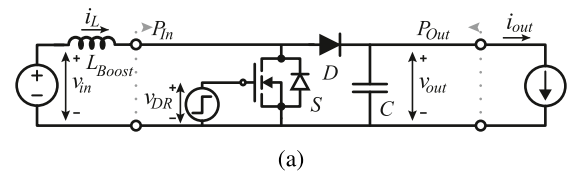

(a)

(b)

FIGURE 8. Experimental verification: (a) Asynchronous boost topology, with loss measurement points for input (P_{in}) and output power (P_{out}); (b) Setup, including high-precision power analyzer, pulse generating board, and power stage.
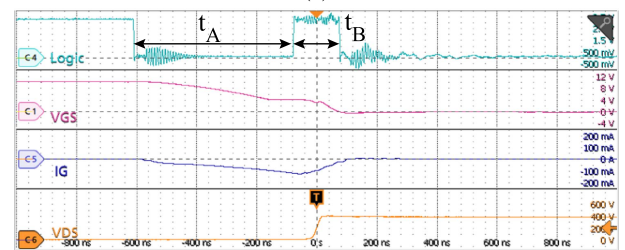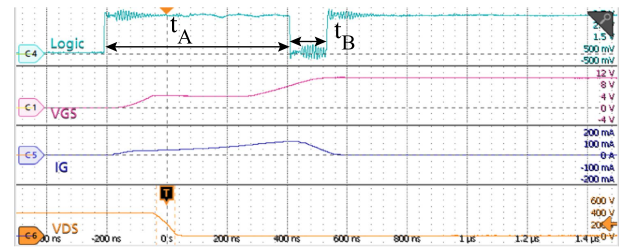

(a)

(b)

FIGURE 9. Proof of concept of proposed MP-Sequence (Logic) with $L_G = 15\mu H$, incorporating t_A and t_B resulting in minimal oscillations in v_{GS} and i_G: (a) turn-ON; (b) turn-OFF.

MP-Sequence will become much more dominant when L_G approaches L_{Par}, as described in the next paragraph. In particular, Fig. 9(a) displays the turn-ON transient, and Fig. 9(b) depicts the turn-OFF transient with the driving signal (Logic), containing the MP-Sequence with t_A and t_B, and the anticipated waveforms for v_{GS}, i_G, and v_{DS}. Both captures show a successful transition with low voltage stress and minimal oscillations for ON- and OFF-transitions, respectively. In addition, the accuracy of the proposed MP-Sequence with respect to calculations and approximations have been compared to experimental results for $L_G = 10\mu H$. The results are displayed in Table 3, which show excellent alignment for t_A,

TABLE 3. Timing Estimation Accuracy With $L_G = 10\mu H$

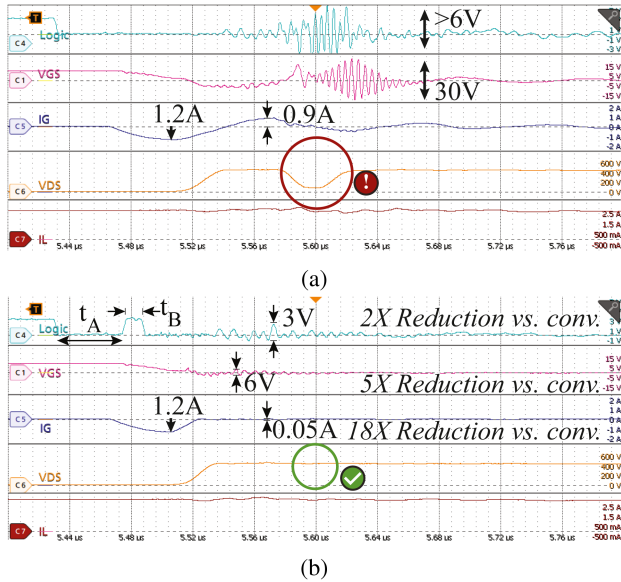|	Meas. [ns]	Calc. Err. [%]	Approx. Err. [%]
t_A	273	≈ 1	≈ 4
t_B	190	≈ 8	≈ 10

(a)

(b)

FIGURE 10. Experimental captures of the turn-OFF with extreme slew-rate ($R_G = 0$, $L_G = L_{Par}$): (a) Traditional single pulse with significant oscillations in v_{GS} and i_G during transients and consequent false turn-ON failure; (b) Proposed MP-Sequence achieving stable operation with significant reduction of oscillations in v_{GS} and i_G.

whereas the estimation for t_B is within the expected error margin that allows for $\pm 5\%$ variation in timing-related parameters discussed earlier.

B. EXTREME SLEW-RATE OPERATION

Fig. 10 depicts the experimental captures with the extreme case of $R_G = 0$ and $L_G = L_{Par}$ resulting in a swift commutation with high slew-rates during turn-OFF. In particular, Fig. 10(a) displays the traditional approach with a single pulse, resulting in significant oscillations in v_{GS} and i_G. These oscillations result in excessive voltage stress on the gate of the power switch as well as a false turn-ON failure. Further, Fig. 10(b) presents the waveforms of the proposed MP-Sequence, with t_A and t_B in the driving signal (Logic). These pulses result in a significant reduction of oscillations in v_{GS} and i_G during the transient. In particular, the MP-Sequence achieves an outstanding 5X and 18X reduction in oscillation amplitude, while delivering the same peak output current (1.2 A), with respect to the conventional approach for v_{GS} and i_G respectively. This advantage allows the MP-Sequence, in contrast to the traditional approach, to safely operate the power switch with extreme slew-rates, while mitigating false turn-ON failures.
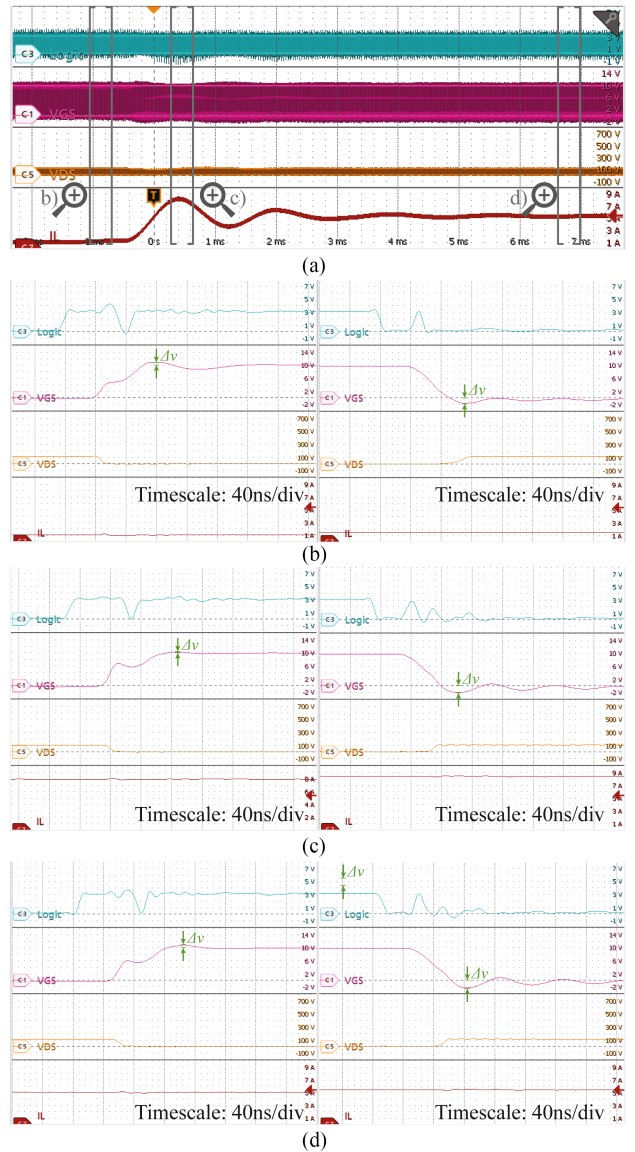

FIGURE 11. Experimental capture with $L_G = L_{Par}$ and consistent timing achieving minor oscillations and voltage stress during load step at $v_{out} = 100~V$: (a) full capture (b) transients at low loading condition (c) transients during peak transient current (d) transients at medium loading condition.

C. CONSTANT TIMING ACROSS WIDE OPERATING RANGE

The proposed MP-Sequence has been employed under various loading conditions with $L_G = L_{Par}$ while maintaining consistent timings to demonstrate the robustness of the proposed MP-Sequence across a wide operating range. In particular, a load-step (10% to 50% of the rated device current) with 100V (see Fig. 11) and 400V (see Fig. 12) has been performed with the previously described boost topology. Overall, both captures demonstrate that the MP-Sequence with constant timing achieves successful commutation without false turn-ON events and minor oscillations across a wide loading range. In particular, it can be seen in Figs. 11(b) and 12(b)
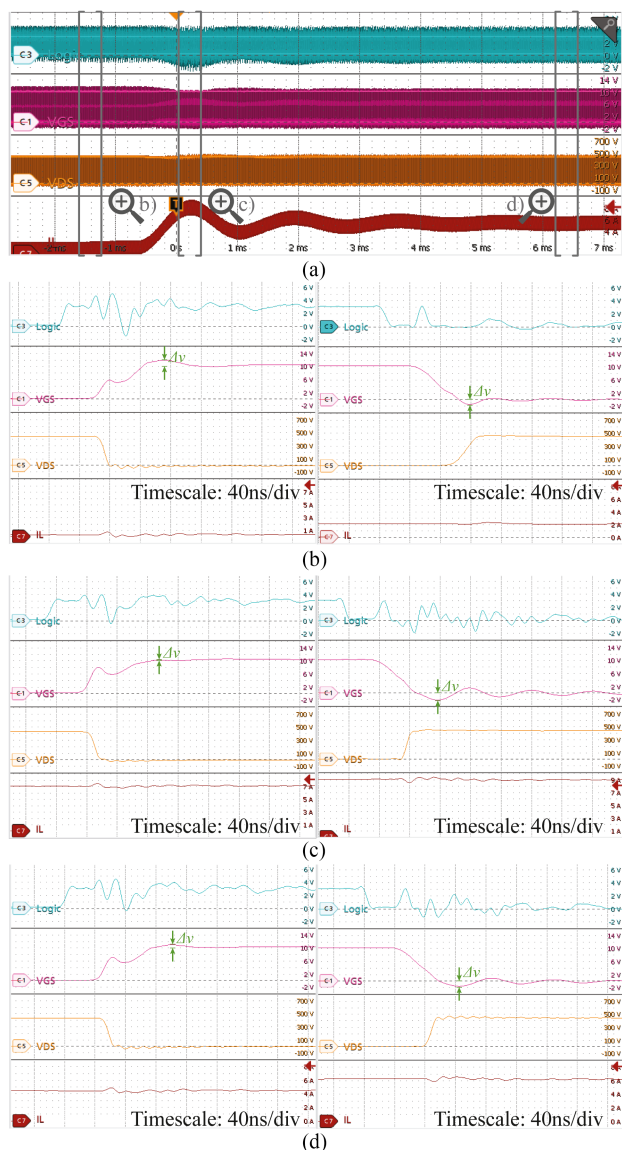
FIGURE 12. Experimental capture with $L_G = L_{Par}$ and consistent timing achieving minor oscillations and voltage stress during load step at $v_{out} = 400\,V$: (a) full capture (b)transients at low loading condition (c) transients during peak transient current (d) transients at medium loading condition.

that the MP-Sequence achieves minor over- and undershoot in v_{GS} during low loading conditions for low- and high-voltage operation respectively. During high loading conditions depicted in Figs. 11(c) and 12(c) the MP-Sequence achieves near-zero overshoot and little under-shoot in v_{GS} for low- and high-voltage operation respectively. At medium loading conditions illustrated in Figs. 11(d) and 12(d) the MP-Sequence provides minor over- and undershoot in v_{GS} for low- and high-voltage operation respectively. This demonstrates that the MP-Sequence with consistent timing performs well across a wide range of operation conditions for a given MOSFET, which supports the versatility and robustness of the proposed method.
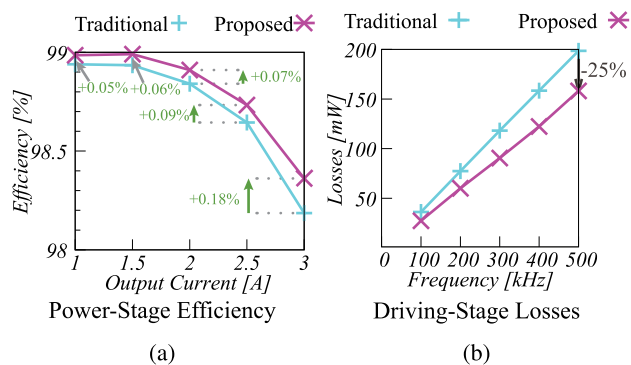

FIGURE 13. Experimental loss measurements: (a) Power-stage efficiency with traditional ($R_G = 5\Omega$) and proposed MP driving scheme ($L_G = L_{Par}$) with respect to load current with up to. 2 % efficiency improvement; (b) Driving losses of traditional and proposed MP driving scheme with respect to switching frequency with up to 25 % gate drive loss reduction.

D. EFFICIENCY INVESTIGATION

The impact of the proposed MP-Sequence on the power as well as the driving stage with respect to efficiency and losses have been investigated for different operation conditions of the asynchronous boost topology with a high-precision power analyzer. For the power losses, the operating conditions in Table 2 are used for different loading conditions, while the losses in the power stage are measured. The results are depicted in Fig. 13(a) for the conventional driving scheme with $R_G = 5\Omega$ and the proposed MP-Sequence with $L_G = L_{Par}$. It can be seen that the proposed MP driving sequence achieves up to. 2 % efficiency improvement compared to the traditional approach. For the driving losses, the power stage has been powered off to emulate soft-switching conditions and to eliminate thermal limitations. In this condition, the driving losses for switching frequencies ranging from 100 kHz to 500 kHz are investigated. The results are shown in Fig. 13(b), which indicates a significant loss reduction (up to 25 %) compared to the traditional approach at high frequencies.

V. CONCLUSION

In this paper, a novel multi-pulse (MP) gate driving sequence was proposed, that enables a simple driving circuit utilizing the gate loop inductance for Si-MOSFETs. This MP-Sequence provides the ability to rapidly commutate MOSFETs efficiently with low voltage stress and reduced oscillations in the gate circuitry. The theoretical derivation of the MP-Sequence has been verified by simulations and experiments, showing an excellent performance. The MP-Sequence extends the feasible operation range of gate drivers during extreme slew-rates, as it provides outstanding 5X and 18X reduction in oscillation amplitude while delivering the same peak output current, with respect to the conventional approach for v_{GS} and i_G respectively. Moreover, the proposed MP-Sequence has demonstrated to effectively mitigate false turn-ON failures through oscillation suppression. With the extreme slew-rate capability, the proposed MP-Sequence is

able to significantly improve the power-stage efficiency by up to. 2 % compared to conventional driving. In addition, the proposed MP-Sequence demonstrated a significant reduction in driving losses of approximately 25 % compared to the traditional resistive driving scheme. Finally, this work enables the use of a simple driving circuit architecture with an exceptional reduction in voltage stress and oscillation suppression during extreme slew-rate operation, which results in improved efficiency of the driving- and the power stage. Moreover, this work establishes a novel approach to non-linear gate driving with further opportunities with respect to power stage voltage stress mitigation, efficiency improvements, and EMI reduction.

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