

Hardware-Based Comparative Analysis of Multilevel Inverter Topologies for Integrated Motor Drives Considering Overload Operation

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ABSTRACT With today's demand for increased industrial process automation a trend towards Integrated Motor Drives (IMDs) has evolved allowing a low complexity and compact installation of the drive system. Especially servo applications with high short-term overload requirements (e.g., three times the nominal current for several seconds) are a thermal challenge for the power electronics. Consequently, high efficiencies and power densities are key requirements of these motor-integrated Variable Speed Drives (VSDs). Multi-Level (ML) inverter topologies allow small LC output filter designs and benefit from utilizing low-voltage semiconductors with superior conduction and switching performance, and thus represent an interesting approach for future IMDs. In this work an experimental comparison between three different 800 V DC link supplied drive systems is presented, namely between a 3L Flying Capacitor Converter (3L-FCC) (employing 650 V GaN HEMTs), a 7L Flying Capacitor Converter (7L-FCC) (using 200 V Si MOSFETs) and its promising alternative, a 7L Hybrid Active Neutral-Point Clamped Converter (7L-HANPC) (using both, 650 V GaN HEMTs and 200 V Si MOSFETs). All three systems are realized as hardware demonstrators for the same specifications, i.e., for integration into a Permanent Magnet Synchronous Motor (PMSM) with a case temperature of 90 °C, 7.5 kW nominal output power at >99% efficiency and a short-term overload capability of three times the nominal current for 3 s. Thereby, the efficiencies and the thermally critical overload capability are experimentally verified. Overall, the 3L-FCC shows the best performance trade-off with lowest complexity and/or highest reliability and minimal control effort.

INDEX TERMS Integrated motor drive, multi-level inverter, overload operation, variable speed drive, WBG power semiconductors.

I. INTRODUCTION

Variable Speed Drives (VSD) are omnipresent in industrial automation processes, e.g., in servo systems for assembly lines, material machining and processing, and packaging [1]. In recent years a strong interest in so-called IMDs has emerged, where the power electronics (active/passive rectifier front end and inverter output stage) is directly integrated into the motor unit, omitting expensive shielded cables and allowing a space saving installation of the system [2], [3]. This trend is favored

by the fact that a shift towards DC supplied VSDs is developing in the industry at the same time [4], which reduces the number of components to be integrated into the motor to the inverter stage only.

Achieving high power densities of the power electronics is a key aspect of IMDs as the space available for motor integration is limited [5], [6], [7]. Moreover, additional losses in the vicinity of the motor must be minimized in order to limit the additional cooling effort and/or to limit the self-heating of

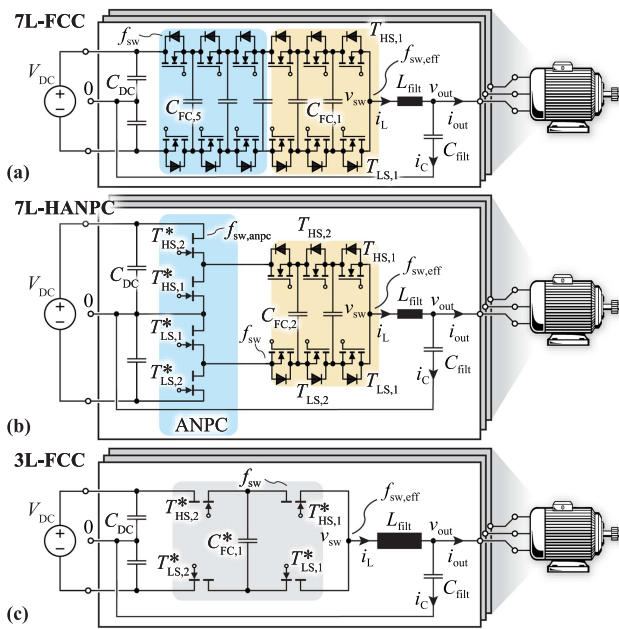


FIGURE 1. Circuit schematics of the phase modules of a motor-integrated three-phase inverter stage considered in the comparative evaluation in this paper: (a) 7L-FCC, (b) 7L-HANPC and (c) 3L-FCC. Assuming a DC link voltage of 800 V, the 7L-FCC and the FC-cells of the 7L-HANPC are built with 200 V Si MOSFETs, while the 3L-FCC and the ANPC stage of the 7L-HANPC are realized with 650 V GaN HEMTs. The DC link referenced full-sine-wave output filter largely attenuates Differential Mode (DM) and Common Mode (CM) switching frequency voltage components.

the power electronics in the already high ambient temperatures of the motor (e.g., in the case at hand, for thermally connecting the power electronics to a naturally cooled motor housing, typically a temperature of $T_{\text{case}} = 90^\circ\text{C}$ has to be considered.)

The predominant two-level three-phase inverters apply Pulse Width Modulated (PWM) voltages to the motor windings, which potentially lead to, e.g., bearing currents [8], High-Frequency (HF) harmonic losses [9], over-voltages between the coils [10] and Low-Frequency (LF) oscillations at the neutral point [11] inside the motor. These effects can be entirely avoided by inserting a full-sine-wave LC output filter between switching stage and motor [12]. Moreover, when the filter capacitors are connected to the DC-midpoint (cf. “ C_{filt} ” connected to “0” in Fig. 1), the Common Mode (CM) Electromagnetic Interference (EMI) emissions into the supplying DC grid can be reduced [13]. With Wide-Bandgap (WBG) semiconductor devices instead of standard Insulated-Gate Bipolar Transistor (IGBT) technology, the inverter switching frequency can be increased from a few kHz to several tens of kHz, which allows a relatively small (but still significant) LC -filter volume in a standard 2-level inverter approach [14], while the motor is protected from the high dv/dt switching transients of WBG semiconductors. The filter volume can be further reduced by employing ML inverters [15], which generate an inherently more sinusoidal multi-level output voltage waveform requiring less filtering. Furthermore, lower blocking voltage devices can be used which feature an improved

TABLE 1. Specifications for the Analyzed Integrated Motor Drive (IMD)

Parameter		Value
DC Link Voltage	V_{DC}	800 V
Nominal Output Power (3-Phase)	P_{nom}	$3 \cdot 2.5$ kW
Nominal Peak Output Voltage Amp.	$v_{\text{out,nom}}$	330 V
Nominal Peak Phase Current Amp.	$i_{\text{out,nom}}$	15 A
Overload Peak Phase Current Amp.	$i_{\text{out,OL}}$	45 A
Overload Duration	t_{OL}	3 s
Max. Inverter Output Frequency	$f_{\text{out,max}}$	300 Hz
Motor Case (Ambient) Temperature	T_{case}	90°C
Min. Nominal Inverter Efficiency	$\eta_{\text{nom,min}}$	99 %
Filter Output Voltage Ripple	$\Delta v_{\text{out,pp}}$	1 % of V_{DC}
Filter Inductor Current Ripple	$\Delta i_{\text{L,pp}}$	80 % of $i_{\text{out,nom}}$

conduction and switching performance compared to higher voltage devices (captured in the so-called Figure-of-Merit (FOM) [16], [17]), and thus an additional increase in efficiency is possible. However, these multi-level benefits come at the expense of increased complexity and a higher required number of discrete components (e.g., semiconductors and gate drives), which leads to the question of which level number is the optimum for motor integration.

We performed an according analysis in [18] and [19] for an 800 V DC link supplied 7.5 kW three-phase motor drive with a high short-term overload current capability (three times nominal current during 3 s, cf. Table 1), which is typical for servo applications [20]. The optimization was limited to Multi-Level Flying Capacitor inverter (ML-FCi) topologies and showed, that a 3L-FCC with GaN semiconductor (cf. Fig. 1(c)) achieves the nominal target efficiency specification of 99 % (cf. Table 1) at a maximum power density and minimal complexity, which was experimentally verified with a hardware demonstrator employing 650 V GaN semiconductors [19]. However, in the analysis a 7L-FCC design with 200 V Si MOSFETs was also considered, cf. Fig. 1(a), and promised a similar power density with a remarkably smaller filter volume but dominating PCB volume (more semiconductors, gate drives and flying capacitors) compared to the 3L-FCC. The same small filter volume can be achieved with a 7L-HANPC [21], i.e., a combination of a four transistor Active Neutral-Point Clamped (ANPC) switching stage and only three additional flying capacitor cells (cf. Fig. 1(b)). Therefore, the 7L-HANPC requires a significantly lower number of semiconductors and passive energy storage elements (i.e., flying capacitors) and thus qualifies as attractive 7L alternative with reduced complexity.

These findings finally motivate a full hardware-based comparison of the three possible IMD implementations (7L-FCC, 7L-HANPC, and 3L-FCC), which is performed in this paper for the target specifications of Table 1, i.e., they also include the challenging short-term overload capability. In the following, the different phase module hardware demonstrators are presented in Section II, briefly summarizing the main hardware design aspects. Subsequently, their performance is

TABLE 2. Maximum Switching Frequencies of the Hardware Demonstrators During Nominal ($f_{sw,nom}$) and Overload Operation ($f_{sw,OL}$) and their Respective Effective Switching Frequencies at the Switch Node ($f_{eff,nom}$ and $f_{eff,OL}$)

	$f_{sw,nom}$	$f_{sw,OL}$	$f_{eff,nom}$	$f_{eff,OL}$
3L-FCC	35 kHz	67 kHz	70 kHz	134 kHz
7L-FCC	25 kHz	75 kHz	150 kHz	450 kHz
7L-HANPC	50 kHz	85 kHz	150 kHz	255 kHz

experimentally verified in Section III, followed by an overall comparison of the three IMD solutions in Section IV. A compact IMD design is proposed in Section V for the topology with the best overall trade-offs. Finally, Section VI concludes the paper.

II. DESIGN AND REALIZATION

All three inverter hardware demonstrators are designed to meet the target specifications of Table 1, including identical DC link voltage, nominal output power, minimum nominal efficiency, short-term overload capability and nominal output waveform quality (i.e., peak-to-peak output voltage ripple $\Delta v_{out,pp}$). For the sake of brevity, only main aspects of the design are described here. However, the employed design procedure including component modeling has been comprehensively discussed in [19], especially for the 3L-FCC and 7L-FCC. The most important operating parameters are listed in Table 2, whereas the main components utilized in the presented phase module demonstrators are given in Table 3.

A. DESIGN OF THE 7L-FCC AND 3L-FCC

Both, the 7L-FCC and 3L-FCC designs aim at a nominal efficiency of minimum 99% with minimal volume. During overload operation the semiconductor conduction losses increase quadratically with current (ohmic on-state characteristic of the power transistors) and dominate the mostly linear switching loss increase. Thus, high overload capability calls for power transistors with low on-state resistance (R_{dson}) and good cooling performance (i.e., low thermal resistance from junction to case and a large cooling pad). Considering the devices available on the market, the 7L-FCC can be implemented using single bottom-cooled 200 V Si MOSFETs (IPT111N20NFD, 11 m Ω , [22]), which are optimized for hard-switched applications. The 99% efficiency target can be achieved with a device switching frequency of $f_{sw} = 25$ kHz and for the overload operation the semiconductor cooling capability is improved with copper inlays and thermal vias in the PCB as shown in Fig. 2(a.ii). In contrast, for the realization of the 3L-FCC two parallel top-cooled 650 V GaN HEMTs (GS66516-T, 25 m Ω , [23]) per switch are required (cf. Fig. 2(b.ii)), which operate at a switching frequency of $f_{sw} = 35$ kHz. In order to keep the impact of the overload capability on the resulting system volume as small as possible, the switching frequency is increased linearly with the output current as soon as the nominal current amplitude of 15 A

TABLE 3. Main Power Components of the Different Hardware Demonstrators Shown in Fig. 2(a) and (b) with Total Quantities Used for a Single Phase Module

Component	Value	Details
Transistors 650 V (3L-FCC/ANPC)	12.5 m Ω	GaN Systems GS66516T (25 m Ω ; 2 x parallel per position; 27.2 mm ² meas. device chip area)
Transistors 200 V (7L-FCC/7L-HANPC)	11 m Ω	Infineon IPT111N20NFD (11 m Ω ; 29 mm ² meas. device chip area [16])
Gate Driver (GD)		Infineon 1EDN7511B
GD Insulator		Analog Devices ADuM121N
L_{filt} (3L-FCC)	120 μ H	Magnetics Powder Core 0076076A7, 3x stacked per inductor, 32 turns of litz wire with 630 strands
C_{filt} (3L-FCC)	2.2 μ F	22 x CGA9Q4NP02W104J280KA (NPO, 100 nF, 450 V)
L_{filt} (7L-FCC/7L-HANPC)	18 μ H	Magnetics Powder Core 0076059A7, 2x stacked per inductor, 17 turns of litz wire with 630 strands
C_{filt} (7L-FCC/7L-HANPC)	1.5 μ F	15 x CGA9Q4NP02W104J280KA (NPO, 100 nF, 450 V)
C_{fc} (3L-FCC)	11.2 μ F	26 x C5750X6S2W225K250KA (X6S, 2.2 μ F, 450 V)
C_{fc} (7L-FCC)	min. 6.9 μ F per FC-cell	132 x C5750X6S2W225K250KA (X6S, 2.2 μ F, 450 V)
C_{fc} (7L-HANPC)	min. 14 μ F per FC-cell	37 x C5750X6S2W225K250KA (X6S, 2.2 μ F, 450 V)
Current Sensor		Allegro ACS733KLATR-65AB-T
OpAmp Volt. Meas		Analog Devices LTC6362
ADC		Analog Devices LTC2311-12

is exceeded [19]. This (seemingly counterintuitive) measure allows to design the flying capacitors according to

$$C_{FC,cell} = \frac{i_{out}}{f_{sw} \cdot \Delta v_{FC,pp} \cdot N_{FC,cell}} \quad (1)$$

(with $N_{FC,cell}$ as number of FC-cells) [18] and the HF DC link capacitors according to

$$C_{DC} = \frac{i_{out}}{4 \cdot f_{sw} \cdot \Delta v_{DC,pp}} \quad (2)$$

mainly for nominal operation [19]. Hence, the capacitance can be chosen such that certain maximum allowed voltage ripple (i.e., $\Delta v_{FC,pp}$ and $\Delta v_{DC,pp}$) is maintained for nominal output current, while the overload current only has to be taken into account for thermal considerations (i.e., a minimum number of parallel capacitors is required to limit the temperature

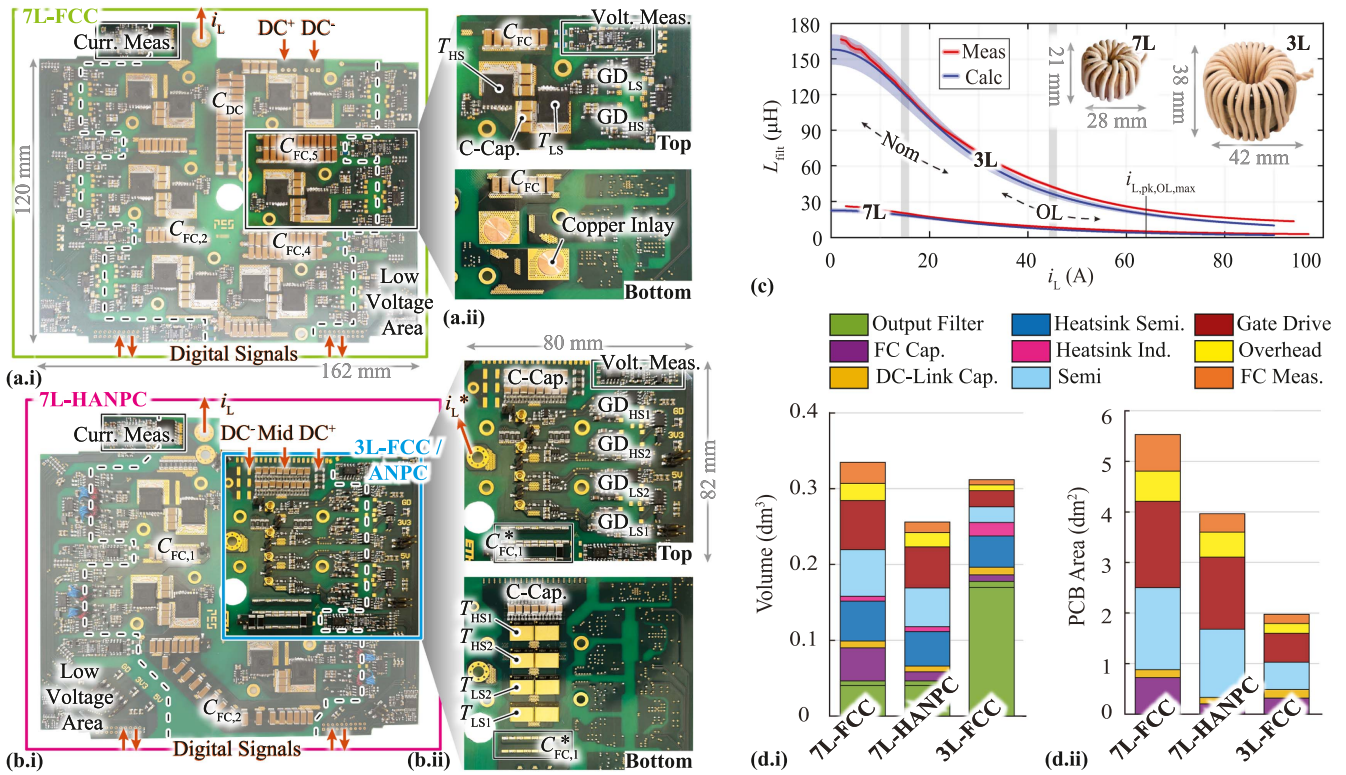


FIGURE 2. (a.i) Implemented phase module of the 7L-FCC hardware prototype (green box). A single Flying Capacitor (FC)-cell is shown in more detail in (a.ii) with top and bottom view. (b.i) Implemented phase module of the 7L-HANPC (magenta box). The ANPC stage (blue box) can be configured and used as 3L-FCC directly (cf. schematics of Fig. 1). (b.ii) Enlarged view on the top and bottom of the 3L-FCC / ANPC area with labels of the most important components. (c) Output filter inductance vs. current of the 7L (7L-FCC and 7L-HANPC) design and 3L-FCC design realized with soft magnetic powder cores. Indicated are the operating range during nominal and overload current, the maximum accepted inductor peak current and the mechanical dimensions of the respective phase module inductor realizations. (d.i) Volume breakdown and (d.ii) PCB area breakdown expected from the three IMD solutions in comparison. For the 7L-FCC and 3L-FCC they match well with their realizations shown in (a) and (b) (considering a non-ideal packaging overhead factor 1.3 for the volume), while the realization of the 7L-HANPC is larger than necessary due to the multipurpose PCB layout.

increase per capacitor due to Equivalent Series Resistance (ESR) losses). Furthermore, the output filter inductor is advantageously designed with a soft magnetic alloy powder core (in the present case with Kool M μ Hf by Magnetics for low HF core losses), which is characterized by a smooth reduction in inductance with increasing current. The filter inductor can then be designed according to [18] as

$$L_{\text{filt}} = \frac{V_{\text{DC}}}{4 \cdot N_{\text{FC,cell}}^2 \cdot f_{\text{sw}} \cdot \Delta i_{\text{L,pp}}} \quad (3)$$

for a maximum peak-to-peak filter inductor current ripple of $\Delta i_{\text{L,pp}}$ during nominal operation, while during overload a drop in inductance is accepted (cf. Fig. 2(c)). Thereby, the simultaneous increase in switching frequency guarantees that a certain peak current including current ripple is not exceeded (e.g., in the case at hand 64 A). Consequently, these limitations lead to a design-specific required increase in switching frequencies during overload, i.e., an overload factor of 3 for the 7L-FCC and 1.9 for the 3L-FCC, respectively.

B. DESIGN OF THE 7L-HANPC

The realization of the 7L-HANPC as an alternative solution to the 7L-FCC should use the same small output filter as labeled

in Fig. 2(c) with “7L”. Consequently, the generated output waveforms must be identical, which means that besides the number of output voltage levels also the effective switching frequency measured at the switch node must match. As visualized and described in more detailed in [21], the 7L-HANPC consists of two stages, namely the ANPC stage (highlighted blue in Fig. 1(b)) and a FC stage with three FC-cells (highlighted orange in Fig. 1(b)). The ANPC acts as a selector switch and/or unfold, and connects the FC stage to DC+/0 or 0/DC- respectively, depending on the sign of the desired output voltage. Accordingly, the number of output voltage levels provided by the HANPC is given as

$$N_{\text{lev,HANPC}} = 2 \cdot N_{\text{FC,cell}} + 1 \quad (4)$$

with $N_{\text{FC,cell}}$ as the number of FC-cells. In order to match the seven output voltage levels of the 7L-FCC three FC-cells are required. As highlighted in orange in Fig. 1(a) and (b), they FC-cells are exactly identical to the lower voltage FC-cells of the 7L-FCC, i.e., they experience the same blocking voltages and can be realized with the same 200 V Si MOSFETs. Meanwhile, the ANPC stage in the 7L-HANPC replaces the higher voltage FC-cells of the 7L-FCC and must withstand $V_{\text{DC}}/2$, which requires 650 V semiconductors. The effective

switching frequency f_{eff} at the switch node is given only by the FC-cells and is a multiple of the FC-cell device switching frequency f_{sw} , i.e.,

$$f_{\text{eff}} = N_{\text{FC,cell}} \cdot f_{\text{sw}}. \quad (5)$$

Consequently, due to the lower number of FC-cells in the 7L-HANPC, the device switching frequency has to be doubled compared to the 7L-FCC leading to $f_{\text{sw}} = 50$ kHz. Note however, that this does not necessarily reduce the total efficiency. The ANPC stage has negligible switching losses due to the infrequent switching operations (determined by the motor speed and/or inverter stage fundamental output voltage frequency which is limited to values below 300 Hz in the case at hand), and thus only contributes to the conduction losses, which can be kept low by small R_{dson} values. As mentioned previously, a low R_{dson} value is anyways required for the overload operation.

Taking into account the somewhat similar structure of the ANPC stage and the 3L-FCC (cf. Fig. 1), combined with the chosen low R_{dson} GaN semiconductors, a multi-purpose PCB layout can be realized, i.e., the same PCB can be reconfigured and used as 3L-FCC or as 7L-HANPC as shown in Fig. 2(b). Nonetheless, the rarely switching ANPC stage of the 7L-HANPC could also be realized with 650 V Si devices instead of GaN semiconductors, provided that both feature similar low R_{dson} values. Considering the overload restrictions of the capacitors and the filter inductor, a switching frequency increase of up to 1.7 is required during overload in the 7L-HANPC. This is considerably lower than the factor 3 required for the 7L-FCC as the flying capacitors at lower levels are mainly thermally limited (i.e., more capacitors are required than absolutely necessary for the maximum voltage ripple at nominal operation) and thus do not need a full switching frequency increase during overload.

Finally, these considerations result in the volume breakdown and required PCB area as shown in Fig. 2(d.i) and 2(d.ii) respectively. Clearly visible is the overall lower capacitor volume of the 7L-HANPC compared to the 7L-FCC as three higher voltage flying capacitors are eliminated (which previously required two 450 V X6S ceramic capacitors in series) and in total less switches are needed and consequently also less gate drives. Combined with the small inductor volume, the 7L-HANPC can achieve the overall smallest volume, while the 3L-FCC requires the overall smallest PCB area.

III. EXPERIMENTAL PERFORMANCE VERIFICATION

The measured key waveforms of all three phase module hardware demonstrators are shown in Fig. 3 for nominal and overload operation at 300 Hz electrical output frequency with a mainly resistive load; including switching frequency increase for output currents above 15 A. Thereby, all measurements were performed in open-loop with phase-shifted PWM modulation, however, a closed-loop controller for the FC voltage balancing was implemented [24]. The baseplate where the respective PCBs are mounted is externally heated to a temperature of 100 °C to thermally emulate the motor of

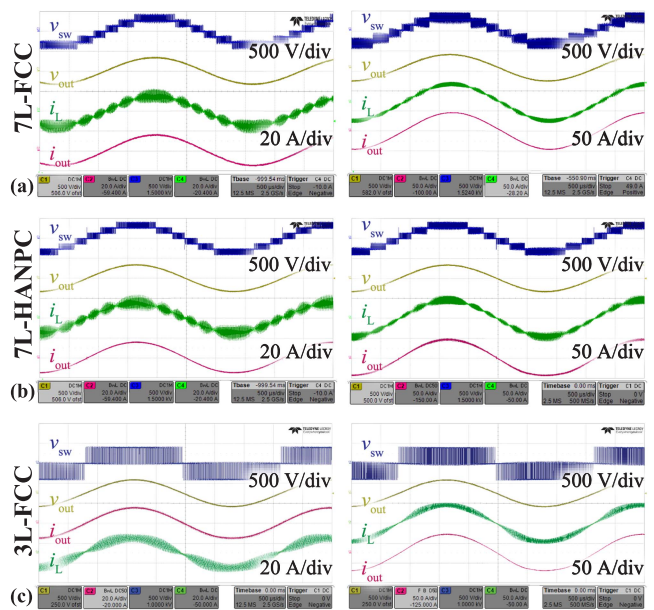


FIGURE 3. (a) Measured phase module waveforms of the 7L-FCC, (b) 7L-HANPC and (c) 3L-FCC hardware prototype featuring the switch node voltage v_{sw} , the inductor current i_L , the filtered output voltage v_{out} and the filtered output current i_{out} during nominal operation (left) and overload operation (right), all with 300 Hz output frequency. The waveforms of the 7L-FCC and 7L-HANPC are nearly identical, except for the ripple amplitude in the inductor current waveform during overload, which originates from the different switching frequency increase during overload operation (i.e., up to factor 3 for the 7L-FCC and factor 1.7 for the 7L-HANPC).

the IMD system in a simple but effective manner. Under the same conditions electrical efficiency measurements are conducted with a Yokogawa WT3000 precision power analyzer, which according to measurements performed in [25] achieves highly accurate results exceeding its official specifications. The results for nominal and partial load operation are shown in Fig. 4(a) achieving a final measured nominal efficiency of 98.90 % for the 7L-FCC, of 99.11 % for the 7L-HANPC and of 98.94 % for the 3L-FCC. The 7L-FCC and 3L-FCC closely match their target efficiency of 99 % and the additional losses (highlighted in yellow in the calculated loss breakdown of Fig. 4(b)–(d) can be explained by ohmic resistances of, e.g., tracks, connectors and current measurement sensors, which have not been accounted for during the design process (corresponds to about 22 mΩ total resistance in the 7L-FCC and 15 mΩ in the 3L-FCC). The 7L-HANPC was designed to generate the same output voltage waveform as the 7L-FCC and thereby manages to exceed the 99 % efficiency mark. Mainly the chosen semiconductors of the ANPC stage have a lower R_{dson} than strictly necessary for the target efficiency at nominal load, since they were chosen for the thermally challenging overload operation. Compared to the 3L-FCC, both 7L implementations (i.e., 7L-FCC and 7L-HANPC) show a flat loss characteristic over varying output voltage for the same current (cf. Fig. 4(b.i)–(d.i) and (b.ii)–(d.ii)). Given the seven output voltage levels, the mean current ripple remains similar for most generated output voltages, and hence also the

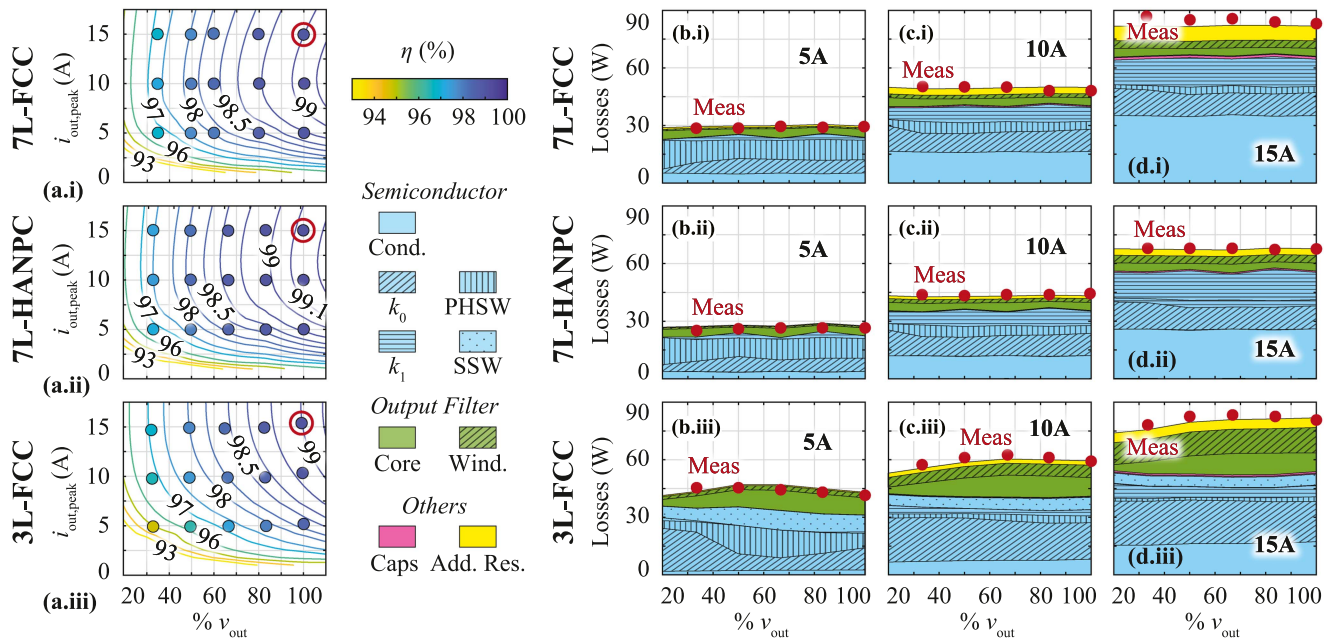


FIGURE 4. (a.i)–(a.iii) Measured (dots) and calculated (lines) efficiencies for nominal and partial load operation at a baseplate temperature of 100 °C featuring the 7L-FCC, the 7L-HANPC and the 3L-FCC respectively. Thereby, the output voltage v_{out} of 100% corresponds to 330 V peak amplitude for nominal output power. Hence, note that the nominal operating point, where the design target of minimum 99% efficiency is defined, corresponds to the measurement at $i_{out,peak} = 15$ A and 100% v_{out} (highlighted with a red circle). The respective measured total losses and the calculated loss breakdowns for $i_{out,peak} = [5$ A, 10 A and 15 A] are given in (b.i), (c.i) and (d.i) for the 7L-FCC, in (b.ii), (c.ii) and (d.ii) for the 7L-HANPC and in (b.iii), (c.iii) and (d.iii) for the 3L-FCC. The semiconductor losses are colored in light blue with the pattern indicating the distinction between conduction losses (“Cond.”), the Hard Switching (HSW) (“ k_0 ,” “ k_1 ”) according to $P_{sw} = k_0 + k_1 \cdot i_{sw} + k_2 \cdot i_{sw}^2$ [19], the Partial-Hard Switching (“PHSW”) losses, and the Soft Switching (“SSW”) losses. Note that partial load is measured for a fixed current with gradually reducing v_{out} . Simultaneously, the output frequency is linearly reduced with v_{out} (i.e., starting from 300 Hz at 100% v_{out}), which corresponds to a practically relevant scenario, where a constant torque at reduced rotational speed is provided.

semiconductor switching losses and inductor core losses. As already discussed in [19] and clearly visible in Fig. 4(b.ii)–(d.iii), this is not the case for the 3L-FCC. Note also that the distribution between semiconductor switching and conduction losses in the 3L-FCC (cf. Fig. 4(d.iii) in light blue) is dominated by the switching losses. According to [17] the optimum would be a more even distribution, which, however, could not be achieved with off-the-shelf power semiconductors and the overload operation constraints. Thus, a lower $R_{ds(on)}$ (i.e., larger die area) than optimal for nominal operation had to be chosen.

In Fig. 5(a)–(c) thermal camera measurements taken during nominal and overload operation are shown. The Si MOSFET packages of the 7L-FCC and 7L-HANPC are directly visible, e.g., $T_{HS,3}$ and $T_{LS,3}$, while for the top cooled GaN HEMTs only the area where they are located on the bottom side of the PCB is discernible (highlighted box labeled with “Semi. ANPC” in Fig. 5(a.ii)–(c.ii) or with “Semi.” in Fig. 5(a.iii)–(c.iii) respectively). The high efficiency and thus small losses during nominal operation (cf. Fig. 5(d.i)) do not lead to visible hot spots in the thermal images of Fig. 5(a). However, a local temperature increase around the semiconductors can be seen after the 3 s short-term overload operation with 300 Hz electrical output frequency (cf. Fig. 5(b)) due to the strongly increased losses shown in Fig. 5(d.ii). Note that due to the generated 300 Hz AC output voltage, the losses and

thus also the resulting temperatures are expected to even out over all semiconductor devices, i.e., among others also over the visible packages of $T_{HS,3}$ and $T_{LS,3}$. However, mechanical tolerances during the assembly affect the cooling performance in particular and thus can lead to noticeable temperature differences causing uneven stress among the semiconductor devices. Finally, the motor standstill overload (i.e., DC output voltage) highlights the most critical operating point, as one single phase with a peak overload current of 45 A experiences similar losses as the sum of all three phases together in overload operation with rotation (cf. Fig. 5(d.iii)). Consequently, thermal hot spots are clearly noticeable for all three prototypes, and as already discussed in detail in [19], the limited heatspreading of the baseplate has an additional impact, especially for the 3L-FCC. Note, however, that the multi-purpose PCB layout of the 3L-FCC leads to further heating in PCB tracks/vias and an even higher concentration of the thermal hot spots, which could be further optimized.

IV. COMPARATIVE EVALUATION

All three hardware prototypes have been built for the same specifications, operate at similar nominal efficiencies and have been tested in nominal and overload operation under the same

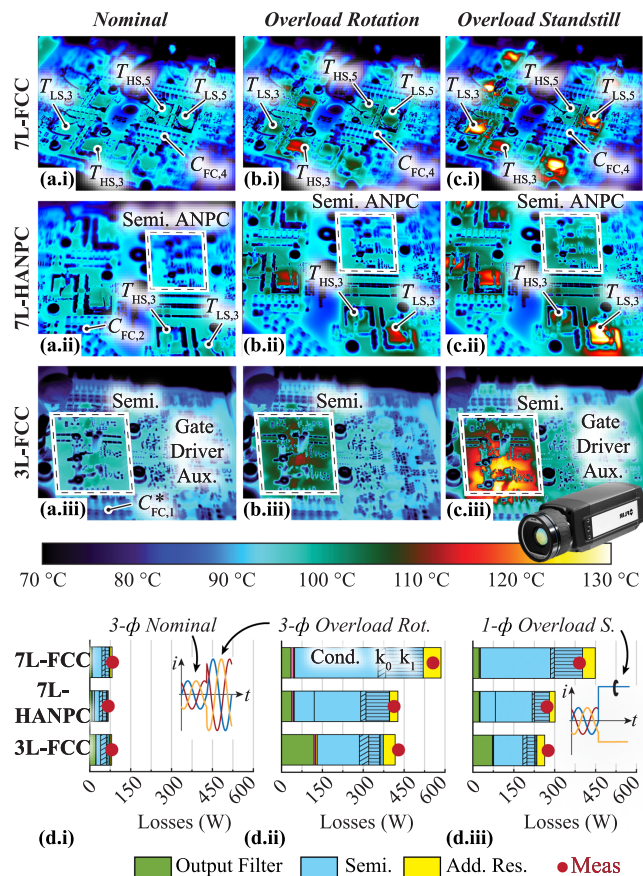


FIGURE 5. Thermal Camera recordings at 100 °C baseplate temperature of (a.i)–(a.iii) nominal operation, (b.i)–(b.iii) overload operation with 300 Hz output frequency and (c.i)–(c.iii) overload motor standstill operation with 0 Hz output frequency. Note that besides the limited heatspreading in the mounting baseplate combined with high concentration of losses during standstill overload, the PCB tracks and vias of the 3L-FCC are additionally heated due to the multi-purpose PCB layout. (d.i)–(d.iii) features the measured losses (red dots) during the different operations together with the calculated loss breakdowns, where “Semi.” (colored in light blue) represents the semiconductor losses, which are further divided in conduction and switching losses using the patterns as specified in Fig. 4.

conditions with a baseplate temperature of 100 °C. This allows an overall comparison visualized in the radar chart of Fig. 6. In the following, the main aspects are briefly discussed.

A. MECHANICAL DIMENSIONS AND REALIZATION EFFORTS

The obvious benefit of higher number of levels (e.g., 7L) over lower levels (e.g., 3L) is the reduced output filter volume, which is dominated by the filter inductor. While the required inductance value for the same current ripple at nominal load drops by a factor 6 from 120 μH (3L-FCC) to about 20 μH (7L-FCC/7L-HANPC), the inductor volume only reduces by a factor of 4, mainly due to the available core dimensions and the chosen surface cooling, which limit the possible reduction in size. As clearly visible in the schematics of Fig. 1, the small inductor volume comes at the cost of an increased number of switches and capacitive energy storage units. While both can

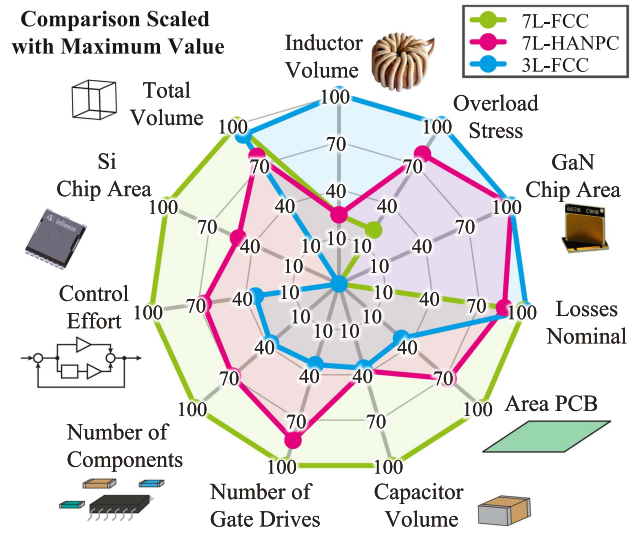


FIGURE 6. Radar chart indicating key characteristics of the 7L-FCC (green), 7L-HANPC (magenta) and 3L-FCC (blue) built hardware demonstrators of Fig. 2. 100% corresponds to the maximum value of each category. For a three-phase realization these maximum values are given in the following: Total Volume = 0.33 dm^3 (7L-FCC), Inductor Volume = 0.17 dm^3 (3L-FCC), Capacitor Volume = 0.052 dm^3 (7L-FCC), Area PCB = 5.5 dm^2 (7L-FCC), GaN Chip Area = 652.8 mm^2 (7L-HANPC/3L-FCC), Si Chip Area = 1044 mm^2 (7L-FCC), Number of Gate Drives = 36 (7L-FCC), Number of Components = 2616 (7L-FCC) and Losses Nominal = 75.5 W (7L-FCC). The Control Effort is quantified as number of passive components to be controlled, resulting in 18 units (7L-FCC) for 100%. The overload stress is defined as inverse of the remaining temperature budget to the maximal allowed junction temperature when peak current is provided during standstill overload. In this case the 100% value corresponds to 1/7 °C (3L-FCC).

be recognized in the radar chart of Fig. 6 for the 7L-FCC in form of a high number of gate drives and a large total capacitor volume, the latter nearly coincides for the 7L-HANPC with the 3L-FCC capacitor volume. Even though the 7L-HANPC has an additional flying capacitor unit, its higher f_{sw} allows a reduced HF DC link volume, while the volume of the flying capacitors itself is relatively small (and rather thermally limited), due to the large capacitance/volume density of the Class II ceramic capacitors at lower voltages (i.e., for 133 V and 266 V). Nevertheless, the 3L-FCC shows a clear advantage in terms of a small total number of components (includes besides semiconductors and capacitors also all Surface-Mounted Devices (SMDs) of the measurement circuits, gate drives, etc.), which strongly correlates with the required PCB area. All in all, the total achievable volumes are fairly similar with a slight advantage for the 7L-HANPC.

B. CHIP AREA

Due to the challenging temperatures close to the motor ($T_{\text{case}} = 90\text{ }^\circ\text{C}$) and the required short-term overload torque semiconductors with low R_{dson} values are required for all three prototypes. The corresponding measured device die areas (i.e., packaging removed) of the chosen power transistors are given in Table 3. In order to achieve the low R_{dson} values for the 650 V GaN semiconductors (employed in the 3L-FCC and

also in the ANPC stage of the 7L-HANPC), paralleling is required, effectively doubling the total semiconductor chip area of the three-phase inverter to 652.8 mm^2 compared to a design where only efficient nominal operation would be required. Similarly, with a total die area of 1044 mm^2 for 200 V Si MOSFETs in the 7L-FCC and 522 mm^2 in the 7L-HANPC, devices with a larger R_{dson} could have been considered (as can be seen in [19]), and thus reducing the total chip area.

C. CONTROL EFFORT

With today's digital control approaches, e.g., utilizing Field-Programmable Gate Arrays (FPGAs), the modulation of a large number of switches is a relatively simple task and hence does not heavily contribute to the overall control effort. However, the flying capacitors must be actively balanced as natural balancing might be insufficient [26], [27], [28] and passive balancing concepts [29] result in additional losses and volume. Thus, the number of energy storage elements that need to be controlled increases with the number of flying capacitors to be balanced. Realization-wise, separate voltage sensors (as here) or "advanced" methods based on output current or output voltage measurements [30], [31] are needed to detect imbalances in the voltages. While the selected measurement approach affects the required total number of components, it does not change the number of energy storage elements that need to be managed, which is therefore a good measure for the encountered control effort. Obviously, the filter inductors are a common additional energy storage element in all three prototypes, as their currents need to be actively regulated according to the required motor supply voltage and finally motor torque. The voltage of the (HF) DC link capacitors is directly enforced by the DC grid/source for the 7L-FCC and 3L-FCC. In contrast, the 7L-HANPC involves the (floating) DC link midpoint (also called Neutral Point) in the output voltage generation, which consequently represents an additional energy storage element to account for [32], [33]. All in all, the resulting measure of control effort highlights the comparatively small complexity of the 3L-FCC (i.e., 6 units for three phases), which increases with the 7L-HANPC and is highest for the 7L-FCC (with 18 units for three phases).

D. OVERLOAD STRESS

In [19] a detailed thermal Cauer model for the 3L-FCC has been elaborated, including the heatspreading in the baseplate extracted from Finite Element Method (FEM) thermal simulation. With this dynamic thermal model and the (temperature dependent) semiconductor losses the expected transient peak junction temperature could be approximated. This method is used to introduce a measure of overload stress, which considers the reciprocal of the difference between maximum allowed and the calculated semiconductor junction temperature for the worst case overload operation at standstill. Overall, the 3L-FCC encounters a higher overload stress with the 650 V GaN semiconductors, which are only rated up to 150°C , compared to the 200 V Si MOSFETs rated up to 175°C . Combined

with non-ideal heatspreading and the high loss density in the 3L arrangement this results in a calculated margin of only 7°C . However, the overload stress could be further reduced by more elaborated cooling approaches such as, e.g., heat pipes and heat spreaders, but additional effort compared to the 7L implementations would be required and/or the peak current for standstill overload could be reduced as suggested in [19].

E. SUMMARY OF THE COMPARATIVE EVALUATION

Everything considered, similar nominal efficiencies of around 99% are achieved for all three solutions. The 7L-FCC offers a small inductor volume at the price of a large capacitor volume, numerous gate drives, semiconductors and overall components, which require a spacious PCB to accommodate. Furthermore, for a three-phase system in total 18 passive energy storage elements need to be regulated, resulting in a comparatively high control effort. With the introduction of the 7L-HANPC, not only the efficiency can be slightly improved, but also most other metrics as for example the number of components, the capacitor volume and the control effort. However, the complexity is still not comparable to the 3L-FCC implementation. Since the overall volumes are similar for all proposed solutions, the main drawback of the 3L-FCC lies in a constrained form factor (defined by the relatively large filter inductor volume), which determines in some cases the minimal achievable height of the power electronics of the IMD.

Of course, future trends develop towards more device integration (e.g., Integrated Power Modules (IPM) and Bipolar-CMOS-DMOS (BCD) technologies), where the gate drive and the power semiconductor are integrated on a single chip and/or in a single package. This will strongly lower the number of discrete components in a 7L implementation while simultaneously lowering the required PCB area. However, even though the 7L implementations will benefit more from this trend, the number of discrete components will inevitably exceed those of the 3L-FCC drive, and thus result in a lower reliability. Moreover, the control effort, which correlates with the number of energy storage elements such as flying capacitors, will be unaffected by future device integration.

V. PROPOSED 3L-FCC IMD REALIZATION

Highlighting the very interesting overall trade-offs of the 3L-FCC, a possible IMD realization is shown in Fig. 7. The dimensions of motor and 3L-FCC allow mounting of the power boards (i.e., PCBs that include semiconductors, non-insulated gate drives, flying capacitors, local HF DC link capacitors and the inductor current measurement) directly on the walls of the elongated motor case (cf. Fig. 7(a.ii)). This results in a superior (dynamic) cooling performance for the temperature critical semiconductors. The gate drive insulation (labeled as GD_{iso} in Fig. 7(a.iii)), voltage measurements, controller and auxiliaries (low voltage supplies, encoder, communication interface, etc.) can be placed on an additional PCB on top as no or limited cooling is required. As a side remark, the controller is usually a thermal hot-spot which in this case can be cooled

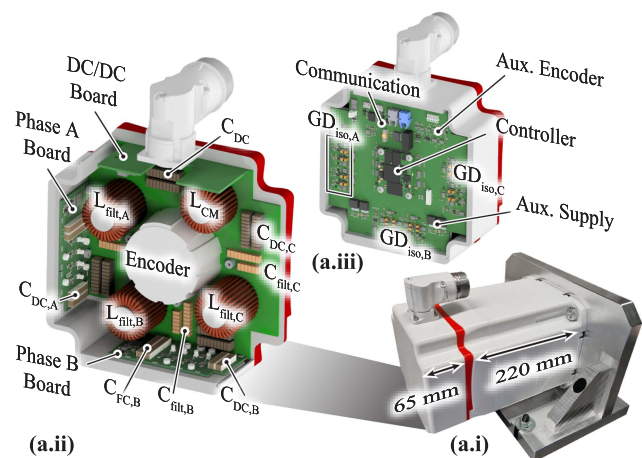


FIGURE 7. Motor-integrated 3L-FCC design. (a.i) Axial extension of the motor housing by 65 mm for inverter placement. (a.ii) Proposed arrangement of the IMD, where the modular power stages (i.e., Phase A Board, Phase B Board and Phase C Board) are directly mounted onto the elongated motor case for improved semiconductor cooling. The output filter as well as additional distributed DC link capacitance are placed around the encoder, while the DC/DC board provides a 800 V to 24 V voltage conversion for supplying measurement, control, and gate drive circuits of the IMD. (a.iii) View on the Top-PCB, which accommodates the isolated gate drive circuits (i.e., $GD_{150,A}$, $GD_{150,B}$ and $GD_{150,C}$), controller, and communication as well as auxiliary circuits.

directly through a Thermal Interface Material (TIM) over the case of the IMD. The LC output filters, additional distributed DC link capacitors as well as a possible CM filter inductor (L_{CM}) to limit the CM EMI emissions into the supplying DC grid [13], [34] are placed around the encoder. Last but not least, a DC/DC board visible in Fig. 7(a.ii) is mounted to the remaining wall and accommodates a 800 V to 24 V power conversion circuit to supply the low voltage electronics directly from the DC link. This proposed IMD solution results in a motor case elongation of only 30%, which is typically acceptable in industrial installations.

VI. CONCLUSION

In this article, three three-phase AC/DC converter hardware prototypes, namely a 7L-FCC, a 7L-HANPC and a 3L-FCC, have been built for the same specifications of an 800 V supplied, 7.5 kW IMD. Thereby, high operating temperatures of the naturally cooled motor ($T_{case} = 90^\circ\text{C}$) require high nominal efficiencies of the converter stage (around 99%) and a low transient thermal impedance of the semiconductor cooling for the short-term overload operation (i.e., 3 times nominal current for 3 s). In order to minimize the volume of the demonstrators, an additional increase in switching frequency during overload operation is implemented, which allows to dimension the passives (e.g., flying capacitors and filter inductors) mainly for nominal operation. All three demonstrators have been tested with 100°C baseplate temperature (incorporates an expected 10°C temperature difference to the 90°C motor case) for nominal and overload operation, including the challenging 3 s motor standstill overload with three times the

nominal peak current flowing continuously in one phase, i.e., with a DC output voltage and peak losses in one single phase.

All in all, the 3L-FCC meets the nominal and overload design targets with a similar total volume as the alternatively considered 7L topologies, although with a different form-factor. Advantageously, it has the lowest complexity in terms of control effort and, due to the small number of discrete components, the highest reliability can be expected, i.e., the 3L-FCC features the most interesting overall trade-offs.

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