IEEE Open Journal of
Power Electronics

Received 20 September 2023; revised 9 October 2023; accepted 18 October 2023. Date of publication 23 October 2023;
date of current version 8 November 2023. The review of this article was arranged by Associate Editor Roberto Armin Fantino.

Digital Object Identifier 10.1109/OJPEL.2023.3326909

Electrothermal Power Cycling to Failure of Discrete Planar, Symmetrical Double-Trench and Asymmetrical Trench SiC MOSFETs

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This work was supported by the U.K. Engineering and Physical Research Council as Supergen Energy Networks Hub under Grant EP/S00078X/2.

ABSTRACT While SiC MOSFETs are now being utilized in industry their robustness under heavy-duty applications still remains a concern. In this paper, the results of experimental measurements of degradation to failure of different structured SiC power MOSFETs, namely the planar, symmetrical double-trench and asymmetrical trench structures are presented following electrothermal stressing by power cycling to beyond the safe operating area (SOA) limits. The tests are categorised in to subsets with/without forced cooling. The first set of tests involve successive switchings of the devices under constant DC current supply while their case temperature is monitored in real-time to evaluate their thermal performance. The symmetrical double-trench and asymmetrical trench MOSFETs are found to experience a higher case temperature rise thus prone to breakdown while failure is not observed in the planar structured device. The second experiment stresses the devices during continuous power cyclings with force cooling applied, in which the symmetrical and asymmetrical double-trench MOSFETs still encounter failure with detectable breakdown on the gate oxides, compared with the planar device which only exhibits degradation, without failure, with indications of aging.

INDEX TERMS SiC MOSFET, double-trench, electrothermal stress, power cycling, trench.

I. INTRODUCTION

Wide-bandgap SiC MOSFETs present advantages like high voltage blocking, fast switching transients and compactness [1], [2], [3]. However, as replacement of the established Silicon counterparts, the robustness under extreme conditions still needs further analysis, i.e. in cases of short-circuits [4], [5], [6] and avalanche [7], [8], while other less severe stress conditions such as the bias temperature instability [9], [10] also need further study.

Temperature swing is a frequent phenomenon that applies electro-thermo-mechanical stress to the semiconductor devices in the circuit. To evaluate the robustness under such conditions, two reliability tests are usually performed: one is applying temperature swing externally by varying ambient temperature, referred to as temperature cycling; and the other being applying temperature swings internally by power dissipation, referred to as power cycling. The power cycling degradation mechanisms are typically categorized into die-associated and package-associated issues. The physics behind the package degradation is covered in [11], where the main reason of degradation is explained to be the mismatch of thermal expansion coefficients between the material layers or melting at hot-spots [12]. This has been reported to be responsible for the increase of on-state resistance and the thermal resistance [13]. The die degradation is also discovered to appear in terms of threshold voltage drift in [14]. The relationship between the power cycling and robustness under other extreme driving conditions such as repetitive short-circuit ruggedness is discussed in [15], [16], [17] which reveals that the power cycled devices, even in absence of indications of degradation, i.e. in transfer characteristics, are more prone to failure at repetitive short-circuit events than the

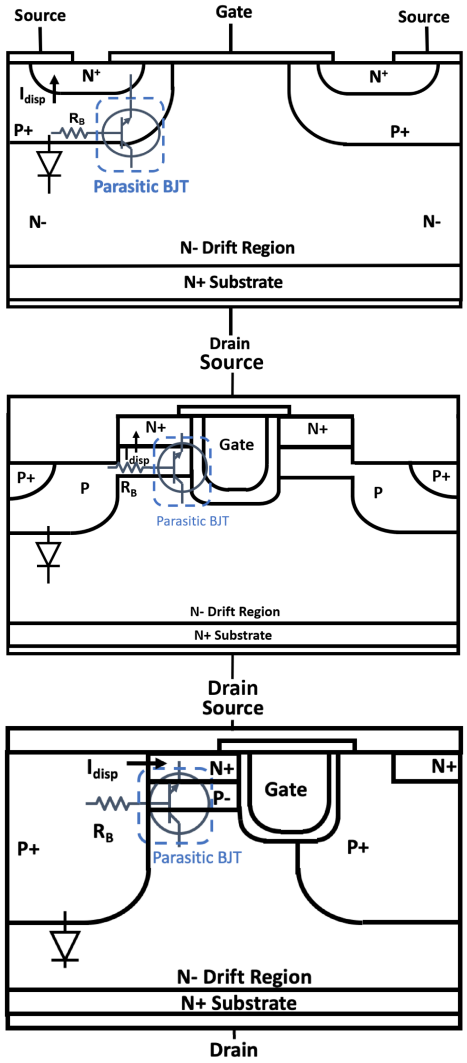

FIGURE 1. From top: cross-section of SiC Planar MOSFET, Symmetrical Double-Trench SiC MOSFET and Asymmetrical Trench SiC MOSFET.

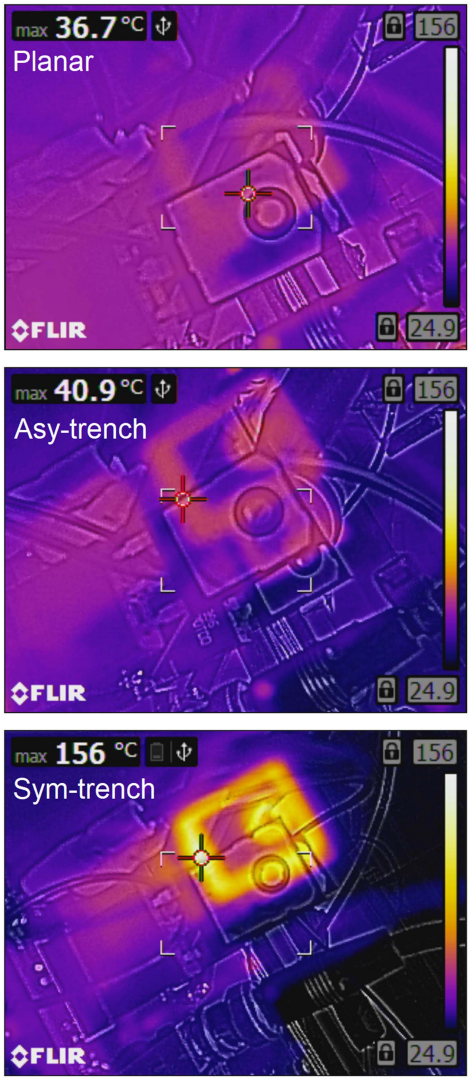

FIGURE 2. Maximum case temperature rise under continuous crosstalk in similarly rated planar, symmetrical and asymmetrical trench MOSFETs [22].

fresh devices. However, these studied have primarily focused on conventional planar structured SiC MOSFETs, while there are newly developed trench-structured SiC MOSFETs with improved dynamic performance [18], [19] which lack similar studies. The cross-sectional schematics for planar structured power MOSFETs and the two trench power MOSFETs as symmetric & asymmetric are shown in Fig. 1. In symmetrical double-trench MOSFETs, the source trench protects the gate trench by reducing the electric field strength [20]. In the asymmetrical trench structure, source trench semi-surrounds the gate trench which further reduces the gate-source capacitance, enabling faster switchings [21].

Even though these different structured power MOSFETs could have similar ratings as given in the datasheet, their performance would differ under the same operating conditions. It is previously shown that the thermal behaviour of these three different structured MOSFETs are distinct in terms of observed case temperature under repetitive crosstalk events with continuous occurrence of shoot-through in [22], [23], [24]. The thermal image of each MOSFET structure at its peak case temperature is shown in Fig. 2 under these repetitive crosstalk events, with the symmetrical double-trench experiencing the highest temperature in contrast to the lowest on the planar MOSFET. Under normal operating conditions, the junction temperature of devices is not expected to exceed the SOA limits. However, in cases such as continuous occurrences of shoot-through current by crosstalk, the junction temperature could rapidly increase beyond the SOA [23]. The measurements of the trajectory of the case temperature rise under repetitive crosstalk for these three structures of MOSFETs is provided in Fig. 3 where it can be clearly seen that even though the devices under test have the same key ratings, their performance under this reliability criterion have been widely different. In typical applications, the working conditions of a switching device is determined by its electrical parameters

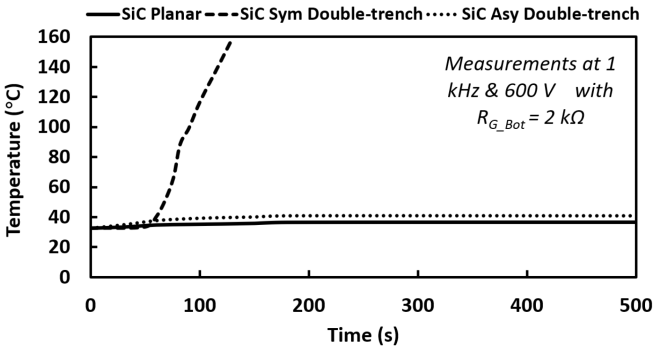

FIGURE 3. Temperature rise profile under continuous crosstalk for SiC planar, symmetrical and asymmetrical trench MOSFETs [22].

such as the load current and DC link voltage through variation of which power cycling experiments electrothermally stress the device. Hence, with different structures, the SiC MOSFETs are experiencing different levels of stress through power cycling. This paper presents the experimental results regarding the robustness of SiC MOSFETs with these three structures during power cycling with identical electrothermal stress.

II. EXPERIMENTAL SET-UP

The measurements are done on devices under test (DUTs) listed as E3M0075120 K as a planar SiC MOSFET rated at 31 A, 1200 V, 75 mΩ & R_{thJC} *of* $0.88\,K/W$, SCT3080 as a symmetrical double-trench SiC MOSFET rated at 30 A, 1200 V, 80 mΩ & R_{thJC} *of* $0.7\,K/W$ and IMZ120R090M1HXKSA1 as an asymmetrical trench SiC MOSFET rated at 26 A, 1200 V, 90 mΩ & R_{thJC} *of* $1\,K/W$, all encapsulated in TO-247-4 packages. Although the selected devices appear to have the same packaging structure of TO-247-4, the different use of materials could lead to performance deviations [25]. For example, the wire bond materials (Aluminium, Copper, etc) and substrate can directly influence the reliability. Nevertheless, this is not a property that can be influence the selection of these closely-rated devices by application engineer as replacements. The case to ambient thermal resistance in the devices is expected to be in the range of 50–100 K/W, dominating the overall junction to ambient thermal path. Power supply ALR3220 is used as a constant current source with the test circuit schematic shown in Fig. 4.

There are two experimental conditions adopted. The first one is demonstrated in Fig. 5(a) in which DUTs are successively switched-on with periods fixed at 20 seconds with DUT turn-ON time T_{ON} equal to 0.5 sec and 1 sec, with a constant supply of current. Here, the DUT is not equipped with an external heatsink so cooling happens via still air at room temperature which results in accumulation of heat and hence referred to as 'successive turn-ON' sequence. This enables finding out the thermal gradient of the three devices, i.e. how fast each device heats-up under same level of power, and to determine the failure points at high temperatures

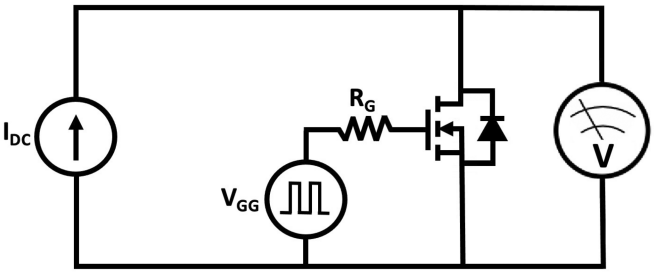

FIGURE 4. Test circuit schematic.

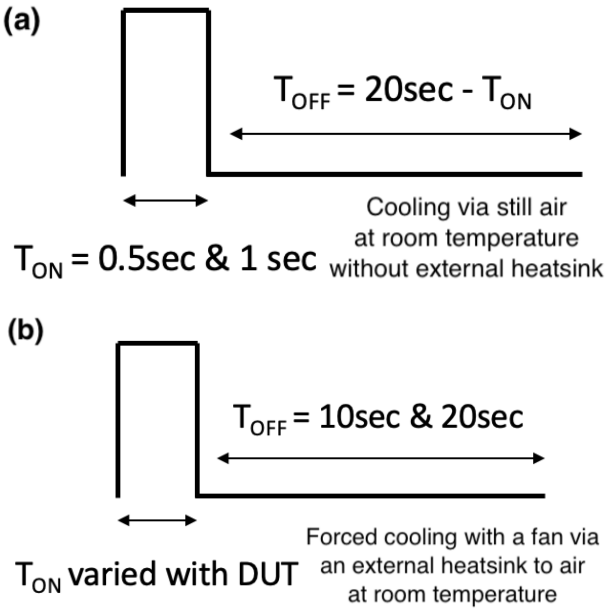

FIGURE 5. Experimental procedures for the (a) successive turn-ON tests and (b) power cyclings.

when the cooling is not as effective [26], [27]. The second approach achieves the power cycling with forced cooling and is demonstrated in Fig. 5(b). Here, the turn-ON time varies with different DUTs under constant supply of current until the targeted peak junction temperature is achieved, then DUTs are turned-OFF for 10 sec and 20 sec periods, respectively, during which forced air cooling happens with an external fan. A heatsink is also screwed to the DUTs with thermal pad SP2000-0.015-00-122 in between to assist the effectiveness of cooling, so the temperature swing is larger than the 'successive turn-ON' experiment. Thermal camera FLIR E5-XT with time resolution of 3.7 datapoints per second was used for real-time monitoring of the case temperature while the drain-source voltage of the DUTs are measured during conduction as an indicator for estimation of the internal junction temperature of the device. The thermal camera is targeting at the backside of the device which is painted in black to improve measurement accuracy.

The typical indicators for temperature are the threshold voltage and the body diode forward voltage [28], [29]. Here,

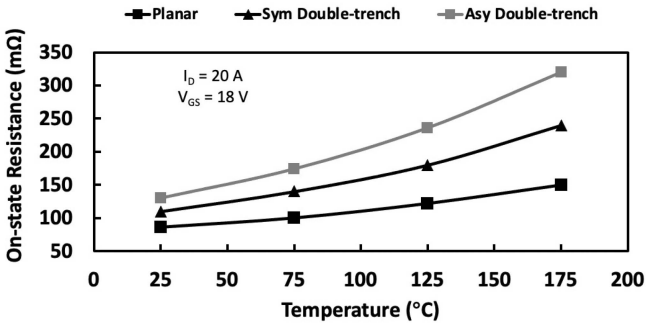

FIGURE 6. Calibration measurements of on-state resistance against temperature.

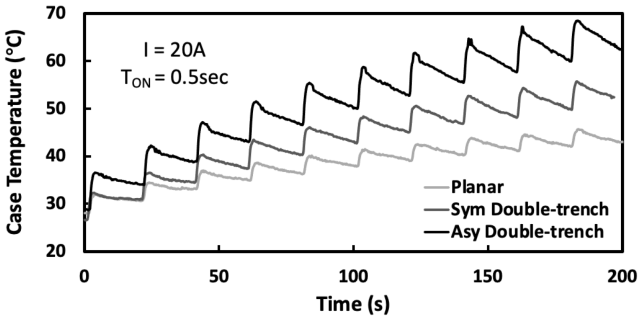

FIGURE 7. Case temperature rise at 10 successive turn-ON events of 0.5 sec by 20 A.

to analyse the thermal behaviour of DUTs, the on-state resistance at a fixed gate voltage is utilized to virtually indicate the junction temperature. The measured on-state resistance of the DUTs at 20 A calibrated to temperature is shown in Fig. 6. The applied gate-source voltage is fixed at 18 V and is used for the experiments unless otherwise specified. To avoid the self-heating effect during the measurements, the current pulse injected lasts only 10 ms with no change in drain-source voltage observed across this period, indicating that self-heating has been negligible.

III. EXPERIMENTAL MEASUREMENTS

As described in Fig. 5, the performance of DUTs will be measured by undergoing two distinct range of measurements. The first will be 'successive turn-on' which will effectively heat up of the device at the two conditions of 'same current' and 'same power' to analyse the heat accumulation trajectory between the three device structures. This is repeated for 'same power' in an attempt to cancel the impact of small differences in the on-state resistance of selected DUTs as these are selected to be close but still were not identical. To enable heat accumulation, no enforced external cooling mechanism is applied. In the second range of measurements, the devices undergo power cycling comprised of heat generation, and enforced air cooling periods. This is continued until failure or observable degradation of devices to evaluate the robustness under the same level of electrothermal stress.

A. SUCCESSIVE TURN-ON

Under the test conditions demonstrated in Fig. 5(a), the DUT first experiences 20 A of constant current supply flowing through for 0.5 sec followed by 19.5 sec OFF time before the next cycle initiates. DUTs are not equipped with heatsinks, so the minimal cooling is just by the still air at room temperature to the case of device. Fig. 7 shows the measured case temperature under such conditions for 10 successive turn-ON events. Under the same stress conditions, the three DUTs display different trends of rise of the case temperature. The fastest temperature increase is seen in the asymmetrical trench device while the least is seen in the planar. This corresponds to the on-state measurement in Fig. 6 which had indicated that under the same conduction current, the on-state resistance determines the power dissipation together with its slight trend of rise of on-state resistance. The temperature increase gap becomes progressively larger as the number of turn-ON cycles increase.

After 50 turn-ON events, the peak case temperature in the asymmetrical trench device reaches 150 °C while it is still 75 °C for the symmetrical double-trench device and 50 °C for the planar device as shown in Fig. 9. At the 40th turn-ON cycle in asymmetrical trench device, as annotated in Fig. 8, the device encounters failure with short-circuit detected between the drain and source terminals due to the rapid increase of the case temperature. The measurements suggest that the drain-source short-circuit happened after the device turned-OFF since there is a short period during which the case temperature drops prior to the rise-up of the case temperature. Therefore, thermal runaway mechanism is unlikely to be the main contributor to this failure case with short-circuit between the drain and source terminals. By further stressing of the DUT, short-circuit also happens between the gate and source terminals. This is due to the charge-dependent oxide breakdown when charge is trapped into the oxide and develops locally high electric fields that breaks SiO_2 bonds [30], [31] by charge trapping on the gate oxide which develops locally high electric field. It has also been experimentally proven that high temperature would accelerate this process [32], [33]. Therefore, it is established that the device failure is a consequence of the initial oxide breakdown between gate and source, leading to device turn-OFF, followed by oxide breakdown between gate and drain so that drain-source once again indirectly conducts current.

Following on, the turn-ON time is increased from 0.5 sec to 1 sec while turn-OFF time is decreased to 19 sec to maintain the constant period of 20 sec. This helps the heat generation but suppresses the cooling thus more heat is accumulated, so the DUTs are more prone to failure. Up to 25 successive turn-ON cycles are performed with results shown in Figs. 10 and 11. Under this stressing condition, the asymmetrical trench device failed after only 5 switchings, and symmetrical double-trench failed after 20 switchings, compared with the planar device that survived all the 25 switching events. In the cycle of

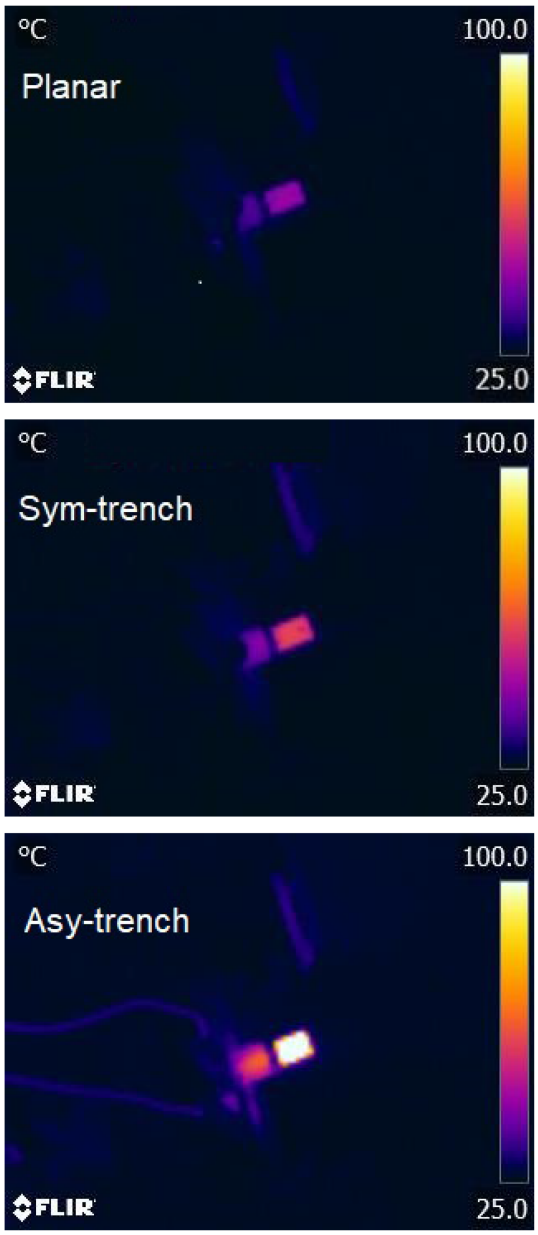

FIGURE 9. Thermal image indicating the peak case temperature reached during 50 successive turn-ON under 20 A and 0.5 sec turn-ON time.

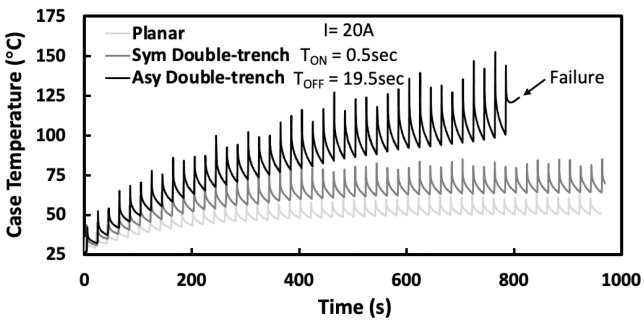

FIGURE 8. Case temperature rise at 50 successive turn-ON events of 0.5 sec by 20 A.

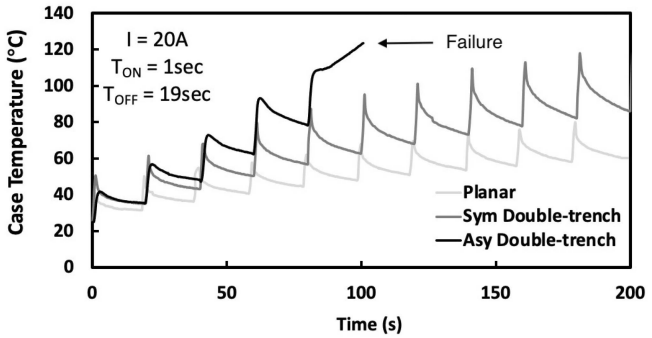

FIGURE 10. Case temperature rise at 10 successive turn-ON events of 1 sec by 20 A.

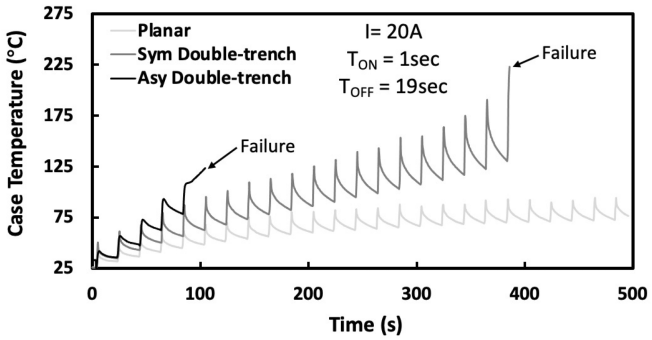

FIGURE 11. Case temperature rise at 25 successive turn-ON events of 1 sec by 20 A.

failure, the on-state resistance at the ramp-up point measured for asymmetrical and symmetrical double-trench MOSFETs are 205 mΩ and 195 mΩ, respectively. Referring to Fig. 6, the starting junction temperature at the cycle of failure is estimated to be approximately 100 °C for asymmetrical trench MOSFET and 150 °C for the symmetrical double-trench MOSFET. Thermal runaway has reported to be able to happen on SiC power MOSFETs at much lower junction temperatures than the material temperature limit (800 °C for SiC) [34]. With such ineffective cooling by still room-temperature air and without a heatsink, it is possible to rapidly push the symmetrical and asymmetrical trench DUTs into thermal runaway mode and the subsequent failure.

When lowering the stressing conditions to 10 A and 1 sec turn-ON periods, all three DUTs retain their functionality up to 50 switchings, with the case temperature measurements shown in Fig. 12 and Fig. 13. The temperature still exhibits the same trend with further case temperature increase exhibited in the asymmetrical trench device followed by the symmetrical double-trench DUT and then the planar DUT, though the difference between asymmetrical and symmetrical double-trench is now less clear as shown in Fig. 8 due to the smaller power dissipation by the DUT at a lower current. Such difference can be categorized by two factors, the power dissipation and the thermal resistance to the ambient. Since the DC current supplies a constant level of current, the different on-state

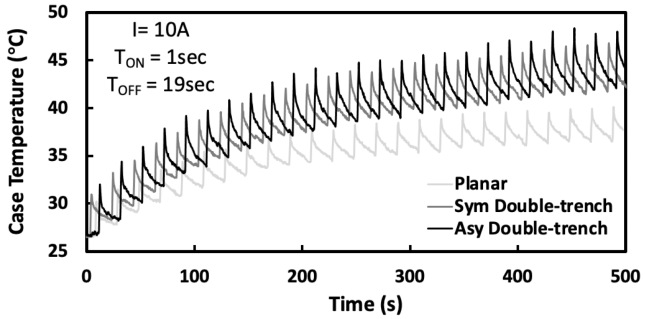

FIGURE 12. Case temperature rise at 25 successive turn-ON events of 1 sec by 10 A.

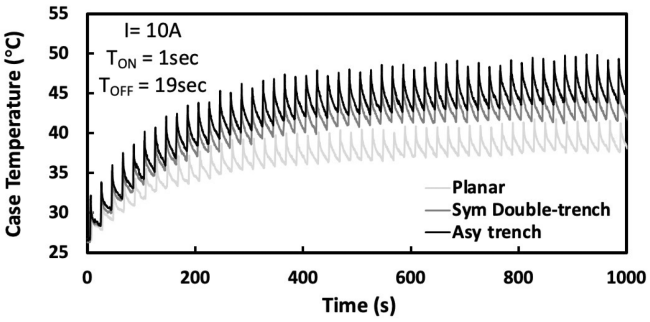

FIGURE 13. Case temperature rise at 50 successive turn-ON events of 1 sec by 10 A.

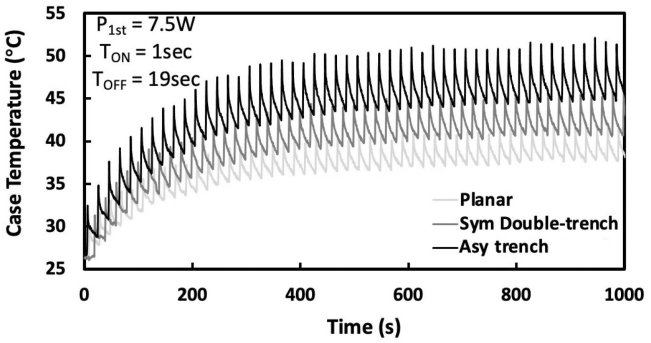

FIGURE 14. Case temperature rise at 50 successive turn-ON events of 1 sec by 7.5 W.

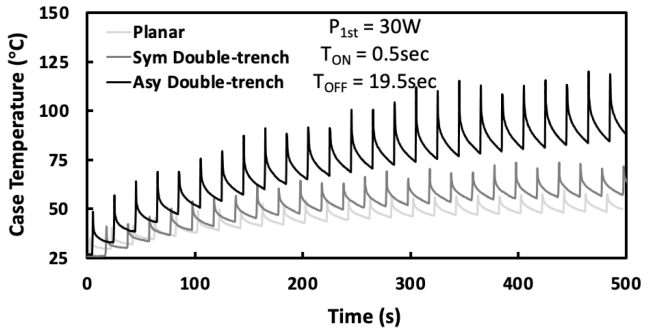

FIGURE 15. Case temperature rise at 25 successive turn-ON events of 0.5 sec by 30 W.

resistance of DUTs results in different power dissipations, with the values stated in Section II, although all are relatively close. The three DUTs are encapsulated in the same type of package of TO-247. Since no external heatsink is connected to the devices, their thermal junction-to-ambient resistance are close, verified by the thermal resistances given in the datasheets. These experiments are performed at the same current level for all three DUTs which generate different power dissipations. However, by intentionally adjusting the current level according to the individual DUT's on-state resistance, the calculated power dissipation can be set to be identical. Despite applying the proportional power level to offset the differences in the on-state resistance, the case temperature of the three DUT structures still deviates from one other under multiple switching cycles. This is because temperature changes their operational properties in different manners, i.e. varying rate of rise of the on-state resistance with temperature.

Considering the individual DUTs' on-state resistance at 25 °C, the precise current level is calculated for the two selected power values of 7.5 W and 30 W, so that at the instant after the first turn-ON cycle, the power dissipation is identical in all three DUTs. The recorded case temperatures are shown in Figs. 14 and 15. The corresponding thermal images of the DUTs' packages have been captured at the instant when the peak case temperature is obtained for identical 30 W experimental condition as shown in Fig. 16. Even though the initial power dissipation is controlled identically the case temperature the asymmetrical trench MOSFET still leads the symmetrical double-trench and the planar DUTs. This observation is due to two reasons. Firstly, the thermal characteristics vary, as despite the datasheets giving similar junction-case thermal resistance among the three DUTs, it still can lead to different heat dissipation efficiency considering the case to ambient resistance while the die area embodying the thermal capacitance is also of different sizes. The difference in the die sizes are shown by CT-scan imaging of the three SiC power MOSFETs in Fig. 17 which demonstrates that the planar and symmetric trench device have areas of 5.75 mm^2 while the size of the asymmetric device is 2/3 of these devices to 3.6 mm^2. Secondly, the on-state resistance of SiC MOSFETs rise with temperature which has the potential to lead it to thermal runaway. The sensitivity of devices' on-state resistance to temperature differ, and even small difference in temperature rise could be amplified leading to varying levels of rise of temperature in different structures.

B. POWER CYCLING

Once the trajectory of temperature rise for the DUTs is established at the normalised current level per on-resistance for the same power, the DUTs undergo the power cycling experiment condition that was demonstrated in Fig. 5(b). Equipped with the heatsink under enforced air cooling with a fan, the junction swing is now more significant, while the on-state resistance

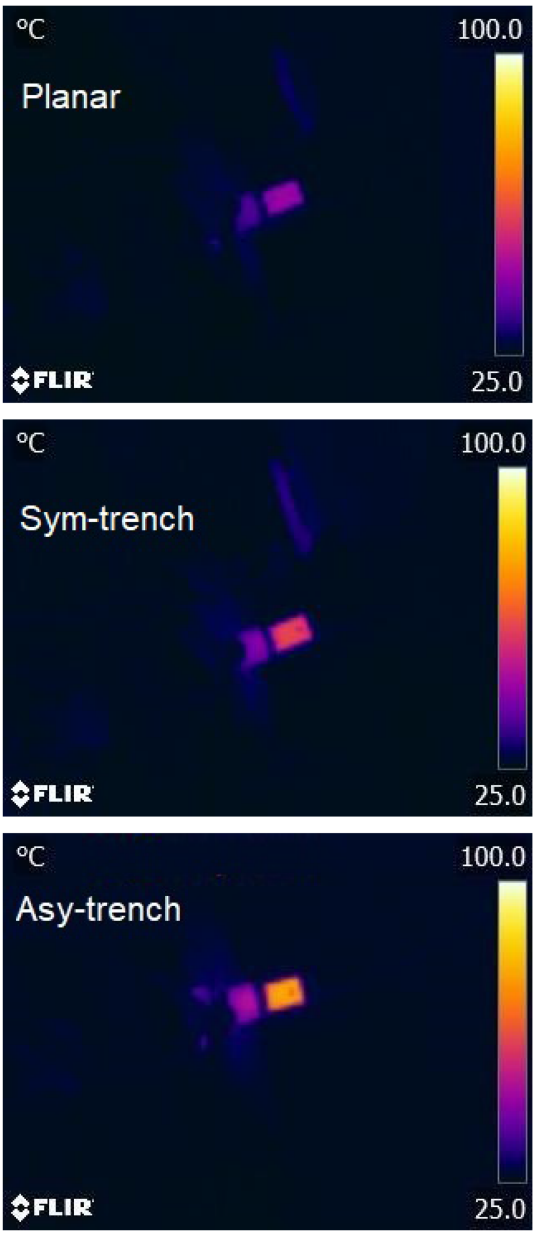

FIGURE 16. Thermal image indicating the peak case temperature reached after 25 successive turn-ON under 30 W and 0.5 sec turn-ON time.

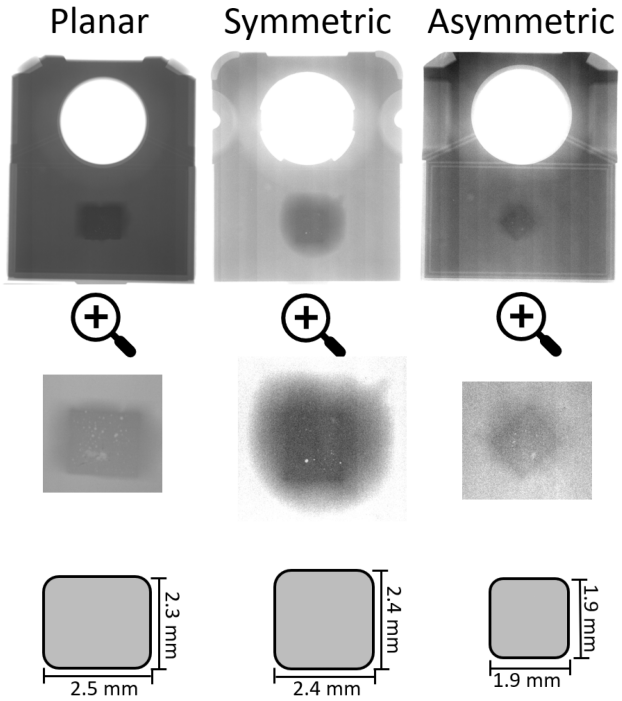

FIGURE 17. Die sizes by CT-scan imaging of the three SiC power MOSFETs with the planar and symmetric trench device areas of 5.75 mm^2 while the size of the asymmetric device is 2/3 of these devices to 3.6 mm^2.

is used to estimate the junction temperature. Fig. 18 show the heat accumulation phenomenon in symmetrical and asymmetrical trench MOSFETs when the turn-ON time is set to heat the junction from 25 °C to 175 °C and the turn-OFF time is set fixed to 10 sec. Although the drain-source voltage at the start of each cycle is close, the drain-source voltage at the end of cycles drift up with increase of number of cycles for the symmetrical double-trench DUT. As for the asymmetrical trench MOSFET, the rise of junction temperature is very fast resulting in highly increased on-state resistance, hence, the drain-source voltage measured in those later cycles are flattened, indicating that the current supply enters the voltage control mode, in this case at 9 V. It is noted that under the same condition, the temperature at the planar DUT is not even able to reach 175 °C.

Fig. 19 shows the same measurement under 20 A supply current and the same external cooling set-up, with the asymmetrical trench DUT requiring the shortest pulse length to reach 175 °C, while planar enters thermal equilibrium at around 125 °C. By feeding 20 A at the same pulse length of 3.5 sec, the drain-source voltage variation with time is compared in Fig. 20, where it can be seen that heating by 20 A DC current is not impacting the planar DUT but is significant on the asymmetrical trench DUT displayed in terms of drain-source voltage rise up with time.

By lowering the current pulse length, the junction temperature in DUTs is now rising from 25 °C to only 100 °C in the first switching cycle with 20 A current supply by extending the cooling time to 20 sec. Here, the drain-source voltage measurements at increasing cycles are plotted in Fig. 21. The drain-source voltage drifts up for all three DUTs, signifying that there is still additional heat remained from the previous cycle. This phenomenon is more significant when the current pulse length is increased so that 175 °C is reached at the end of the first cycle, as illustrated in Fig. 22 and will push the device beyond its SOA. In this case, the heatsink attached to DUTs are adjusted, under which it takes 10 sec for the planar DUT to reach 175 °C with 20 A, while this is 1.8 sec for the asymmetrical trench DUT and 6 sec for the symmetrical double-trench DUT. As seen in Fig. 19, the planar DUT is not able to reach 175 °C with 20 A, so its driving gate voltage is lowered to 13 V from 18 V to raise its on-state resistance

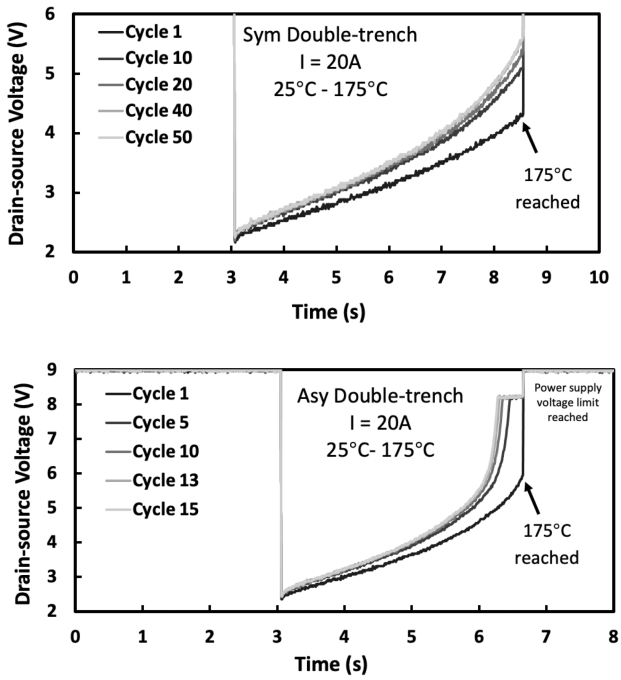

FIGURE 18. Drain-source voltage of the symmetric and asymmetric trench MOSFETs under repetitive cycling with junction rise from 25 °C to 175 °C (the planar DUT cannot reach 175 °C under this condition, thus not included).

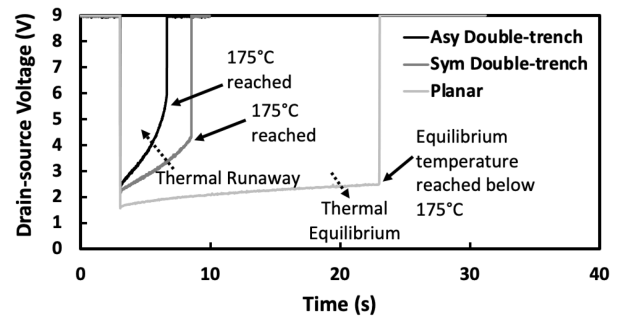

FIGURE 19. Drain-source voltage variation in accordance with constant 20 A current heating time until junction temperature reach 175 °C for the 3 DUTs.

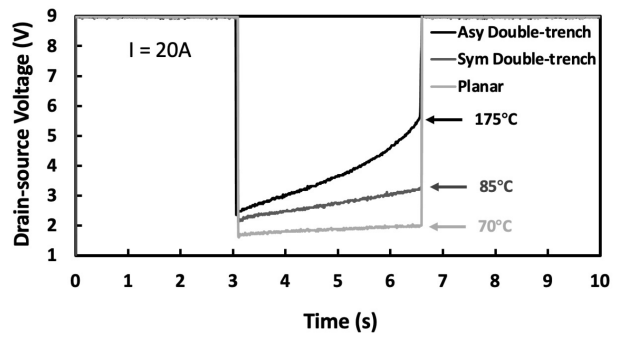

FIGURE 20. Drain-source voltage variation in accordance with constant 20 A current heating for 3.5 sec for the three DUTs.

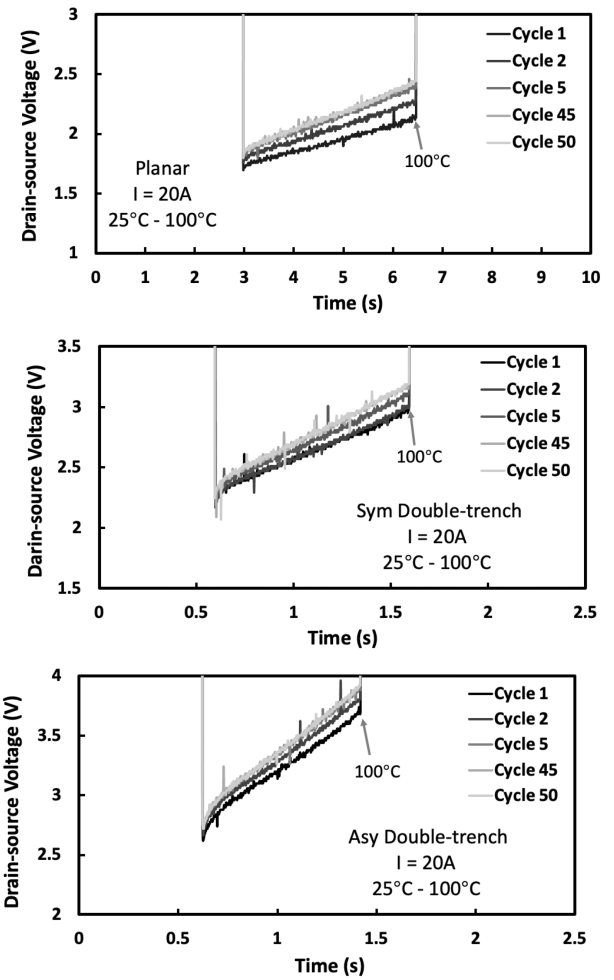

FIGURE 21. Drain-source voltage under power cycling condition of junction temperature rising from 25 °C to 100 °C, by 20 A with 20 sec cooling time.

from 86 mΩ to 120 mΩ at 25°and from 150 mΩ to 165 mΩ at 175°. Even with intentionally reduced gate voltage on the planar DUT, it still has lower on-state resistance compared with the other two trench DUTs at 18 V gate-source voltage.

The DUTs are cycles for 500 cycles at 20 A, with junction temperature swinging from 25 °C to 175 °C in the first cycle with the 20 sec cooling time. The transfer characteristics of the DUTs as well as the 3rd quadrant conduction characteristics after the stress are obtained using the Keysight source measure unit B2902 A. Results are presented in Fig. 23 for the post 500 cycles, while Figs. 24 and 25 show this for post 1000 cycles. The transfer characteristics are measured under 0.1 V constant drain-source voltage and gate-source voltage sweeping from 0 V to 20 V. Looking at the low gate-source voltage operation region, there is some rightward shift of the post-stress curve for the asymmetrical trench DUT but not clear for the other two DUTs while at high gate-source voltage operation region, there is also some change of the on-state resistance. The 3rd quadrant conduction characteristics are

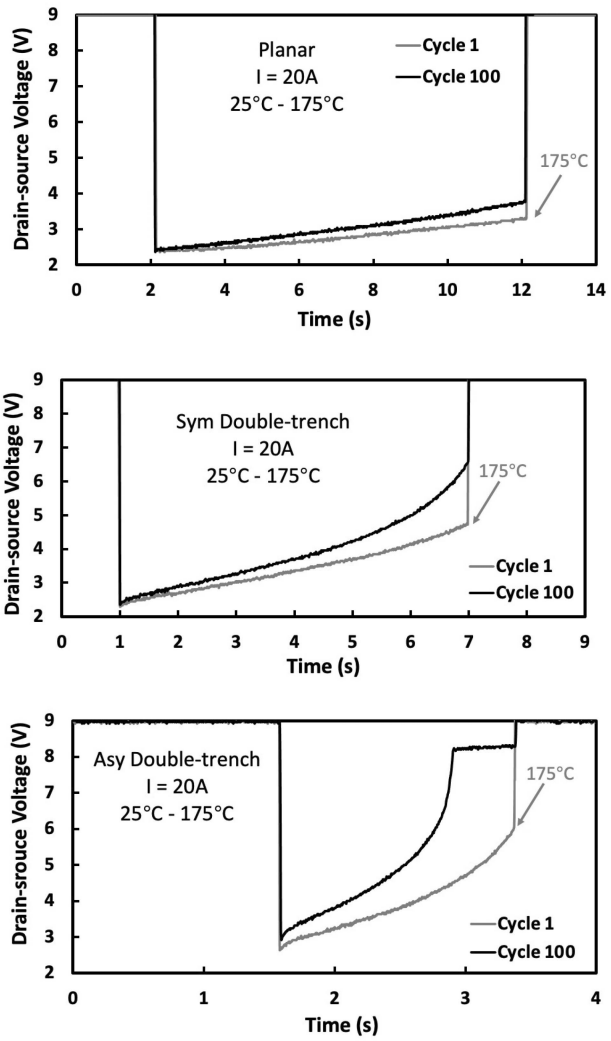

FIGURE 22. Drain-source voltage under power cycling condition of junction temperature rising from 25 °C to 175 °C, by 20 A with 20 sec cooling time.

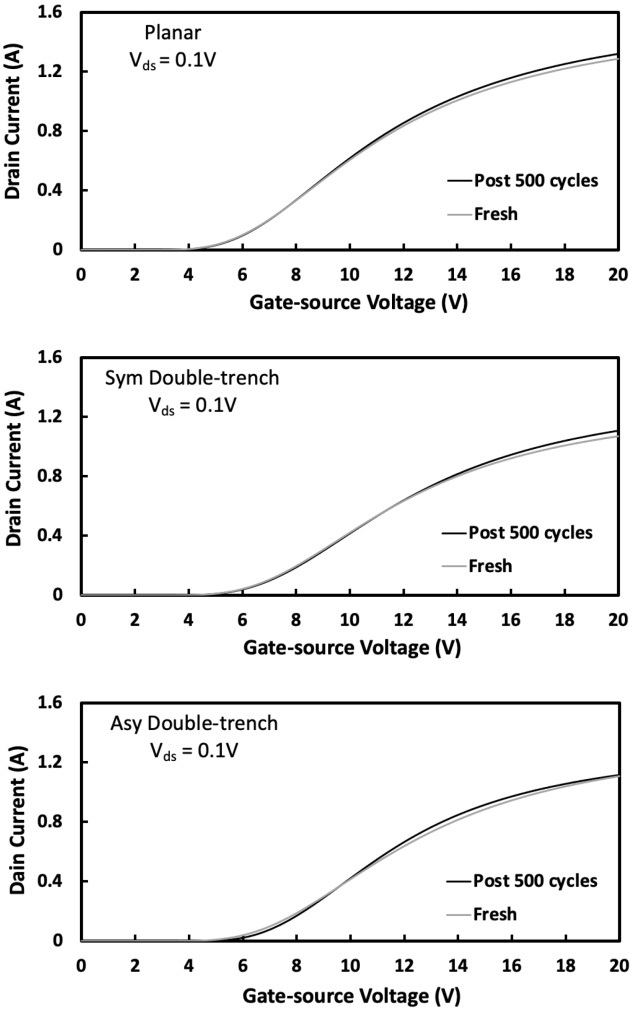

FIGURE 23. Transfer IV characteristics of DUTs after 500-cycle power cycling of 20 A current with 20 sec cooling and the junction temperature rising from 25 °C to 175 °C in the first cycle in comparison with fresh state.

obtained using 100 mA sense current feeding from the source to drain while gate-source voltage is sweeping from 0 V to -8 V. The intentionally applied low sense current is to exclude the impact of any parasitic resistance on the device. Results are plotted in Fig. 25 and show that there is some minor deviations between the post-stress and fresh-state measurement. It must be noted that direct temperature measurements at the case indicate temperatures lower than its junction due to the thermal capacitance and resistance in the path from junction to case, which could be lower than the SOA range at the case but not at the junction.

Since under the power cycling condition of 1000 cycles with 20 sec cooling time with the junction temperature rising from 25 °C to 175 °C in the first cycle, the DUTs still did not show any obvious sign of degradation in terms of deviations in transfer characteristics or the 3rd quadrant conduction characteristics, the stressing period is enhanced by decreasing the cooling time to 10 sec in an attempt to accelerate aging toward failure. In this scenario, when the DUTs enter the thermal equilibrium, the and maximum junction temperature is raised. The experiments show that asymmetrical trench DUT survived only 237 cycles while the symmetrical double-trench DUT survived 494 cycles. Since these two DUTs failed during the cycling, the transfer characteristics and 3rd quadrant conduction characteristics could not be extracted. Therefore, the drain-source voltage measurement at different cycles are presented to exhibit the transition process of the two double-trench DUTs from healthy to failure.

In Fig. 26, the drain-source voltage measurement is plotted at steps of 100 cycles until the last cycle. During the entire experiment, the symmetrical double-trench DUT consistently exhibits drift up of the drain-source voltage, and this drift is becomes more significant closer to the last cycle before failure. In the case of the asymmetrical double-trench DUT, however, no drifting on the drain-source voltage can be observed which means it has entered a stable thermal

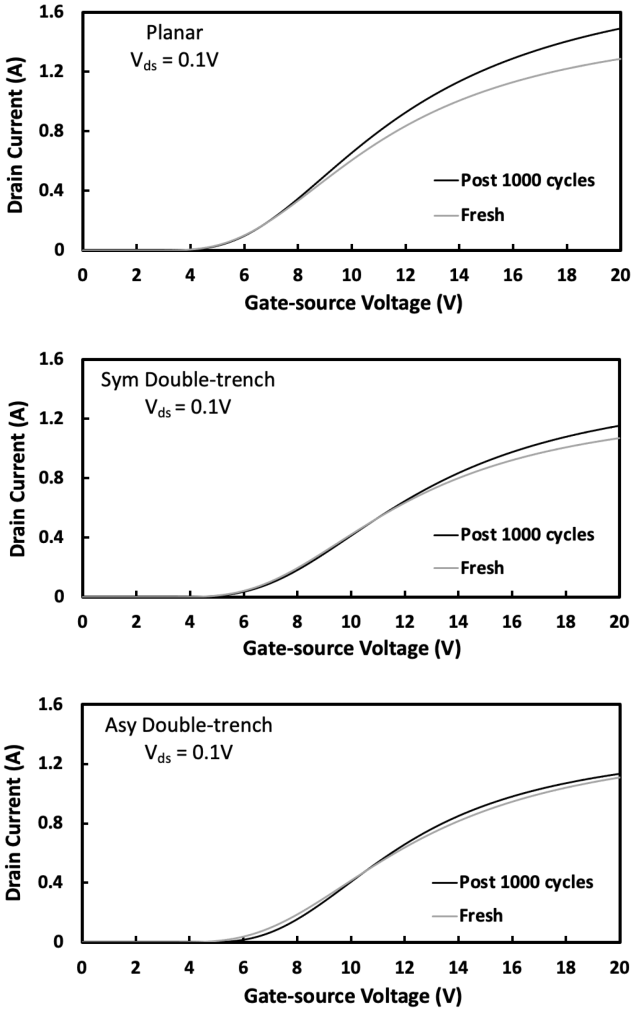

FIGURE 24. Transfer IV characteristics of DUTs after 1000-cycle power cycling of 20 A current with 20 sec cooling and the junction temperature rising from 25 °C to 175 °C in the first cycle in comparison with fresh state.

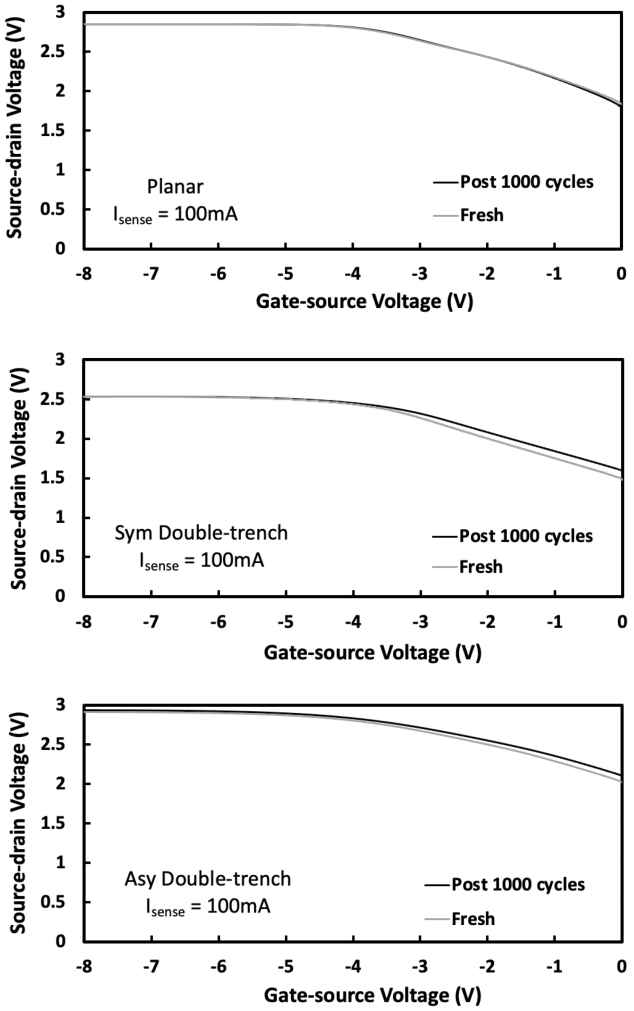

FIGURE 25. The 3rd quadrant forward voltage of DUTs after 1000-cycle power cycling of 20 A current with 20 sec cooling and junction temperature rising from 25 °C to 175 °C in the first cycle in comparison with fresh state.

saturation state. In Fig. 27, the drain-source voltage is plotted in smaller steps of cycles at proximity of the failure point, with the arrow pointing out to the failure point. The symmetrical double-trench DUT at the cycle of failure has an abnormal fluctuation of drain-source voltage followed by a step increase of drain-source voltage lasting until completion of the cycle, suggesting a sudden increase of the on-state resistance. The asymmetrical trench DUT is destroyed in the midst of the turn-ON phase, represented by the drain-source voltage reaching 9 V limited by the voltage limit of the current supply, significantly earlier than the previous cycles. Both failed DUTs have their gate and source terminals short-circuited but not on drain and source terminals. In the last cycle of failure, the symmetrical double-trench DUT completes the turn-OFF in time despite showing abnormality in the drain-source voltage measurement at turn-ON phase. This suggests that the gate oxide layer breaks when the symmetrical double-trench is at the OFF state while heating is spreading over the entirety of the DUT. Since the applied gate voltage is low and within the recommended range of the datasheets, the oxide breakdown is attributed to the charge trapping with the charge trapped in the oxide layer building up locally high electric field strength and finally destroying the oxide. This failure mode is not seen in the planar MOSFET since this failure process is temperature dependent, with the high temperature leading to earlier failure. The planar MOSFET has lower on-state resistance even with lowered driving gate-source voltage compared with the two trench MOSFETs. Hence its junction temperature in these power cycling experiments is not raised high enough to fail it. The reading of the peak on-state resistance reached in the last cycle before failure for the symmetrical and asymmetrical trench MOSFETs is 490 mΩ and 500 mΩ, respectively. Since these values are beyond the temperature calibration range in Fig. 6, the peak junction temperature is estimated by doing linear extrapolation along the line from 25 °C to 175 °C, which yields 463 °C and 317 °C for the symmetrical and asymmetrical trench MOSFETs, respectively. Since the on-state resistance to temperature would approach a quadratic shape as temperature rises, the estimated values would be an

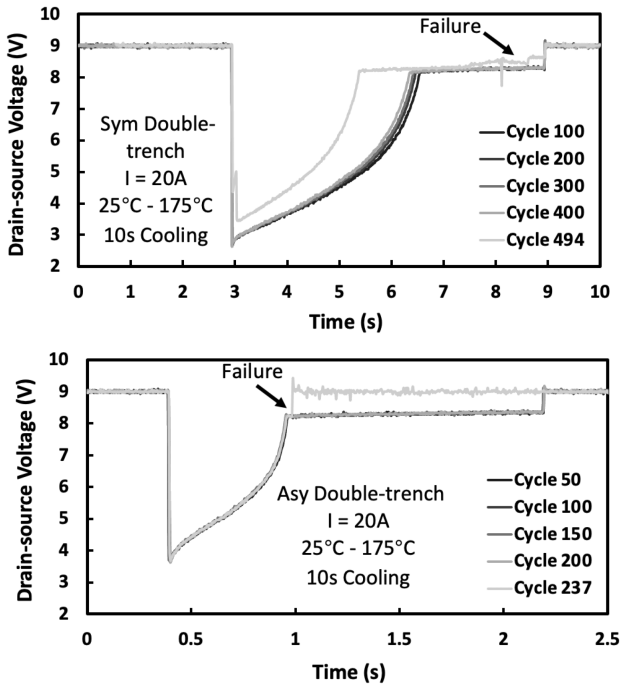

FIGURE. 26. Drain-source voltage measurement at different cycles under 1000-cycles power cycling with 20 A current by 10 sec cooling. The junction temperature has raised from 25 °C to 175 °C in the cycles up to failure (Planar DUT is not failed thus not included).

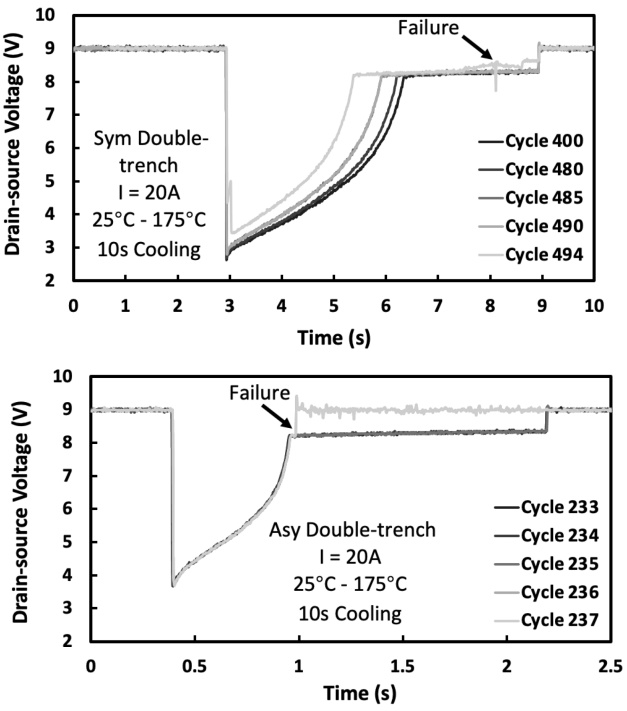

FIGURE 27. Drain-source voltage measurement at different cycles under 1000-cycles power cycling with 20 A current by 10 sec cooling. The junction temperature has raised from 25 °C to 175 °C in the cycles at proximity to failure point (Planar DUT is not failed thus not included).

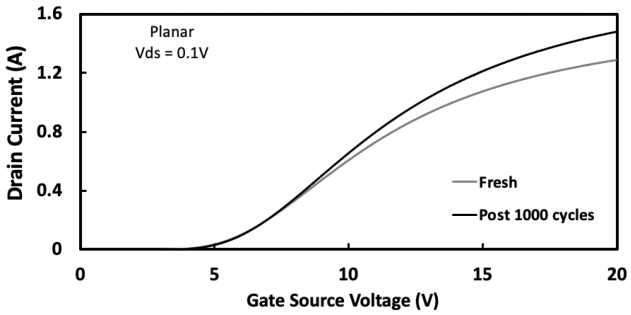

FIGURE 28. Transfer IV characteristics of the planar DUT after 1000-cycles power cycling with 20 A current by 10 sec cooling. The junction temperature has raised from 25 °C to 175 °C in the cycles in comparison with the fresh state (two trench DUTs are failed thus not included). The degradation short of failure can be seen by the change in the IV curve of the device.

overestimate As for the planar MOSFET, since it is not failed, its peak on-state resistance at the final 1000th cycle is selected and measured as 180 mΩ, which gives an approximation of the peak estimated junction temperature of 243 °C. It must be noted that as the number of cycle increase, the temperature within the device increases beyond the SOA, thus the on-state resistance increases exponentially to values outside the normal range. The transfer characteristics of the planar device after 1000 cycles is in Fig. 28 which indicates degradation short of failure compared with the fresh state.

IV. CONCLUSION

In this paper, the case temperature of selected planar, symmetrical and asymmetrical trench SiC MOSFETs are measured under successive switchings under identical electrical conditions with no heatsink to demonstrate their thermal trajectory of temperature rise. It is transpired that the asymmetrical trench MOSFET has the highest level of heat generated in its junction compared with the symmetrical double-trench and planar MOSFETs, respectively. The symmetrical double-trench MOSFET also shows the same failure characteristics but requires more switching cycles until failure while the planar remains functional until the end of the planned experiment. The measurements are continued with power cycling, where degradation is characterized by the electrical parameters of DUTs. When cooling time is set as 20 sec, none of the three device structures degrades while with cooling time reducing to 10 sec, both the symmetrical and asymmetrical trench MOSFETs fail with the gate-source terminals short-circuited after intensive switchings while the planar MOSFET survived past 1000 cycles with degradation observable on its IV characteristics.

ACKNOWLEDGMENT

All underlying data to support the conclusions are provided within this paper.

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