

# Design of SiC-Si Hybrid Interleaved 3-Phase 5-Level E-Type Back-to-Back Converter

MARCO DI BENEDETTO <sup>1</sup> (Member, IEEE), ALESSANDRO LIDOZZI <sup>2</sup> (Member, IEEE),  
AND PETAR J. GRBOVIĆ <sup>3</sup> (Senior Member, IEEE)

<sup>1</sup>Department of Industrial, Electronic and Mechanical Engineering, University of Roma Tre, Via Vito Volterra 62, 00146 Roma, Italy

<sup>2</sup>Department of Engineering Civil, Computer Science and Aeronautical Technologies, University of Roma Tre Via della Vasca Navale 79, 00146 Roma, Italy

<sup>3</sup>Innsbruck Power Electronics Laboratory (i-PEL), University of Innsbruck, 6020 Innsbruck, Austria

CORRESPONDING AUTHOR: MARCO DI BENEDETTO (e-mail: marco.dibenedetto@uniroma3.it)

**ABSTRACT** In modern applications, such as variable frequency electric drives, aircraft propulsion, electric vehicles, and uninterruptible power supply units, high power-dense, and efficient AC-AC power converters are the key to reducing power losses, thus limiting the overall costs, and improving the system's reliability. Power electronic equipment can be enhanced thanks to the continuous evolution of conversion topologies and advancements in power semiconductor technology. The design and the optimization strategy of the AC-AC 5-Level converter, called Interleaved 3-Phase 5-Level E-Type Back-to-Back Converter (I-3 $\Phi$ 5L BTB E-Type Converter), has been proposed in this article. The converter is analyzed and experimentally characterized to prove the configuration's high efficiency and high-power density. An introduction to the characteristics of the I-3 $\Phi$ 5L BTB E-Type Converter is described, and afterward, the optimization methodology to design the multilevel converter is presented. The converter prototype is illustrated, which achieves a peak efficiency of 98.2% and a total weight of 6.18 kg using hybrid technology for power semiconductors.

**INDEX TERMS** Multilevel converter, wide bandgap devices, high performance, interleaved topology, power density, specific power.

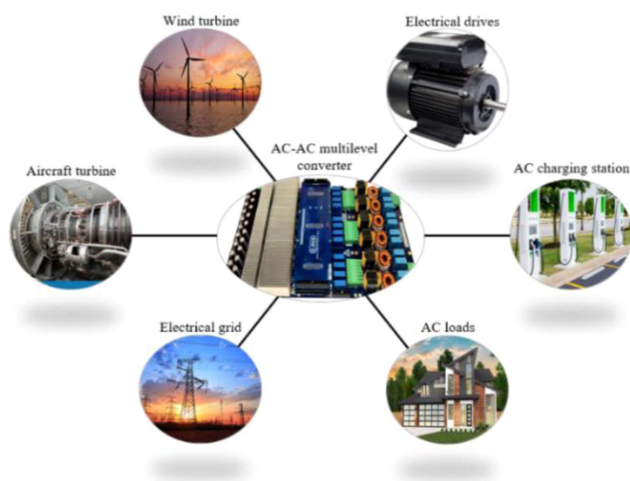
## I. INTRODUCTION

### A. MOTIVATION

High-efficiency and high-power density power conversion systems are fundamental to our life in a wide range of industrial applications such as pumps, compressors, fans, mills, conveyors, transportation (e.g., electric vehicles and railway traction), manufacturing, petrochemical, high voltage direct current (HVDC) transmission, reactive power compensation, wind energy conversion systems and microgrids [1], [2], [3]. Fig. 1 shows the potential applications for a power conversion system based on the multilevel topology to enhance efficiency and power density.

For instance, in Variable-Frequency Drives (VDF) applications, where the source is the aircraft turbine or wind turbine directly connected to the Permanent Magnet Synchronous Generator (PMSG), or in Uninterruptible Power Supplies (UPS) applications, where the source is the grid, the multilevel converter can drastically reduce the current ripple injected through them. In some of these applications,

the double conversion system AC/DC-DC/AC (AC-AC) is required to control the amplitude and frequency, as well as the power factor from the source and the load. Over the past decade, several AC-AC power converters have been developed and commercialized in the form of standard and customized products [4], [5], [6]. The AC-AC converter topologies can be categorized into two groups. In the first one, the AC-AC conversion includes an intermediated DC energy storage component like inductors or capacitors. Voltage Source Converters (VSC) and Current Source Converters (CSC) belong to this group [7]. In the second group, the AC-AC conversion occurs without an intermediate DC energy storage component, such as a matrix converter and cycloconverters [8]. Over the past decade, AC-AC VSCs, that use a DC capacitor as a storage element in the DC-bus, exhibited higher market penetration and more evident development than CSCs and matrix converters [9], [10]. The multilevel converters provide the most prominent developments in VSCs topologies, which have significant advantages compared to two-level converters



**FIGURE 1.** Application of AC-AC power conversion based on multilevel topology.

[11]. Thus, by introducing multilevel topologies, the characteristics of the AC-AC converters with an intermediate section of DC-bus capacitors are significantly improved in terms of efficiency, power density, quality of the waveform, low common-mode voltage, and possible fault-tolerant operation in some instances [12], [13].

An additional benefit of the multilevel converters is to increase the switching frequency by reducing the size of the passive components if the current ripple injected in the source is kept constant. The other benefit of using a multilevel converter to feed the loads, such as electrical drives, AC charging stations, or simple appliances loads in households, is to have low Total Harmonic Distortion (THD) of the injected voltage or current [14].

### B. REQUIREMENTS

Two main factors affect conversion systems' efficiency and power density: the choice of multilevel topology and the power semiconductors technology [15], [16]. Concerning the selection of the converter topology, size and weight of the system, its cost, energy efficiency, thermal efficiency, complexity, and electromagnetic interference are all factors a designer should consider to achieve an optimal design [17], [18]. Of course, it must be recognized that a complex topology may exhibit more pronounced electromagnetic interference effects than a simpler one. Beyond the choice of the topology, there is another essential element in the hardware implementation of a power conversion system, such as the progress in new power components and/or technologies [19]. The use of fast power semiconductors allows either to reduce the power losses by keeping the same switching frequency  $f_{sw}$  or to increase the switching frequency  $f_{sw}$  by keeping the losses constant. On the one hand, lower power losses correspond to less heat generation; this is reflected in more straightforward, cheaper, smaller, and lighter cooling systems and, therefore, in a higher power density. On the other hand, keeping the same power losses, the increase in the switching frequency reduces the size

of the passive components (capacitors, inductors), with a consequent decrease in the system's cost, size, and weight. The system size reduction is proportional to the increase in frequency. Consequently, finding a trade-off between the power losses and the switching frequency is a good starting point for improving the efficiency of the power conversion system.

### C. STATE OF THE ART

Today, many converter designers rely on the use of new power semiconductors based on the Wide Bandgap Semiconductors (WBS), like Silicon Carbide (SiC) or Gallium Nitride (GaN), which support much faster commutations than the silicon power devices and can operate at higher temperatures. [20], [21]. Over the years, several AC-AC multilevel topologies, from the simplest to the most complex, have been introduced in literature [22], [23], [24], [25], [26], [27], [28], [29], [30], [31], [32], [33], [34], [35], [36]. Table 1 compares the AC-AC multilevel topologies in Back-to-Back (BTB) configuration as a function of different characteristics, such as the number of voltage levels, the technology of power semiconductors power rating, DC-bus voltage level application, and efficiency conversion. AC-AC converter based on 2-level topology and Neutral Point Clamped (NPC) topology for VFD applications has been proposed in [22]. The design of the AC-AC converter is aimed at 10 kW of rated power and 650 V of DC-bus voltage using the 2-level and NPC topologies. The design procedure considers different parameters, such as switching frequency, modulation scheme, passive values, harmonics, electromagnetic interference (EMI), control dynamics and stability, and protection. This article has shown no prototype, and the theoretical analysis shows that the efficiency conversion is 97.8 % for the 2-level converter and 97.6% for the NPC converter. In [23], the design of a three-phase AC-AC NPC converter connected between the grid and the AC loads has been proposed. From the carried-out analysis, an efficiency of 88% has been declared with a power of 610 W and DC-bus of 100 V. The single-phase AC-AC 3 kW T-Type converter has been analyzed and implemented in [24] for UPS applications. Using SiC power semiconductors, the maximum efficiency of the proposed converter is 99.0% and its efficiency at the rated power is 98.6%. In [25], an AC-AC multilevel converter based on T-Type topology with a peak efficiency of 96.6% and power density of 2.3 kW/dm<sup>3</sup> has been designed and tested for UPS applications. In [26], the three-phase AC-AC NPC converter has been proposed to supply the AC load starting from the grid. This work shows that applying control strategies based on the system model enhances overall performance. However, the authors did not state the peak efficiency of the converter. The three-phase AC-AC NPC converter is proposed for VFD applications in [27] and [28]. The power conversion is based on the NPC topology; the only difference between the topologies is the DC-bus configuration. The three-phase AC-AC NPC converter is proposed for VFD applications in [27] and [28]. The power conversion is based on the NPC topology; the only difference between the topologies is the DC-bus configuration.

**TABLE 1. AC-AC Multilevel Topologies in Back-to-Back (BTB) Configuration**

Refs.	Topology	Number of levels	Technology	Power rating	DC-bus Voltage	Application	Efficiency
[22]	2-Level	2	SiC	10 kW	650 V	VFD	97.8 %
	NPC	3	SiC	10 kW	650 V	VFD	97.6 %
[23]	NPC	3	IGBT	0.61 kW	100V	AC load	88 %
[24]	T-Type	3	SiC	3 kW	300 V	UPS	99 %
[25]	T-Type	3	Si/SiC	20 kW	720 V	UPS	99.6 %
[26]	NPC	3	IGBT	50 kW	400 V	AC Grid	-
[27], [28]	NPC	3	IGBT	3 kW	600 V	VFD	95.7 %
	S3L-NPC	3	IGBT	3 kW	600 V	VFD	97 %
[29], [30]	NPC	3	Si/SiC	20 kW	800 V	UPS	97.6 %
[31]	MP-NPC	5	IGBT	3.5 kW	200 V	AC Grid	-
[32]	NPC	5	IGBT	3.7 kW	200 V	VFD	-
[33]	NPC	5	SiC	50 kW	4000 V	VFD	98.8 %
[34]	ANPC	5	IGBT	10 kW	620 V	VFD	-
[35]	ANPC	5	IGBT	-	400 V	VFD	-
[36]	MPC	5	IGBT	1.5 MW	11.2 kV	AC Grid	-
<b>Proposed</b>	E-Type	5	Si/SiC	20 kW	700 V	VFD/UPS	98.2 %

The DC-bus of the classical NPC topology, composed of two series capacitors, has been replaced by delta-connected capacitors. This new converter has been called a symmetrical three-level back-to-back converter (S3L-BTB). The peak efficiency declared by the authors is 95.7% for the classical 3L-BTB converter and 97% for the S3L-BTB. In [29] and [30], a three-phase 20 kW BTB NPC converter is realized using hybrid technology for the power semiconductors, reaching 97.6% of double-conversion efficiency at full load. A new three-phase AC-AC multiple-pole 5-Level NPC (MP-NPC) has been investigated and implemented in [31]. Compared to the other topologies, the authors claim that the number of the power semiconductor is reduced, and the THD of the current is low, even if the switching frequency is low. However, the article does not provide the performance in terms of efficiency. In [32], the three-phase 5-Level BTB converter based on NPC topology is proposed for VFD applications. The author has not declared the performance of the converter, and two different control strategies are proposed to balance the voltage across the DC-bus capacitors in the 5-Level BTB converter. The efficiency of the 5-Level converter based on the NPC topology presented in [33] is 98.8% by using SiC power semiconductors. A 50kW prototype converter is realized and tested with a developed modified space-vector pulse-width-modulation (SVPWM) algorithm and DC-bus voltage at 4kV. In [34] and [35], the three-phase 5-Level BTB converter based on the Active Neutral-Point-Clamped (ANPC) topology is proposed and analyzed to be used for VDF applications. Both papers focus on the capacitor voltage pre-charge strategy and the multi-objective optimization PWM control method based on zero-sequence voltage injection, no efficiency values were provided. Finally, a 5-Level BTB converter based on the MultiPoint Clamped (MPC) topology is proposed in [36]. A 1.5 MW prototype converter has been built by using IGBT power semiconductors and tested when operated by the AC grid.

#### D. CONTRIBUTION OF THE ARTICLE

The E-Type topology has been introduced in [37] for grid-connected applications. The E-Type topology has been modified in [38] to improve some critical aspects of the

topology, such as the voltage stress of power semiconductors and the current paths. This work focuses on the optimization design and implementation of the new E-Type topology in the BTB configuration to obtain high efficiency and high-power density to be used in industrial power supply applications. The design methodology has been implemented to find the best compromise regarding the efficiency and power density of the I-3 $\Phi$ 5L BTB E-Type converter. The design methodology uses different steps: 0) choice of the converter parameters, 1) selecting the DC-bus capacitors, 2) optimization loop, 3) heat-sink design, 4) driver circuits implementation, 5) filters design, and finally, saving the results. In the pre-design step, all system requirements are fixed, and initial selections are made with reference to input and output voltage, fundamental frequency, THD, and DC-bus voltage. After that, the optimization loop is accomplished using parameters sweep method. This loop evaluates efficiency as a function of power end efficiency as a function of switching frequency. At the end of this loop, the best configuration in terms of power semiconductors is obtained. After that, the complete thermal network is also evaluated to select the proper heat-sink. After designing the driver circuits, the filter boards are built up by considering the power density and switching frequency trade-offs. Thus, the resulting design is the best compromise between efficiency and power density by considering the parameters of the whole system.

Compared to the other topology, using a DC-bus voltage equal to 700 V, the Interleaved 3-Phase 5-Level E-Type Back-to-Back Converter (I-3 $\Phi$ 5L BTB E-Type Converter) allows to reach a peak efficiency of 98.2%, and the efficiency at nominal power is close to 98%, including filter, driver circuits, control, and fan by using Si and SiC discrete power semiconductors. The realized prototype shows the size equal to 580 mm x 300 mm x 45 mm, the power density, and the specific power equal to 8.4 kW/dm<sup>3</sup> and 3.24 kW/kg. When the converter is connected to the grid and AC loads, the input current total harmonic distortion (THD<sub>i</sub>) is less than 3%, and the output voltage total harmonic distortion (THD<sub>v</sub>) is less than 1%.

The article is organized into five sections. The motivations, the applications, and the review topologies of the AC-AC multilevel converter were argued in Section I. Section II discuss



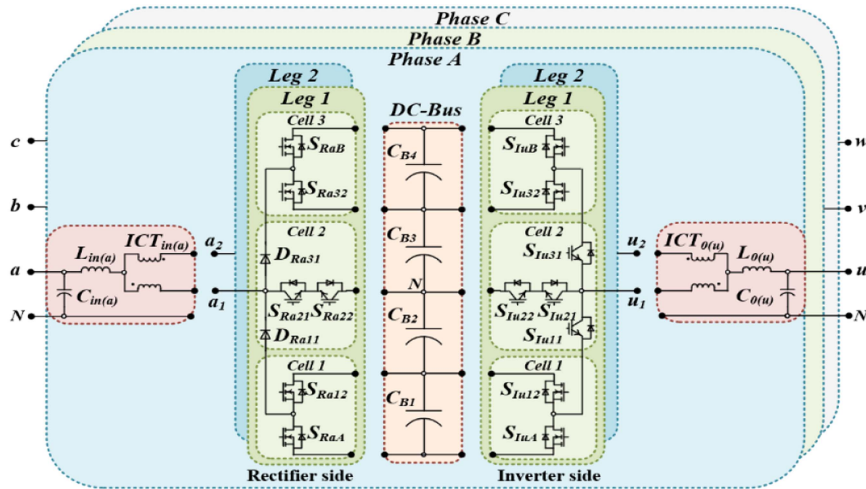


FIGURE 2. Interleaved 3-phase 5-level e-type BTB (I-3Φ5L BTB E-type) converter.

the operation principle of the I-3Φ5L BTB E-Type Converter. The optimization design procedure of the converter is discussed in Section III. Experimental results are illustrated in Section IV, and the comparison of the proposed topology and other topologies in terms of cost, volume, power density, and weight are illustrated in Section V. Finally, the article's conclusions are given in Section VI.

## II. OPERATION OF I-3Φ5L BTB E-TYPE CONVERTER

Fig. 2 shows the I-3Φ5L BTB E-Type converter circuit, which consists of the rectifier and inverter sides. Each phase of the rectifier and inverter has two legs (Leg 1, Leg 2) connected in parallel through the InterCell Transformer (ICT) [39]. Each leg is composed of eight power semiconductors grouped in three cells. The power semiconductors of the middle cell (cell 2) are connected to obtain a T-Type configuration. The vertical switches are replaced with the power diodes on the rectifier side, realizing the unidirectional T-Type cell. Using the I-Type configuration, the negative and positive DC-bus of the bidirectional and unidirectional T-Type topologies are managed by two cells (cell 1 and cell 2). The common DC-bus comprises four series DC-bus capacitors  $C_{B1}$ ,  $C_{B2}$ ,  $C_{B3}$ , and  $C_{B4}$ . There are many reasons why ICT has been used in this converter. It is used to share the current between the parallel legs, reducing the power semiconductors rating current. It helps to attenuate the current ripple, and it improves the harmonic contents of input currents and output voltages. The direct consequence of these benefits is the improvement of efficiency and power density of the entire conversion system. The modulation strategy of the converter is based on the Phase Disposition Pulse Width Modulation (PD-PWM) [40]. The gate signals of the power semiconductors located in Leg 1 of the rectifier and the inverter are generated by comparing three modulating signals with four carrier signals having same frequency and amplitude. The switches located in Leg 2 are controlled using the other four carrier signals in opposite phases to those of Leg 1, as illustrated in Fig. 3. The number of the voltage levels

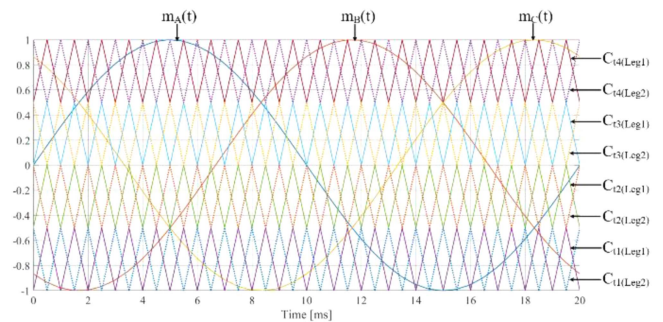


FIGURE 3. Modulation strategy for I-3Φ5L BTB E-type.

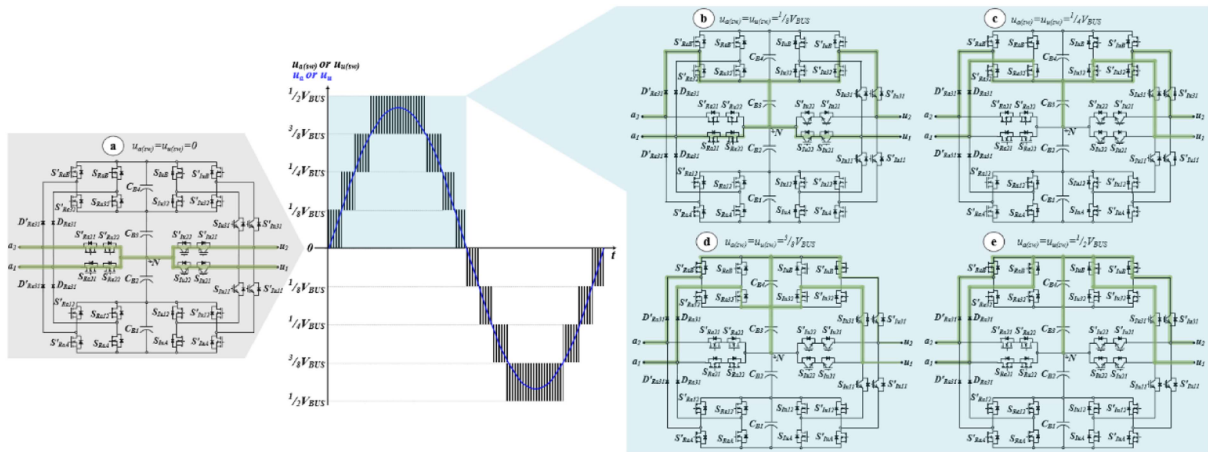
( $N_{L(in/out)}$ ) can be obtained as in (1), where  $N_L$  is the number of the levels of the single leg converter and  $N_C$  is the number of interleaved cells equal to 2 in this converter. Assuming the power factor (PF) close to 1, the phase-to-neutral input voltage  $u_{a(sw)}$  and the phase-to-neutral output voltage  $u_{u(sw)}$  are the combinations of the legs, as defined in (2).

$$N_{L(in/out)} = (N_L - 1) \cdot N_C + 1 \quad (1)$$

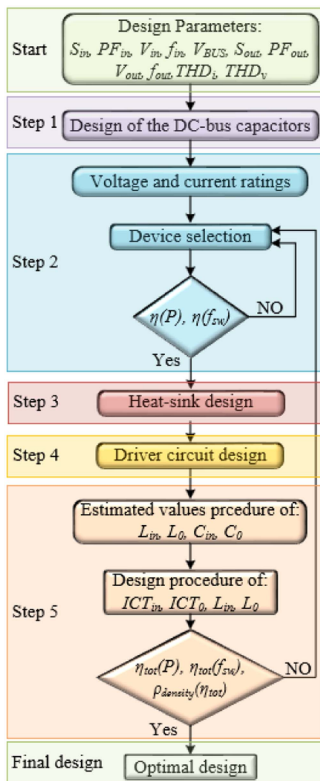
$$u_{a(sw)}(t) = \frac{u_{a1(sw)}(t) + u_{a2(sw)}(t)}{2},$$

$$u_{u(sw)}(t) = \frac{u_{u1(sw)}(t) + u_{u2(sw)}(t)}{2} \quad (2)$$

The current path during the negative half period is not analyzed since the converter is entirely symmetrical concerning the middle branches. It is easy to understand that, according to (1), the input and the output voltage waveforms show nine voltage levels. Fig. 4 shows the current path, highlighted in green for different phase-to-neutral switching voltages  $u_{a(sw)}$  and  $u_{u(sw)}$  of phase A.



**FIGURE 4.** Input and output voltages before  $u_{a(sw)}/u_{u(sw)}$  and after  $u_a/u_u$  the filter including the commutation loop of the single-phase 5L BTB E-Type Converter during the positive half period: (a)  $u_{a(sw)}=u_{u(sw)}=0$ , (b)  $u_{a(sw)}=u_{u(sw)}=1/8V_{BUS}$ , (c)  $u_{a(sw)}=u_{u(sw)}=1/4V_{BUS}$ , (d)  $u_{a(sw)}=u_{u(sw)}=3/8V_{BUS}$ , (e)  $u_{a(sw)}=u_{u(sw)}=1/2V_{BUS}$ .



**FIGURE 5.** Design methodology for I-3Φ5L BTB E-type.

### III. HARDWARE DESIGN AND PROTOTYPE IMPLEMENTATION

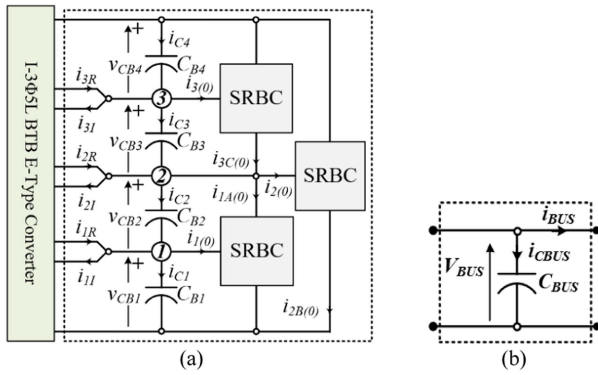
The design procedure to implement the optimized prototype of the I-3Φ5L BTB E-Type is illustrated in Fig. 5. This procedure starts with the definition of the converter parameters, such as input/output apparent power  $S_{in}$ ,  $S_{out}$ , input/output power factor  $PF_{in}$ ,  $PF_{out}$ , input/output fundamental frequency

$f_{in}$ ,  $f_{out}$ , DC-bus voltage  $V_{BUS}$ , Total Harmonic Distortion (THD) of the input current  $THD_i$  and output voltage  $THD_v$ . The procedure is split into five main parts: 1) DC-bus capacitors, 2) power stage, 3) heat-sink, 4) driver circuit, and 5) input/output filters.

Once the DC-bus capacitors have been selected, the optimal power semiconductors' selection is made in step 2. In this step, the stress of the power semiconductors has been analytically evaluated. The power semiconductors have been selected according to the stress in terms of the current and voltage. Afterward, the efficiency as a function of the power  $\eta(P)$  and the efficiency as a function of the switching frequency  $\eta(f_{sw})$  have been analytically estimated. Several combinations of power semiconductors have been considered until optimal efficiency has been found. Afterward, the design of the heat sink was carried out in step 3. The driver circuit design has been considered in step 4 according to the gate charge  $Q_G$ , diver output voltage swing, gate resistance, and switching frequency of the power semiconductors. After that, a proper step-by-step procedure has accomplished the selection and design of passive components, such as the input and output filters (step 5). Finally, the algorithm can estimate the maximum efficiency of the passive and active power devices considering the system's main parameters.

#### A. DC-BUS CAPACITOR

The unbalancing voltage of the DC-bus capacitors is the main problem of the multilevel voltage source converters. In the proposed multilevel converter, the current into capacitors is the sum of the current provided by the rectifier and the inverter, as illustrated in Fig. 6(a). For this reason, to balance the capacitor voltages and obtain four equal DC-bus currents  $i_{C1}=i_{C2}=i_{C3}=i_{C4}=i_{BUS}$ , three Series Resonant Balancing Circuits (SRBCs) [41] are used, and the considered equivalent circuit of the DC-bus is shown in Fig. 6(b). The DC-bus capacitors



**FIGURE 6.** (a) Simplified scheme of the I-3Φ5L BTB E-type, (b) equivalent circuit of the DC-bus capacitors.

are selected according to the DC-bus capacitor RMS current and the DC-bus voltage ripple.

Based on the analysis proposed in [37], the minimum partial DC-bus capacitor value  $C_{BUS}=C_{B1}=C_{B2}=C_{B3}=C_{B4}$  is determined by (3), where  $I_{CBUS}$  is the RMS current of the double fundamental frequency,  $\Delta V_{BUS}$  is the peak-to-peak voltage ripple,  $N_S$  and  $N_P$  are the numbers of series and parallel capacitors.

$$C_{BUS} = \frac{2\sqrt{2}}{(2\pi 100) \Delta V_{BUS}} N_S N_P I_{CBUS} \quad (3)$$

Considering the peak-to-peak voltage ripple  $\Delta V_{BUS}$  equal to 100 V at 20 kW and according to (3), 220  $\mu$ F, 220 V electrolytic capacitors have been selected from United Chemi-Con. Notably, six parallel and four series electrolytic capacitors have been used as DC-bus capacitor tanks. The electrolytic capacitors (e-caps) are selected for several factors compared to the other capacitors. The main reason can be found in the energy density. Aluminium electrolytic capacitors have up to ten times higher energy density than polypropylene film capacitors [42]. The second reason for this choice is that the rated voltage across the capacitors is low (175 V). The e-caps offer lower-rated voltages than the film capacitors [43]. Individual electrolytic capacitors' voltage and ripple current limitations require multiple capacitors to be connected in series and parallel to build a capacitor bank. However, when connecting electrolytic capacitors in series, active or passive balancing is beneficial to ensure a uniform distribution of the DC-link circuit voltage on the individual capacitor. This extra effort may prove immensely helpful in this topology [44]. Furthermore, the capacitance of e-caps decreases with falling temperatures by a double-digit percentage. The third reason for the e-cap choice is the cost. The specific cost to store a given amount of energy with aluminium electrolytic capacitors is significantly less than with film capacitors. In contrast, as well known, the e-caps show an ESR more significant than the film capacitors. The ESR and capacitance of the film capacitor show themselves to be

largely unimpressed by temperature fluctuations. Additionally, the operating parameters temperature, voltage, and ripple current determine the lifetime of electrolytic capacitors. For film capacitors, temperature, voltage, and humidity limit the lifetime [45].

## B. POWER STAGE DESIGN

The selection of the power semiconductors is based on the maximum voltage and current stress. The voltage stress across the power switches has been evaluated according to (4), where  $V_{BL(max)}$  is the maximum blocking voltage at steady state and  $\Delta V$  is the overvoltage commutation. The blocking voltage  $V_{BL(max)}$  is a function of the DC-bus voltage  $V_{BUS}$  and the number of levels  $N_L$ , while the overvoltage commutation  $\Delta V$  depends on the resonance coefficient  $k_R$ , commutation inductance  $L_\xi$ , slope current  $di_{sw}/dt$  and forward recovery voltage of the complementary freewheeling diode  $V_{FR}$  [37].

$$V_{sw} = V_{BL(max)} + \Delta V = \frac{V_{BUS}}{N_L - 1} + k_R L_\xi \frac{di_{sw}}{dt} + V_{FR} \quad (4)$$

The maximum blocking voltage  $V_{BL(max)}$  of the devices  $D_{Rx11}$ ,  $D_{Rx31}$ ,  $S_{Iy11}$ ,  $S_{Iy31}$  is  $3/4V_{BUS}$ . The  $V_{BL(max)}$  of the power semiconductors  $S_{RxA}$ ,  $S_{RxB}$ ,  $S_{Rx12}$ ,  $S_{Rx32}$ ,  $S_{IyA}$ ,  $S_{IyB}$ ,  $S_{Iy12}$ ,  $S_{Iy32}$  is  $1/4V_{BUS}$ , while  $V_{BL(max)}$  of the switches  $S_{Rx21}$ ,  $S_{Rx22}$ ,  $S_{Iy21}$ ,  $S_{Iy22}$  is  $1/2V_{BUS}$ , with  $x \in \{a, b, c\}$  and  $y \in \{u, v, w\}$ . The power devices most stressed in voltage ( $3/4V_{BUS}$ ) are those positioned in the T-Type cell (cell 2) of the leg. However, when the power semiconductors are subjected to a voltage of  $3/4V_{BUS}$ , the overvoltage  $\Delta V$  is zero given that the current flow through them is zero. Overvoltage  $\Delta V$  appears only when the blocking voltage across a power semiconductor is  $1/4V_{BUS}$ . For instance, looking at Fig. 4(e), during the positive peak of the modulating signal, the commutation occurs between the switches  $S_{RaB}$ ,  $S_{Ra32}$  (Leg 1),  $S'_{RaB}$ ,  $S'_{Ra32}$  (Leg 2) in the rectifier side and the switches  $S_{IuB}$ ,  $S_{Iu32}$  (Leg 1),  $S'_{IuB}$ ,  $S'_{Iu32}$  (Leg 2) in the inverter side. The other diodes and switches like  $D_{Ra31}$ ,  $D'_{Ra31}$ ,  $S_{Iu31}$ ,  $S'_{Iu31}$  are in on-state condition and the switches located in the bottom legs like  $S_{RaA}$ ,  $S_{Ra12}$  (Leg 1),  $S'_{RaA}$ ,  $S'_{Ra12}$  (Leg 2) in the rectifier side and the switches  $S_{IuA}$ ,  $S_{Iu12}$  (Leg 1),  $S'_{IuA}$ ,  $S'_{Iu12}$  (Leg 2) in the inverter side are in off-state condition. In this situation, the blocking voltage across the power devices  $S_{RaA}$ ,  $S_{Ra12}$ ,  $S'_{RaA}$ ,  $S'_{Ra12}$ ,  $S_{IuA}$ ,  $S_{Iu12}$ ,  $S'_{IuA}$ ,  $S'_{Iu12}$  is equal to  $3/4V_{BUS}$ , and the current flowing through them is equal to zero. Consequently, the circuit sets the voltage rating, and the commutation overvoltage  $\Delta V$  does not occur since the current is equal to zero. On the other hand, the current flows through the switches  $S_{RaB}$ ,  $S_{Ra32}$ ,  $S'_{RaB}$ ,  $S'_{Ra32}$  and thus, the overvoltage  $\Delta V$  across these devices is different from zero. The analytical approach proposed in [46] has been applied to estimate the current stress of the power semiconductors. The current stress, such as average (AVG) and root mean square (RMS) currents, of the power devices have been analytically estimated starting from the duty cycle of the devices, as given in (5), where  $\omega_{0,R/I} = \omega_{0,R} = \omega_{0,I} = \omega_0 = 2\pi f_0$ ,  $d_{d,R/I}$  is duty cycle of the devices in the rectifier side or in the inverter side,

**TABLE 2. Power Semiconductors in the 1-3 $\Phi$ 5L BTB E-Type Converter**

Device	Part Number	Rated Voltage	Rated Current	R <sub>ON</sub>	Technology
5L E-Type Rectifier					
S <sub>RxA</sub> , S <sub>RxB</sub> , S <sub>Rx12</sub> , S <sub>Rx32</sub>	IPT210N25NFD	250 V	69 A	21 m $\Omega$	OptiMOS™
D <sub>Rx31</sub> , D <sub>Rx11</sub>	STPSC40065C	650 V	40 A	-	SiC Schottky
S <sub>Rx21</sub> , S <sub>Rx22</sub>	IPL60R104C7	650 V	20 A	-	CoolMOS™
5L E-Type Inverter					
S <sub>IxA</sub> , S <sub>IxB</sub> , S <sub>Ix12</sub> , S <sub>Ix32</sub>	IPT210N25NFD	250 V	69 A	21 m $\Omega$	OptiMOS™
S <sub>Ix31</sub> , S <sub>Ix11</sub>	C3M0030090K	900 V	73 A	30 m $\Omega$	SiC Mosfet
S <sub>Ix21</sub> , S <sub>Ix22</sub>	IKW20N60T	600 V	20 A	-	Si-IGBT

**TABLE 3. Thermal Resistances and Case Temperature in the Single-Phase Leg of the Rectifier and Inverter**

	R <sub>S,th(j-c)</sub> [C°/W]	R <sub>D,th(j-c)</sub> [C°/W]
IPT210N25NFD	0.2	0.2
C3M0030090K	0.48	0.48
IKW20N60T	0.9	1.5
STPSC40065C	0.6	0.6
IPL60R104C7	1.026	1.026
Inverter side – phase A Leg 1		
	P <sub>v,R<sub>v,th(j-c)</sub></sub> [C°]	P <sub>v,R<sub>v,th(j-c)</sub></sub> [C°]
S <sub>IuA</sub> -S <sub>IuB</sub>	0.76	S <sub>RaA</sub> -S <sub>RaB</sub> 0.66
S <sub>Iu11</sub> -S <sub>Iu31</sub>	1.13	D <sub>Ra11</sub> -D <sub>Ra31</sub> 1.16
S <sub>Iu12</sub> -S <sub>Iu32</sub>	0.43	S <sub>Ra12</sub> -S <sub>Ra32</sub> 0.53
S <sub>Iu21</sub> -S <sub>Iu22</sub>	0.74	S <sub>Ra21</sub> -S <sub>Ra22</sub> 0.62
Case Temperatures		
T <sub>cl1</sub> =T <sub>cl8</sub> (S <sub>IuA</sub> -S <sub>IuB</sub> ) [C°]	89.42	T <sub>cr1</sub> =T <sub>cr8</sub> (S <sub>RaA</sub> -S <sub>RaB</sub> ) 89.34
T <sub>cl2</sub> =T <sub>cl6</sub> (S <sub>Iu11</sub> -S <sub>Iu31</sub> ) [C°]	88.87	T <sub>cr2</sub> =T <sub>cr6</sub> (D <sub>Ra11</sub> -D <sub>Ra31</sub> ) 88.84
T <sub>cl3</sub> =T <sub>cl7</sub> (S <sub>Iu12</sub> -S <sub>Iu32</sub> ) [C°]	89.57	T <sub>cr3</sub> =T <sub>cr7</sub> (S <sub>Ra12</sub> -S <sub>Ra32</sub> ) 89.47
T <sub>cl4</sub> =T <sub>cl5</sub> (S <sub>Iu21</sub> -S <sub>Iu22</sub> ) [C°]	89.26	T <sub>cr4</sub> =T <sub>cr5</sub> (S <sub>Ra21</sub> -S <sub>Ra22</sub> ) 89.38

and  $i_{R/I}$  is input or output phase current.

$$\begin{aligned}
 & i_{AVG,R/I}(\omega_{0,R/I}t) \\
 &= \frac{1}{2\pi} \int_0^{2\pi} [i_{R/I}(\omega_{0,R/I}t) \cdot d_{d,R/I}(\omega_{0,R/I}t)] d(\omega_{0,R/I}t) \\
 & i_{RMS,R/I}(\omega_{0,R/I}t) \\
 &= \frac{1}{2\pi} \int_0^{2\pi} [i_{R/I}^2(\omega_{0,R/I}t) \cdot d_{d,R/I}(\omega_{0,R/I}t)] d(\omega_{0,R/I}t) \quad (5)
 \end{aligned}$$

The results for the currents is given in (6), where  $M_{0,R}/M_{0,I}$  is the modulation depth of the rectifier or inverter,  $I_{in}/I_{out}$  is the RMS phase current of the rectifier or inverter and the  $a_{RMS,i}$ ,  $b_{RMS,i}$ ,  $a_{AVG,i}$ ,  $b_{AVG,i}$ ,  $a_{RMS,j}$ ,  $b_{RMS,j}$ ,  $a_{AVG,j}$ ,  $b_{AVG,j}$  are the coefficients listed in Tables 10 and 11 in the appendix.

$$\begin{aligned}
 i_{RMS,R}(t) &= \sqrt{\frac{(\sqrt{2}I_{in})^2 M_{0,R}}{12\pi} \left( \frac{a_{RMS,i}}{M_{0,R}} + b_{RMS,i} \right)} \\
 |i_{AVG,R}(t)| &= \frac{\sqrt{2}I_{in}M_{0,R}}{2\pi} \left( \frac{a_{AVG,i}}{M_{0,R}} + b_{AVG,i} \right)
 \end{aligned}$$

**TABLE 4. Parameters of the Infineon IC 1EDI60112AF Gate Drivers**

Main parameters		Estimated parameters		
$I_{G,max}^{OFF}$ [A]	3.5	R <sub>G</sub> [ $\Omega$ ]	1.5	
$I_{G,max}^{ON}$ [A]	4	f <sub>swE</sub> [kHz]	8	
P <sub>OL</sub> [mW] @ 25°C	400	P <sub>ID</sub> [mW]	5	
r <sub>on</sub> /r <sub>off</sub> [ $\Omega$ ]	2.25	P <sub>OD</sub> [mW]	30	
I <sub>Q1</sub> [mA]	1	P <sub>D</sub> [mW] @ 85°C	11.7	
I <sub>Q2</sub> [mA]	2	P <sub>OL</sub> [mW]	82.65	
V <sub>CC1,max</sub> [V]	5			
(V <sub>CC+</sub> + V <sub>EE</sub>  ) [V]	15			
	Q <sub>G</sub> [nC]	R <sub>int</sub> [ $\Omega$ ]	I <sub>G,peak</sub> <sup>ON/OFF</sup> [A]	P <sub>OL,wc</sub> [mW]
IPT210N25NFD	65	0.82	3.28	3.84
C3M0030090K	74	3	2.22	2.96
IKW20N60T	120	2.8	2.29	4.95
IPL60R104C7	42	2.8	2.29	1.73

**TABLE 5. Main Parameters of the Selected E-Cap and Potential Film Capacitor**

	Selected capacitor (e-cap)	Film Capacitor
Manufacturer	United Chemi-Con	TDK
Part number	EKXJ221ELL221MUP1S	B3232014267K000
Working Voltage	220 V	450 V
Cap Value	220 $\mu$ F	260 $\mu$ F
Case size	14.5×35.5 mm	50 × 120 mm
ESR	1.2 $\Omega$ (120 Hz)	5 m $\Omega$ (10 kHz)
Rated ripple current	1.095 A	23 A
Cost (PU)	1.11 €	20,19 €

**TABLE 6. Comparison of the Selected and Film Capacitors in Terms of Surface Area, Cost, and Losses**

	Surface area	Cost	Losses at rated power
e-cap	46,713.78 mm <sup>2</sup>	26,64 €	18 W
Film cap	455,300.00 mm <sup>2</sup>	403,8 €	0.05 W

**TABLE 7. Filter Values Comparison Between Three-Phase 2-Level BTB Converter, Three-Phase 3-Level BTB Converter, and Three-Phase 5-Level BTB Converter**

	BTB 2L Converter	3L T-Type Converter	Proposed Converter
Inductance	850 $\mu$ H	420 $\mu$ H	60 $\mu$ H
Capacitance	22 $\mu$ F	10 $\mu$ F	4.7 $\mu$ F
Area-Product (AP <sub>ICT</sub> )	9.16 cm <sup>4</sup>	4.58 cm <sup>4</sup>	2.29 cm <sup>4</sup>

$$\begin{aligned}
 i_{RMS,I}(t) &= \sqrt{\frac{(\sqrt{2}I_{out})^2 M_{0,I}}{12\pi} \left( \frac{a_{RMS,j}}{M_{0,I}} + b_{RMS,i} \right)} \\
 |i_{RMS,I}(t)| &= \frac{\sqrt{2}I_{out}M_{0,I}}{2\pi} \left( \frac{a_{AVG,j}}{M_{0,I}} + b_{AVG,j} \right) \quad (6)
 \end{aligned}$$

Once the power semiconductors' voltage and current ratings are defined, it is possible to select the power semiconductors. However, the final power configuration is also chosen to respect the minimum power loss criteria. The power semiconductor losses have been evaluated as the sum of the conduction and switching losses. The conduction losses are obtained using the (7), where  $V_{FO}$  is the forward voltage drop (only related to the diodes and IGBTs),  $R_{ON}$  is the on-state



resistance,  $i_{AVG}$  and  $i_{RMS}$  are the previously estimated AVG and RMS currents flowing in the devices.

$$P_c \cong V_{FO}i_{AVG} + R_{ON}(V_{sw})i_{RMS}^2 \quad (7)$$

Concerning the switching losses, estimating the turn-on and turn-off energy losses at the operating point for each device is essential. The turn-on  $E_{on}$  and turn-off  $E_{off}$  energies are functions of the current flowing through the power semiconductors, junction temperature, and blocking voltage. Turn-on and turn-off energy losses of the switches can be estimated from the energy losses provided in the device datasheet according to (8), where  $E_{on\_OP}$  and  $E_{off\_OP}$  are the turn-on and turn-off energy losses close to the operating point,  $i_{RMS}$  is the RMS current flowing into devices,  $V_{BUS}$  is the DC-bus voltage across the device during the commutation,  $I_{nom}$  and  $V_{nom}$  are the device datasheet reference value RMS current and voltage obtained from the datasheet,  $\alpha_1, \alpha_2, \beta_1, \beta_2, \gamma_1, \gamma_2$  are the empirical coefficients of approximation used for energy loss scaling between device datasheet reference value and actual converter operating conditions.

$$\begin{aligned} E_{on}(T_j, V_{BUS}, i_{RMS}) &= E_{on\_OP} \left( \frac{i_{RMS}}{I_{nom}} \right)^{\alpha_1} \left( \frac{V_{BUS}/4}{V_{nom}} \right)^{\alpha_2} \left( \frac{T_j}{T_{nom}} \right)^{\gamma_1} \\ E_{off}(T_j, V_{BUS}, i_{RMS}) &= E_{off\_OP} \left( \frac{i_{RMS}}{I_{nom}} \right)^{\beta_1} \left( \frac{V_{BUS}/4}{V_{nom}} \right)^{\beta_2} \left( \frac{T_j}{T_{nom}} \right)^{\gamma_2} \end{aligned} \quad (8)$$

The switching losses of the power semiconductors at the operating condition can be estimated according to the (9).

$$P_{sw} = f_{sw} [E_{on}(T_j, V_{BUS}, i_{RMS}) + E_{off}(T_j, V_{BUS}, i_{RMS})] \quad (9)$$

The reverse recovery losses in the freewheeling diodes have been estimated as the product between the switching frequency and the reverse recovery energy  $E_{rr}$  according to (10), where  $Q_{rr\_OP}$  is the reverse recovery charge obtained from the datasheet and  $\alpha_{rr}, \beta_{rr}$  and  $\gamma_{rr}$  are the coefficients used for scaling between the datasheet recovery charge value and the actual converter operating conditions.

$$\begin{aligned} P_{rr} &= f_{sw} \left( \frac{V_{BUS}}{4} \right) Q_{rr\_OP} \left( \frac{i_{RMS}}{I_{nom}} \right)^{\alpha_{rr}} \left( \frac{V_{BUS}/4}{V_{nom}} \right)^{\beta_{rr}} \left( \frac{T_j}{T_{nom}} \right)^{\gamma_{rr}} \end{aligned} \quad (10)$$

The power semiconductors have been selected using the achieved analytical equations for the calculation of RMS and AVG currents and the power dissipation.

In Table 2 the selected power semiconductors devices are listed. The losses and efficiency distributions of the power semiconductors are estimated, as shown in Fig. 7. This figure illustrates the losses and the efficiency as a function of the output power for the 3Φ5L E-Type rectifier and the inverter,

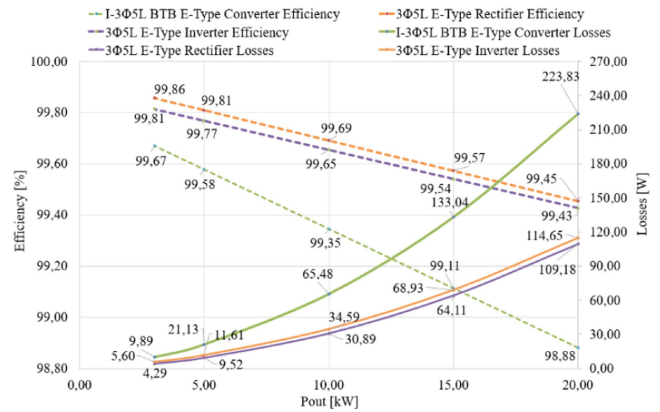


FIGURE 7. Losses and efficiency of the power semiconductors: (1) 1-3Φ5L BTB E-type converter losses (solid green line), (2) 3Φ5L E-type rectifier losses (solid red line), (3) 3Φ5L E-type inverter losses (solid violet line), (4) 1-3Φ5L BTB E-type converter efficiency (solid green line), (5) 3Φ5L E-type rectifier efficiency (solid red line), (6) 3Φ5L E-type inverter efficiency (solid violet line). Operating point:  $V_{BUS}=700$  V,  $f_{sw}=24$  kHz,  $U_{in}=U_0=220$  V,  $P_N=20$  kW.

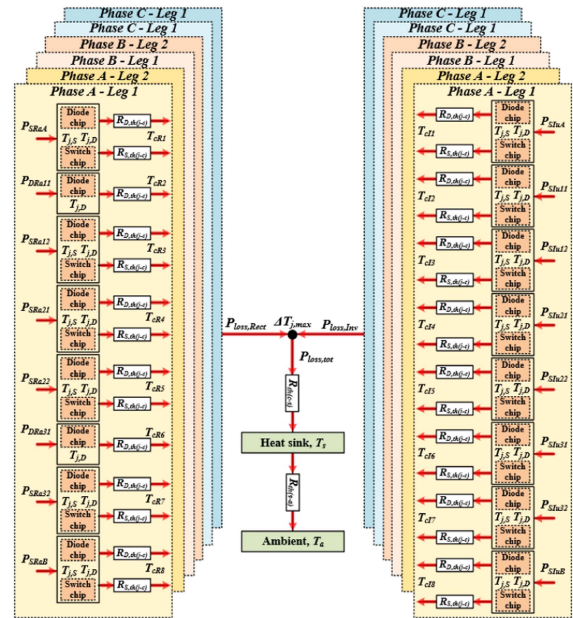


FIGURE 8. Thermal equivalent circuit of the I-3Φ5L BTB E-type converter.

as well as for the total converter. As it can be seen, the total losses at 24 kHz of switching frequency and rated power (20 kW) is about 223.83 W.

### C. HEAT-SINK DESIGN

After calculating the power losses, the next task is properly selecting the heat-sink. To reach this purpose, it is imperative to determine the thermal resistance between the heat sink and ambient  $R_{th(s-a)}$ . The equivalent thermal circuit of the I-3Φ5L BTB E-Type Converter is shown in Fig. 8, where  $T_{j,D}$ ,  $T_{j,S}$  are the junction temperature of the generic diode and switch,  $T_c$  is the case temperature,  $T_s$  is the heat sink temperature,  $T_a$



is the ambient temperature,  $R_{D,th(j-c)}$ ,  $R_{S,th(j-c)}$  are the thermal resistance between the device junction and the case,  $R_{th(c-s)}$  is the thermal resistance between the case and the heat-sink. Finally,  $R_{th(s-a)}$  is the thermal resistance between the heat sink and the ambient. The thermal resistance between the heat-sink and the ambient  $R_{th(s-a)}$  must be found to select the heat-sink. The ambient temperature  $T_a$  for cooling electronic equipment depends on the operating environment in which the component is expected to be used. Typical ambient temperature values in VFD applications [47] are between 30 °C to 45 °C if the external air is used; in this case,  $T_a$  has been chosen equal to 40 °C. A maximum junction temperature  $T_{j,max}$  at 90 °C has been assumed as reference. Knowing also the thermal resistances between the junction and the case  $R_{D,th(j-c)}$ ,  $R_{S,th(j-c)}$  from the datasheet, and the losses in each power semiconductor at rated power, the case temperature for each discrete power semiconductor can be obtained. In Table 3 are listed both the thermal resistances  $R_{D,th(j-c)}$ ,  $R_{S,th(j-c)}$  for each device and the case temperature of the power devices related to the rectifier and the inverter in the Leg 1 estimated according to (11), where  $v$  is the variable used to indicate the diode or the switch.

$$T_{C,v} = T_{j,max} - R_{v,th(j-c)} P_{v,loss} \quad (11)$$

The maximum junction-case temperature drop  $\Delta T_{j,max}$  occurs in the pairs of switches  $S_{Iu11}$ - $S_{Iu31}$  and diodes  $D_{Ra11}$ - $D_{Ra31}$  due to the high power losses compared to the other devices. Knowing  $\Delta T_{j,max}$  equal to 88.84°C, the heat-sink temperature  $T_s$  can be found as in (12).

$$T_s = \Delta T_{j,max} - R_{th(c-s)} P_{loss,tot} \quad (12)$$

The thermal resistance  $R_{th(c-s)}$  depends not only on the module and the packaging of the power semiconductors but also on how the element is mounted on the heat sink. In this case, the power semiconductors are mounted with silicon-pad isolation foil (manufacturer: Bergquist, part number: SPK10-0.006-00-11.512) having a thickness equal to 0.152 mm and the thermal resistance  $R_{th(c-s)}$  is about 129 mm<sup>2</sup>/W which leads to a resistance  $R_{th(c-s)}$  of 0.034 °C/W, considering a surface area of approximately 3800 mm<sup>2</sup>. Thus, the heat-sink temperature  $T_s$  is equal to 82 °C. Based on this analysis, the thermal resistance  $R_{th(s-a)}$  can be obtained by (13).

$$R_{th(s-a)} = \frac{T_s - T_a}{P_{loss,tot}} \quad (13)$$

Thus, the thermal resistance of the heat sink should be less than 0.187 °C/W to meet the desired working temperature at full power. In this project, the heat-sink series 890SP-03000-A100 (manufacturer HS MARSTON) has been selected. Given that the power semiconductors are placed into two distinct parts, the heat-sink has been split into two pieces: the first has a height and width equal to 303 mm and 85 mm; the second has a height and width equal to 303 mm and 40 mm. The selected heat-sink can provide the thermal resistance  $R_{th(s-a)}$  lower than 0.04 °C/W when the fan speed

is set at 3000 rpm. This thermal resistance value is acceptable throughout the converter's operating range. However, the fan speed is regulated as a function of the junction temperature to handle the cooling efficiency and meet the design criteria adequately.

#### D. DRIVER BOARD

The gate driver circuit must be carefully designed to achieve good power switch performance. Furthermore, gate drive resistance plays an important role, since it influences the turn-on and turn-off time and also it can affect the  $dv/dt$  during the switching [48]. The gate driver integrated circuit (IC) has been selected according to the constraints on the peak gate current and the driver output power losses during the commutation. The peak current during the turn-off and the turn-on of the switch is a function of the positive supply voltage  $V_{CC}$ , negative supply voltage  $V_{EE}$ , internal switch gate resistance  $R_{int}$ , external gate resistance  $R_G$ , and the turn-on/turn-off gate driver resistances  $r_{on}$ ,  $r_{off}$  according to (14).

$$I_{G,peak}^{ON} = \frac{V_{CC} + |V_{EE}|}{R_G + R_{int} + r_{ON}}, I_{G,peak}^{OFF} = \frac{V_{CC} + |V_{EE}|}{R_G + R_{int} + r_{OFF}} \quad (14)$$

The first constraint is that the turn-on and the turn-off currents must not exceed the maximum currents provided by the gate driver IC during the commutation. Power loss inside the gate driver IC must also be considered during commutation. Furthermore, the drive IC package can achieve maximum power dissipation without exceeding the maximum junction temperature at a given operating point. The gate driver's maximum allowed total power consumption  $P_D$  is given by the sum of the total input power  $P_{ID}$ , the total output power  $P_{OD}$ , and the output power under load,  $P_{OL}$  as in (15).

$$P_D = \overbrace{V_{CC1,max} I_{Q1}}^{P_{ID}} + \overbrace{(V_{CC} - V_{EE}) I_{Q2}}^{P_{OD}} + P_{OL} \quad (15)$$

Knowing the power consumption  $P_D$ , the input power  $P_{ID}$  and the operating supply current  $I_{Q2}$  from the datasheet, it is possible to obtain the output power under load,  $P_{OL}$ . Moreover, the dynamic output power under the worst condition  $P_{OL,wc}$  is a function of the equivalent switching frequency  $f_{swE}$ , power device gate charge  $Q_G$ , as in (16).

$$P_{OL,wc} = \frac{1}{2} \cdot Q_G \cdot f_{swE} \cdot (V_{CC} + |V_{EE}|) \left[ \frac{r_{ON}}{r_{ON} + R_G + R_{int}} + \frac{r_{OFF}}{r_{OFF} + R_G + R_{int}} \right] \quad (16)$$

In this case, the equivalent switching frequency  $f_{swE} = f_{sw}/3$ , given that two power semiconductors can switch in opposite phases for 120° in one fundamental period  $T_0 = 1/f_0$  when the modulation depth  $M_{0,R}$  (and/or  $M_{0,I}$ ) is close to one. The second constraint must be to comply with the output power  $P_{OL,wc}$ , under the worst case condition, must not exceed the load output power  $P_{OL}$  ( $P_{OL,wc} < P_{OL}$ ).

The external resistance  $R_G$  and the gate driver IC have been selected according to these two constraints. The gate driver

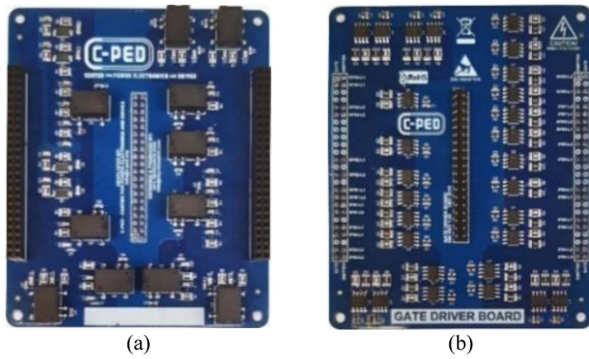


FIGURE 9. Picture of the driver board: (a) top view, (b) bottom view.

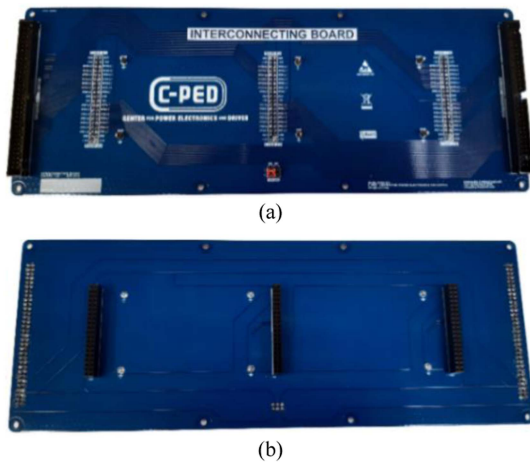


FIGURE 10. Picture of the interconnecting board which collects the gate signals of the power semiconductors: (a) top view, (b) bottom view.

chip used in this case is the Infineon IC 1EDI60I12AF. An isolated power supply is used for each device in order to obtain isolated gate voltages of 0–15 V. The main and estimated parameters of the IC 1EDI60I12AF gate driver are listed in Table 4. The maximum current of the power semiconductors during the turn-on and the turn-off is lower than the maximum current provided by the IC gate driver ( $I_{G,max}^{OFF}=3.5$  A,  $I_{G,max}^{ON}=4$  A).

Furthermore, the  $P_{OL,wc}$  is lower than the load output power at 85 °C ( $P_{OL}(@85^{\circ}C)=82.65mW$ ). The I-3 $\Phi$ 5L BTB E-Type Converter has a lot of discrete power semiconductors; thus, three driver boards have been built. The power switches of each phase of the converter are controlled by one driver board. Fig. 9 shows the top and bottom sides of the driver circuit, which controls the single phase of the converter. The interconnecting board, which routes all the signals between the driver boards to the control board, has also been realized, as shown in Fig. 10.

#### E. INPUT/OUTPUT FILTERS

The filters comprise the input and output ICTs, the inductors, and the capacitors. The passive components values are

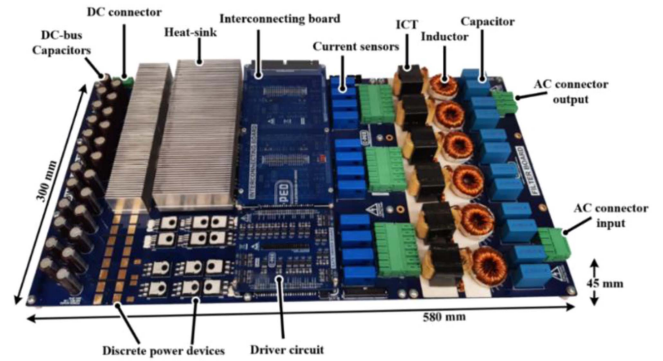


FIGURE 11. Prototype of the 20 kVA I-3 $\Phi$ 5L BTB E-type converter including the filter board, measuring 580 mm x 300 mm x 45 mm.

designed to fulfill  $THD_i$  less than 3% and  $THD_v$  less than 1%. Notably, in order to develop the ICTs and the inductors, the procedure proposed in [38] has been followed. This procedure is based on the trade-off between different parameters, such as shape and size of the core, winding and core losses, weight, and temperature, to optimize the power density and the efficiency of the whole power conversion system. The power and filter boards are connected through the PCB connector, as shown in Fig. 11.

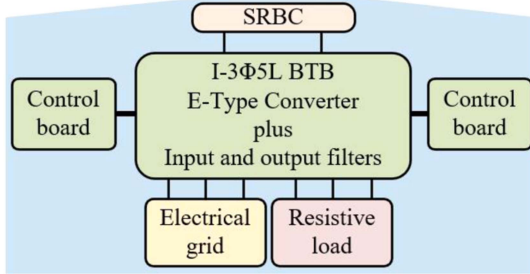
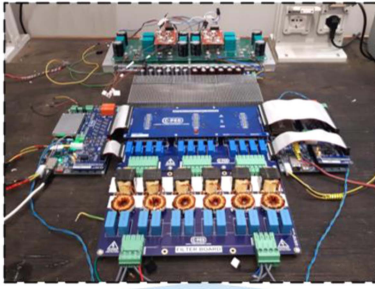
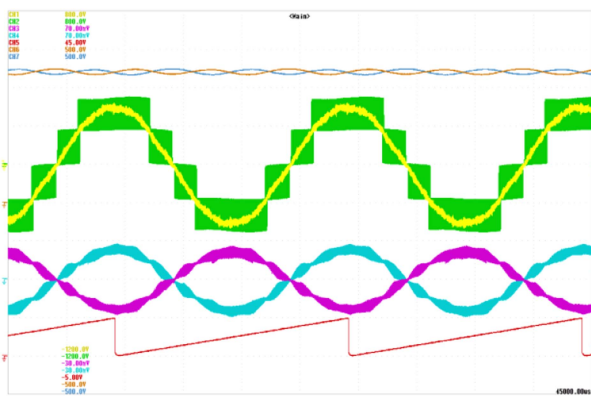
#### IV. EXPERIMENTAL RESULTS

Based on the previous analysis, the converter prototype has been built and shown in Fig. 11.

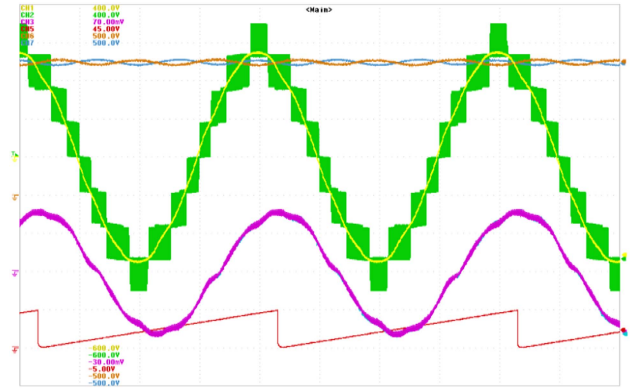
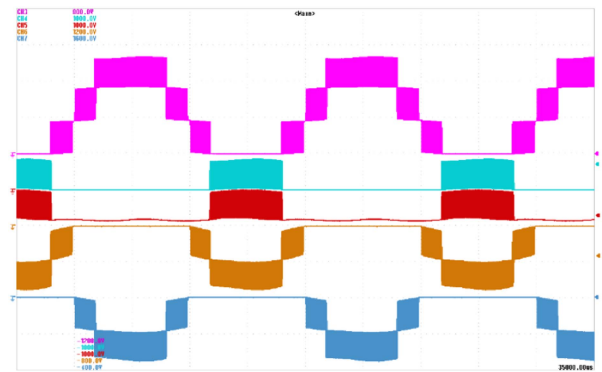
It can be noted that on the power board are present the DC-bus capacitors and the discrete power semiconductors, as mentioned in the previous section, some of them mounted on the top layer, and others mounted on the bottom layer of the power board. The prototype includes the driver circuit and the interconnecting board mounted on the top side, four current sensors (LAH 25-NP), and four voltage sensors (AMC1200). The control algorithm has been implemented in LabVIEW, and the resulting program comprises two different targets: FPGA and Real-time, which are run on dedicated hardware. The SRBC is used to share the voltage across the DC-bus capacitors equally. The I-3 $\Phi$ 5L BTB E-Type Converter experimental test bench is illustrated in Fig. 12. It is possible to identify the converter prototype, the balancing circuit, and the two control boards; one controls the rectifier side, and the other controls the inverter side. The rectifier side is connected to the grid, while the inverter side is connected to the resistive load. The Yokogawa DL850 oscilloscope is used to analyze voltage and current waveforms.

##### A. I-3 $\Phi$ 5L E-TYPE RECTIFIER WAVEFORMS

The rectifier side is controlled using two proportional-integral regulators: the first one regulates the DC-bus voltage, and the second one controls the q-axis current [49]. The d-axis current reference is set at zero, while an additional loop handles the current circulating into  $ICT_{in}$ . The grid angle is estimated


**FIGURE 12.** Experimental test bench.

**FIGURE 13.** Voltage and current waveforms at a steady state: phase-to-neutral switching voltage  $u_{a1(sw)}$  (CH2-green line, 200V/div), phase-to-neutral grid voltage  $u_a$  (CH1-yellow line, 200V/div), input current into Leg 1 of phase A  $i_{a1}$  (CH3-violet line, 20A/div), input current into Leg 2 of phase A  $i_{a2}$  (CH4-cyan line, 20A/div), grid angle  $\theta_g$  (CH5-red line, 5rad/div), bottom half DC-bus voltage  $V_{CB,L}=V_{CB1}+V_{CB2}$  (CH6-brown line, 100V/div) and top half DC-bus voltage  $V_{CB,H}=V_{CB3}+V_{CB4}$  (CH7-blue line, 100V/div). Time scale 5ms/div.

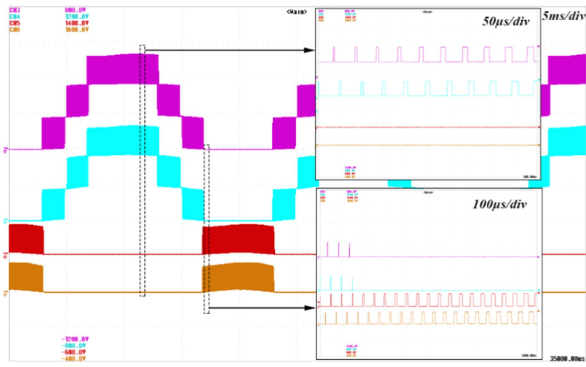
according to the PLL structure based on the steady-state linear Kalman Filter [50]. Fig. 13 shows the steady state waveforms of the phase-to-neutral switching voltage  $u_{a1(sw)}$ , the phase-to-neutral grid voltage  $u_a$ , when the operating point is:  $P_{in}=10$  kW,  $U_{in}=220$  V,  $f_0=50$  Hz,  $f_{sw}=24$  kHz,  $V_{BUS}=700$  V and  $M_{0,R}=0.9$ . As it can be seen, the DC-bus voltages are balanced by SRBCs, and the five voltage levels on Leg 1 of phase A are clearly visible. The currents flowing in the two legs are perfectly identical and they show the minimum current ripple near zero and 0.5. The input phase current flowing in the inductance  $L_{in(a)}$  and the line-to-line switching voltage  $u_{ab(sw)}$  are illustrated in Fig. 14.


**FIGURE 14.** Voltage and current waveforms at a steady state: line-to-line switching voltage  $u_{ab(sw)}$  (CH2-green line, 100V/div), phase-to-neutral voltage  $u_a$  (CH1-yellow line, 200V/div), input inductor current  $A i_a$  (CH3-violet line, 20A/div), grid angle  $\theta_g$  (CH5-red line, 5rad/div), bottom half DC-bus voltage  $V_{CB,L}=V_{CB1}+V_{CB2}$  (CH6-brown line, 100V/div) and top half DC-bus voltage  $V_{CB,H}=V_{CB3}+V_{CB4}$  (CH7-blue line, 100V/div). Time scale: 5ms/div.

**FIGURE 15.** Blocking voltage waveforms of the power semiconductors into Leg 1 at a steady state:  $D_{Ra31(L1)}$  (CH3-violet line, 200V/div),  $S_{Ra32(L1)}$  (CH4-cyan line, 200V/div),  $S_{RaB(L1)}$  (CH5-red line, 200V/div),  $S_{Ra21(L1)}$  (CH6-brown line, 200V/div)  $S_{Ra22(L1)}$  (CH7-blue line, 200V/div). Time scale: 5ms/div.

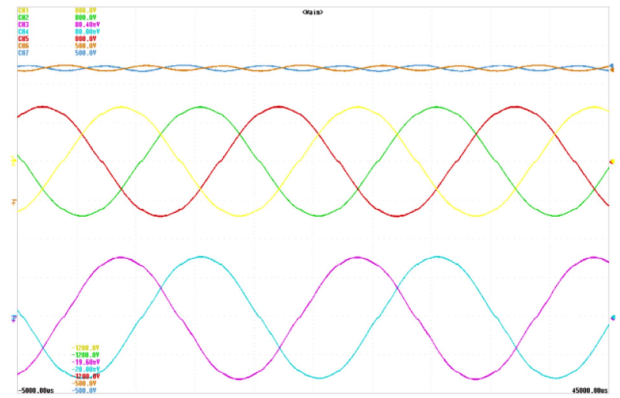
The total harmonic distortion of the phase current is close to  $THD_i=2.8\%$ . Fig. 15 shows the blocking voltage across the power semiconductors located in the half circuit of phase A - Leg 1.

The stress of the power diode  $D_{Ra31(L1)}$  is equal to  $3/4 V_{BUS}$ , while the stress of the power semiconductors  $S_{Ra32(L1)}-S_{RaB(L1)}$  and  $S_{Ra21(L1)}-S_{Ra22(L1)}$  are equal to  $1/4 V_{BUS}$  and  $1/2 V_{BUS}$ . There is a completely dual situation on the blocking voltage of the power semiconductors located in the other half of the converter. Fig. 16 illustrates the comparison between the blocking voltage of the power diodes  $D_{Ra31(L1)}$ ,  $D_{Ra31(L2)}$  and power switches  $S_{Ra32(L1)}$ ,  $S_{Ra32(L2)}$  located in the Leg 1 and Leg 2 of the phase A. As it is clearly visible from the zoom, the commutation between the power semiconductors placed in both legs occurs in opposite phase.

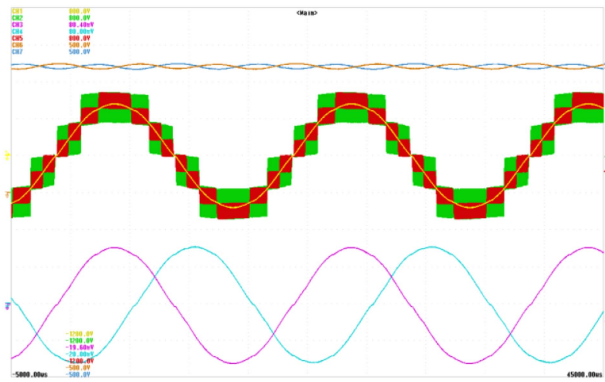




**FIGURE 16.** Blocking voltage waveforms of the power semiconductors into Leg 1 and Leg 2 at a steady state:  $D_{Ra31(L1)}$  (CH3-violet line, 200V/div),  $D_{Ra31(L2)}$  (CH4-cyan line, 200V/div),  $S_{Ra32(L1)}$  (CH5-red line, 200V/div),  $S_{Ra32(L2)}$  (CH6-brown line, 200 V/div). Time scale: 5 ms/div.



**FIGURE 18.** Voltage and current waveforms at a steady state: output voltage  $u_u$  (CH1-yellow line, 200V/div), output voltage  $u_v$  (CH2-green line, 200V/div), output voltage  $u_w$  (CH5-red line, 200V/div), output inductor current  $i_u$  (CH3-violet line, 20A/div), output inductor current  $i_v$  (CH4-cyan line, 20A/div), bottom half DC-bus voltage  $V_{CB,L}=V_{CB1}+V_{CB2}$  (CH6-brown line, 100V/div) and top half DC-bus voltage  $V_{CB,H}=V_{CB3}+V_{CB4}$  (CH7-blue line, 100V/div). Time scale: 5ms/div.



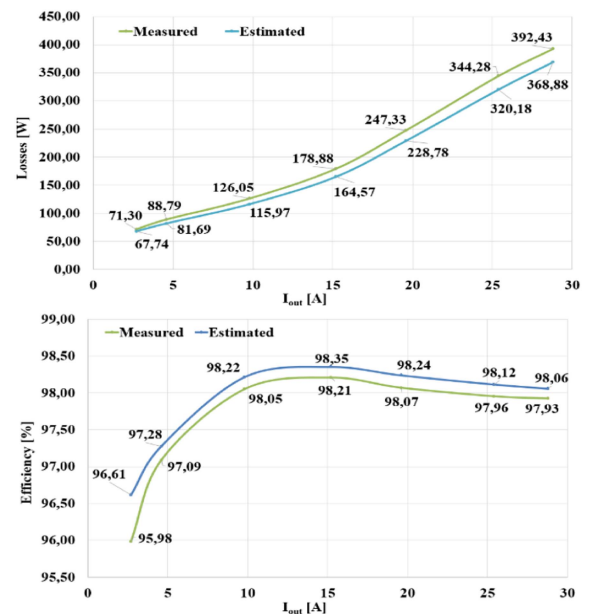
**FIGURE 17.** Voltage and current waveforms at a steady state: output voltage  $u_u$  (CH1-yellow line, 200V/div), output phase-to-neutral switching voltage  $u_{u1(sw)}$  (CH2-green line, 200V/div), output phase-to-neutral switching voltage  $u_{u(sw)}$  (CH5-red line, 200V/div), output inductor current  $i_u$  (CH3-violet line, 20A/div), output inductor current  $i_v$  (CH4-cyan line, 20A/div), bottom half DC-bus voltage  $V_{CB,L}=V_{CB1}+V_{CB2}$  (CH6-brown line, 100V/div) and top half DC-bus voltage  $V_{CB,H}=V_{CB3}+V_{CB4}$  (CH7-blue line, 100V/div). Time scale: 5ms/div.

### B. 1-3 $\Phi$ 5L E-TYPE INVERTER WAVEFORMS

According to the closed loop proposed in [37], the inverter side is controlled using a multi-resonant controller. Fig. 17 shows the voltages and currents under resistive load when the output power is closed to 10kW and  $U_0=220V$ ,  $f_0=50Hz$ ,  $f_{sw}=24kHz$ ,  $V_{BUS}=700V$  and  $M_{0,I}=0.9$ . The voltage of Leg 1  $u_{u1(sw)}$  shows five levels the voltage at the output of phase A  $u_{u(sw)}$  shows nine levels. Fig. 18 illustrates the three-phase output voltages  $u_u$ ,  $u_v$ ,  $u_w$ , and the phase currents  $i_u$  and  $i_v$ . The total harmonic distortion of the output voltage is close to  $THD_v=0.85\%$ .

### C. EFFICIENCY MEASUREMENTS

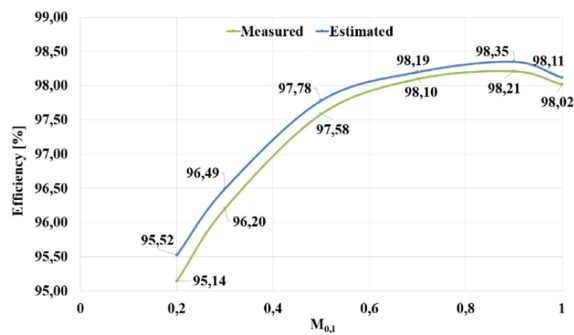
The converter's efficiency has been evaluated using the power analyzer Voltech PM3000A, where one channel has been used to measure the input power at the DC-bus, and two channels have been used to measure the output power through Aron's insertion. The efficiency measurement results are compared



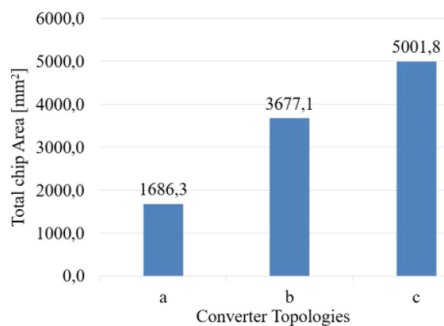
**FIGURE 19.** Estimated and measured losses and efficiency of the 1-3 $\Phi$ 5L BTB E-type converter as a function of output current.

with those calculated analytically, as illustrated in Fig. 19. Efficiency results are evaluated at  $U_{in}=U_0=220 V$ ,  $f_0=50 Hz$ ,  $f_{sw}=24 kHz$ ,  $V_{BUS}=700 V$  and  $M_{0,R}=M_{0,I}=0.9$ , where all the converter losses, including the input and output filters and the auxiliary power, have been considered. The efficiency measurement results of the prototype converter match the calculated losses over a wide output range. Furthermore, the efficiency at rated power is above 98%, while the peak efficiency is close to 98.35%.





**FIGURE 20.** Measured and estimated efficiency as a function of inverter modulation depth  $M_{0,I}$ , when the three-phase resistive load is  $10\Omega$ .



**FIGURE 21.** Total chip area for different BTB topologies: (a) 1-3Φ2L BTB converter, (b) 1-3Φ3L BTB T-type converter, and (c) 1-3Φ5L BTB E-type converter.

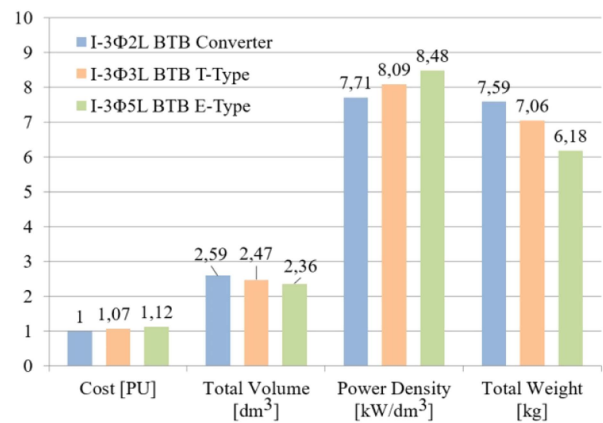
The conversion efficiency changes as the modulation depth decreases. Fig. 20 shows the measured and estimated efficiency as a function of inverter modulation depth  $M_{0,I}$  when the three-phase resistive load is  $10\Omega$ .

When the inverter modulation depth  $M_{0,I}$  is above 0.6, the converter works with five voltage levels at the output, and the converter's efficiency is almost constant. When the inverter modulation depth  $M_{0,I}$  close to 0.5, the converter works with the three voltage levels, and the efficiency decreases. When the inverter modulation depth  $M_{0,I}$  is low 0.5, the converter operates with two or three voltage levels at the output, and efficiency drops dramatically.

## V. REMARKS

This section addresses the selection of the electrolytic capacitors and the proposed topology's increasing number of power semiconductors. Due to the high energy density, low rated voltage, and costs, the electrolytic capacitors (e-caps) have been selected to build the bulk DC-bus. An alternative solution to electrolytic capacitors could be given by film capacitors. Table 5 shows the main parameters of the selected e-caps and potential film capacitors that are suitable for the proposed topology.

The size of the selected capacitor is minimal compared to the film capacitor. Six parallel e-cap capacitors provide a capacitance of  $1320\mu\text{F}$ , while five parallel film capacitors



**FIGURE 22.** Comparison between 1-3Φ5L BTB E-type converter, 1-3Φ2L BTB converter and 1-3Φ3L BTB converter. Nominal power  $20\text{ kW}$ ,  $f_0=50\text{ Hz}$ ,  $f_{sw}=24\text{ kHz}$ ,  $V_{BUS}=700\text{ V}$ .

provide  $1300\mu\text{F}$ . The comparison between the selected and film capacitors in terms of surface area, cost, and losses is given in Table 6. Considering the same total capacitance for  $1/4V_{BUS}$ , the surface area used by the film capacitors is enormously more significant than the e-cap capacitors, as shown in Table 6.

This significantly impacts on the power density of the converter. Considering Table 6, it can be seen that the price to build up the DC-bus arrangement by using the e-cap is definitely lower than using film capacitor. In contrast, since the ESR of the selected e-cap is high, the losses provided by the film capacitors are lower when compared to the e-caps. Thus, the resulting efficiency could have been higher by using film capacitors despite the cost.

The proposed topology shows a high number of power semiconductors, and consequently, the surface chip areas increase too, including the gate driver circuit. However, increasing the number of power semiconductors to increase the voltage levels results in the low weight and volume of the passive components. In fact, keeping the device's losses constant, a classic two-level converter must use two times the switching frequency of a three-level converter to achieve the same ripple in the output current. Thus, the input/output filter components in a 5-Level converter will be smaller in both value and size than the filter components for a two-level converter [51]. Furthermore, using two interleaving multilevel cells reduces the current ripple further [52]. The harmonics content of the voltage improves due to eliminating harmonics below  $f_{sw} \cdot N_c$ , where  $N_c$  is the number of interleaved cells. If the current ripple is reduced and the voltage harmonics content improves, the interleaved topology considerably reduces the required filter size. Besides, sharing the current among several converter legs enables smaller, lower current power devices than those used in a conventional converter; the smaller power semiconductors can switch at a significantly higher frequency than the larger ones, thus reducing inductor size. Let's compare the interleaved three-phase 2-Level and 3-Level BTB topologies

(I-3Φ2L BTB Converter, I-3Φ3L BTB T-Type Converter) and the proposed converter. Assuming the 3-level T-Type topology is built using 1200 V and 650 V SiC devices (part number: AIMW120R045M1 and IMZA65R083M1H) and the 2-level converter has been built using 1200 V power semiconductors (part number: AIMW120R045M1). The proposed topology uses 84 power switches and 12 power diodes, while the 3-level T-Type and 2-level topologies use 48 and 24 switches.

Fig. 21 shows the total chip areas for each topology and the proposed converter uses more chip areas than the other topologies. The high number of power switches has a negative impact on the realization of the gate driver circuit. The length and height of the driver board are 90 mm and 110 mm, respectively. Thus, the surface area of the driver boards is 29700 mm<sup>2</sup>. The driver boards of the 2-Level and 3-Level converters will be smaller in size. However, to obtain the same THD voltage and current at the input and output of the converter, the capacitance and inductance values of the filters are more significant in the 2-level and 3-level converters compared to the 5-level converter. This latter results in increasing the size and weight of the converter. Considering the THD of the input current less than 3% and the THD of the output voltage less than 1%, the input and output capacitance and inductance values are 60 μH and 4.7 μF, respectively. Applying the procedure [38] to the 2-level and 3-level topologies leads to the capacitance and inductance values listed in Table 7.

The values of the capacitance and inductance are low in the proposed converter. Regarding the ICT, the core cross-section  $A_E$  in the 2L and 3L converters is four times and double that of 5-level converter. As can be seen, the volume, size, and weight of the ICTs and inductors in the case of 2L and 3L T-Type BTB topologies are very high compared with those of the proposed converter. Finally, to better compare the topologies, the cost-benefit of the 2L, 3L and 5L BTB converters have been carried out. Fig. 22 shows the comparison of the topologies based on the figures of merit (FOM) such as cost, volume power density and weight, considering all parts of the converters, DC-bus, power stage, had-sink driver, and filter boards.

The proposed converter shows a slight increment of cost compared to the other topologies. The cost comparison between the topologies has been carried out considering the price per unit. In contrast, from this analysis, it is possible to understand how the proposed conversion system's weight and volume are reduced even with a high number of power semiconductors.

## VI. CONCLUSION

The optimization design procedure of the I-3Φ5L BTB E-Type Converter used for VDF and UPS applications has been presented in this article. The working principle of the converter and the advantages of using the interleaving topology have been explained. The design procedure of the proposed multilevel converter has been described step by step. The selection of the DC-bus capacitors has been shown, and the loss distribution as a function of the operating conditions has been

estimated starting from the analytical analysis. The thermal model of power semiconductors has been created, considering the parameters provided by the manufacturers. The Si and SiC power semiconductors have been selected according to the design procedure. The design and the realization of the driver board have been exhibited. Furthermore, the design and selection of passive components used in the filter board have been illustrated. Thanks to the use of two cells interleaved topology, the advantages in terms of size and losses have been demonstrated. According to the proposed procedure, the prototype of the converter has been built, achieving a total weight of 6.18 kg and a power density of 8.4 kW/dm<sup>3</sup>. Experimental waveforms validate the illustrated theoretical analysis, showing a total harmonic distortion of the current  $THDi=2.8\%$  and a total harmonic distortion of the voltage  $THDv=0.85\%$ , and a peak efficiency close to 98.2%, including input and output filters, gate driver board and the auxiliary power supplies.

## APPENDIX

The duty cycles for each power semiconductor in both the rectifier and the inverter of a single leg of the converter, when the PD-PWM modulation is used, are listed in Tables 8 and 9,

**TABLE 8. List of the Duty Cycles for Each Power Semiconductors of the Single Leg 5L Rectifier**

$d_{S_{ro1}}(t) = \begin{cases} 0 & \theta_R \in [0, \pi], \theta_R \in [\pi, \pi + \alpha_1], \theta_R \in [2\pi - \alpha_1, 2\pi] \\ -1 - 2M_{0,R} \sin(\theta_R) & \theta_R \in [\pi, 2\pi - \alpha_1] \end{cases}$
$d_{S_{ro12}}(t) = \begin{cases} 1 & \theta_R \in [0, \pi], \theta_R \in [\pi, \pi + \alpha_1], \theta_R \in [2\pi - \alpha_1, 2\pi] \\ 2[1 + M_{0,R} \sin(\theta_R)] & \theta_R \in [\pi + \alpha_1, 2\pi - \alpha_1] \end{cases}$
$d_{S_{ro21}}(t) = \begin{cases} 1 - 2M_{0,R} \sin(\theta_R) & \theta_R \in [0, \alpha_1], \theta_R \in [\pi - \alpha_1, \pi] \\ 0 & \theta_R \in [\alpha_1, \pi - \alpha_1] \\ 1 & \theta_R \in [\pi, 2\pi] \end{cases}$
$d_{S_{ro22}}(t) = \begin{cases} 1 & \theta_R \in [0, \pi] \\ 1 + 2M_{0,R} \sin(\theta_R) & \theta_R \in [\pi, \pi + \alpha_1], \theta_R \in [2\pi - \alpha_1, 2\pi] \\ 0 & \theta_R \in [\pi + \alpha_1, 2\pi - \alpha_1] \end{cases}$
$d_{S_{ro32}}(t) = \begin{cases} 1 & \theta_R \in [0, \alpha_1], \theta_R \in [\pi - \alpha_1, \pi], \theta_R \in [\pi, 2\pi] \\ 2[1 - M_{0,R} \sin(\theta_R)] & \theta_R \in [\alpha_1, \pi - \alpha_1] \end{cases}$
$d_{S_{roB}}(t) = \begin{cases} -1 + 2M_{0,R} \sin(\theta_R) & [\alpha_1, \pi - \alpha_1] \\ 0 & \theta_R \in [0, \alpha_1], \theta_R \in [\pi - \alpha_1, \pi], \theta_R \in [\pi, 2\pi] \end{cases}$

where  $\theta_R = \omega_{int}t$  and  $\theta_I = \omega_{out}t$ .

The AVG and RMS currents flowing through the power semiconductors are function of duty cycle as they can be seen from (17).

$$I_{RMS} = \sqrt{\frac{1}{2\pi} \int_0^\pi [i^2(t) \cdot d_d(t)] d(\omega t)}$$

$$I_{AVG} = \frac{1}{2\pi} \int_0^\pi [i(t) \cdot d_d(t)] d(\omega t) \quad (17)$$

Replacing the duty cycles listed in Tables 8 and 9 into (17), the (6) can be obtained, where the coefficients of the AVG

**TABLE 9.** List of the Duty Cycles for Each Power Semiconductor of the Single Leg 5L Inverter

$d_{S_{ht1}}(t) = \begin{cases} 0 & \theta_i \in [0, \pi], \theta_i \in [\pi, \alpha_1 + \pi], \theta_i \in [2\pi - \alpha_1, 2\pi] \\ -1 - 2M_{0,i} \sin(\theta_i) & \theta_i \in [\alpha_1 + \pi, 2\pi - \alpha_1] \end{cases}$
$d_{S_{ht2}}(t) = \begin{cases} 1 & \theta_i \in [0, \pi], \theta_i \in [\pi, \alpha_1 + \pi], \theta_i \in [2\pi - \alpha_1, 2\pi] \\ 2[1 + M_{0,i} \sin(\theta_i)] & \theta_i \in [\alpha_1 + \pi, 2\pi - \alpha_1] \end{cases}$
$d_{S_{ht3}}(t) = \begin{cases} 0 & \theta_i \in [0, \pi] \\ -2M_{0,i} \sin(\theta_i) & \theta_i \in [\pi, \alpha_1 + \pi], \theta_i \in [2\pi - \alpha_1, 2\pi] \\ 1 & \theta_i \in [\alpha_1 + \pi, 2\pi - \alpha_1] \end{cases}$
$d_{S_{ht4}}(t) = \begin{cases} 1 - 2M_{0,i} \sin(\theta_i) & \theta_i \in [0, \alpha_1], \theta_i \in [\pi - \alpha_1, \pi] \\ 0 & \theta_i \in [\alpha_1, \pi - \alpha_1] \\ 1 & \theta_i \in [\pi, 2\pi] \end{cases}$
$d_{S_{ht5}}(t) = \begin{cases} 1 & \theta_i \in [0, \pi] \\ 1 + 2M_{0,i} \sin(\theta_i) & \theta_i \in [\pi, \alpha_1 + \pi], \theta_i \in [2\pi - \alpha_1, 2\pi] \\ 0 & \theta_i \in [\alpha_1 + \pi, 2\pi - \alpha_1] \end{cases}$
$d_{S_{ht6}}(t) = \begin{cases} 2M_{0,i} \sin(\theta_i) & \theta_i \in [0, \alpha_1], \theta_i \in [\pi - \alpha_1, \pi] \\ 1 & \theta_i \in [\alpha_1, \pi - \alpha_1] \\ 0 & \theta_i \in [\pi, 2\pi] \end{cases}$
$d_{S_{ht7}}(t) = \begin{cases} 1 & \theta_i \in [0, \alpha_1], \theta_i \in [\pi - \alpha_1, \pi], \theta_i \in [\pi, 2\pi] \\ 2[1 - M_{0,i} \sin(\theta_i)] & \theta_i \in [\alpha_1, \pi - \alpha_1] \end{cases}$
$d_{S_{ht8}}(t) = \begin{cases} 0 & \theta_i \in [0, \alpha_1], \theta_i \in [\pi - \alpha_1, \pi], \theta_i \in [\pi, 2\pi] \\ -1 + 2M_{0,i} \sin(\theta_i) & \theta_i \in [\alpha_1, \pi - \alpha_1] \end{cases}$

**TABLE 10.** RMS and AVG Current Coefficients of the Rectifier

$i$	Devices	Coefficients
1	$D_{Rxt1}, D_{Rxt31}$	$a_{RMS,1} = 3\pi - 6\alpha_1 - 3\sin(2\alpha_1)$
		$b_{RMS,1} = 8(\cos(\alpha_1) + 2)(\cos(\alpha_1) - 1)^2$
		$a_{AVG,1} = 2\cos(\alpha_1)$
		$b_{AVG,1} = 2\alpha_1 - \sin(2\alpha_1)$
2	$S_{Rxt4}, S_{RxtB}$	$a_{RMS,2} = 3\pi - 6\alpha_1 + 3\sin(2\alpha_1)$
		$b_{RMS,2} = -4\cos(\alpha_1)(\cos^2(\alpha_1) - 3)$
		$a_{AVG,2} = -2\cos(\alpha_1)$
		$b_{AVG,2} = \sin(2\alpha_1) - 2\alpha_1 + \pi$
3	$S_{Rxt2}, S_{Rxt32}$	$a_{RMS,3} = \frac{3}{2}(\pi - 2\alpha_1 + \sin(2\alpha_1))$
		$b_{RMS,3} = 2\left[\cos(\alpha_1)(\cos^2(\alpha_1) - 3) + (\cos(\alpha_1) + 2)(\cos(\alpha_1) - 1)^2\right]$
		$a_{AVG,3} = 4\cos(\alpha_1)$
		$b_{AVG,3} = 4\alpha_1 - 2\sin(2\alpha_1) - \pi$
4	$S_{Rxt21}, S_{Rxt22}$	$a_{RMS,4} = \frac{1}{2}\left[2\alpha_1 - \sin(2\alpha_1)\right]$
		$b_{RMS,4} = 2(\cos(\alpha_1) - 1)^2(-\cos(\alpha_1) - 2)$
		$a_{AVG,4} = 2(1 - \cos(\alpha_1))$
		$b_{AVG,4} = \sin(2\alpha_1) - 2\alpha_1$

**TABLE 11.** RMS and AVG Current Coefficients of the Inverter

$j$	Devices	Coefficients
1	$S_{ly31}, S_{ly11}$	$a_{RMS,1} = 3\pi - 6\alpha_1 - 3\sin(2\alpha_1) + 6\sin(2\alpha_1)\cos^2(\varphi_{out})$
		$b_{RMS,1} = -4\sin(\varphi_{out})^2 + 6\sin\left(\frac{\alpha_1 + \varphi_{out}}{2}\right)^2 - 2\sin\left(\frac{3\alpha_1 + \varphi_{out}}{2}\right)^2 + \sin(3\alpha_1 - \varphi_{out}) - 6\cos(\alpha_1) + 8\cos(\varphi_{out}) - 3\cos(\alpha_1 - 2\varphi_{out})$
		$a_{AVG,1} = 4\cos(\alpha_1)\cos(\varphi_{out})$
		$b_{AVG,1} = 2\sin(\alpha_1) + \cos(\varphi_{out})[4\alpha_1 - 2\sin(2\alpha_1) - 2\varphi_{out}]$
2	$S_{ly34}, S_{lyB}$	$a_{RMS,2} = 6\alpha_1 - 3\pi + 3\sin(2\alpha_1) - 3(1 + \cos(2\varphi_{out}))\sin(2\alpha_1)$
		$b_{RMS,2} = 8\cos^3(\alpha_1) + 24\cos^2(\varphi_{out})\cos(\alpha_1) - 12\cos^3(\alpha_1)\cos(\varphi_{out})$
		$a_{AVG,2} = -2\cos(\varphi_{out})\cos(\alpha_1)$
		$b_{AVG,2} = \cos(\varphi_{out})[\sin(2\alpha_1) - 2\alpha_1 + \pi]$
3	$S_{ly12}, S_{ly32}$	$a_{RMS,3} = \frac{3}{2}\left[\pi - 2\alpha_1 + \sin(2\alpha_1)\cos(2\varphi_{out})\right]$
		$b_{RMS,3} = \frac{1}{2}\left[3 - 12\cos(\alpha_1) + 4\cos(\varphi_{out}) + \cos(2\varphi_{out}) - 6\cos(2\varphi_{out})\cos(\alpha_1) + 2\cos(3\alpha_1)\cos(2\varphi_{out})\right]$
		$a_{AVG,3} = 8\cos(\alpha_1)\cos(\varphi_{out})$
		$b_{AVG,3} = 2\sin(\varphi_{out}) + 2\alpha_1\cos(\varphi_{out}) - 2\varphi_{OUT}\cos(\varphi_{out}) + 3\sin(2\alpha_1)\cos(\varphi_{out}) - \pi\cos(\varphi_{out})$
4	$S_{ly21}, S_{ly22}$	$a_{RMS,4} = 3\alpha_1 - 3\cos(2\varphi_{out})\cos(\alpha_1)\sin(\alpha_1)$
		$b_{RMS,4} = -6 + 6\cos(\alpha_1) - 2\cos(2\varphi_{out}) + 6\cos(2\varphi_{out})\cos(\alpha_1) - 4\cos(2\varphi_{out})\cos^3(\alpha_1)$
		$a_{AVG,4} = 2 - 2\cos(\varphi_{out})\cos(\alpha_1)$
		$b_{AVG,4} = -2\cos(\varphi_{out}) + \sin(2\alpha_1)\cos(\varphi_{out}) - 2\alpha_1\cos(\varphi_{out}) + 2\varphi_{out}\cos(\varphi_{out})$

and RMS currents  $a_{RMS,i}, b_{RMS,i}, a_{AVG,i}, b_{AVG,i}, a_{RMS,j}, b_{RMS,j}, a_{AVG,j}, b_{AVG,j}$  are listed in Tables 10 and 11.

## ACKNOWLEDGMENT

The Authors are thankful to "Sky Research doo" for building the prototype of the multilevel converters including the power filter used in the experimental campaign.

## REFERENCES

- [1] J. Zhang, J. Liu, J. Yang, N. Zhao, Y. Wang, and T. Q. Zheng, "A modified DC power electronic transformer based on series connection of full-bridge converters," *IEEE Trans. Power Electron.*, vol. 34, no. 3, pp. 2119–2133, Mar. 2019, doi: [10.1109/TPEL.2018.2842728](https://doi.org/10.1109/TPEL.2018.2842728).
- [2] M. Naderi, Y. Khayat, Q. Shafiee, T. Dragicevic, H. Bevrani, and F. Blaabjerg, "Interconnected autonomous AC microgrids via back-to-back converters—Part I: Small-signal modeling," *IEEE Trans. Power Electron.*, vol. 35, no. 5, pp. 4728–4740, May 2020, doi: [10.1109/TPEL.2019.2943996](https://doi.org/10.1109/TPEL.2019.2943996).
- [3] M. Naderi, Y. Khayat, Q. Shafiee, T. Dragičević, H. Bevrani, and F. Blaabjerg, "Interconnected autonomous AC microgrids via back-to-back converters—Part II: Stability analysis," *IEEE Trans. Power Electron.*, vol. 35, no. 11, pp. 11801–11812, Nov. 2020, doi: [10.1109/TPEL.2020.2986695](https://doi.org/10.1109/TPEL.2020.2986695).
- [4] E. Afshari and M. Amirabadi, "An input-series output-parallel modular three-phase AC–AC capacitive-link power converter," *IEEE Trans. Power Electron.*, vol. 36, no. 12, pp. 13603–13620, Dec. 2021, doi: [10.1109/TPEL.2021.3085873](https://doi.org/10.1109/TPEL.2021.3085873).

- [5] R. Kawashima, T. Mishima, and C. Ide, "Three-phase to single-phase multiresonant direct AC-AC converter for metal hardening high-frequency induction heating applications," *IEEE Trans. Power Electron.*, vol. 36, no. 1, pp. 639–653, Jan. 2021, doi: [10.1109/TPEL.2020.3003026](https://doi.org/10.1109/TPEL.2020.3003026).
- [6] A. A. Khan, H. Cha, and H. F. Ahmed, "A new reliable three-phase buck-boost AC-AC converter," *IEEE Trans. Ind. Electron.*, vol. 65, no. 2, pp. 1000–1010, Feb. 2018, doi: [10.1109/TIE.2017.2733439](https://doi.org/10.1109/TIE.2017.2733439).
- [7] J. W. Kolar, T. Friedli, J. Rodriguez, and P. W. Wheeler, "Review of three-phase PWM AC-AC converter topologies," *IEEE Trans. Ind. Electron.*, vol. 58, no. 11, pp. 4988–5006, Nov. 2011, doi: [10.1109/TIE.2011.2159353](https://doi.org/10.1109/TIE.2011.2159353).
- [8] A. Ammar, H. Y. Kanaan, N. Moubayed, M. Hamouda, and K. Al-Haddad, "Original approach toward three-phase indirect matrix converters through hybrid PWM modulation and DSP implementation," *IEEE Access*, vol. 8, pp. 45837–45852, 2020, doi: [10.1109/ACCESS.2020.2977502](https://doi.org/10.1109/ACCESS.2020.2977502).
- [9] T. Friedli, J. W. Kolar, J. Rodriguez, and P. W. Wheeler, "Comparative evaluation of three-phase AC-AC matrix converter and voltage DC-link back-to-back converter systems," *IEEE Trans. Ind. Electron.*, vol. 59, no. 12, pp. 4487–4510, Dec. 2012, doi: [10.1109/TIE.2011.2179278](https://doi.org/10.1109/TIE.2011.2179278).
- [10] S. Pipolo, A. Formentini, A. Trentin, P. Zanchetta, M. Calvini, and M. Venturini, "A novel matrix converter modulation with reduced number of commutations," *IEEE Trans. Ind. Appl.*, vol. 57, no. 5, pp. 4991–5000, Sep./Oct. 2021, doi: [10.1109/TIA.2021.3087121](https://doi.org/10.1109/TIA.2021.3087121).
- [11] J. Fang, F. Blaabjerg, S. Liu, and S. M. Goetz, "A review of multilevel converters with parallel connectivity," *IEEE Trans. Power Electron.*, vol. 36, no. 11, pp. 12468–12489, Nov. 2021, doi: [10.1109/TPEL.2021.3075211](https://doi.org/10.1109/TPEL.2021.3075211).
- [12] P. Bakas et al., "Review of hybrid multilevel converter topologies utilizing thyristors for HVDC applications," *IEEE Trans. Power Electron.*, vol. 36, no. 1, pp. 174–190, Jan. 2021, doi: [10.1109/TPEL.2020.2997961](https://doi.org/10.1109/TPEL.2020.2997961).
- [13] A. Salem, H. Van Khang, K. G. Robbersmyr, M. Norambuena, and J. Rodriguez, "Voltage source multilevel inverters with reduced device count: Topological review and novel comparative factors," *IEEE Trans. Power Electron.*, vol. 36, no. 3, pp. 2720–2747, Mar. 2021, doi: [10.1109/TPEL.2020.3011908](https://doi.org/10.1109/TPEL.2020.3011908).
- [14] C. Terbrack, J. Stöttner, and C. Endisch, "Design and validation of the parallel enhanced commutation integrated nested multilevel inverter topology," *IEEE Trans. Power Electron.*, vol. 37, no. 12, pp. 15163–15174, Dec. 2022, doi: [10.1109/TPEL.2022.3183859](https://doi.org/10.1109/TPEL.2022.3183859).
- [15] T. Ilahi et al., "Design and performance analysis of ultra-wide bandgap power devices-based EV fast charger using bi-directional power converters," *IEEE Access*, vol. 11, pp. 25285–25297, 2023, doi: [10.1109/ACCESS.2023.3255780](https://doi.org/10.1109/ACCESS.2023.3255780).
- [16] B. S. Revathi and M. Prabhakar, "Solar PV fed DC microgrid: Applications, converter selection, design and testing," *IEEE Access*, vol. 10, pp. 87227–87240, 2022, doi: [10.1109/ACCESS.2022.3199701](https://doi.org/10.1109/ACCESS.2022.3199701).
- [17] D. Neumayr, D. Bortis, and J. W. Kolar, "The essence of the little box challenge-part A: Key design challenges & solutions," *CPSS Trans. Power Electron. Appl.*, vol. 5, no. 2, pp. 158–179, Jun. 2020, doi: [10.24295/CPSSSTPEA.2020.00014](https://doi.org/10.24295/CPSSSTPEA.2020.00014).
- [18] D. Neumayr, D. Bortis, and J. W. Kolar, "The essence of the little box challenge-part B: Hardware demonstrators & comparative evaluations," *CPSS Trans. Power Electron. Appl.*, vol. 5, no. 3, pp. 251–272, Sep. 2020, doi: [10.24295/CPSSSTPEA.2020.00022](https://doi.org/10.24295/CPSSSTPEA.2020.00022).
- [19] J. Xu, L. Gu, Z. Ye, S. Kargarrizi, and J. M. Rivas-Davila, "Cascade GaN/SiC: A wide-bandgap heterogenous power device for high-frequency applications," *IEEE Trans. Power Electron.*, vol. 35, no. 6, pp. 6340–6349, Jun. 2020, doi: [10.1109/TPEL.2019.2954322](https://doi.org/10.1109/TPEL.2019.2954322).
- [20] L. Nela, R. Van Erp, G. Kampitsis, H. K. Yildirim, J. Ma, and E. Matioli, "Ultra-compact, high-frequency power integrated circuits based on GaN-on-Si Schottky barrier diodes," *IEEE Trans. Power Electron.*, vol. 36, no. 2, pp. 1269–1273, Feb. 2021, doi: [10.1109/TPEL.2020.3008226](https://doi.org/10.1109/TPEL.2020.3008226).
- [21] G. Lyu et al., "A normally-off copackaged SiC-JFET/GaN-HEMT cascode device for high-voltage and high-frequency applications," *IEEE Trans. Power Electron.*, vol. 35, no. 9, pp. 9669–9679, Sep. 2020, doi: [10.1109/TPEL.2020.2971789](https://doi.org/10.1109/TPEL.2020.2971789).
- [22] R. Lai et al., "A systematic topology evaluation methodology for high-density three-phase PWM AC-AC converters," *IEEE Trans. Power Electron.*, vol. 23, no. 6, pp. 2665–2680, Nov. 2008, doi: [10.1109/TPEL.2008.2005381](https://doi.org/10.1109/TPEL.2008.2005381).
- [23] L. de Macedo Barros, C. B. Jacobina, A. C. Oliveira, I. S. de Freitas, and E. R. C. da Silva, "Three-phase-to-three-phase AC/AC DC-link five-leg converters based on three- and two-level legs," *IEEE Trans. Ind. Appl.*, vol. 51, no. 1, pp. 521–530, Jan./Feb. 2015, doi: [10.1109/TIA.2014.2336978](https://doi.org/10.1109/TIA.2014.2336978).
- [24] O. Kwon, J.-M. Kwon, and B.-H. Kwon, "Highly efficient single-phase three-level three-leg converter using SiC MOSFETs for AC-AC applications," *IEEE Trans. Ind. Electron.*, vol. 65, no. 9, pp. 7015–7024, Sep. 2018, doi: [10.1109/TIE.2018.2793231](https://doi.org/10.1109/TIE.2018.2793231).
- [25] H. Uemura, F. Krismer, Y. Okuma, and J. W. Kolar, " $\eta$ - $\rho$  pareto optimization of 3-phase 3-level T-type AC-DC-AC converter comprising Si and SiC hybrid power stage," in *Proc. IEEE Int. Power Electron. Conf.*, 2014, pp. 2834–2841, doi: [10.1109/IPEC.2014.6870083](https://doi.org/10.1109/IPEC.2014.6870083).
- [26] R. Portillo, S. Vazquez, J. I. Leon, M. M. Prats, and L. G. Franquelo, "Model based adaptive direct power control for three-level NPC converters," *IEEE Trans. Ind. Informat.*, vol. 9, no. 2, pp. 1148–1157, May 2013, doi: [10.1109/TII.2012.2209667](https://doi.org/10.1109/TII.2012.2209667).
- [27] K. Niyomsatian, S. Samermurn, S. Suwankawin, and S. Sangwongwanich, "Novel topologies for three-level back-to-back converters based on matrix converter theory," in *Proc. IEEE 38th Annu. Conf. Ind. Electron. Soc.*, 2012, pp. 6099–6104, doi: [10.1109/IECON.2012.6389084](https://doi.org/10.1109/IECON.2012.6389084).
- [28] S. Sangwongwanich, K. Niyomsatian, S. Samermurn, S. Nuchnoi, and S. Suwankawin, "Novel three-level back-to-back converters: Structure, modulation method, and experiment," in *Proc. IEEE Int. Power Electron. Conf.*, 2018, pp. 4096–4103, doi: [10.23919/IPEC.2018.8507487](https://doi.org/10.23919/IPEC.2018.8507487).
- [29] S. Ohn et al., "Design of 20 kW full-SiC, three-level three-phase uninterruptible power supply," in *Proc. IEEE 6th Workshop Wide Bandgap Power Devices Appl.*, 2018, pp. 167–173, doi: [10.1109/WiPDA.2018.8569195](https://doi.org/10.1109/WiPDA.2018.8569195).
- [30] S. Ohn, J. Yu, R. Burgos, D. Boroyevich, and H. Suryanarayana, "Reduced common-mode voltage PWM scheme for full-SiC three-level uninterruptible power supply with small DC-link capacitors," *IEEE Trans. Power Electron.*, vol. 35, no. 8, pp. 8638–8651, Aug. 2020, doi: [10.1109/TPEL.2019.2962964](https://doi.org/10.1109/TPEL.2019.2962964).
- [31] G. H. P. Ooi, A. I. Maswood, and Z. Lim, "Five-level multiple-pole PWM AC-AC converters with reduced components count," *IEEE Trans. Ind. Electron.*, vol. 62, no. 8, pp. 4739–4748, Aug. 2015, doi: [10.1109/TIE.2015.2405504](https://doi.org/10.1109/TIE.2015.2405504).
- [32] T. Ishida, K. Matsuse, T. Miyamoto, K. Sasagawa, and L. Huang, "Fundamental characteristics of five-level double converters with adjustable dc voltages for induction motor drives," *IEEE Trans. Ind. Electron.*, vol. 49, no. 4, pp. 775–782, Aug. 2002, doi: [10.1109/TIE.2002.801061](https://doi.org/10.1109/TIE.2002.801061).
- [33] G. Mademlis and Y. Liu, "DC link voltage balancing technique utilizing space vector control in SiC-based five-level back-to-back-connected NPC converters," in *Proc. IEEE Energy Convers. Congr. Expo.*, 2018, pp. 3032–3037, doi: [10.1109/ECCE.2018.8558080](https://doi.org/10.1109/ECCE.2018.8558080).
- [34] K. Wang, Z. Zheng, Y. Li, L. Xu, and H. Ma, "Multi-objective optimization PWM control for a back-to-back five-level ANPC converter," in *Proc. IEEE Energy Convers. Congr. Expo.*, 2012, pp. 3514–3519, doi: [10.1109/ECCE.2012.6342492](https://doi.org/10.1109/ECCE.2012.6342492).
- [35] Z. Liu, Z. Xia, F. Li, G. Wang, and C. Li, "A capacitor voltage precharge method for back-to-back five-level active neutral-point-clamped converter," *IEEE Trans. Ind. Electron.*, vol. 68, no. 10, pp. 9277–9286, Oct. 2021, doi: [10.1109/TIE.2020.3026274](https://doi.org/10.1109/TIE.2020.3026274).
- [36] M. Mazuela, I. Baraia, A. Sanchez-Ruiz, I. Echeverria, I. Torre, and I. Atutxa, "DC-link voltage balancing strategy based on SVM and reactive power exchange for a 5L-MPC back-to-back converter for medium-voltage drives," *IEEE Trans. Ind. Electron.*, vol. 63, no. 12, pp. 7864–7875, Dec. 2016, doi: [10.1109/TIE.2016.2580128](https://doi.org/10.1109/TIE.2016.2580128).
- [37] M. di Benedetto, A. Lidozzi, L. Solero, F. Crescimbin, and P. J. Grbović, "Five-level E-type inverter for grid-connected applications," *IEEE Trans. Ind. Appl.*, vol. 54, no. 5, pp. 5536–5548, Sep./Oct. 2018, doi: [10.1109/TIA.2018.2859040](https://doi.org/10.1109/TIA.2018.2859040).
- [38] M. di Benedetto, A. Lidozzi, L. Solero, F. Crescimbin, and P. J. Grbović, "Low volume and low weight 3-phase 5-level back-to-back E-type converter," *IEEE Trans. Ind. Appl.*, vol. 55, no. 6, pp. 7377–7388, Nov./Dec. 2019, doi: [10.1109/TIA.2019.2928508](https://doi.org/10.1109/TIA.2019.2928508).
- [39] K. Park, F. D. Kieferndorf, U. Drofenik, S. Pettersson, and F. Canales, "Optimization of LCL filter with integrated intercell transformer for two-interleaved high-power grid-tied converters," *IEEE Trans. Power Electron.*, vol. 35, no. 3, pp. 2317–2333, Mar. 2020, doi: [10.1109/TPEL.2019.2926312](https://doi.org/10.1109/TPEL.2019.2926312).



- [40] A. M. Y. M. Ghias, J. Pou, G. J. Capella, V. G. Agelidis, R. P. Aguilera, and T. Meynard, "Single-carrier phase-disposition PWM implementation for multilevel flying capacitor converters," *IEEE Trans. Power Electron.*, vol. 30, no. 10, pp. 5376–5380, Oct. 2015, doi: [10.1109/TPEL.2015.2427201](https://doi.org/10.1109/TPEL.2015.2427201).
- [41] L. M. Grzesiak and J. Tomasik, "DC link balancing method in back-to-back UPS system with multi-level converters," in *Proc. IEEE Int. Symp. Ind. Electron.*, 2006, pp. 908–913, doi: [10.1109/ISIE.2006.295756](https://doi.org/10.1109/ISIE.2006.295756).
- [42] H. Wang and F. Blaabjerg, "Reliability of capacitors for DC-link applications in power electronic converters—An overview," *IEEE Trans. Ind. Appl.*, vol. 50, no. 5, pp. 3569–3578, Sep./Oct. 2014, doi: [10.1109/TIA.2014.2308357](https://doi.org/10.1109/TIA.2014.2308357).
- [43] Z. Qin, H. Wang, F. Blaabjerg, and P. C. Loh, "Investigation into the control methods to reduce the DC-link capacitor ripple current in a back-to-back converter," in *Proc. IEEE Energy Convers. Congr. Expo.*, 2014, pp. 203–210, doi: [10.1109/ECCE.2014.6953395](https://doi.org/10.1109/ECCE.2014.6953395).
- [44] N. Kim, C. Park, S. Kwak, and J. Baek, "Experimental comparisons and evaluations of different types of DC-link capacitors for VSI-based electric compressors in battery electric vehicle systems," *Electronics*, vol. 9, no. 8, 2020, Art. no. 1276, doi: [10.3390/electronics9081276](https://doi.org/10.3390/electronics9081276).
- [45] Z. Yang, L. Xi, Y. Zhang, and X. Chen, "An online parameter identification method for non-solid aluminum electrolytic capacitors," *IEEE Trans. Circuits Syst. II: Exp. Briefs*, vol. 69, no. 8, pp. 3475–3479, Aug. 2022, doi: [10.1109/TCSII.2022.3158938](https://doi.org/10.1109/TCSII.2022.3158938).
- [46] M. Di Benedetto, A. Lidozzi, L. Solero, F. Crescimbin, and P. J. Grbovic, "Performance assessment of the 5-level 3-phase back to back E-type converter," in *Proc. IEEE Energy Convers. Congr. Expo.*, 2017, pp. 2106–2113, doi: [10.1109/ECCE.2017.8096418](https://doi.org/10.1109/ECCE.2017.8096418).
- [47] C.-L. Su, W.-L. Chung, and K.-T. Yu, "An energy-savings evaluation method for variable-frequency-drive applications on ship central cooling systems," *IEEE Trans. Ind. Appl.*, vol. 50, no. 2, pp. 1286–1294, Mar./Apr. 2014, doi: [10.1109/TIA.2013.2271991](https://doi.org/10.1109/TIA.2013.2271991).
- [48] D. Liu et al., "Full custom design of an arbitrary waveform gate driver with 10-GHz waypoint rates for GaN FETs," *IEEE Trans. Power Electron.*, vol. 36, no. 7, pp. 8267–8279, Jul. 2021, doi: [10.1109/TPEL.2020.3044874](https://doi.org/10.1109/TPEL.2020.3044874).
- [49] A. Mallik and A. Khaligh, "Control of a three-phase boost PFC converter using a single DC-link voltage sensor," *IEEE Trans. Power Electron.*, vol. 32, no. 8, pp. 6481–6492, Aug. 2017, doi: [10.1109/TPEL.2016.2614769](https://doi.org/10.1109/TPEL.2016.2614769).
- [50] M. Tang, S. Bifaretti, S. Pipolo, S. Odhano, and P. Zanchetta, "A novel repetitive controller assisted phase-locked loop with self-learning disturbance rejection capability for three-phase grids," *IEEE J. Emerg. Sel. Topics Power Electron.*, vol. 8, no. 2, pp. 1870–1879, Jun. 2020, doi: [10.1109/JESTPE.2019.2941835](https://doi.org/10.1109/JESTPE.2019.2941835).
- [51] P. J. Grbovic, A. Lidozzi, L. Solero, and F. Crescimbin, "Five-level unidirectional T-rectifier for high-speed gen-set applications," *IEEE Trans. Ind. Appl.*, vol. 52, no. 2, pp. 1642–1651, Mar./Apr. 2016, doi: [10.1109/TIA.2015.2504469](https://doi.org/10.1109/TIA.2015.2504469).
- [52] P. J. Grbovic, "Closed form analysis of N-cell interleaved two-level DC-DC converters: The DC bus capacitor current stress," in *Proc. IEEE ECCE Asia Downunder*, 2013, pp. 122–129, doi: [10.1109/ECCE-Asia.2013.6579084](https://doi.org/10.1109/ECCE-Asia.2013.6579084).



**MARCO DI BENEDETTO** (Member, IEEE) received the M.Eng. degree in electronic engineering from the University of Roma Tor Vergata, Rome, Italy, in 2014, and the Ph.D. in mechanical and industrial engineering from the Roma Tre University, Rome, in 2018. Since 2018, he has been a Research Fellow with the Center of Power Electronics and Drives, Roma Tre University. In October 2022, he was appointed to position of an Assistant Professor with the Department of Industrial, Electronic and Mechanical Engineering, Roma Tre University. His main research is focuses on hardware and FPGA control design for multilevel power converter topologies.



**ALESSANDRO LIDOZZI** (Member, IEEE) received the Electronic Engineering and Ph.D. degrees from the Roma Tre University, Rome, Italy, in 2003 and 2007, respectively.

From 2010 to 2017, he was a Researcher with the Department of Engineering, Roma Tre University, where since 2017, he has been an Associate Professor. His main research interests include power converter modeling and control, control of permanent magnet motor drives, control aspects for power electronics in diesel-electric generating units, four-leg converters and development of high-performance control platforms based on combined DSP-FPGA systems. He is an Associate Editor for IEEE TRANSACTION ON INDUSTRY APPLICATIONS.



**PETAR J. GRBOVIĆ** (Senior Member, IEEE) received the Dipl. Ing. (B.Sc.) and Magister (M.Sc.) degrees from the School of Electrical Engineering, University of Belgrade, Belgrade, Serbia, in 1999 and 2005, respectively, and the Doctor (Ph.D) degree from the Laboratoire 'Électrotechnique et d'Electronique de Puissance de Lille, l'Ecole Centrale de Lille, Villeneuve-d'Ascq, France, in 2010.

From March 1999 to September 2018, he had various worldwide R&D centers; RDA Company, Serbia, CESET, Italy, PDL Electronics Ltd., New Zealand, Schneider Electric, France, General Electric, Germany, and Huawei Technologies, Germany. Since 2016, he has been a Member of the Scientific Committee of Centre of Power Electronics and Drives, C-PED Lab., Roma TRE University, Rome, Italy. In 2018, he was appointed to position of a Full Professor with Innsbruck Power Electronics Laboratory (i-PEL), University of Innsbruck, Innsbruck, Austria. His research interests include on cutting-edge technology of power semiconductors and their applications, application of energy storage devices, active gate driving for high power IGBTs and JFET SiC, power converters and topologies, and control of power converters and power semiconductors.

Open Access funding provided by 'Universit? degli Studi Roma Tre' within the CRUI CARE Agreement