IEEE Open Journal of
Power Electronics

Received 30 August 2023; revised 27 September 2023; accepted 29 September 2023. Date of publication 3 October 2023; date of current version 13 October 2023. The review of this paper was arranged by Associate Editor Shanshan Gao.

*Digital Object Identifier 10.1109/OJPEL.2023.3321636*

# An AC Voltage Balancer and its Improved Modulation Strategy for CHB Based PV Inverters

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This work was supported in part by the National Natural Science Foundation of China under Grants 62163036 and 62065001, and in part by Yunnan Young and Middle-aged Academic and Technical Leaders Reserve Talent Project under Grant 202205AC160001.

**ABSTRACT** Cascaded H-bridge (CHB) inverters have been widely used in distributed photovoltaic (PV) power generation systems due to their attractive features in terms of power quality and easy to expand compared to two-level or three-level inverters. Especially the modular inverters with an interphase structure composed of four-port isolated DC/DC converters and CHB inverters are preferred by academia and industry because it can naturally balance the power difference between phases. However, such modular inverters still suffer from some issues that need to be addressed, such as power mismatch between modules within the same phase. This will lead to overmodulation of some H-bridge inverter units and grid-connected current distortion, and even threaten the safe and stable operation of the entire modular inverter. In view of this problem, an AC voltage balancer (ACVB) is proposed in this article to achieve power balance between adjacent H-bridge inverter units. Furthermore, an improved modulation strategy is also presented to achieve soft switching of ACVB. Finally, the effectiveness of the proposed ACVB and its improved modulation strategy is verified by experimental results.

**INDEX TERMS** AC voltage balancer, cascaded H-bridge inverter, distributed photovoltaic power generation, improved modulation strategy.

## I. INTRODUCTION

In future large-scale clean energy generation applications, CHB inverters are a preferable option for integrating large-scale distributed PV into the grid due to their attractive features such as better power quality and generating output voltages much greater than the withstand voltage of the switching devices [1], [2], [3], [4]. In addition, CHB inverters are also suitable for integrating large-scale energy storage systems and wind turbines into the grid. Based on this, the application of CHB inverters has attracted the attention of both academia and industry.

The most straightforward way to integrate PV into the grid using CHB inverters is to connect PV panels to the DC side of each H-bridge inverter unit. However, the method has several drawbacks. The first problem is the common mode leakage current of PV panels, which requires additional common mode leakage current suppression devices. Secondly, the DC side of each H-bridge inverter unit has double-line-frequency power fluctuation, which requires a large capacity filter capacitor or an additional stage of DC/DC converter to achieve the maximum power point tracking (MPPT) of the PV panel. Finally, the output power of each PV panel varies due to the influence of irradiance and temperature. Differences in output power between different H-bridge inverter units will cause interphase power imbalance and power imbalance between H-bridge inverter units within the same phase (hereinafter referred to as 'intra-phase power imbalance'). Interphase power imbalance will cause three-phase grid-connected currents to be asymmetrical. Existing solutions include zero-sequence current injection [5] and zero-sequence voltage injection [6], but these schemes have limited compensation capabilities [7]. In order to address the issue of interphase power imbalance

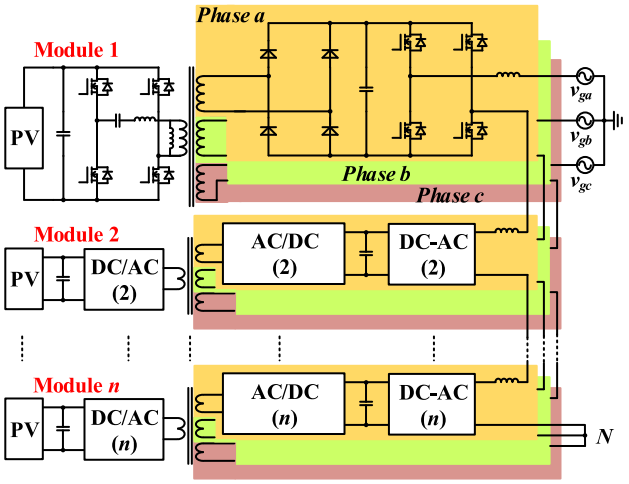


**FIGURE 1.** Two-stage converter structure combining four-port LLC converter and CHB.

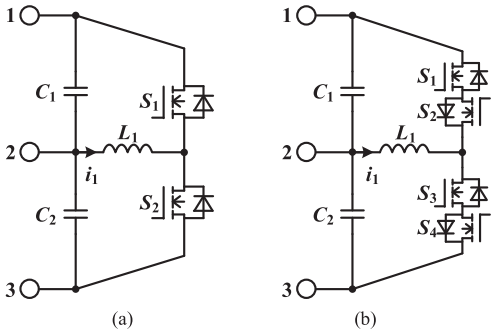


**FIGURE 2.** Voltage balancer based on Buck/Boost converter unit. (a) DC voltage balancer. (b) Proposed ACVB.

thoroughly, researchers proposed a two-stage converter combining quadruple active bridge (QAB) converters and CHB inverters [8], [9], [10], [11], [12], [13], [14], [15], [16]. Attractive features of this two-stage converter include: 1) the output power of a single PV module is evenly distributed among the three phases, thereby achieving natural power balance between phases; 2) the double-line-frequency fluctuating power of the H-bridge inverter unit is offset in the four-winding transformer to avoid the use of bulky capacitors; 3) the use of high-frequency isolation transformers completely solves the common mode leakage current problem of PV panels. The above advantages have made this topology widely concerned. In addition to distributed PV power generation systems, this topology has also been applied to unified power quality conditioner (UPQC) [17], motor drives [18], and electric vehicle charging stations [19]. In addition, there is also a scheme to replace the QAB with a four-port LLC converter, and its working principle is similar to the original scheme [20], [21], as shown in Fig. 1.

The above research work is devoted to addressing the issue of interphase power imbalance, but does not involve intra-phase power imbalance. The rear-stage H-bridge inverter units of different PV modules are connected in series, and the output currents are equal. When there is a power difference between different PV modules, the output voltage of the rear-stage H-bridge inverter unit will be proportional to the output power of the corresponding PV module. When the output power difference between the PV modules exceeds a certain level, some H-bridge units will be overmodulated. Overmodulation will cause grid-connected current distortion, and even lead to instability, thereby affecting the reliability and safety of the entire converter. Therefore, it is necessary to address the intra-phase power imbalance issue to improve the practical application value.

At present, there have been studies on the intra-phase power imbalance of CHB converters, such as adjusting the fundamental phase angle between H-bridge inverter units [22] and vector superposition voltage equalization method [23]. The essence of these two methods is to achieve voltage balance by changing the active power output of each H-bridge inverter unit, which requires a centralized controller and has lower reliability than distributed control. Other researchers have proposed using pulse prediction sorting [24] and discrete commutations modulation methods [25] to solve the problem of intra-phase power imbalance. But such methods also rely on centralized controllers and greatly increase the computational burden of the controllers.

In the field of utilizing additional hardware circuits to assist in voltage balancing, researchers have conducted extensive research in battery and supercapacitor applications, and these techniques have been applied to other areas as well. Such equalization techniques can be divided into two categories: passive equalization and active equalization [26]. Passive equalization is now widely used in electric vehicles and other applications, but has the inherent drawbacks of low efficiency and the need for an extra heat management system. Active equalization techniques include capacitor-based [27], inductor-based [28], transformer-based [29], and converter-based [30] equalization techniques. Transformer-based and converter-based active equalization techniques have been applied to the voltage equalization of cascaded converters. In [31], the authors add a multi-winding transformer to the isolated modular converter, which is connected to the output of the high-frequency transformer of each sub-module converter, and equalize the output voltage between the sub-module converters by means of phase shift control. The advantage of this method is high efficiency, but the multi-winding transformer needs to be redesigned when the number of submodule converters changes, which is not conducive to the expansion of modular converters. In addition, some researchers use DC voltage balancer to realize output voltage equalization of cascade converter [32], [33], [34], as shown in Fig. 2(a), which is essentially a converter-based equalization technique. Port 1, port 2, and port 3 in Fig. 2(a) are respectively connected to the positive pole of the previous output terminal, the positive pole of the latter output terminal, and the negative pole of the latter output terminal in the adjacent two submodule converters. The working principle of the DC voltage balancer is to control the

energy exchange between the two capacitors by adjusting the duty cycle of the switching device, and then realize the voltage equalization of the two capacitors. This DC voltage equalizer is not suitable for CHB voltage equalization because it cannot work when the capacitor voltage polarity is negative. In view of this, this article proposes an ACVB circuit as shown in Fig. 2(b). Similarly, port 1, port 2, and port 3 in Fig. 2(b) are connected to the midpoint of the left bridge arm of the previous unit, the midpoint of the left bridge arm of the latter unit, and the midpoint of the right bridge arm of the latter unit, respectively, in two adjacent H-bridge inverter units. The bidirectional switch setting allows the ACVB to operate properly even when the voltage polarity of capacitors $C_1$ and $C_2$ is negative. However, the presence of bidirectional switching causes the current of inductor $L_1$ to lose its continuous current circuit during the dead zone. A momentary drop in inductor current to zero will produce a very high voltage across the inductor, potentially causing the switching device to burn out. This means that the modulation strategy applied to the DC voltage balancer is not applicable to the ACVB. To address this issue, this article proposes an improved modulation strategy that not only ensures the continuous current circuit of the inductor during the dead zone, but also assists in the soft switching of the switching devices of the ACVB.

The main contributions of this article are summarized as follows:

1) An ACVB is proposed to solve the problem of intra-phase power imbalance of cascaded H-bridge inverters. Also, the proposed ACVB overcomes the drawback that the existing DC voltage equalizer cannot operate when the voltage polarity is negative.
2) An improved modulation strategy for ACVB is proposed to ensure the continuous current circuit of the inductor while also assisting in the soft switching of the switching devices of ACVB.
3) Each ACVB unit works independently, which is conducive to achieving distributed control and improving system reliability.

The remaining of this article is organized as follows. Section II provides a detailed description of the topology and control strategy of the ACVB-based distributed PV grid-connected system. Also, the effect of ACVB on grid-connected current ripple is also given in this Section. In Section III, the improved modulation strategy is presented, as well as the principle of the ACVB's switching devices to achieve soft switching. The experimental results and related analysis are given in Section IV, and finally, conclusions are provided in Section V.

## II. CONFIGURATION AND ANALYSIS OF ACVB-BASED DISTRIBUTED PV GRID-CONNECTED SYSTEM

### A. CONFIGURATION OF ACVB-BASED DISTRIBUTED PV GRID-CONNECTED SYSTEM

Due to the advantages of simple structure and high efficiency of LLC converter, the topology shown in Fig. 1 is chosen to build the distributed PV power generation system in this article. In addition, the unidirectional nature of the topology shown in Fig. 1 is compatible with the requirements of PV power generation systems. The topology of the distributed PV inverter with ACVB is shown in Fig. 3. For the sake of demonstration, only the rear-stage cascaded H-bridge inverter is shown in Fig. 3. Phase $b$ and phase $c$ are configured in the same way as phase $a$.

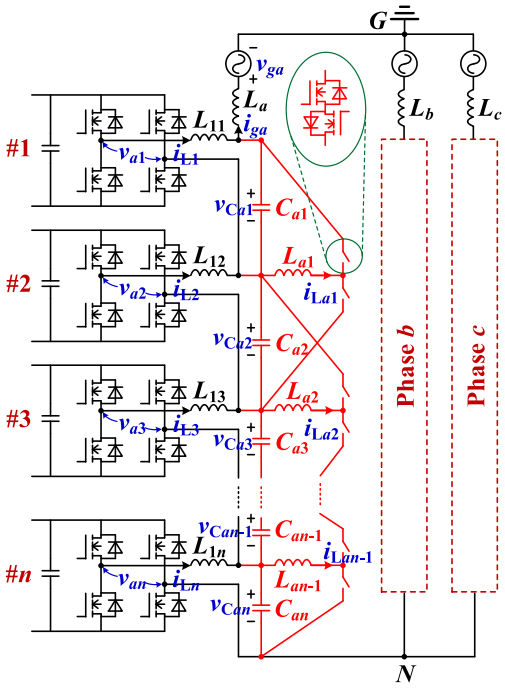


**FIGURE 3.** Schematic diagram of distributed PV inverter with ACVB.

The impact of the difference in the output power of the PV panels within each sub-module on the whole modular inverter is briefly analyzed here when the distributed PV inverter is not configured with ACVB. Ideally, the power output from the PV panels within a single sub-module would be equally distributed among the three rear-stage H-bridge inverters. Define the PV panel output power in all sub-module converters as $P_{\mathrm{PV}k}$ $(k = 1, 2, \ldots, n)$ and all rear-stage H-bridge inverter active power as $P_{\mathrm{inv}x,y}$ $(x = a, b, c;\ y = 1, 2, \ldots, n)$, then the relationship between the above powers can be expressed as

$$\begin{cases} \sum_{k=1}^{n} P_{\mathrm{PV}k} = \sum_{x=a,b,c} \sum_{y=1}^{n} P_{\mathrm{inv}x,y} \\ P_{\mathrm{inva,y}} = P_{\mathrm{invb,y}} = P_{\mathrm{invc,y}} \end{cases} \tag{1}$$

In addition, the active power of each H-bridge inverter can be expressed as

$$P_{\mathrm{inv}x,y} = \frac{V_{\mathrm{inv}x,y} I_x \cos\varphi}{2} (x = a, b, c;\ y = 1, 2, \ldots, n) \tag{2}$$

where $V_{\mathrm{inv}x,y}$, $I_x$, and $\varphi$ denote the peak value of output voltage of H-bridge inverters, the peak value of grid-connected current, and power factor angle, respectively. Combining (1) and (2), the relationship between the output voltage of each

H-bridge inverter in the same phase is given by

$$P_{\mathrm{inv}x,1} : P_{\mathrm{inv}x,2} : \ldots : P_{\mathrm{inv}x,y} = V_{\mathrm{inv}x,1} : V_{\mathrm{inv}x,2} : \ldots : V_{\mathrm{inv}x,y} \tag{3}$$

It can be found from (3) that since the output currents of the H-bridge inverters within the same phase are all equal to the grid-connected currents, the difference in the output power of the PV panels within each sub-module will be reflected in the output voltage of the H-bridge inverters. Therefore, the output power of the H-bridge inverter can be balanced by means of output voltage equalization.

Then, the distributed PV inverter equipped with ACVB is modeled and analyzed. The ACVB operates in the mode of complementary conduction of the upper and lower bridge arms. Define the duty cycle of the upper bridge arm of each ACVB in Fig. 3 as $d_{i,j}$ ($i = a, b, c$; $j = 1, 2, \ldots, n-1$). Then, taking phase $a$ as an example and adopting the state space averaging method, the mathematical model of the rear-stage cascaded H-bridge inverter can be expressed as

$$\begin{cases} L_{1k}\frac{di_{\mathrm{L}k}}{dt} = v_{ak} - v_{\mathrm{C}ak}(k = 1, 2, \ldots, n) \\ L_{aj}\frac{di_{\mathrm{L}aj}}{dt} = \left(1 - d_{a,j}\right) v_{\mathrm{C}aj+1} - d_{a,j} v_{\mathrm{C}aj} \\ (j = 1, 2, \ldots, n-1) \\ L_a\frac{di_{ga}}{dt} = \sum_{k=1}^{n} v_{\mathrm{C}ak} - v_{ga} \\ C_{a1}\frac{dv_{\mathrm{C}a1}}{dt} = i_{\mathrm{L}1} + d_{a,1} i_{\mathrm{L}a1} - i_{ga} \\ C_{ai}\frac{dv_{\mathrm{C}ai}}{dt} = i_{\mathrm{L}i} - \left(1 - d_{a,i-1}\right) i_{\mathrm{L}ai-1} + d_{a,i} i_{\mathrm{L}ai} - i_{ga} \\ (i = 2, 3, \ldots, n-1) \\ C_{an}\frac{dv_{\mathrm{C}an}}{dt} = i_{\mathrm{L}n} - \left(1 - d_{a,n-1}\right) i_{\mathrm{L}an-1} - i_{ga} \end{cases} \tag{4}$$

Since the output voltage of each H-bridge inverter unit is the same under steady-state conditions, the power difference between the sub-module converters will be reflected in the output current of each H-bridge inverter. Then the relationship between the output currents of each H-bridge inverter within the same phase can be expressed as

$$P_{\mathrm{inv}x,1} : P_{\mathrm{inv}x,2} : \ldots : P_{\mathrm{inv}x,y} = I_{x1} : I_{x2} : \ldots : I_{xn} \tag{5}$$

where $I_{x\mathrm{n}}$ denote the peak value of the output current of each H-bridge inverter unit. The inductor of the ACVB is responsible for the power transfer between the two adjacent H-bridge inverter units. The following will analyze in detail the influence of ACVB parameters on its power balancing capability.

$$\begin{cases} L_{1k}\frac{di_{ak}}{dt} = v_{ak} - v_{\mathrm{C}ak}(k = 1, 2) \\ L_{a1}\frac{di_{\mathrm{L}a1}}{dt} = \left(1 - d_{a,1}\right) v_{\mathrm{C}a2} - d_{a,1} v_{\mathrm{C}a1} \\ L_a\frac{di_{ga}}{dt} = v_{\mathrm{C}a1} + v_{\mathrm{C}a2} - v_{ga} \\ i_{\mathrm{C}1} = C_{a1}\frac{dv_{\mathrm{C}a1}}{dt} = i_{a1} + d_{a,1} i_{\mathrm{L}a1} - i_{ga} \\ i_{\mathrm{C}2} = C_{a2}\frac{dv_{\mathrm{C}a2}}{dt} = i_{a2} - \left(1 - d_{a,1}\right) i_{\mathrm{L}a1} - i_{ga} \end{cases} \tag{6}$$

To facilitate the analysis, define the following assumptions:

1) Ignore the power loss of the entire modular inverter.
2) The voltage of the filter inductor is much smaller than the grid voltage and can be ignored.
3) The current of the filter capacitor is much smaller than the grid-connected current and can be ignored.

Taking a distributed PV inverter composed of two sub-module converters as an example, based on (4), the mathematical model of the rear-stage cascaded H-bridge inverter are given by (6).

The time-domain expressions for the grid voltage and grid-connected current in phase $a$ can be expressed as

$$\begin{cases} v_{ga}(t) = V_g \sin(\omega_0 t) \\ i_{ga}(t) = I_g \sin(\omega_0 t + \varphi) \end{cases} \tag{7}$$

where $V_{\mathrm{g}}$ and $\omega_0$ denote the peak value of the grid voltage and the angular frequency. Then, according to (5), the output current of each H-bridge inverter unit under steady-state conditions is given by

$$\begin{cases} i_{a1}(t) = \frac{P_1 I_g \sin(\omega_0 t+\varphi)}{P_1+P_2} = \frac{2P_1 \sin(\omega_0 t+\varphi)}{3V_g} \\ i_{a2}(t) = \frac{P_2 I_g \sin(\omega_0 t+\varphi)}{P_1+P_2} = \frac{2P_2 \sin(\omega_0 t+\varphi)}{3V_g} \end{cases} \tag{8}$$

where $P_1$ and $P_2$ denote the output power of the first and second submodule converters, respectively. Combining the fourth and fifth terms of (6), and (8) yields

$$i_{\mathrm{L}a1}(t) = i_{a2}(t) - i_{a1}(t) = \frac{2(P_2 - P_1)\sin(\omega_0 t + \varphi)}{3V_g} \tag{9}$$

Then the voltage of the inductor $L_{a1}$ can be expressed as

$$L_{a1}\frac{di_{\mathrm{L}a1}(t)}{dt} = \frac{2\omega_0 L_{a1}(P_2 - P_1)\cos(\omega_0 t + \varphi)}{3V_g} \tag{10}$$

The voltages of capacitors $C_{a1}$ and $C_{a2}$ are equal under steady-state conditions, and both are half of the grid voltage. Then, combining (10) and the second term of (6) yields

$$\begin{cases} d_{a,1}(t) = 0.5 - \frac{2\omega_0 L_{a1}\Delta P(\cos\varphi\cot(\omega_0 t)+\sin\varphi)}{3V_g^2} \\ \Delta P = P_2 - P_1 \end{cases} \tag{11}$$

Therefore, the output voltage equalization of two adjacent H-bridge inverters can be achieved as long as the duty cycle of ACVB satisfies (11). The waveform of duty cycle according to (11) can be obtained as shown in the dashed line in Fig. 4. However, the duty cycle signal is generated by the proportional-integral (PI) controller, which means that the duty cycle signal does not vary substantially. The actual duty cycle signal is approximated as shown by the solid line in Fig. 4, where the maximum and minimum values correspond to the points where $\cot(\omega_0 t) = \pm 1$, respectively. Then, in order to prevent ACVB overmodulation, the range of the power difference $\Delta P$ between the two sub-module converters can be expressed as

$$\Delta P < \frac{3V_g^2}{4\sqrt{2}\omega_0 L_{a1}\sin\left(\varphi + \frac{\pi}{4}\right)} \Rightarrow \Delta P < \frac{3V_g^2}{4\sqrt{2}\omega_0 L_{a1}} \tag{12}$$

It can also be found from (12) that the larger $L_{a1}$ is, the weaker the power balancing capability of ACVB. In

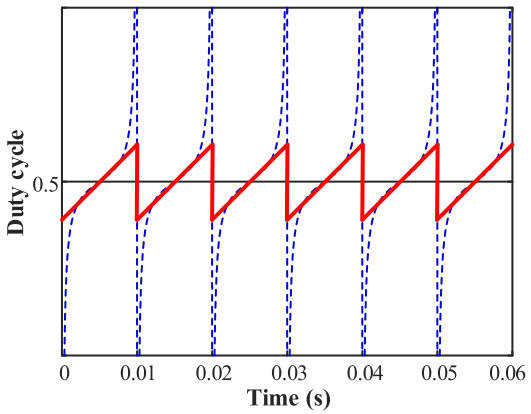


**FIGURE 4.** Waveform of duty cycle ($P_2 > P_1$).

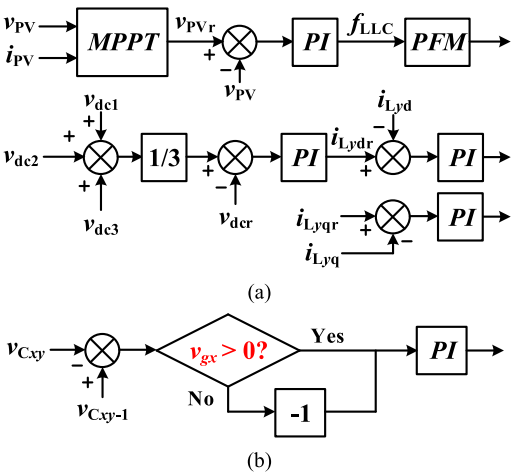


**FIGURE 5.** Schematic diagram of control strategy. (a) Control strategy of sub-module converter. (b) Control strategy of each ACVB unit.

addition, defining the maximum current allowed by the switch of ACVB as $I_D$, another constraint of $\Delta P$ can be found from (9) as

$$\Delta P < \frac{3V_g I_D}{2} \tag{13}$$

In addition, it can be found from the above analysis that the capacitor of the ACVB has no effect on its power balancing capability.

### B. CONTROL STRATEGY OF ACVB-BASED DISTRIBUTED PV GRID-CONNECTED SYSTEM

Since each sub-module converter and ACVB unit of the whole modular converter system is independently controlled and has the same control strategy, to avoid repetition, only the closed-loop control diagram of each sub-module converter and ACVB unit is given in this article. The control strategy of each sub-module converter is shown in Fig. 5(a). Where, $v_{PV}$ and $i_{PV}$ represent the output voltage and current of the PV panel; $f_{LLC}$ represents the switching frequency of the front LLC converter; $v_{dc1}$, $v_{dc2}$, and $v_{dc3}$ represent the DC side voltage of the three rear H-bridge inverter units; $i_{Lyd}$ and $i_{Lyq}$ represent $d$-axis and $q$-axis components of the output current of the $y$th sub-module post-stage H-bridge inverter (Park Transformation). A variable whose subscript ends in 'r' represents the reference value of the corresponding variable. According to the sub-module control strategy, it can be found that the front stage four-port LLC converter is responsible for tracking the maximum power of the PV panel, while the rear-stage H-bridge inverter unit stabilizes the DC side voltage by adjusting the output power.

The function of ACVB is to transfer the power of the H-bridge inverter unit with high output voltage to the H-bridge inverter unit with low output voltage, so as to realize the power balance between H-bridge inverter units. The control strategy of DC voltage balancer is to take the output voltage difference of two adjacent sub-modules as the error signal, and then through a single closed-loop control system with proportional-integral (PI) controller to realize the output power balance of the two sub-modules. However, the control strategy of DC voltage balancer is not fully applicable to ACVB, because when the H-bridge inverter unit output voltage polarity is negative, the higher the output power, the lower the output voltage. The control strategy for the DC voltage balancer needs to be modified. The revised control strategy is shown in Fig. 5(b), that is, when the polarity of the grid voltage is negative, the error signal is multiplied by $-1$, where $v_{Cxy}$ and $v_{Cxy-1}$ ($x = a, b, c$; $y = 1, 2, \ldots, n$) are capacitor voltage, and $v_{gx}$ is grid voltage.

### C. EFFECT OF ACVB ON GRID-CONNECTED CURRENT RIPPLE ATTENUATION

The installation of the ACVB changes the equivalent output impedance of the rear-stage inverter, which inevitably changes the grid-connected current ripple attenuation capability. The following will analyze the effect of ACVB on the ripple attenuation capability of grid-connected currents. In order not to lose generality, an inverter system consisting of three sub-module converters is chosen here for analysis. By linearizing the model shown in (4) and combining it with the mathematical model of the ACVB controller shown in (14), the equivalent impedance small signal model of the output side of the rear stage inverter can be derived as shown in (15).

$$\begin{cases} \hat{d}_{a,1} = PI_2(s)(\hat{v}_{Ca1} - \hat{v}_{Ca2}) \\ \hat{d}_{a,2} = PI_2(s)(\hat{v}_{Ca2} - \hat{v}_{Ca3}) \\ PI_2(s) = k_{p2} + k_{i2}/s \end{cases} \tag{14}$$

$$\dot{x} = \mathbf{A}x + \mathbf{B}_1\hat{v}_{a1} + \mathbf{B}_2\hat{v}_{a2} + \mathbf{B}_3\hat{v}_{a3} + \mathbf{B}_4\hat{v}_{ga} \tag{15}$$

where $x = [\hat{i}_{L1}\ \ \hat{i}_{L2}\ \ \hat{i}_{L3}\ \ \hat{i}_{La1}\ \ \hat{i}_{La2}\ \ \hat{i}_{ga}\ \ \hat{v}_{Ca1}\ \ \hat{v}_{Ca2}\ \ \hat{v}_{Ca3}]^T$. $\mathbf{A} = \begin{bmatrix} a_{11} & \cdots & a_{19} \\ \vdots & \ddots & \vdots \\ a_{91} & \cdots & a_{99} \end{bmatrix}$, where $a_{17} = -1/L_{11}$, $a_{28} = -1/L_{12}$, $a_{39} = -1/L_{13}$, $a_{47} = H_2/L_{a1}$, $a_{48} = H_1/L_{a1}$, $a_{58} = H_4/L_{a2}$, $a_{59} = H_3/L_{a2}$, $a_{67} = a_{68} = a_{69} = 1/L_a$, $a_{71} = 1/C_{a1}$, $a_{74} = D_{a,1}/C_{a1}$, $a_{76} = -1/C_{a1}$, $a_{77} = H_5/C_{a1}$, $a_{78} = -a_{77}$, $a_{82} = 1/C_{a2}$, $a_{84} = (D_{a,1} - 1)/C_{a2}$, $a_{85} = D_{a,2}/C_{a2}$, $a_{86} = -1/C_{a2}$, $a_{87} = H_5/C_{a2}$, $a_{88} = -H_6/C_{a2}$, $a_{89} = -H_7/C_{a2}$, $a_{93} = 1/C_{a3}$,

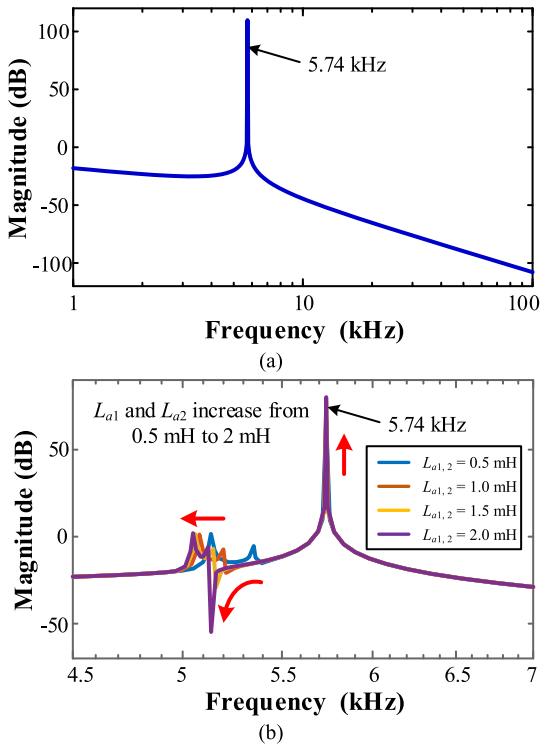


**FIGURE 6.** Bode diagram of the equivalent conductance of the output side of the rear stage inverter. (a) The output power of each sub-module converter is the same. (b) The output power of each sub-module converter is different.

$a_{95} = (D_{a,2} - 1)/C_{a3}$, $a_{96} = -1/C_{a3}$, $a_{98} = H_7/C_{a3}$, $a_{99} = -a_{98}$, the rest of the elements are 0. $\mathbf{B}_1$ is a 9∗1 matrix, where the first element is $b_{11} = 1/L_{11}$ and all other elements are 0. $\mathbf{B}_2$ is a 9∗1 matrix, where the second element is $b_{22} = 1/L_{12}$ and all other elements are 0. $\mathbf{B}_3$ is a 9∗1 matrix, where the third element is $b_{33} = 1/L_{13}$ and all other elements are 0. $\mathbf{B}_4$ is a 9∗1 matrix, where the sixth element is $b_{46} = -1/L_a$ and all other elements are 0. Then the equivalent conductance of the output side of the rear stage inverter can be derived as (16).

$$\begin{cases} G_{a1}(s) = \dfrac{\hat{i}_{ga}(s)}{\hat{v}_{a1}(s)} = \mathbf{C}(s\mathbf{I} - \mathbf{A})^{-1}\mathbf{B}_1 \\ G_{a2}(s) = \dfrac{\hat{i}_{ga}(s)}{\hat{v}_{a2}(s)} = \mathbf{C}(s\mathbf{I} - \mathbf{A})^{-1}\mathbf{B}_2 \\ G_{a3}(s) = \dfrac{\hat{i}_{ga}(s)}{\hat{v}_{a3}(s)} = \mathbf{C}(s\mathbf{I} - \mathbf{A})^{-1}\mathbf{B}_3 \end{cases} \tag{16}$$

where $\mathbf{C} = [00\ 00\ 01\ 00\ 0]$, $\mathbf{I}$ is the ninth order unit matrix. Fig. 6(a) shows the Bode diagram of $G_{a1}(s)$ under the condition of equal output power of the three submodule converters (the Bode diagrams of $G_{a2}(s)$ and $G_{a3}(s)$ are almost identical to $G_{a1}(s)$). It can be found that the grid-connected current ripple attenuation capability is increased to −60 dB/dec after equipping ACVB, and there is a resonance peak, similar to *LCL* filter. When the output power of each sub-module converter is different, the Bode diagram of $G_{a1}(s)$ is shown in Fig. 6(b). The ripple attenuation capability in the high frequency region remains at −60 dB/dec, but with two additional resonant peaks. The amplitude of the two additional resonance peaks is much smaller than the original resonance peak. As La1 and La2 increase, the amplitude of the original resonant peak increases and the two additional resonant peaks are shifted toward the lower frequency region, but always greater than 5 kHz. In summary, the effect of ACVB on the ripple attenuation capability of grid-connected current is mainly reflected in the two voltage regulator capacitors, while the effect of internal inductor of ACVB on grid-connected current can be ignored.

## III. IMPROVED MODULATION STRATEGY OF ACVB

The modulation strategy of traditional DC voltage balancer is that the upper and lower bridge arms are switched on alternately. If this modulation strategy is applied to ACVB, two switches in the same bridge arm are required to be turned on and off at the same time. In order to avoid the capacitor short circuit caused by the bridge arm shoot-through, it is necessary to insert dead zones between the upper and lower bridge arm conduction. Due to the configuration of the bidirectional switch, the inductor will lose the continuous current circuit during the dead zone. As can be seen from the characteristics of the inductor, when the current drops to zero instantaneously, the inductor will produce a very high induced voltage, which may lead to the switch overvoltage damage. The modulation strategy applied to the DC voltage balancer needs to be modified to apply to ACVB.

The improved modulation strategy, as shown in Fig. 7, can be divided into four operation modes, and the operation principles of ACVB under each operation mode will be analyzed in detail as follows.

*Mode 1. ($v_g$ and $i_1$ are positive):* At $t_0$, $S_2$ is turned on in advance and $S_4$ is turned off in advance. After $S_4$ is turned off, the current $i_1$ flows by the anti-parallel diode of $S_4$, thus achieving zero-voltage turn-off (zero-voltage-switching, ZVS) of $S_4$. Since no current flows during the turn-on process, $S_2$ achieves zero-current turn-on (zero-current-switching, ZCS). The equivalent circuit of ACVB at $t_0$ is shown in Fig. 8(a). At $t_1$, $S_3$ is turned off and the continuous current circuit of $i_1$ switches to $S_1$'s anti-parallel diode and $S_2$ so that the zero-voltage turn-on (ZVS) of $S_1$ can be achieved at $t_2$. The equivalent circuit of ACVB at $t_1$ is shown in Fig. 8(b). During the period $t_2$ to $t_3$, the inductor $L_1$ charges the capacitor $C_1$. At $t_3$, $S_1$ is turned off in advance and the continuous current circuit of $i_1$ switches to $S_1$'s anti-parallel diode and $S_2$, thus achieving the zero-voltage turn-off (ZVS) of $S_1$. The equivalent circuit of ACVB at $t_3$ is the same as Fig. 8(b). $S_3$ is turned on at $t_4$, the anti-parallel diode of $S_4$ is turned on due to the forward voltage and the anti-parallel diode of $S_1$ is turned off due to the reverse voltage. The continuous current circuit of $i_1$ is switched to $S_4$'s anti-parallel diode and $S_3$, so that zero-current turn-off (ZCS) of $S_2$ and zero-voltage turn-on (ZVS) of $S_4$ can be achieved at $t_5$. The equivalent circuit of ACVB at $t_4$ is the same as Fig. 8(a). During the period $t_5$ to $t_6$, the capacitor $C_2$ charges the inductor $L_1$. The switching state

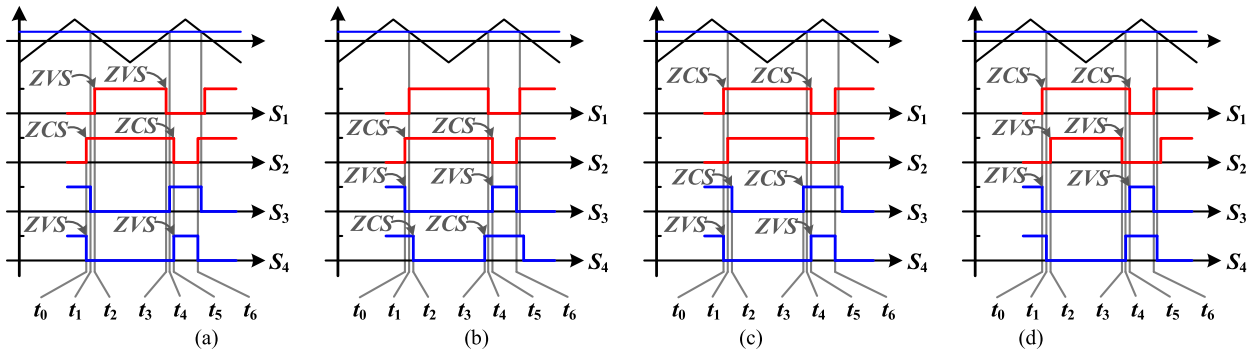


**FIGURE 7.** Improved modulation strategy for ACVB. (a) Grid voltage $v_g$ and inductor current $i_1$ ($i_1$ is shown in Fig. 2) are positive. (b) $v_g$ is positive and $i_1$ is negative. (c) $v_g$ is negative and $i_1$ is positive. (d) $v_g$ and $i_1$ are negative.

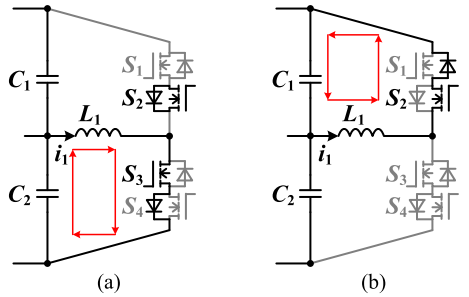


**FIGURE 8.** Equivalent circuit of ACVB in Mode 1. (a) Equivalent circuit at $t_0$ and $t_4$. (b) Equivalent circuit at $t_1$ and $t_3$.

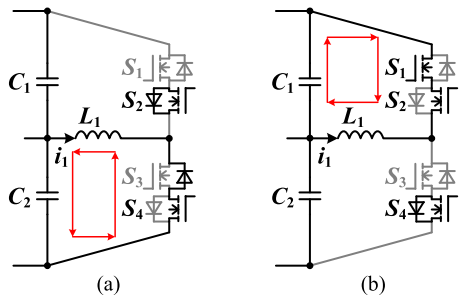


**FIGURE 9.** Equivalent circuit of ACVB in Mode 2. (a) Equivalent circuit at $t_0$ and $t_4$. (b) Equivalent circuit at $t_1$ and $t_3$.

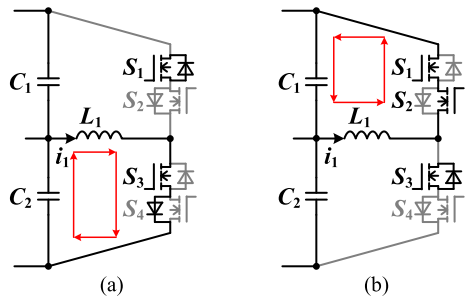


**FIGURE 10.** Equivalent circuit of ACVB in Mode 3. (a) Equivalent circuit at $t_0$ and $t_4$. (b) Equivalent circuit at $t_1$ and $t_3$.

at $t_6$ is the same as that at $t_0$, which is the start of the next switching cycle.

*Mode 2. ($v_g$ is positive and $i_1$ is negative):* At $t_0$, $S_2$ is turned on in advance and $S_3$ is turned off in advance. After $S_3$ is turned off, the current $i_1$ flows by the anti-parallel diode of $S_3$, thus achieving zero-voltage turn-off (ZVS) of $S_3$. Since no current flows during the turn-on process, $S_2$ achieves zero-current turn-on (ZCS). The equivalent circuit of ACVB at $t_0$ is shown in Fig. 9(a). At $t_1$, $S_1$ is turned on, and the anti-parallel diode of $S_3$ is turned off due to the reverse voltage. The continuous current circuit of $i_1$ is switched to $S_1$ and $S_2$, so that zero-current turn-off (ZCS) of $S_4$ can be achieved at $t_2$. The equivalent circuit of ACVB at $t_1$ is shown in Fig. 9(b). During the period $t_2$ to $t_3$, the capacitor $C_1$ charges the inductor $L_1$. At $t_3$, $S_4$ is turned on in advance. Since no current flows during the turn-on process, $S_4$ achieves zero-current turn-on (ZCS). The equivalent circuit of ACVB at $t_3$ is the same as Fig. 9(b). At $t_4$, $S_1$ is turned off, and the continuous current circuit of $i_1$ is switched to $S_3$'s anti-parallel diode and $S_4$, so that zero-current turn-off (ZCS) of $S_2$ and zero-voltage turn-on (ZVS) of $S_3$ can be achieved at $t_5$. The equivalent circuit of ACVB at $t_4$ is the same as Fig. 9(a). During the period $t_5$ to $t_6$, the inductor $L_1$ charges the capacitor $C_2$. The switching state at $t_6$ is the same as that at $t_0$, which is the start of the next switching cycle.

*Mode 3. ($v_g$ is negative and $i_1$ is positive):* At $t_0$, $S_1$ is turned on in advance and $S_4$ is turned off in advance. After $S_4$ is turned off, the current $i_1$ flows by the anti-parallel diode of $S_4$, thus achieving zero-voltage turn-off (ZVS) of $S_4$. Since no current flows during the turn-on process, $S_1$ achieves zero-current turn-on (ZCS). The equivalent circuit of ACVB at $t_0$ is shown in Fig. 10(a). At $t_1$, $S_2$ is turned on, and the anti-parallel diode of $S_4$ is turned off due to the reverse voltage. The continuous current circuit of $i_1$ is switched to $S_1$ and $S_2$, so that zero-current turn-off (ZCS) of $S_3$ can be achieved at $t_2$. The equivalent circuit of ACVB at $t_1$ is shown in Fig. 10(b). During the period $t_2$ to $t_3$, the inductor $L_1$ charges the capacitor $C_1$. At $t_3$, $S_3$ is turned on in advance. Since no current flows during the turn-on process, $S_3$ achieves zero-current turn-on (ZCS). The equivalent circuit of ACVB at $t_3$ is the same as Fig. 10(b). At $t_4$, $S_2$ is turned off, and the continuous current circuit of $i_1$ is switched to $S_4$'s anti-parallel diode and $S_3$,

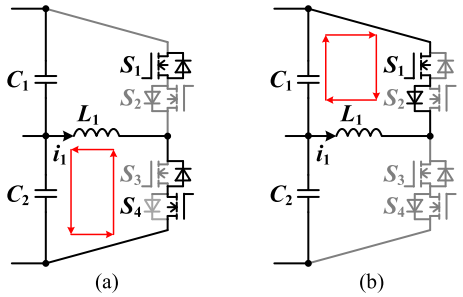


**FIGURE 11.** Equivalent circuit of ACVB in Mode 4. (a) Equivalent circuit at $t_0$ and $t_4$. (b) Equivalent circuit at $t_1$ and $t_3$.

so that zero-current turn-off (ZCS) of $S_1$ and zero-voltage turn-on (ZVS) of $S_4$ can be achieved at $t_5$. The equivalent circuit of ACVB at $t_4$ is the same as Fig. 10(a). During the period $t_5$ to $t_6$, the capacitor $C_2$ charges the inductor $L_1$. The switching state at $t_6$ is the same as that at $t_0$, which is the start of the next switching cycle.

*Mode 4. ($v_g$ and $i_1$ are negative):* At $t_0$, $S_1$ is turned on in advance and $S_3$ is turned off in advance. After $S_3$ is turned off, the current $i_1$ flows by the anti-parallel diode of $S_3$, thus achieving zero-voltage turn-off (ZVS) of $S_3$. Since no current flows during the turn-on process, $S_1$ achieves zero-current turn-on (ZCS). The equivalent circuit of ACVB at $t_0$ is shown in Fig. 11(a). At $t_1$, $S_4$ is turned off and the continuous current circuit of $i_1$ switches to $S_2$'s anti-parallel diode and $S_1$ so that the zero-voltage turn-on (ZVS) of $S_2$ can be achieved at $t_2$. The equivalent circuit of ACVB at $t_1$ is shown in Fig. 11(b). During the period $t_2$ to $t_3$, the capacitor $C_1$ charges the inductor $L_1$. At $t_3$, $S_2$ is turned off in advance and the continuous current circuit of $i_1$ switches to $S_2$'s anti-parallel diode and $S_1$, thus achieving the zero-voltage turn-off (ZVS) of $S_2$. The equivalent circuit of ACVB at $t_3$ is the same as Fig. 11(b). $S_4$ is turned on at $t_4$, the anti-parallel diode of $S_3$ is turned on due to the forward voltage and the anti-parallel diode of $S_2$ is turned off due to the reverse voltage. The continuous current circuit of $i_1$ is switched to $S_3$'s anti-parallel diode and $S_4$, so that zero-current turn-off (ZCS) of $S_1$ and zero-voltage turn-on (ZVS) of $S_3$ can be achieved at $t_5$. The equivalent circuit of ACVB at $t_4$ is the same as Fig. 11(a). During the period $t_5$ to $t_6$, the inductor $L_1$ charges the capacitor $C_2$. The switching state at $t_6$ is the same as that at $t_0$, which is the start of the next switching cycle.

The above analysis shows that the improved modulation strategy can assist ACVB to achieve soft switching and ensure the continuous current circuit of inductor current in any operation mode. Therefore, the improved modulation strategy is fully applicable to ACVB.

## IV. EXPERIMENTAL VERIFICATION

### A. VERIFICATION OF DISTRIBUTED PV INVERTER AND CONTROL STRATEGY

Due to the complex topology of the modular inverter studied in this article, a real-time hardware-in-loop test platform is built for distributed PV power generation system, as shown in Fig. 12, where the main circuit model is implemented in RT-LAB OP5600 and the controller is STM32G431V6T6. The main circuit consists of three sub-modules, and the system parameters are listed in Table 1. The proportional and integral coefficients of the controller are selected by the conventional engineering tuning method. In this article, experimental validation of distributed PV inverters with and without ACVB is carried out to verify the effectiveness of the proposed ACVB.

A set of control experiments without ACVB is conducted for distributed PV inverters to verify the theoretical analysis in Section II-A. First, the maximum output power of the three sub-modules of PV panels $P_1$, $P_2$, and $P_3$ are set to 54 kW,

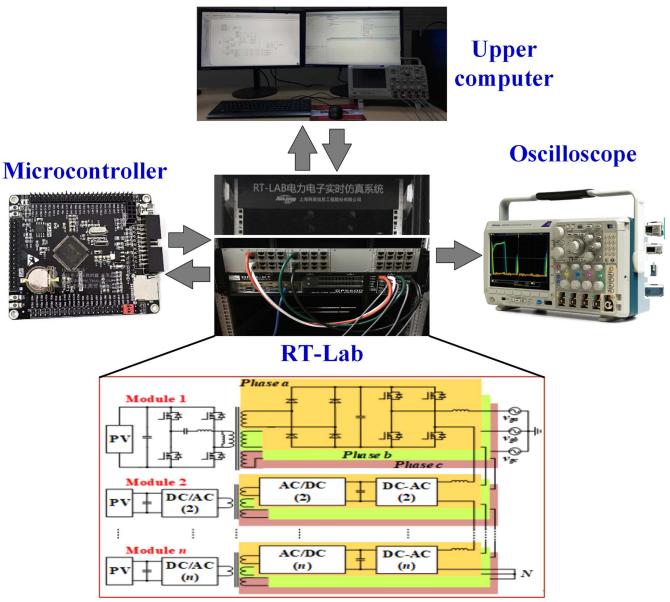


**FIGURE 12.** Hardware-in-loop test platform.

**TABLE 1.** System Parameters

| Symbol | Quantity | Value |
|---|---|---|
| ***Four-port LLC Converter Parameters*** | | |
| $L_r$, $C_r$ | Resonant inductor and capacitor | 1.5 μH, 0.39 μF |
| $L_m$, $C_{in}$ | Magnetic inductor and filter capacitor | 6.8 μH, 22 μF |
| $f_{LLC}$ | Switching frequency range | 90 ~ 220 kHz |
| $k_{p1}$, $k_{i1}$ | Scaling factor and integral factor | 1000, $3*10^5$ |
| ***Rear-stage H-bridge Inverter Parameters*** | | |
| $C_{dc}$, $L_{inv}$ | DC side capacitor and output filter inductor | 47 μF, 0.1 mH |
| $v_{dcr}$ | DC side voltage reference value | 750 V |
| $k_{vp}$, $k_{vi}$ | Voltage loop scaling and integral factor | 0.2, 285 |
| $K_{ip}$, $k_{ii}$ | Current loop scaling and integral factor | 0.02, 10 |
| ***ACVB Parameters*** | | |
| $C_1$, $C_2$ | Voltage regulator capacitor | 10 μF, 10 μF |
| $L_1$ | Energy transfer inductor | 0.5 mH |
| $k_{p2}$, $k_{i2}$ | Scaling factor and integral factor | 0.00005, 0.02 |
| ***Grid Parameters*** | | |
| $V_{ga,b,c}$ | Peak value of the grid voltage | 2 kV |
| $L_{a,b,c}$ | Grid impedance | 1 mH |

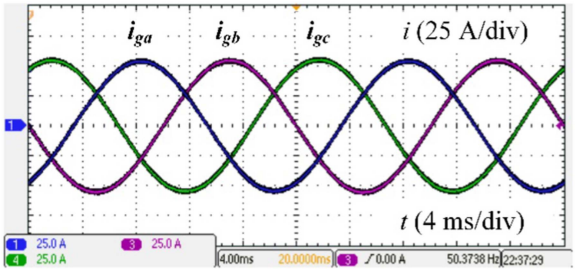


**FIGURE 13.** Waveforms of the three-phase grid-connected currents.

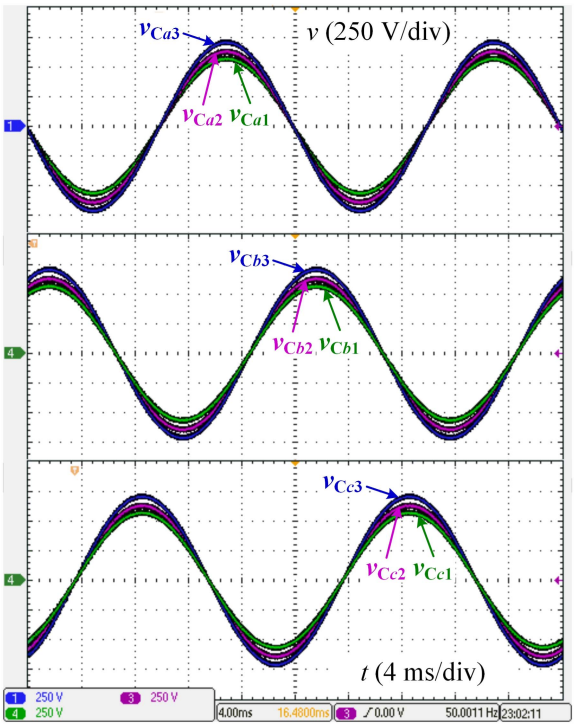


**FIGURE 14.** Output voltage waveforms of each H-bridge inverter unit in each phase.

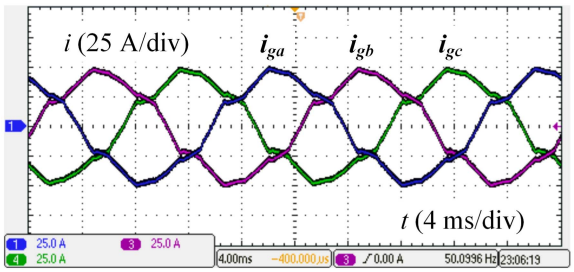


**FIGURE 15.** Waveforms of the three-phase grid-connected currents.

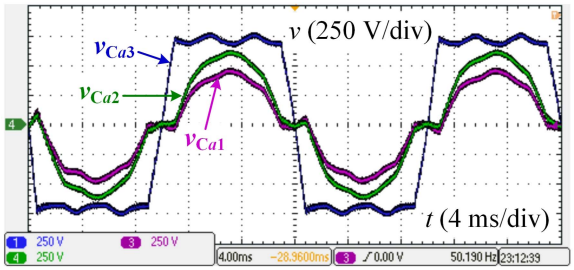


**FIGURE 16.** Output voltage waveforms of each H-bridge inverter unit in phase *a*.

60 kW, and 66 kW, respectively. The terminal voltage corresponding to the maximum power point of all three PV panels is 600 V. The waveforms of the three-phase grid-connected currents are shown in Fig. 13. Fig. 14 shows the output voltage waveforms of each H-bridge inverter unit in each phase, where the peak voltages are 736 V, 666 V and 598 V, respectively. According to (3), the theoretical peak voltages of the three H-bridge inverter units within the same phase can be calculated as 733 V, 667 V, and 600 V, respectively. It can be found that the results of the theoretical calculations remain basically consistent with the experimental results, thus verifying the conclusion that the difference in the output power of the PV panels will be reflected in the output voltage of the rear-stage H-bridge inverter.

Then, the difference of PV panel output power is further increased and $P_1$, $P_2$, and $P_3$ are set to 36 kW, 48 kW, and 72 kW, respectively. The terminal voltage corresponding to the maximum power point of all three PV panels is 600 V. The same theoretical calculation gives the peak output voltages of 462 V, 615 V, and 923 V for the three rear-stage H-bridge inverters. However, the DC-side voltage of the rear-stage H-bridge inverter is 750 V, which means that the rear-stage H-bridge inverter of the third sub-module converter will be over-modulated. The waveforms of the three-phase grid-connected currents are shown in Fig. 15, and the output voltage waveforms of each H-bridge inverter unit in phase *a* are shown in Fig. 16(the output voltage waveforms of each H-bridge inverter unit in phases *b* and *c* are similar to those in phase a and are not shown here). From Fig. 16, it can be found that the large difference in the output power of each PV panel triggers the overmodulation of the rear-stage H-bridge inverter of the third sub-module converter, which in turn causes the grid-connected current distortion as shown in Fig. 15.

The proposed ACVB is added to the output of the rear-stage CHB inverter of the original distributed PV inverter and verified experimentally again. Setting $P_1$, $P_2$, and $P_3$ to 36 kW, 48 kW, and 72 kW, respectively, the grid-connected current waveforms of the distributed PV inverter are shown in Fig. 17. Before the ACVB starts to operate at $T_1$, the grid-connected current is in a serious distortion state, and after $T_1$, the grid-connected current returns to normal. Fig. 18 shows the output voltage waveforms of each H-bridge inverter unit in phase *a*. It can be found that the output voltages of the H-bridge inverters within each phase before $T_1$ are not the same, and all of them have serious distortions. Starting from $T_1$, after a short transient process (about 9 ms), the H-bridge inverter output voltages within each phase are almost equal and all distortions are eliminated. The above experimental results demonstrate

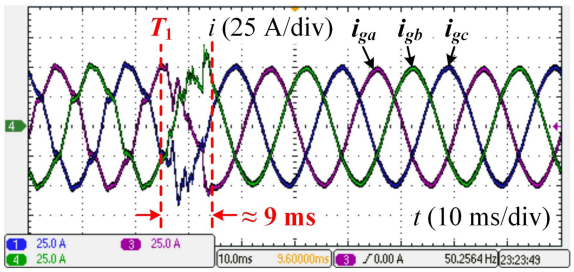


**FIGURE 17.** Waveforms of the three-phase grid-connected currents.

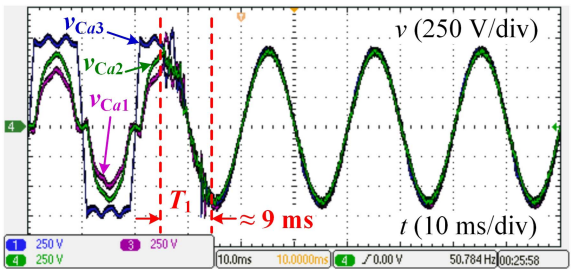


**FIGURE 18.** Output voltage waveforms of each H-bridge inverter in phase *a*.

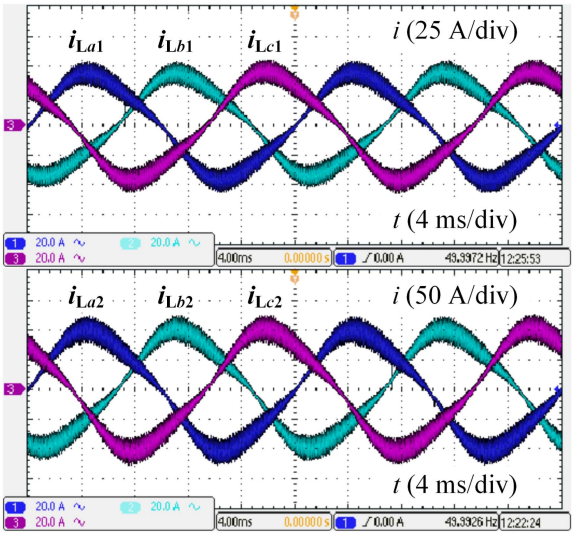


**FIGURE 19.** Current waveforms of each energy transfer inductor.

the good dynamic performance and excellent voltage balancing capability of the proposed ACVB circuit.

In addition, the inductor current waveform of ACVB is shown in Fig. 19. It can be found that the inductor current of ACVB alternates positively and negatively at the fundamental frequency of 50 Hz, which is due to the fact that in the grid voltage polarity also alternates positively and negatively at the frequency of 50 Hz. Thus, the effectiveness of the control strategy shown in Fig. 5(b) is verified.

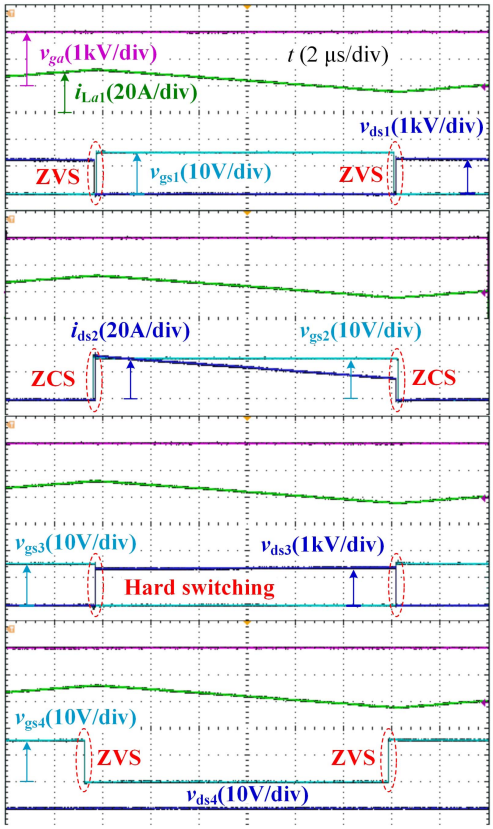


**FIGURE 20.** Experimental results of ***Mode 1***.

### *B. VALIDATION OF THE IMPROVED MODULATION STRATEGY*

Here, the first ACVB cell in phase *a* is used as an example to demonstrate the validation of the effectiveness of the proposed improved modulation strategy. Similar to Fig. 2(b), the switches of the selected ACVB unit are named $S_1$, $S_2$, $S_3$, and $S_4$ in that order. Fig. 20 illustrates the implementation of soft switching for each switch in the selected ACVB unit under ***Mode 1*** conditions. It can be found that: 1) the voltage between the drain and source of $S_1$ ($v_{ds1}$) is zero when $S_1$ is turned on and off, thus achieving zero voltage turn-on and zero voltage turn-off; 2) the current flowing through $S_2$ ($i_{ds2}$) is zero when $S_2$ is turned on and off, thus achieving zero current turn-on and zero current turn-off; 3) the voltage between the drain and source of $S_4$ is zero when $S_4$ is turned on and off, then zero voltage turn-on and zero voltage turn-off are achieved; 4) $S_3$ cannot achieve soft switching. The above results are consistent with the theoretical analysis.

The reason that $v_{ds4}$ is always zero in ***Mode 1*** is that the voltage at the source is higher than the drain during $S_4$ turn-off, which in turn causes the anti-parallel diode of $S_4$ to conduct.

In addition, Fig. 21 show the results of implementing soft switching for each switch in ***Mode 2*** (the experimental results of ***Mode 3*** and ***Mode 4*** are similar to those of ***Mode 1*** and ***Mode 2*** and are not shown here). The above experimental

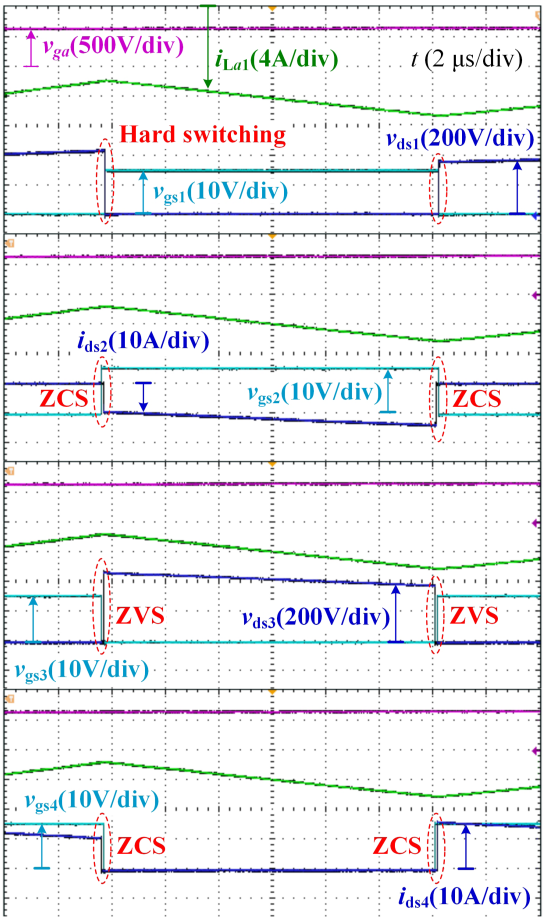


**FIGURE 21.** Experimental results of *Mode 2*.

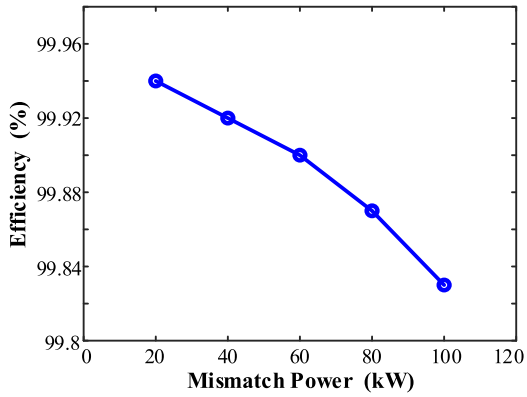


**FIGURE 22.** Efficiency of ACVB under different mismatched power.

results are also identical to the theoretical analysis. It can be seen from Figs. 20 and 21 that the voltage $v_{ds}$ of each switch does not have a voltage spike when the switching state changes, which proves that the improved modulation strategy can effectively prevent the inductor current from losing the continuous current circuit. Therefore, the effectiveness of the improved modulation strategy is verified.

### C. EFFECT OF ACVB ON EFFICIENCY AND POWER DENSITY

It is true that the use of ACVB inevitably leads to an increase in power losses and size. The effect of ACVB on the efficiency and power density of the whole system will be analyzed in detail below.

The power loss of ACVB mainly includes the loss of inductor, capacitor, and switching devices. The loss of capacitance is mainly internal resistance loss, which can be calculated as

$$P_C = I_C^2 R_C \tag{17}$$

where $I_C$ and $R_C$ denote the root-mean-square (RMS) value of the capacitor current and the internal resistance of the capacitor. The loss of an inductor consists of copper loss and magnetic core loss. The copper loss can be calculated from the internal resistance ($R_L$) of the coil and the RMS value of the inductor current ($I_L$), which can be expressed as

$$P_{copper} = I_L^2 R_L \tag{18}$$

The magnetic core loss per unit volume can be calculated by the classical Steinmetz equation shown in (19), where $k$, $\alpha$, and $\beta$ are parameters related to the core material. $f$ is the switching frequency and $B$ is the magnitude of the magnetic flux density.

$$P_{core} = k f^{\alpha} B^{\beta} \tag{19}$$

The losses in switching devices include turn-on losses $P_{on}$, turn-off losses $P_{off}$, and conduction losses $P_{con}$, which can be expressed as

$$\begin{cases} P_{on} = \frac{f V_{DS} I_D T_{on}}{2}, P_{con} = R_{on} I_D^2 \\ P_{off} = \frac{f V_{DS} I_D T_{off}}{2}, P_{sw} = P_{on} + P_{con} + P_{off} \end{cases} \tag{20}$$

where $V_{DS}$, $I_D$, $T_{on}$, $T_{off}$, and $R_{on}$ denote the drain-source voltage, drain current, turn-on time, turn-off time, and on-state resistance respectively. G3R20MT17N SiC MOSFET is selected as switching device of the ACVB, and film capacitors and MPP-26$\mu$ magnetic ring inductors are selected as capacitors and inductors for the ACVB. Taking the experimental system used in this article as an example, the efficiency of ACVB under different mismatched power conditions is shown in Fig. 22. It can be found that ACVB has a small impact on the efficiency of the entire system, and even under the condition of 100 kW mismatch, the efficiency reduction is less than 0.2%.

Since this article did not design a laboratory prototype, the impact of ACVB on the power density of the entire system can only be analyzed through estimation. The volume of similar devices can be seen as proportional to their power level. Taking the experimental system in this article as an example, adding ACVB increased the number of semiconductor devices in the original system by 28.57%, the number of capacitors by 60%, and the number of magnetic components by 40%. Meanwhile, considering that the power level of ACVB is less than 1/6 of that of a single submodule converter. Based on the above analysis, adding ACVB will result in a power density reduction of no more than 10% in the original system.

## V. CONCLUSION

To address the problem of intra-phase power imbalance of distributed PV inverters, this article proposes an ACVB circuit to balance the output voltage of each sub-module post-stage H-bridge inverter. Also, an improved modulation strategy for ACVB is proposed, and this modulation strategy can assist in implementing soft switching. The proposed ACVB circuit and the improved modulation strategy are simple in structure and convenient in control, which are beneficial to be extended to practical applications. The disadvantage of this ACVB circuit is that it cannot realize the soft switching of all switches, and subsequent research to realize the soft switching of all switches will be carried out. The experimental results verify the effectiveness of the ACVB circuit and the improved modulation strategy.

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