ZVS Turn-on Triangular Current Mode (TCM) Control for Three-Phase Two-Level Converters With Reactive Power Control

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ABSTRACT High switching frequency operation in power converters leads to a significant reduction in size at the cost of increased switching losses. Thus, soft switching techniques become necessary to reduce the losses. WBG devices have the benefit of low turn-off losses, but the turn-on losses are still significant. Triangular Current Mode (TCM) control can achieve zero voltage switching (ZVS) turn-on without adding extra resonant components or active devices to the converter. For three-phase operation, soft switching, sinusoidal currents, and phase synchronization are achieved by operating the phases in a combination of Discontinuous Conduction Mode (DCM), TCM and clamped mode. This method is extended to reactive power cases in this article. The proposed scheme can achieve full ZVS turn-on for all the three phases. The phases still operate in a combination of DCM+TCM+Clamped modes of operation. The proposed algorithms are tested and validated on a GaN converter, achieving 99% efficiency at 700 VA with a power density of 110 W/in^3.

INDEX TERMS Active + Reactive Power, Critical Conduction Mode (CRM), Discontinuous Conduction Mode (DCM), Sinusoidal Input Current Control (S.I.C.C), Sinusoidal Input Current, Six-switch three-phase two-level converter, Space Vector Modulation (SVM), Triangular Current Mode (TCM), Unity Power Factor (u.p.f.), Zero Voltage Switching (ZVS).

I. INTRODUCTION

AC/DC and DC/AC converters (shown in Fig. 1) are widely used in electrical systems such as grids, servers, and electric vehicles. The push until now for power electronic systems has been to achieve higher efficiency, however recently the drive has shifted to achieve higher power density. To achieve higher density, the size of the active bridge, dc capacitance, magnetics, and electromagnetic interference (EMI) filters must be reduced. The active bridge size can be reduced by decreasing the number of devices, using smaller devices, and packaging the devices more compactly as discussed in [1], [2], [3], [4], [5]. One of the most space consuming parts in power converters is the EMI filter. The size of EMI filters can be reduced by operating at high frequency ranges [6].

An increase in switching frequency will also lead to an increase in switching losses in the devices. For WBG devices, turn-on losses>> turn-off losses ([7], [8]), hence, ZVS turn-on is required and sufficient ([3]). Critical conduction mode (CRM) for achieving ZVS turn-on is proven to be highly beneficial for single phase PFC ([9], [10], [11], [12]). The inductor current just touches zero and then starts to increase again in every switching cycle, the resonance between the inductor and switch parasitic capacitors brings switch drain-source voltage to zero thus enabling ZVS turn-on. Soft turn-on is achieved in CRM without adding any extra resonant elements to the system.

However, when input voltage is greater than half the DC bus voltage, full ZVS turn-on cannot be achieved in CRM ([13],
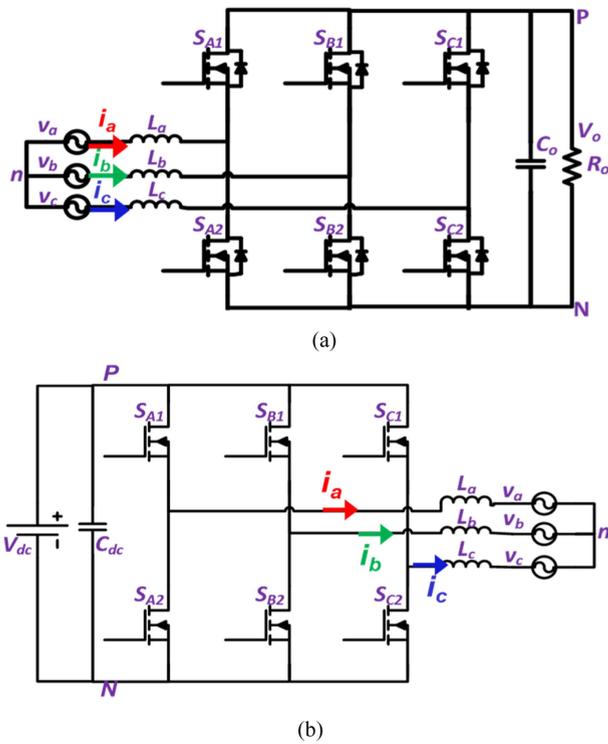
(a)

(b)

FIGURE 1. Three phase (a) AC/DC and (b) DC/AC converter schematic.

[14]). To solve this issue, TCM for single phase PFC is proposed in [13], such that the current is allowed to go to below zero. The negative current is just sufficient to drive the drain source voltage of the switch to 0 V. Single phase TCM can be directly extended to three phase converters when the DC bus is split, and the mid-point is connected to the AC neutral ([15], [16]). This connection results in independent asynchronous operation of the three phases, however since CRM and TCM are variable switching frequency control techniques, asynchronous operation leads to the three phases running at different switching frequencies simultaneously ([18], [19], [20]). Also, this connection limits the modulation index to 1 ([21]).

To address both issues, three-phase CRM with phase synchronization is proposed in [22] and [23]. In [22], it is shown that CRM with phase synchronization can be achieved in a three-phase diode rectifier + boost converter topology by operating the phases in a combination of CRM+DCM modes.

However, the currents are not completely sinusoidal with this technique as the above control method employs only one independent control variable (T_I) to control three currents ([24]). For achieving sinusoidal currents in all the three phases, at least two independent control variables and more active devices are required. The issue of non-sinusoidal currents is addressed in [24] for a Vienna Rectifier. It is proposed that by introducing two independent control variables, sinusoidal currents can be achieved for all the three phases. However, the switching pattern discussed in [24] is limited

to the specific topology of Vienna Rectifier and cannot be directly extended to two-level converters. Also, complete ZVS turn-on is not possible due to the presence of a diode bridge.

TCM for bidirectional two-level converters is discussed in [18], [19], [25], [26]. It is shown that two independent control variables in every switching cycle are necessary and sufficient to achieve sinusoidal currents and phase synchronization ([20] & [29]). Each phase is clamped for 1/3rd of the line cycle like in standard SVM techniques. Only one switch conducts in the clamped phase for 1/3rd of the line cycle thus reducing switching losses. Each switching cycle has four main switching states (as discussed in ([18] and [19]) and two more states to allow the current magnitude to increase such that ZVS can be achieved. The detailed operation is discussed in Section II. The phases operate in DCM, TCM and clamped modes in circular rotation.

TCM for reactive power control has been introduced in [18] and [19]. This article presents a detailed analysis of DCM+TCM+Clamped algorithm for phase shifted currents in Section II. The detailed analysis for ZVS turn-on is presented in Section III. Further improvements are proposed as state-of-the-art switching schemes only achieve valley switching for DCM phase. It is shown in this article in Section III that both TCM and DCM phases can achieve complete ZVS turn-on with the modified switching sequence and a minimum negative current. ZVS turn-on in DCM phase leads to significant reduction in losses at high switching frequencies. TCM for reactive power transfer in inverter mode is discussed in [34] too, however ZVS turn-on is not achieved in the DCM phase leading to significant losses at high switching frequencies.

The implementation of the proposed algorithms is presented in Section IV. The algorithm is implemented with average current controllers like the technique adopted in CCM ([27]). The experimental verification of the proposed algorithm is shown in Section V. The algorithm is implemented with a single core DSP processor on a three-phase 700 W GaN converter. Finally, conclusions of the work presented are discussed in Section VI.

II. BASIC OPERATION

TCM+DCM+Clamped operation for PFC running in unity power factor mode is discussed in detail in [18]. The algorithm is extended to inverter mode in [19]. The whole line cycle is divided into 12 sectors as shown in Fig. 2, where in each sector, the voltage direction and relative magnitude of the three-phase input voltage is same. The input voltages are given by:

$$v_a = V_m \sin(\omega t)$$
$$v_b = V_m \sin(\omega t - 2\pi/3)$$
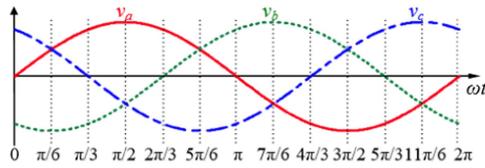$$v_c = V_m \sin(\omega t + 2\pi/3) \tag{1}$$

FIGURE 2. Line cycle divided into twelve sectors.

A. UNITY POWER FACTOR

1) RECTIFIER MODE

One switching cycle waveform in sector I ($0 < \omega t < \pi/6$) is shown in Fig. 3. Each switching cycle can be divided into nine intervals. The ac voltages are assumed to be constant for one switching cycle as the switching frequency (f_{sw}) >> line cycle frequency. The detailed operation during each interval is discussed in [18] and [19], hence, it's discussed briefly here.

During interval I (0-T_1), the phase currents increase linearly proportional to input voltages. The equivalent circuit is shown in Table I. Once i_c reaches i_{cp1}, S_{C2} is turned off, resonance occurs in between phase C devices' output source capacitors and L_C. V_{dsC2} reaches V_o and V_{dsC1} reaches 0, the body diode of S_{C1} starts conducting and the device can be turned on at 0 V.
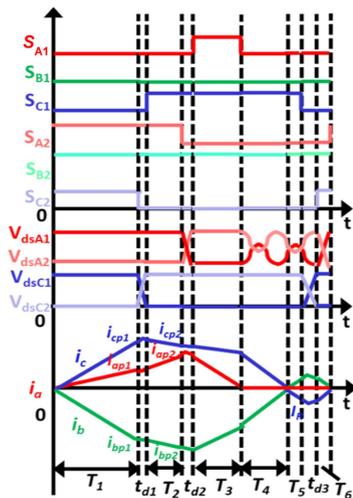

FIGURE 3. One switching cycle waveform in Sector I in rectifier mode, unity power factor.

After S_{C1} is turned on, the current in phase A continues to increase until i_a reaches i_{ap2}. At the end of T_2, S_{A2} is turned off and i_a starts to decrease. The equivalent circuit is shown in Table I. When i_a reaches 0 at the end of T_3, i_c continues to decrease. Once i_c reaches 0 at end of T_4, S_{C1} is allowed to conduct for a little more time (T_5) till i_c reaches a negative value I_R which is enough to discharge the phase C devices' output source capacitors for ZVS turn-on of S_{C2}. After S_{C1} is turned off, resonance occurs between phase C devices' output source capacitors and L_c. By the end of this interval, V_{dsC1} reaches V_o and V_{dsC2} reaches 0, the body diode of S_{C2} starts conducting (as $i_c < 0$) and the switch can be turned on at 0 V.

TABLE 1. Equivalent Circuit in Each Interval in Rectifier Mode

Interval	Equivalent Circuit
$0 < t < T_1$	
$T_1 < t < T_1 + t_{d1} + T_2$	
$T_1 + t_{d1} + T_2$ $< t < T_1 + t_{d1} + T_2 + t_{d2} + T_3$	
$T_1 + t_{d1} + T_2 + t_{d2} + T_3$ $< t < T_1 + t_{d1} + T_2 + t_{d2} + T_3 + T_4 + T_5$	
$T_1 + t_{d1} + T_2 + t_{d2} + T_3 + T_4 + T_5$ $< t < T_s$	

Thus, in sector I, phase A is in DCM mode, phase C is in TCM mode and phase B is clamped. The switching times (T_1–T_6) calculation is discussed in [18] and [19] in detail, it is left here for the sake of brevity. However, the detailed mathematical model for calculating I_R considering parasitic capacitor (C_{oss}) resonance is discussed in Section III as it has been missing from the existing literature.

2) INVERTER MODE

Like rectifier mode discussed above, one switching cycle waveform in sector I ($0 < \omega t < \pi/6$) in inverter mode is divided into nine intervals (including dead time) as shown in Fig. 4 from [19]. The detailed switching cycle operation is not discussed for the sake of brevity. Like rectifier mode, phase A is in DCM mode, phase C is in TCM mode and phase B is clamped. Thus, phase with maximum current is still clamped.
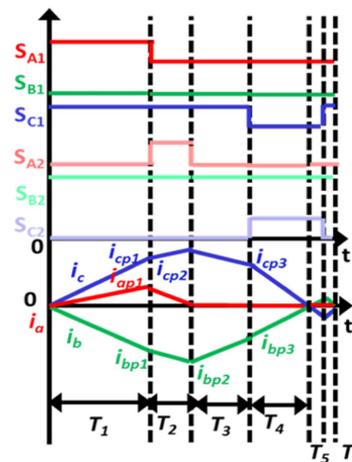

FIGURE 4. One switching cycle waveform in Sector I in inverter mode, unity power factor.

3) FULL LINE CYCLE CONTROL

The controller assigns DCM/TCM/Clamped mode of operation to each phase as shown in Fig. 5. After every 30°, the phase operating in DCM and TCM mode changes. For unity power factor (u.p.f.), the relative magnitude of required average currents and phase voltages is the same. The phase with the maximum, minimum and medium values of absolute average currents are denoted by $|i_{av}|min$, $|i_{av}|max$, $|i_{av}|med$ respectively.
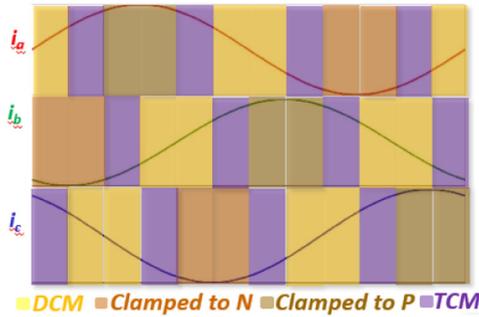
FIGURE 5. Full line cycle control showing control symmetry after every 30° for unity power factor.

The modes of operation are assigned as per the relative magnitude of average phase current:

$$/i_{av}/min \rightarrow \text{DCM}, \quad /i_{av}/med \rightarrow \text{TCM}, \quad /i_{av}/max \rightarrow \text{Clamped}$$

The phase with maximum current is clamped similar to clamped SVM technique to minimize the losses.

The mathematical model for calculating T_1, T_2, T_3 and T_4 considering ideal devices is discussed in [18] and [19] for rectifier and inverter mode respectively. Hence, it's not discussed here. The simulated phase currents based on pre-calculated switching times are shown in Fig. 6. The inductor is designed to achieve a minimum switching frequency of 1 MHz.
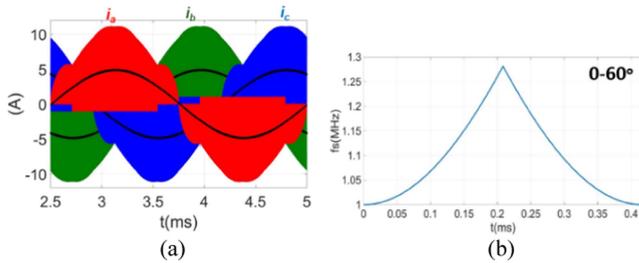
FIGURE 6. (a) Simulated phase currents and (b) Switching frequency variation for 700 W P_o, 300 V V_{dc}, 86 V V_{acrms}, L∼ 4 μH.

B. REACTIVE POWER CONTROL

TCM for reactive power control has been introduced in [18] and [19]. The literature for TCM before that has been limited to unity power factor. For practical and commercial applications, u.p.f. operation is not guaranteed. There can be reactive power requirement from the grid in case of inverter or the EMI filter can also introduce a phase lag between ac voltages and boost inductor currents for both rectifier and inverter.

As discussed in previous sections, in the case of unity power factor operation, the average phase currents are directly proportional to respective phase voltages. For active +reactive power or purely reactive power generation, the average phase current phasor can be expressed as the vector addiction of two voltages. The average currents are given by:

$$i_a = I_m \sin(\omega t - \phi) = k_1 v_a + k_2 v_b$$
$$i_b = I_m \sin(\omega t - 2\pi/3 - \phi) = k_1 v_b + k_2 v_c$$
$$i_c = I_m \sin(\omega t + 2\pi/3 - \phi) = k_1 v_c + k_2 v_a \tag{2}$$

Where

$$k_1 = \left(\cos\phi + \sin\phi/\sqrt{3}\right) I_m/V_m$$
$$k_2 = \left(2\sin\phi/\sqrt{3}\right) I_m/V_m \tag{3}$$

Where ϕ is the phase shift between current and voltage phasor. It can be inferred from these equations that the required current slopes and hence, average currents are generated from multiple phase voltages in the case of reactive power transfer. Particularly, when phase voltage and current are opposite in sign, the other phases' voltage helps construct the required current slopes. The detailed switching cycle operation is discussed below.

1) SWITCHING CYCLE OPERATION: INVERTER MODE

a) Sector I & II ($0 < \omega t < \pi/3$): Each switching cycle is divided into six intervals like unity power factor. The phases still operate in DCM, TCM and clamped mode. The gating signals and currents for one switching cycle in sector I and II in inverter mode for 30° phase lag are shown in Fig. 7(a) and (b) respectively. Reference currents for 30° lagging case are shown in Fig. 8. In sector I, when phase A voltage is positive while lagging reference current is negative, S_{A2} is turned on before S_{A1} s.t. negative current is generated in phase A (as shown in Fig. 7(a)). While in sector II, when voltage and current are in same direction, S_{A1} is turned on first.
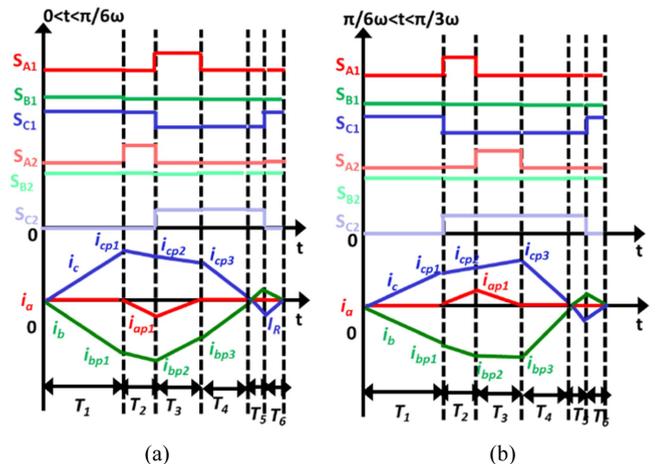
FIGURE 7. One switching cycle waveform for 30° phase lag in sector (a) I and (b) II in inverter mode.
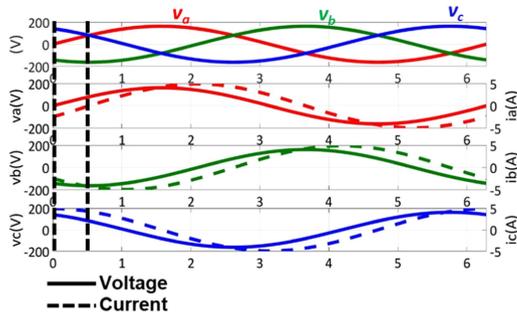
FIGURE 8. Voltages and reference currents for 30° lagging power factor.

b) Phase Clamping: Similar to unity power factor operation, the phases still operate in DCM, TCM and clamped mode. Usually in standard SVM, the phase with maximum magnitude of current is clamped as was done in the case of unity power factor. For example, in the case of 30° lagging power factor shown in Fig. 8(a), phase C has maximum magnitude of current in Sector I. If phase C is clamped to P, phase A will be in DCM as it has minimum magnitude of current.

The simulated currents (for a few switching cycles in rectifier mode) when phase C is clamped to P, phase A is in DCM and phase B is in TCM are shown in Fig. 9. The body diode of S_{A1} starts to conduct current in the positive direction when phase A is programmed to be off. The current starts increasing from 0 and to compensate for it, one more switching state needs to be added to create a negative average current for the DCM phase. Similarly in inverter mode, if phase with maximum current is clamped, the body diode of phase in DCM conducts which leads to undesirable current ripple that cannot be compensated by the controller. Thus, phase with maximum voltage is clamped.
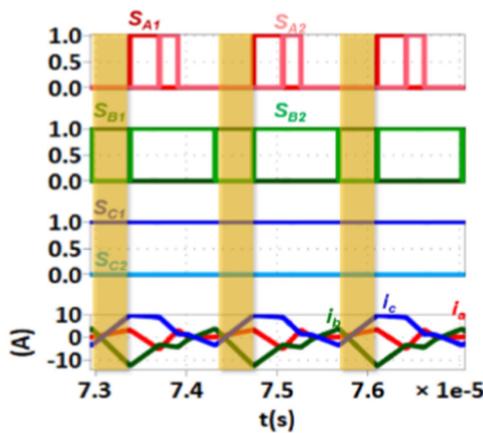

FIGURE 9. Phase A current increasing in positive direction as body diode of S_{A1} becomes forward biased.

Thus the phase with maximum absolute voltage is clamped, minimum absolute average current is in DCM, and the third phase operates in TCM as shown in Fig. 10(a).

$/v_{av}/\max \rightarrow$ Clamped, $/i_{av}/\min \rightarrow$ DCM, 3rd phase $\rightarrow$ TCM

The switching frequency variation for 1/6th of line cycle in 30°° phase shift is shown in Fig. 10(b). The variation is just 20%.
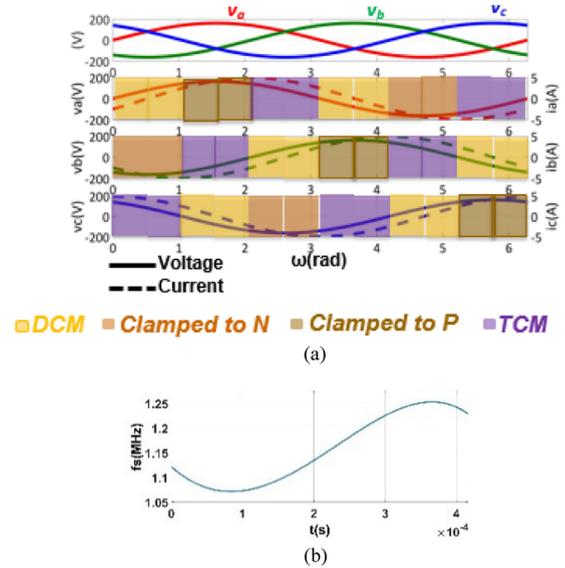

FIGURE 10. (a) Full line cycle control showing control symmetry after every 60° for 30° phase lag (b) Switching frequency variation for 0.7 kVA S_o, 300 V V_o, 86 V V_{acrms}, L~ 4 μH for 30° lagging.

III. ZVS TURN-ON ANALYSIS

The models discussed in [18] and [19] are accurate for duty cycle calculation required to achieve sinusoidal currents. However, to understand the ZVS turn-on mechanism in TCM and DCM phases, the mathematical model considering device output source capacitors (C_{oss}) is required. The minimum negative current required to achieve full ZVS turn-on in TCM phase is calculated in this section for both rectifier and inverter mode. ZVS turn-on for DCM phase is also discussed.

A. RECTIFIER MODE

After S_{C1} is turned off (from Fig. 3), resonance occurs in between phase C devices' output source capacitors and L_c as shown in Fig. 11. S_{B2} is conducting and phase A and phase C output source capacitors are resonating with L_a and L_c. The state equations are given by:

$$\frac{d}{dt}\begin{bmatrix} i_a \\ i_c \\ V_{dsA2} \\ V_{dsC2} \end{bmatrix}$$

$$= \begin{bmatrix} 0 & 0 & -2/3L & 1/3L \\ 0 & 0 & 1/3L & -2/3L \\ 1/2C_{oss} & 0 & 0 & 0 \\ 0 & 1/2C_{oss} & 0 & 0 \end{bmatrix}\begin{bmatrix} i_a \\ i_c \\ V_{dsA2} \\ V_{dsC2} \end{bmatrix}$$

$$+ \begin{bmatrix} 1/L & 0 & 0 & 0 \\ 0 & 0 & 1/L & 0 \\ 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 \end{bmatrix}\begin{bmatrix} v_a \\ v_b \\ v_c \\ V_{dc} \end{bmatrix} \tag{4}$$

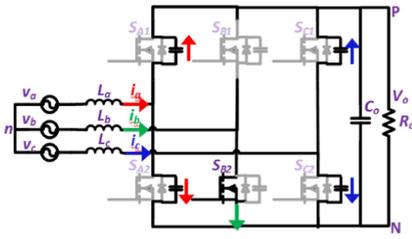Where $i_c(0) = I_R$, $V_{dsC2}(0) = V_{dc}$

FIGURE 11. Equivalent circuit during resonance after turn-off of S_{C1}.

Let $i_a(0) = I_{a0}$, $V_{dsA2}(0) = V_{dsA20}$,

The above equations are solved in MATLAB, the solutions are very complex to explicitly write here, however, minimum values of V_{dsC2} & V_{dsA2} are plotted to determine the minimum value of I_R required for ZVS turn-on of S_{C2} & S_{A2} as shown in Figs. 12, 13 and 14. For these calculations, $V_{dc} = 300$ V, $V_{acrms} = 86$ V, $L = 4$ μH, $C_{oss} = 200$ pF. (As C_{oss} varies from 0-V_{dc}, the equivalent C_{oss} is considered). When S_{C1} is turned off, $V_{dsA2}(0) \in (0\text{-}V_{dc})$ & $i_a(0)$ can also start from any value as both phase A devices have already been turned off, hence $V_{dsC2min}$ & $V_{dsA2min}$ are plotted for the entire sweep. For $I_R = 0$ A, $V_{dsC2min}$ and $V_{dsA2min}$ do not reach 0 V for all values of $V_{dsA2}(0)$ and $i_a(0)$ as can be seen from Figs. 12 & 13. while for $I_R > -1$ A, $V_{dsC2min}$ and $V_{dsA2min}$ reach 0 V (from Fig. 14).
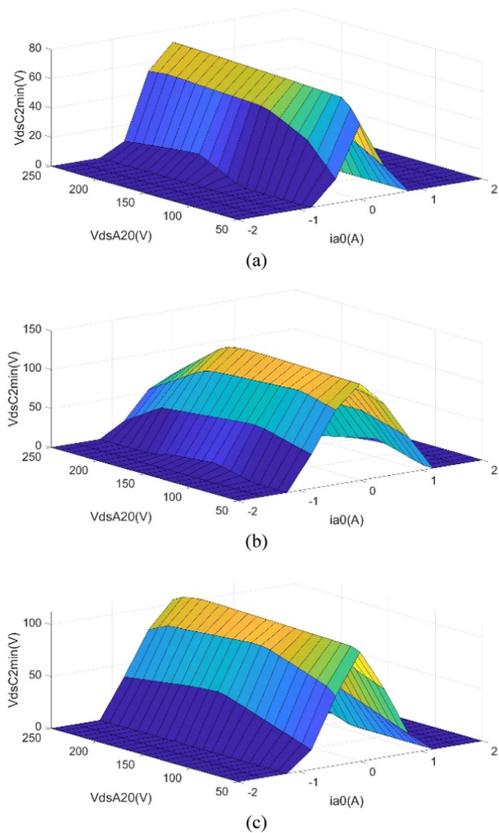

FIGURE 12. $V_{dsC2min}$ vs I_{a0} and V_{dsA20} in rectifier mode (a) $\omega t = 0$, (b) $\omega t = \pi/6$, and (c) $\omega t = \pi/12$ for $I_R = 0$.
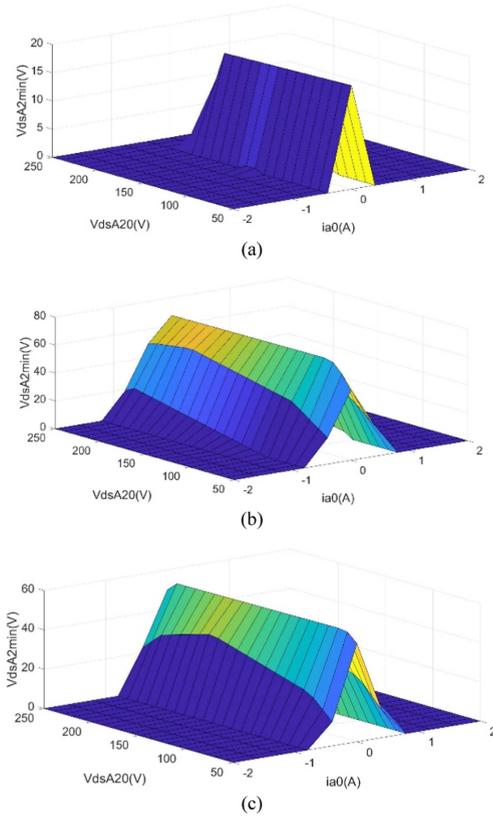

FIGURE 13. $V_{dsA2min}$ vs I_{a0} and V_{dsA20} in rectifier mode (a) $\omega t = 0$, (b) $\omega t = \pi/6$, and (c) $\omega t = \pi/12$ for $I_R = 0$.

From Figs. 12 and 13, $V_{dsA2min}$ and $V_{dsC2min}$ are highest when $i_a(0) = 0$ A and $V_{dsA2}(0) = V_{dc}/2$. Hence, for calculation of minimum I_R (required for ZVS turn-on), $i_a(0)$ and $V_{dsA2}(0)$ are considered to be 0 A and $V_{dc}/2$ respectively. $V_{dsA2min}$ and $V_{dsC2min}$ are plotted for $\omega t = 0$, $\pi/6$ and $\pi/3$ in Fig. 14. For $I_R > -1$ A, ZVS turn-on of both DCM and TCM phases is always achieved.
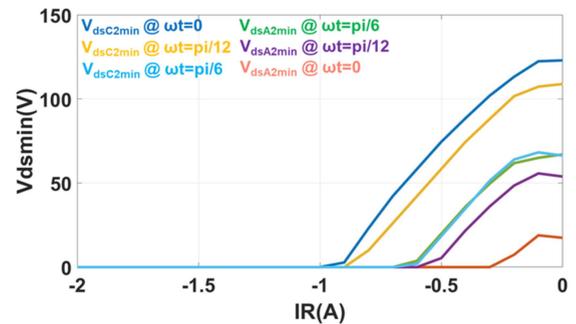

FIGURE 14. $V_{dsA2min}$ and $V_{dsC2min}$ vs I_R for $\omega t = 0$, $\pi/6$ and $\pi/3$ for rectifier mode.

B. INVERTER MODE

After S_{C2} is turned off (from Fig. 16(a)), resonance occurs between phase A and C inductors and device C_{oss}. It is represented by the following equations:

$$\frac{d}{dt}\begin{bmatrix} i_a \\ i_c \\ V_{dsA1} \\ V_{dsC1} \end{bmatrix}$$

$$=\begin{bmatrix} 0 & 0 & -2/3L & 1/3L \\ 0 & 0 & 1/3L & -2/3L \\ 1/2C_{oss} & 0 & 0 & 0 \\ 0 & 1/2C_{oss} & 0 & 0 \end{bmatrix}\begin{bmatrix} i_a \\ i_c \\ V_{dsA1} \\ V_{dsC1} \end{bmatrix}$$

$$+\begin{bmatrix} -1/L & 0 & 0 & 1/3L \\ 0 & 0 & -1/L & 1/3L \\ 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 \end{bmatrix}\begin{bmatrix} v_a \\ v_b \\ v_c \\ V_{dc} \end{bmatrix} \qquad (5)$$

Where $i_c(0) = I_R$, $V_{dsC1}(0) = V_{dc}$

Let $i_a(0) = I_{a0}$, $V_{dsA1}(0) = V_{dsA10}$

The minimum values of V_{dsC1} for several values of ωt are plotted in Fig. 15. The minimum value achieved is always 0 V. Hence, no minimum negative current is required for ZVS turn-on in inverter mode for TCM phase.
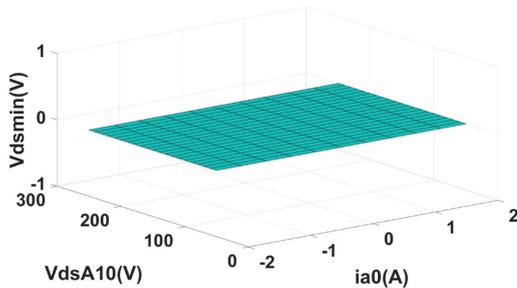
FIGURE 15. $V_{dsC1min}$ vs I_{a0} and V_{dsA10} in inverter mode for $\omega t = 0$, $\omega t = \pi/6$, and $\omega t = \pi/12$ for $I_R = 0$ A.

One switching cycle with detailed dead time operation in sector I is shown in Fig. 16(a). During Interval IV, resonance occurs between L_a, L_c, output source capacitors of phase A and C devices. The equations are complex to be derived explicitly, however it can be seen from the V-Zi diagram in Fig. 16(b) that once V_{dsC1} becomes zero and S_{C1} is turned on during t_{d3}, then the amplitude of V_{dsA1} resonance increases and minimum V_{dsA1} achieved is 0 V(during t_{d4}). During interval IV when S_{C2} is on, the minimum V_{dsA1} achieved is given by Minimum

$$v_{dsA1}\ (in\ Interval\ \text{IV}) = V_{dc} - 3v_a > 0 \qquad (6)$$

However, during t_{d4}, when S_{C1} starts conducting, the minimum V_{dsA1} achieved is 0 V.

Thus, ZVS turn-on of S_{A1} is achieved by turning it on with a short delay after turning on S_{C1} as shown in Fig. 16(a).
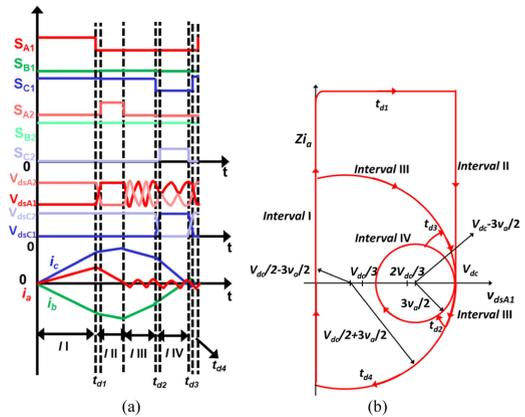
FIGURE 16. (a) One switching cycle operation in inverter mode in sector I (b) V-Zi plot of phase A in sector I showing ZVS turn-on is achieved for DCM phase during t_{d4}.

IV. CONTROL IMPLEMENTATION

The switching times discussed in [18] and [19] are calculated for ideal devices neglecting the effect of C_{oss} and L resonance ripple on average current. The resonance ripple causes distortion in average current when the above switching times are used with device parasitics in an actual circuit. This ripple is significant especially in DCM phase in low current applications, it affects the average currents such that the current becomes highly distorted. The mathematical model considering the effect of this ripple on average currents is very complex, hence, to solve this issue, feedback control is used such that the average current follows the desired sinusoidal reference. Feedback controllers controlling average current can be used like in [28] for CRM.

A. AVERAGE CURRENT CONTROL

The closed loop implementation for average current control is shown in Fig. 17. The grid voltages' phase is measured with phase locked loop (PLL) and average sinusoidal currents are generated. Based on the relative magnitudes of reference currents and voltages, the controller assigns a mode of operation (DCM, TCM or clamped) to each phase as shown in Fig. 18.
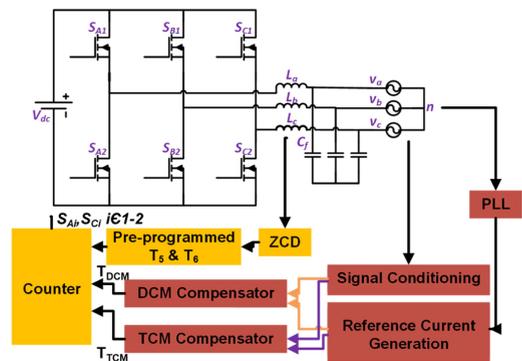
FIGURE 17. Digital control block diagram for average current control from 0-30°.

Based on the error between the measured and the reference average current value, the compensator generates the switching times. The compensator is a PI compensator with feedforward control. In Fig. 17, T_{DCM} and T_{TCM} denote the

conduction times of DCM and TCM phase respectively in one switching cycle s.t. $T_{DCM} = T_1$ and $T_{TCM} = T_1 + T_2 + T_3$ from Fig. 4.

B. MODE ALLOCATION

The controller divides i_a, i_b, i_c phase currents into i_{DCM}, i_{TCM} and i_{Cl} as shown in Fig. 18(a) & (b) for u.p.f. and 30° lagging power factor respectively. Modes are allocated based on magnitude of reference currents and voltages as discussed in Section II.
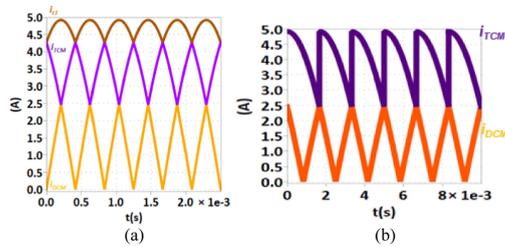

FIGURE 18. Reference currents division into DCM, TCM and clamped operation for (a) unity power factor (u.p.f.) and (b) 30° lagging.

V. EXPERIMENTAL VERIFICATION

The above algorithm is tested on a three-phase two-level GaN converter (shown in Fig. 19(a)) with 650 V/ 60 A GaN devices. The converter specifications are shown in Table II. The experimental setup with ZCD boards is shown in Fig. 19(b). To avoid false multiple ZCD signals due to resonance, the ZCD circuit is designed to detect −0.5 A. Further, the controller is programmed to wait for a minimum time interval before acting on the next ZCD signal which is chosen based on the minimum switching period.
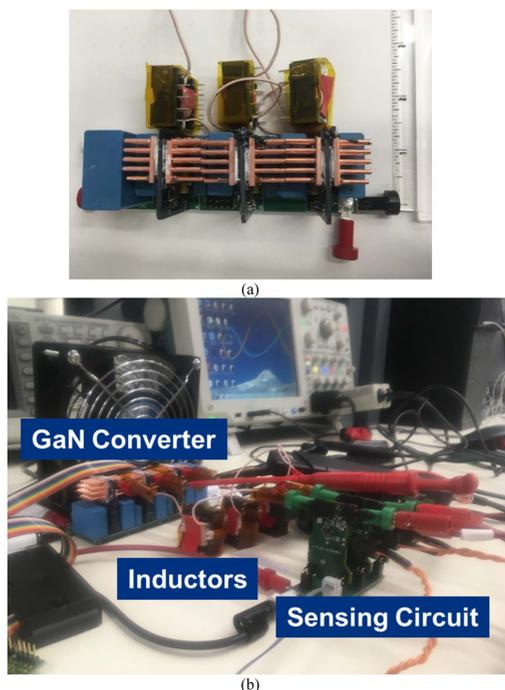

FIGURE 19. (a) GaN converter with filter inductors deigned to operate at ~1 MHz switching frequency (b) Experimental setup with GaN converter, inductors and sensing circuit.

TABLE 2. Converter Specifications

$V_{dc}(V)$	300	$P_o(W)$	700
$V_{acrms=}(V)$	86	L (μH)	4

A. UNITY POWER FACTOR

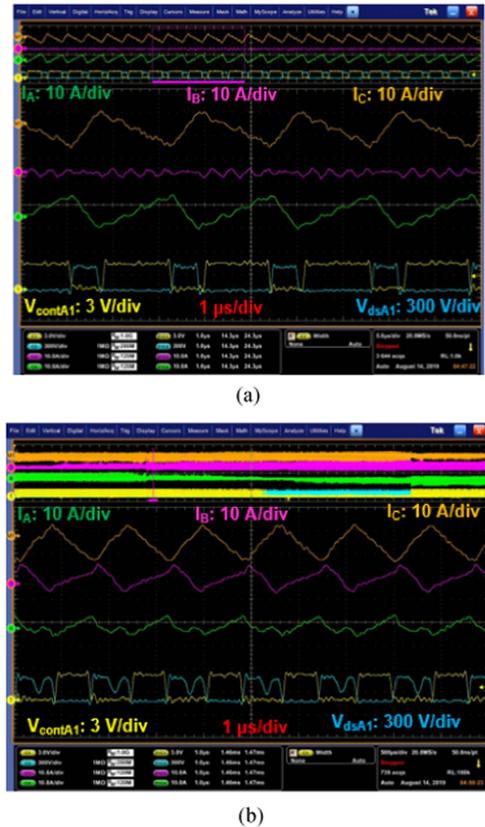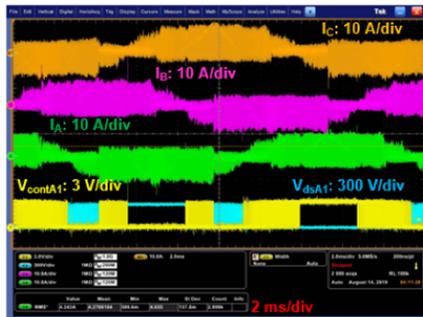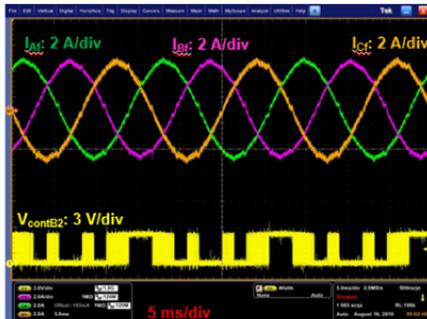TCM and DCM phase ZVS turn-on is validated as shown in Fig. 20.

FIGURE 20. Phase A operating in (a) TCM mode and (b) DCM mode, controller signal goes high after V_{dsA1} has reduced to 0 V.

Full line cycle currents are shown in Fig. 21. The measured system efficiency is 98.7% at V_{dc} = 300 V, P_o = 700 W, V_{acrms} = 86 V. This measurement includes the device losses, inductor losses, ZCD shunt resistor losses and connector losses. Switching frequency range is 400–530 kHz, this drop is owing to delay in ZCD detection and other hardware and controller delays. The final density achieved is 110 W/in^3. Measured filtered currents are shown in Fig. 21(b), the THD is 6.59%. The THD can be improved with higher feedforward control specifically for TCM compensator. Also, the glitch during mode transition can be reduced with higher feedforward gain Resonant mode transition control [33] can also help in reducing the current deflection during mode change.
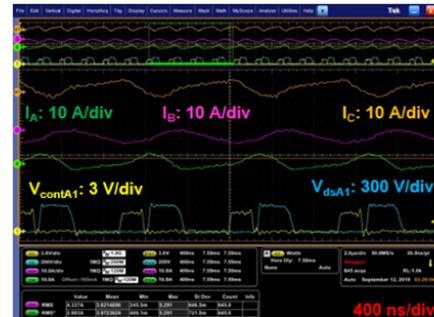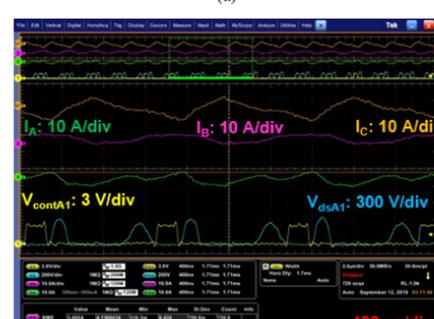
(a)

(b)

FIGURE 21. (a) Phase currents for V_{dc} = 300 V, P_o = 700 W, V_{acrms} = 86 V (b) Filtered phase currents, measured THD= 6.59%.

B. REACTIVE POWER TRANSFER

ZVS turn-on is achieved for both TCM and DCM phase as shown in Fig. 22 and 23.
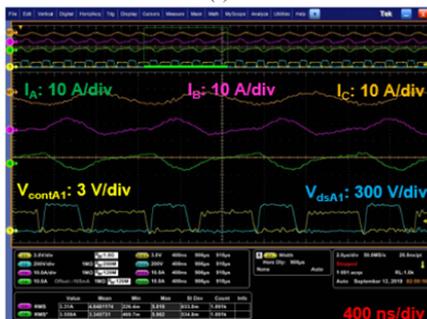

(a)

(b)

FIGURE 22. (a). Phase A operating in TCM mode in (a) Sector V and (b) Sector VI, controller signal goes high after V_{dsA1} has reduced to 0 V.

(a)

(b)

FIGURE 23. Phase A operating in DCM mode in (a) Sector II and (b) Sector VII, controller signal goes high after V_{dsA1} has reduced to 0 V.

Full line cycle currents are shown in Fig. 24. The measured system efficiency is 98.54% at V_{dc} = 300 V, S_o = 700 VA, p.f. = 0.866, V_{acrms} = 86 V and 600- 850 kHz switching frequency range. The final density achieved is 110 W/in^3. Measured filtered currents are shown in Fig. 24(b). The measured THD is 6.51%.
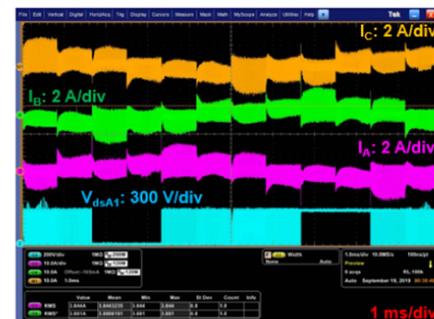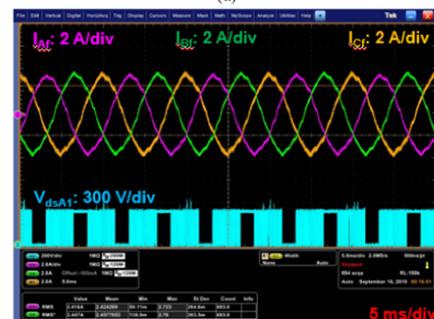

(a)

(b)

FIGURE 24. (a). Phase currents for V_{dc} = 300 V, S_o = 700 VA, V_{acrms} = 86 V, p.f. = 0.866 lagging (b) Filtered phase currents, measured THD = 6.51%.

VI. CONCLUSION

For three-phase converters, TCM with phase synchronization is achieved by a combination of DCM+TCM+Clamped operation. The switching frequency variation is reduced to 34% by combining conduction modes as compared to more than double variation in decoupled TCM control in which the AC neutral needs to be connected to the mid-point. It is discussed in Section II that the key to achieving sinusoidal currents is two independent duty ratios to control three phase currents. The algorithm is extended for reactive power requirement as commercial power converters are not limited to unity power factor operation. The biggest challenge for phase shifted current TCM is that the average phase currents can be opposite in sign to the phase voltages and hence the ripple needs to be generated from other phase voltages. When the phase with maximum average current magnitude is clamped, it leads to instability in the system as the body diode of one of the devices in DCM phase starts conducting when the DCM phase should be off. This current is opposite in sign compared to the reference current, this leads to undesirable ripple in all the phases which the controller is unable to compensate for. Thus, the phase with maximum magnitude of voltage is clamped.

Soft switching conditions are analyzed in detail with a mathematical model in Section III and it is shown that DCM phase can also be turned on at 0 V by adjusting the timing of the turn-on. It is shown that a minimum negative current in the TCM phase ensures ZVS turn-on of both the TCM and DCM phases while in inverter mode ZVS turn-on can be achieved with zero negative current too. Thus, all the three phases turn on at 0 V reducing the losses and CM noise.

The algorithm is implemented with two average current controllers as discussed in Section IV. One of the challenges faced in implementation is synchronizing the microcontroller with a variable frequency ZCD signal without halting all the operations of the MCU. In the proposed controller architecture, DSP EPWM SYNCI signal is used to synchronize PWM module with the variable frequency ZCD signal. Thus, an implementation method with a single core CPU is shown.

Finally, experimental results are shown in Section V on a GaN converter. The DCM and TCM phases ZVS turn on is validated. The final system efficiency measured is 98.7% at 300 V DC voltage, 0.7 kW, unity power factor and 400–530 kHz switching frequency and 98.54% at 0.7 kVA, 0.866 lagging power factor, and 600–850 kHz switching frequency range. The power density achieved is 110 W/in^3.

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