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A Comparison of the Hard-Switching Performance of 650 V Power Transistors With Calorimetric Verification

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ABSTRACT We compare the switching losses of four equivalent silicon and wide-bandgap 650 V power transistors operated in a hard-switched half-bridge configuration, switching 400 V at 40 A. Each transistor is mounted on an identical PCB and driven by a gate drive circuit matched to its requirements. Switching speed is maximised by a PCB design featuring very low parasitic inductance and the use of zero external gate resistance (where possible). Switching losses are measured electrically using a Double Pulse Test (DPT) method. However, high-bandwidth electrical measurements are prone to error and so we assess the gain accuracy, offset accuracy, and the bandwidth requirements of the DPT measurements, and then verify the DPT results by calorimetry. The electrical and calorimetric measurements are shown to agree to within 5%. Comprehensive plots of gate-source voltage, drain-source voltage, and source current are provided for all transistors over a junction temperature range of 50–150°C. The ratio of the total half-bridge switching losses is 1:3.2:14:31 for the GaN HEMT, SiC MOSFET, Si IGBT, and Si superjunction MOSFET, respectively.

INDEX TERMS AC-DC power conversion, DC-DC power conversion, insulated gate bipolar transistors, power MOSFETs, semiconductor device measurements, silicon carbide devices, wide-band-gap devices.

I. INTRODUCTION

The power electronics community is fortunate to have access to a large range of power transistors thanks to the recent commercialisation of wide-band-gap (WBG) silicon carbide (SiC) and gallium nitride (GaN) technology, as well as the continuing development of silicon (Si) IGBTs and MOSFETs. All normally-off power transistors are essentially interchangeable, assuming a part with the necessary voltage and current rating is available and suitable adaptations to the gate driver circuit are made. Assuming all candidate transistors are adequately reliable, which type is chosen for a particular application depends on the trade-off between unit cost and total transistor loss, i.e., the sum of the conduction and switching losses. Conduction loss is relatively easy to estimate using the static characteristics given in the transistor manufacturer's datasheet. In contrast, switching losses are difficult to predict accurately because they are a result of the switching behaviour of the transistor interacting with the parasitic elements in the circuit. The precise physical layout (e.g., the PCB design) of a converter is often challenging to model and/or not known until late in the design cycle.

This article characterises the switching losses of four best-in-class Si and WBG transistors when placed on a level playing field, that is, when placed in the same half-bridge circuit and switched as fast as possible. The Double Pulse Test (DPT) is used to evaluate switching losses in a similar

manner to many recent studies [1], [2], [3], [4], [5], [6], [7], [8], [9], [10], [11], [12], [13]. DPT requires high-bandwidth measurements to capture drain-source voltage and source (or drain) current over the transistor on → off and off → on transitions; these two waveforms are multiplied and integrated to obtain a switching loss (an excellent overview of the technique is given in [14]). Direct comparisons of WBG transistors to Si superjunction MOSFETs (SJMs) and IGBTs have been performed by several authors [2], [3], [4] but it has been observed that the fast switching edges of GaN HEMTs [15] and SJMs are difficult to capture accurately, and so large errors in the switching losses obtained from electrical measurements may result. This article:

- Presents a method of measuring switching losses using high-bandwidth measurement circuits embedded on the power converter PCB. The performance of the measurement circuits is examined and the accuracy of the electrically-derived switching loss measurements is verified by independent calorimetric measurements.
- Demonstrates PCB layout and construction techniques that reduce Switched Current Commutation Loop (SCCL) inductance to a very low level, by the use of a 25 μm polyamide layer between the top two copper layers, and a very low inductance resistive current shunt design.
- Showcases the switching behaviour of a range of 650 V power transistors when they are used in a hard-switched half-bridge circuit across a wide range of junction temperatures (50–150 °C). Current and voltage waveforms, along with comprehensive switching loss figures are presented.

II. DEVICE SELECTION

The power transistors were selected based on their advertised best-in-class performance. They are listed in Table 1 along with their key characteristics. All transistors have a similar on-state resistance or, in the case of the Si IGBT, similar on-state voltage drop at 40 A, making them 'drop-in' replacements for one another, assuming their varied gate drive requirement can be accommodated.

Although the static on-state characteristics are similar, the reverse conduction behaviour is markedly different between the transistors. The GaN HEMT (High Electron Mobility Transistor) does not contain an anti-parallel diode structure and so has no reverse recovery charge. Instead, when the transistor is off and under reverse bias, a combination of the gate threshold voltage (∼1.7 V), plus a bias voltage to support the channel current due to finite gain, plus any negative off-state gate voltage applied by the gate driver, appears between source and drain (which can total 3–5 V). This causes the channel of the GaN HEMT to turn-on and conduct. In a half-bridge circuit, the GaN HEMT must only conduct in this mode for the dead-time (< 50 ns), and so it does not contribute significantly to overall transistor losses. The Si SJM body-diode exhibits an exceptionally large reverse recovery charge and a high reverse recovery current peak; this limits its performance in half-bridge circuits with active upper and lower switches, as shall be seen later. The large quantity of stored charge accumulated during body-diode conduction is due to the large area of the pn junction inherent in the superjunction structure. In contrast, the SiC body-diode exhibits very low reverse recovery charge because, although it is a PiN-type structure, the junction area is small. The Si IGBT PiN diode is a separate die that exhibits an intermediate level of reverse recovery charge, which contributes modestly to overall losses. The Si IGBT also exhibits a characteristic tail-current after the turn-off transition due to charge stored in the bulk semiconductor, which the other transistors in this study do not. It is this charge-injection structure that enables the IGBT's high on-state current density and so a small die, leading to low C_{oss}.

TABLE 1 Selected 650 V Power Transistors (Datasheet Values)

	Si SJ MOSFET	Si IGBT	SiC MOSFET	GaN HEMT
Part no.	IPT60R028 G7	IKB40N65 EF5	SCT3030 AW7	GS66516T
Package	HSOF-8	D2PAK	H2PAK-7	GANPX
On-state[a] @ 25 °C	28 mΩ	1.65 V (41 mΩ)	32 mΩ	25 mΩ
On-state[a] @ 100 °C	42 mΩ	1.80 V (45 mΩ)	36 mΩ	45 mΩ
$T_{j(max)}$	150 °C	175 °C	175 °C	150 °C
Reverse conduction	body diode	PiN diode	body diode	reverse-bias chnl.
Q_{rr}	8.7 µC	1.85 µC	130 nC	zero
C_{oss}[b]	184 pF	71 pF	230 pF	207 pF
C_{gs}	4.82 nF	2.5 nF	1.53 nF	520 pF
$C_{gd(min)}$	1.5 pF	9 pF	60 pF	2.2 pF
$C_{gd(max)}$	6 nF	350 pF	1.4 nF	1.3 nF
g_{fs}	75 S[c]	50 S	9.4 S	60 S[c]
R_g manufr. recom'd.	1.8 Ω	15 Ω	0 Ω	R_{on}:10 Ω R_{off}:1.1 Ω
R_g internal	0.85 Ω	no data	7 Ω	0.34 Ω
V_{th} typ.	3.5 V	4.0 V	2.7-5.6 V	1.3 V
V_{gs} off	0/ − 3 V	0/ − 5 V	0/ − 6 V	0/ − 6 V
V_{gs} on	10 V	14 V	18 V	6 V
Price[d]	12.75 USD	3.21 USD	26.67 USD	34.28 USD

[a] @ 40 A, [b] energy equivalent @ 400 V
[c] gain values from I_{ds}-V_{gs} graphs in manufacturer datasheets
[d] min. price ea. @ 1k qty. from *digikey.com* and *mouser.com*, Feb 2023

III. TEST PLATFORM

A high-level schematic and block diagram of the test platform is shown in Fig. 1. The core of the system is a half-bridge switching cell comprising a tightly coupled DC-link capacitor bank, two transistors and a current sense resistor, mounted on a PCB. This PCB also mounts isolated gate drivers, three high-bandwidth measurement channels, and supporting power supply circuitry as shown in Fig. 2.

A. LOW INDUCTANCE PCB LAYOUT

The Printed Circuit Board (PCB) stack-up of the half-bridge power circuit is shown in Fig. 3. It was designed to have the lowest possible SCCL inductance within the limits of the manufacturing process, using the following two principles:

- The layout of the SCCL is such that the magnetic field created by the current flowing in one direction along the

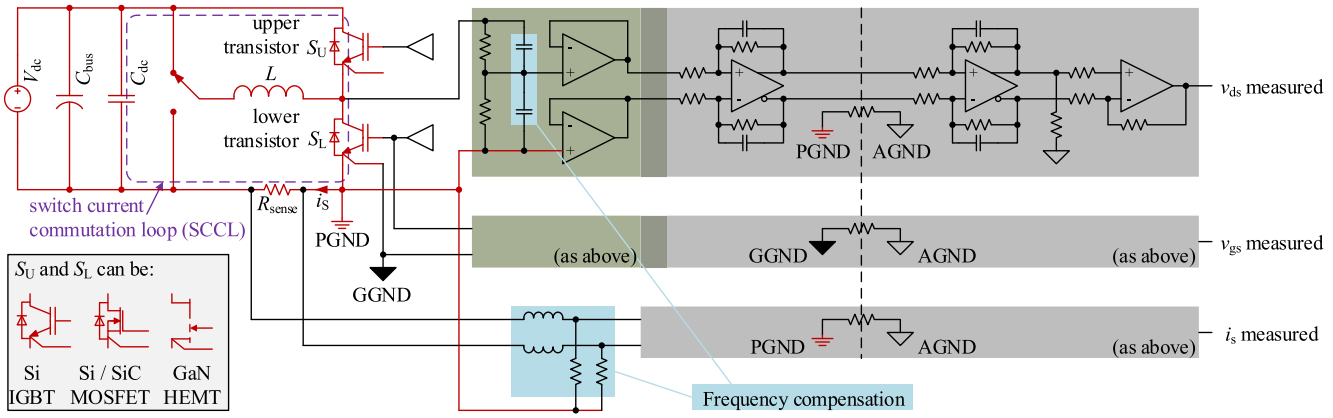


FIGURE 1. Schematic of the test platform showing power (red) and signal (black) chains.

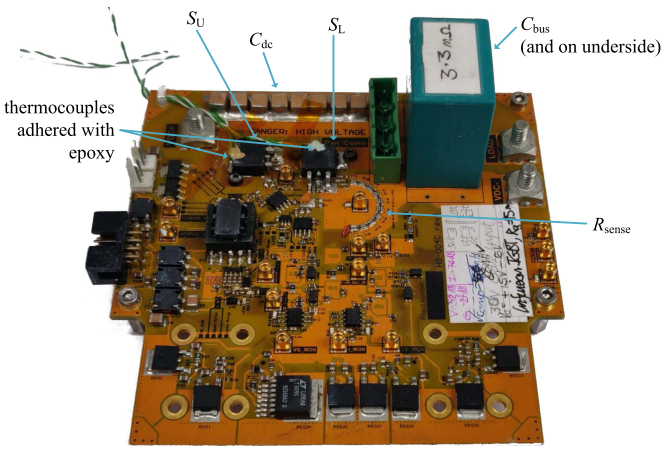
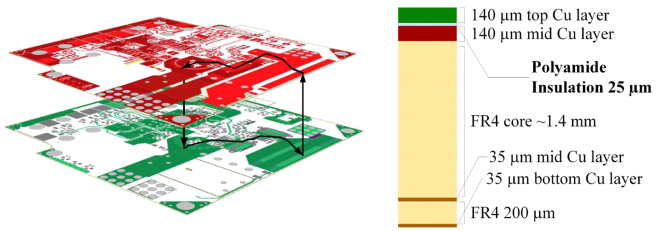


FIGURE 2. Photograph of the PCB with D2PAK transistors mounted.



(a) Switch current commutation loop (SCCL) current path.

(b) PCB stackup (layer thicknesses shown to scale).

FIGURE 3. Images of top-copper layer and the first mid-copper layer, which are separated by a 25 μm polyamide layer. The SCCL current path is shown.

top copper layer is mostly cancelled by the magnetic field of the current flowing in the opposite direction in the layer below it [16], [17].

- A very thin (25 μm) polyamide insulating layer between the top and first inner layer copper conductors is used to minimise the volume enclosed by the SCCL (see Fig. 3). The board has four layers in total: the top two layers contain the SCCL and other power interconnections, and the bottom two layers are used for logic power supply and signal routing, and are separated by conventional FR4 material.

The SCCL inductance, i.e., the inductance of the loop linking the upper and lower transistors, the local DC-link capacitor bank, and the current sense shunt resistors, was measured at 1.4 nH using a Rohde & Schwarz ZND (100 kHz-3 GHz) network analyser, and verified using Ansys Q3D Extractor. At 40 A load current, the energy stored in the SCCL inductance is 1.1 μJ and so contributes negligibly to switching losses (E_{sw} is greater than 200 μJ in all cases).

The parasitic capacitance of the switch node was minimised by ensuring that the overlap with the ground plane is kept small, whilst still achieving a low SCCL. Switch node capacitance with no transistors mounted to the board was measured at $C_{node} = 90$ pF, which is of a similar magnitude to the C_{oss} values of the transistors. Therefore, the charging and discharging of the parasitic switch node capacitance represents a significant, but not dominant, additional switching loss (7.2 μJ at 400 V).

The same PCB is used for each transistor type, with minor modifications to the pad layout to accommodate different transistor packages (all packages are surface-mount type of comparable dimensions). By minimising SCCL and switch node capacitance, the PCB design achieves high switching speeds and low switching losses and so showcases the potential performance of each transistor. The results obtained are likely to represent an upper limit on the performance obtainable in an end application using similar PCB technology and layouts because, in practice, some design compromise would likely be necessary to incorporate mechanical mounting, heatsinks, etc.

B. ELECTRICAL DESIGN

The gate drive circuits are built around the SI8271GB-ISR, a fast isolated silicon driver, capable of delivering up to 4 A gate current and providing transition times of about 10 ns. It provides internal isolation for the gate control signal path. The gate drive supply is isolated from the high-voltage side using a custom-made ferrite-cored transformer with low interwinding

capacitance (2.45 pF), switched by an H-bridge driver IC at 400 kHz. Importantly, the gate drive power supply voltage is adjustable, allowing the same gate driver circuit to be adapted to driving any of the four power transistors in this study. The gate drive circuit uses selector links to set the off-state drive voltage (relative to the Kelvin source pin) to either zero or a negative level that is approximately equal to, or one-third of, the magnitude of the positive on-state level (e.g., +15 V and −5 V, or +6 V and −6 V).

The current sense resistor (R_{sense}) is 10 × 33 mΩ thin-film resistors in a 0508 package connected in parallel and arranged in a semicircular pattern as shown in Fig. 2. This design was found to offer high bandwidth and current carrying capacity while adding a parasitic inductance of 300 pH, which is about one-fifth of the SCCL inductance.

The SCCL DC-link capacitor is composed of eight 470 nF surface-mount X7R dielectric Multi-Layer Ceramic Capacitors (MLCCs) connected in parallel on the top side of the PCB (C_{dc}). A bank of 16 330 nF MLCCs and a through-hole mounted 12.5 μF polypropylene capacitor connected in parallel provide additional bulk DC capacitance (C_{bus}).

An air-cored toroidal inductor of value 100 μH is used as the load at the output of the half-bridge cell. The inductor is wound on a 300 × 175 × 90 mm (OD × ID×height) polystyrene former using 1 mm^2 wire. The turns are separated by 5 mm to minimise inter-turn capacitance. Small-gauge wire is adequate because the duty-cycle is low and so negligible heating occurs. The toroidal design ensures low stray flux and a low equivalent parallel capacitance (2.2 pF). Control over the half-bridge output current direction is obtained by connecting one terminal of the inductor to the positive supply rail (current flowing in) or negative supply rail (current flowing out).

The test platform includes a flexible FPGA-based signal generator to create the gate drive signals and, via a serial connection to a PC, allow automation of the testing process. High-voltage power is supplied by an EA-PSI 9750-06DT bench-top supply.

C. MEASUREMENT CIRCUITS

The test platform PCB integrates three high-bandwidth measurements:

- The source current (i_{s}) in the lower transistor, by measuring the voltage across the current sense resistor.
- The drain-source voltage (v_{ds}), measured across the lower transistor using a high-voltage potential divider.
- The gate-source voltage (v_{gs}), measured across the gate and Kelvin source connections of the lower transistor.

Each channel measures differential-mode voltages, allowing common-mode noise that is either coupled from the main switching power stage or induced by currents flowing between ground-plane reference points to be cancelled. It is necessary to compensate for the series inductance of the current sense resistors by including a compensating low-pass pole at the input to the amplifier chain as shown in Fig. 1. A compensating inductance of 68 nH was found to give a flat frequency response (Fig. 4) and minimal overshoot for step changes in sense resistor current. For the voltage measurement channels, frequency-compensated potential dividers are used to achieve the desired flat frequency response, as shown in Fig. 4. The outputs of all the measurement channels are fed directly to a 1 GHz, 12.5 GS s^{-1}, 12-bit Tektronix MSO44 oscilloscope using length-matched 50 Ω coaxial lines and 50 Ω termination.

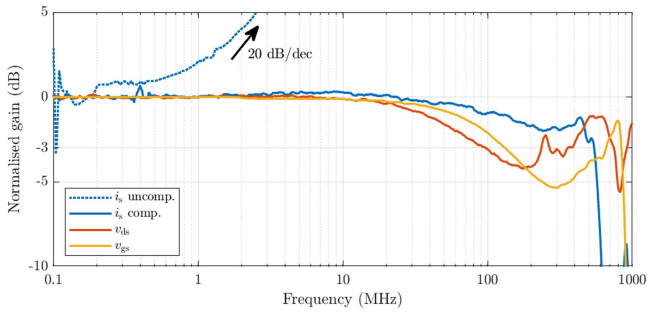
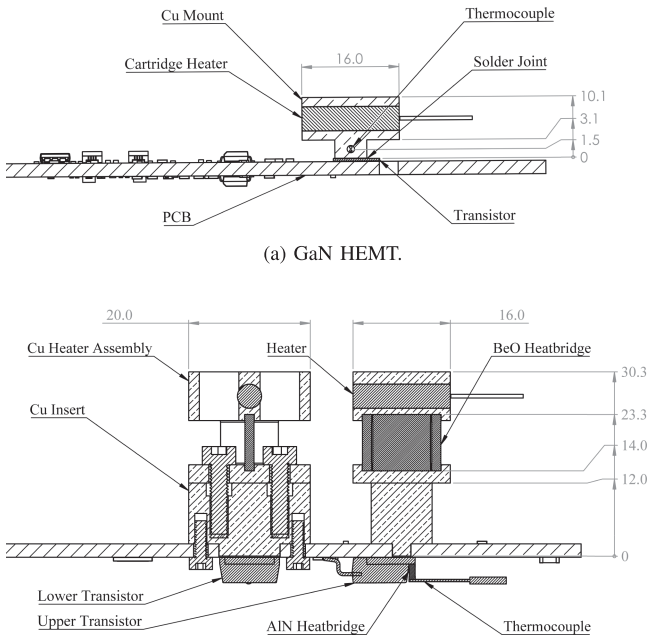


FIGURE 4. Gain responses of the measurement circuits. Gains have been normalised to 0 dB in the passband. The unnormalised passband gain of the i_s channel is −68.5 dB and so the VNA measurement is somewhat noisy, particularly at low frequencies.



(a) GaN HEMT.

(b) Si IGBT, Si SJM, and SiC MOSFET.

FIGURE 5. Heater block and thermocouple assemblies for different transistor types (dimensions in mm).

D. THERMAL DESIGN

External heaters, shown in Fig. 5, are used to maintain each transistor at a temperature above ambient during the test cycle. For the Si SJM, the SI IGBT, and the SiC MOSFET, which have similar packages, the heater is assembled from two copper parts with a beryllium oxide (BeO) thermal bridge soldered between them. The thermal bridges

electrically isolate the heater from the drain pad and maintain a low parasitic capacitance between the switching node and the ground-referenced heater circuit. For the GaN HEMT, only the lower transistor is heated using a cartridge heater inserted into a copper block that is soldered directly to the thermal pad. The thermal pad is connected internally to the source pad, and so the block is at a fixed potential and does not require electrical isolation. Attaching an electrically isolated heater element for the upper GaN HEMT was deemed too difficult due to the small, delicate package. It was found during initial experimentation that the reverse current characteristics of the GaN HEMT remain almost constant across the full temperature range of this study. As a result, we expect that the results reported here would not change significantly if the upper transistor were to be heated.

Transistor temperatures are regulated using a proportional-integral controller implemented in software on a PC. Temperature feedback for the Si SJM, the Si IGBT, and the SiC MOSFET is provided by a K-type thermocouple adhered to the electrically isolated end of a separate aluminium nitride (AlN) thermal bridge, with the other end soldered to the transistor drain tab. For the GaN HEMT, the thermocouple is inserted directly into the copper heater block, close to the transistor thermal pad.

IV. CALCULATING SWITCHING LOSSES USING ELECTRICAL MEASUREMENTS

Switching losses are calculated by integrating the instantaneous lower transistor power $p(t)$:

$$E_{\mathrm{sw},x} = \int_{t_0}^{t_1} p(t).\mathrm{d}t. = \int_{t_0}^{t_1} v_{\mathrm{ds}}(t) i_{\mathrm{s}}(t).\mathrm{d}t, \tag{1}$$

where x can be 'on' (lower transistor turns off $\rightarrow$ on) or 'off' (on $\rightarrow$ off). t_0 and t_1 are chosen to frame the switching edge tightly in order to avoid including conduction losses and accumulating errors from small offsets in the voltage and current measurements. A power threshold, P_{th}, is defined as 5% of the maximum absolute transistor power. t_0^* is defined as the instant at which the absolute value of the transistor power first becomes greater than the power threshold ($|p(t_0^*)| > P_{\mathrm{th}}$). t_1^* is defined as the first instant after the peak transistor power where the absolute value of the transistor power is less than the threshold power ($|p(t_1^*)| < P_{\mathrm{th}}$). The time span is $t_{\mathrm{sw}}^* = t_1^* - t_0^*$. To ensure that oscillations in the power before and after switching has occurred are fully captured, the integration limits are set to $t_0 = t_0^* - t_{\mathrm{sw}}^*$ and $t_1 = t_1^* + t_{\mathrm{sw}}^*$, resulting in an integration frame of length $3t_{\mathrm{sw}}^*$.

The total switching loss occurring in a half-bridge during normal operation is equal to the sum of the current-in and current-out losses. The behaviour of the upper transistor for bridge current flowing out is the same as the behaviour of the lower transistor for bridge current flowing in, and *vice versa*. It is therefore sufficient to measure i_{s} and v_{ds} in both current directions for the lower transistor only in order to calculate the switching losses occurring in the half-bridge.

A. GAIN AND OFFSET ERRORS

The i_{s} shunt resistor voltage drop is small (130 mV at 40 A) and so vulnerable to small offset errors in the measurement circuit. Offsets equivalent to ± 3 A were observed, which would have a large detrimental effect on the accuracy of the switching loss calculation. These offsets were significantly reduced by subtracting an offset value measured in the period of zero current before (for turn-on) or after (for turn-off) the $[t_0, t_1]$ frame of interest. This offset is the mean value over the 50 ns before t_0 or after t_1, and is applied to all i_{s} measurement data during post-processing. It is estimated that the remaining offset error is below ± 0.25 A. The v_{ds} measurement did not require offset correction to achieve an offset below ± 4 V. The DC gain of the v_{ds} and i_{s} channels was calibrated to better than 1 ± 0.02.

Consider (1) with the measurements subject to gain errors ($g_{\mathrm{v}} \neq 1$, $g_{\mathrm{i}} \neq 1$) and offset errors ($\bar{v} \neq 0$ and $\bar{i} \neq 0$):

$$\begin{aligned} E'_{\mathrm{sw},x} &= \int_{t_0}^{t_1} \left[g_{\mathrm{v}}\left(v_{\mathrm{ds}}(t) + \bar{v}\right)\right]\left[g_{\mathrm{i}}\left(i_{\mathrm{s}}(t) + \bar{i}\right)\right].\mathrm{d}t \\ &= g_{\mathrm{v}} g_{\mathrm{i}} \left[E_{\mathrm{sw}} + t_{\mathrm{sw}}\bar{v}\bar{i} + \bar{i}\int_{t_0}^{t_1} v_{\mathrm{ds}}.\mathrm{d}t + \bar{v}\int_{t_0}^{t_1} i_{\mathrm{s}}.\mathrm{d}t\right]. \end{aligned} \tag{2}$$

Under the assumption that the framing algorithm functions correctly and so the switching event occurs halfway between t_0 and t_1, then v_{ds} (i_{s}) will be approximately equal to zero for half the integration period and approximately equal to V_{dc} (I_0) for the remaining half:

$$E'_{\mathrm{sw},x} \approx g_{\mathrm{v}} g_{\mathrm{i}} \left[E_{\mathrm{sw}} + t_{\mathrm{sw}}\left(\bar{v}\bar{i} + \frac{1}{2}\bar{i}V_{\mathrm{dc}} + \frac{1}{2}\bar{v}I_0\right)\right]. \tag{3}$$

Here, V_{dc} is the DC-link voltage applied across the half-bridge and I_0 is the average half-bridge output current (inductor current). Under the further assumption that the offsets are small, i.e., $\bar{v} \ll V_{\mathrm{dc}}$ and $\bar{i} \ll I_0$, then

$$E'_{\mathrm{sw},x} \approx g_{\mathrm{v}} g_{\mathrm{i}} \left[E_{\mathrm{sw}} + \frac{t_{\mathrm{sw}}}{2}\left(\bar{i}V_{\mathrm{dc}} + \bar{v}I_0\right)\right]. \tag{4}$$

This analysis demonstrates that gain errors $g_{\mathrm{v}} g_{\mathrm{i}} \neq 1$ lead to a simple scaling of the calculated switching loss. In the worst case, where the gain error of both channels is 2% and in the same direction, a maximum error of about 4% will be introduced. It also shows that it is desirable to keep t_{sw} as short as possible to minimise the effect of offset errors.

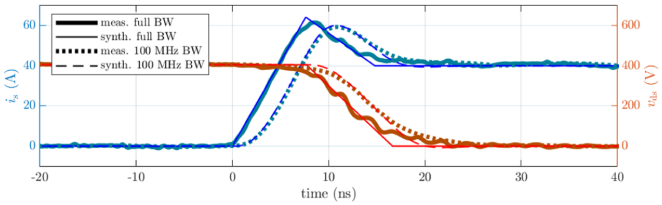
A final approximation is that $\bar{i}/I_0 \approx \bar{v}/V_{\mathrm{dc}} \approx b$ such that:

$$E'_{\mathrm{sw},x} \approx g_{\mathrm{v}} g_{\mathrm{i}} \left[E_{\mathrm{sw}} + b t_{\mathrm{sw}} I_0 V_{\mathrm{dc}}\right]. \tag{5}$$

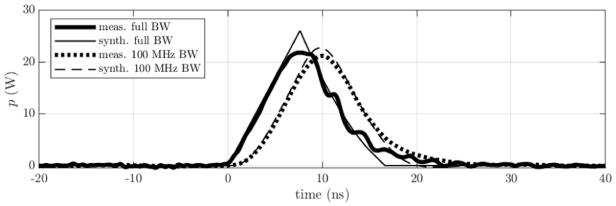
This implies that for $V_{\mathrm{dc}} = 400$ V and $I_0 = 40$ A and a frame length of $t_{\mathrm{sw}} = 100$ ns, an offset error of $b = 2\%$ on both channels will lead to a worst-case error in the calculated switching loss of about 32 μJ.

B. MEASUREMENT BANDWIDTH

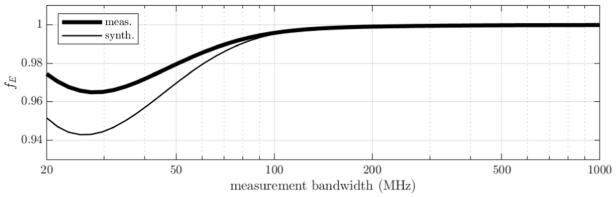
The measurement channels must have sufficient bandwidth to accurately capture the signals of interest. Current (voltage) transition times as short as 4.8 ns (9.0 ns) were observed for



(a) i_s and v_{ds} data.



(b) Transistor instantaneous power dissipation.



(c) Normalised switching loss as the measurement bandwidth is varied.

FIGURE 6. Effect of measurement bandwidth on switching loss calculations. "Full BW" refers to raw measurement data and unfiltered synthesized data.

the GaN HEMT. To ensure signal transition rates are not significantly reduced, a transition time of $t = 4.8$ ns requires a measurement bandwidth of at least $1/\pi t = 65$ MHz. As shown in Fig. 4, the i_s and v_{ds} measurement circuits have a gain of no less than -3.0 dB up to 100 MHz and no less than -4.2 dB up to 500 MHz. Whilst this represents a 'reasonably flat' gain response, it nevertheless implies that, for example, a component in the power waveform at 100 MHz would be attenuated by roughly 3.9 dB (because the gain of the i_s and v_{ds} channels at this frequency are -0.9 dB and -3.0 dB respectively). This results in an underestimate of the power at this frequency component by a factor of 2.45.

The sensitivity of the E_{sw} calculation to imperfect gain flatness is complex and not readably amenable to analysis. Instead, Fig. 6 investigates the effect numerically by comparing E_{sw} values when the calculation is performed using full bandwidth data (solid lines), and data that has an artificially reduced bandwidth (dotted lines). Two sets of input data (Fig. 6(a)) are used:

- Measured waveform data from a GaN HEMT turn-on event with current flowing into the half-bridge. This event produces fast edge rates as well as exhibiting a current overshoot due to the discharge of the switch node capacitance. These data are shown with thick lines.
- Synthesized waveform data intended to recreate idealised measured data not subject to a limited measurement bandwidth. These data are shown with thin lines.

TABLE 2 Summary of Electrical Measurement Error Sources

Measurement	Range	Offset error	Gain error	BW (-3 dB)	Gain @ 100 MHz
i_s [a]	± 100 A	± 0.25 A	$\pm 2\%$	540 MHz	-0.91 dB
v_{ds} [b]	± 660 V	± 4 V	$\pm 2\%$	100 MHz	-3.0 dB

[a] the range was increased to ± 300 A for the Si SJM to capture the reverse recovery current (offset error ± 0.75 A).
[b] v_{ds} to i_s skew less than 0.2 ns.

A second-order Butterworth lowpass filter with a cutoff frequency of 100 MHz is used to reduce the bandwidth of both sets of waveform data. This has the effect of 'softening' sharp corners, as well as introducing a time delay of about 3 ns. It is clear from Fig. 6(b) that the shape of the power waveform is very similar at full and reduced bandwidth, and so the switching loss (area under the curve) is very similar. Fig. 6(c) shows the normalised E_{sw} as the filter cutoff frequency is varied:

$$f_E = \frac{E_{sw}^{\text{reduced BW}}}{E_{sw}^{\text{full BW}}}. \tag{6}$$

At a bandwidth of 100 MHz the error is less than 0.5%. At 50 MHz, the error increases to 2% for the measured data and 3% for the synthesized data. The latter is larger presumably because of the greater high-frequency content in the synthesized data.

C. SENSITIVITY TO MEASUREMENT SKEW

E_{sw} is sensitive to skew (relative delay) between the i_s and v_{ds} channels. A simple numerical analysis shows that for the GaN HEMT waveform of Fig. 6, the change in E_{sw} is 9.5 %ns^{-1} over a skew range of ± 3 ns. As the design and layout of the measurement channel circuits are very similar, there is negligible skew introduced by the circuits themselves. Skew values of under 0.2 ns are readily achievable by ensuring coaxial line lengths are matched to within 4 cm, so the error in E_{sw} caused by skew is less than 2%. Table 2 summarises the performance of the measurement channels after gain calibration and de-offsetting has been performed.

V. MEASUREMENT OF SWITCHING LOSSES BY CALORIMETRY

Calorimetry provides a measurement of switching losses that is not dependent on high-bandwidth electrical measurements and so can be used to validate the approach of Section IV. Validation of the switching losses using calorimetric measurements is performed in [18], [19], [20], [21], [22], [23], [24]. Large errors between the calorimetry and electrical measurements are seen in [19] and estimated to be as large as $\pm 20\%$ in the best performing methods presented in [20]. In this study, we report an accuracy of $\pm 5\%$.

A. CALIBRATION OF THE CALORIMETRIC APPARATUS

Fig. 7 shows an equivalent circuit model of the major thermal connections on the PCB. The lower and upper transistors dissipate P_{TL} and P_{TU}, and the auxiliary components (power supplies, gate drivers, measurement channels) dissipate P_{XL}

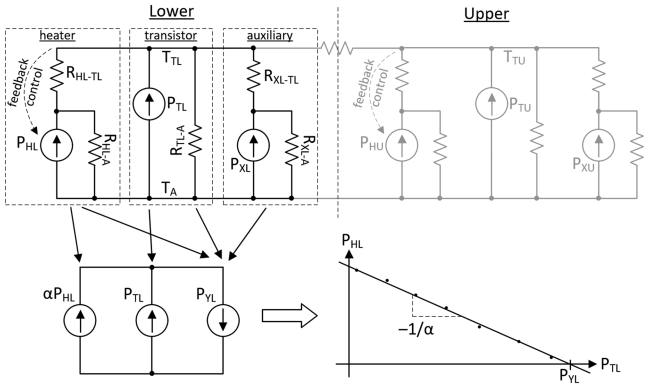


FIGURE 7. Equivalent circuit model showing heat inputs and flows in the calorimetry experiment. Equal transistor temperatures ($T_{TL} = T_{TU} = 100\,°C$) are maintained by feedback control of the heater powers P_{HL} and P_{HU}.

and P_{XU}. Heat flows between components and to ambient temperature T_A through various thermal resistances. The lower and upper heaters inject powers P_{HL} and P_{HU} under independent closed-loop feedback control to maintain the lower and upper transistor temperatures at $T_{TL} = T_{TU} = 100\,°C$. As a result, there is no heat flow between the lower and upper transistors, and so the upper transistor's thermal circuit can be ignored when considering the lower transistor. Furthermore, because T_{TL} is held at a constant value and it is assumed that the auxiliary power P_{XL} is constant, the auxiliary thermal resistances to ambient, and the auxiliary power can be replaced by a single equivalent power P_{YL}. Finally, the heater power can be replaced by an equivalent power αP_{HL} where $\alpha < 1$. As a result, there is a simple relationship between transistor and heater power dissipation in two unknown variables:

$$P_{TL} = P_{YL} - \alpha P_{HL}. \tag{7}$$

The unknowns are found by gating the transistors on and passing a known DC current I_s through them; the voltage drop $V_{ds(on)}$ across the lower transistor is measured using a Kelvin connection, and so the lower transistor power dissipation is known to be $P_{TL} = I_s V_{ds(on)}$. By varying I_s between zero and that required to achieve $P_{HL} = 0$, several data points may be collected and a line of best fit constructed as shown in the bottom-right of Fig. 7. With $T_A = 19.0\,°C$ and still air surrounding the experiment, $\alpha = 0.838$ and $P_{YL} = 4.95\,W$.

B. COMPARISON BETWEEN THE TWO APPROACHES

A comparison can now be made between the switching energies derived from electrical measurements and those by calorimetry. To obtain a calorimetric measurement, the transistor temperatures are held at $T_{TL} = T_{TU} = 100\,°C$ and the half-bridge is operated continuously at a fixed switching frequency f_{sw}. Once the apparatus has achieved thermal steady-state the lower heater power P_{HL} is measured and (7) is used to calculate P_{TL}. A calorimetrically-derived total switching loss can then be calculated by subtracting the conduction loss:

$$E_{sw,on\&off} = \frac{P_{TL} - P_{cond}}{f_{sw}}, \tag{8}$$

where $P_{cond} = DI_0V_{ds(on)}$ is the conduction loss of the lower transistor, $D = 0.03$ is the duty cycle of the lower transistor, I_0 is the average half-bridge output current, and $V_{ds(on)}$ is estimated using the DC $V_{ds(on)}$-I_s relationship recorded during calibration. The duty cycle is low and the switching frequency is set such that $P_{TL} \approx 100P_{cond}$, i.e., switching loss is the dominant component of losses in the lower transistor. In the calorimetric tests, I_0 and/or V_{dc} was reduced because of the limited continuous power dissipation capacity of the apparatus (the calorimetric test operates continuously, whereas DPT testing is discontinuous and so can operate transiently at 40 A and 400 V).

$E_{sw,on}$, $E_{sw,off}$ and P_{HL} are recorded during continuous operation as the switching frequency is varied. The lower frequency limit is chosen to limit the ripple current, and the upper frequency limit occurs when $P_{HL} \to 0$. Two transistors are used to perform calorimetric testing and validation:

1) *Si IGBT:* Provides relatively slow i_s and v_{ds} transitions with large peak reverse recovery currents, and so tests the dynamic range of the measurement circuits. Switching energies are high, meaning that the switching frequency must be kept low, and so a 3.4 mH iron-cored inductor was placed in series with the air-cored load inductor, giving a maximum ripple current of $0.02I_0$ at $V_{dc} = 400\,V$.
2) *SiC MOSFET:* Provides relatively fast i_s and v_{ds} transitions, and so tests the high-frequency response of the measurement circuits. Switching energies are low, allowing high switching frequencies. $V_{dc} = 200\,V$ was chosen to limit the maximum ripple current to $0.2I_0$ using the air-cored load inductor alone.

The results are shown in Fig. 8. The 'calorimetry' curves are obtained by translating P_{HL} to P_{TL} using (7) and then converting to $E_{sw,on}$ and $E_{sw,off}$ using (8). The error bars correspond to the uncertainties in the calibration process such as imperfect measurements of heater power and transistor power, and weak variation in P_{YL} with f_{sw} (due to increased gate-drive losses at higher frequencies). The error bars are smaller at higher switching frequencies because switching losses are a larger proportion of the total transistor losses. The 'integrated-product' curves are obtained by summing the $E_{sw,on}$ and $E_{sw,off}$ values obtained by applying (1) to a single pair of i_s and v_{ds} measurements. The error bars correspond to the uncertainties discussed in Section IV and are fixed because the switching frequency does not affect the calculation of E_{sw}; the small variations with frequency are likely caused by slight changes in the offset and/or gain of the measurement circuits and oscilloscope over time.

At higher switching frequencies (where the calorimetric measurement is the most sensitive), the two measurements agree to within 2.8 μJ (10%) for the SiC MOSFET, and 8.5 μJ (4.5%) for the Si IGBT. It is likely that a large proportion

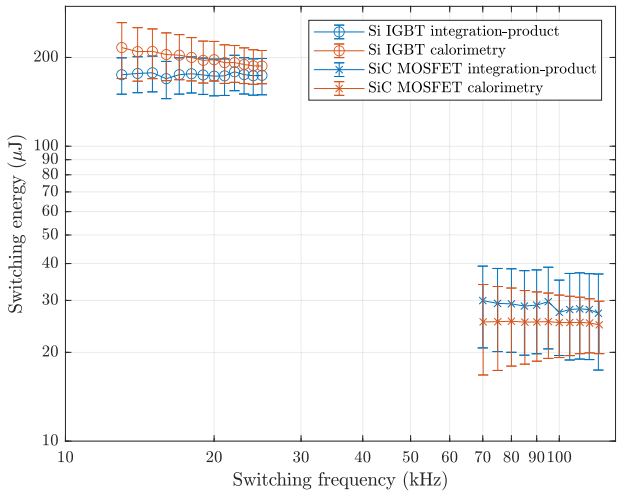


FIGURE 8. Comparison of switching energies calculated by DPT and calorimetry for the Si IGBT at $I_0 = 5$ A and $V_{dc} = 400$ V, and the SiC MOSFET at $I_0 = 2.5$ A and $V_{dc} = 200$ V, both with a junction temperature of 100 °C.

of the differences in Fig. 8 are due to offset errors in the measurements used in the integrated-product method which explains why the fractional difference for the Si IGBT is lower than for the SiC MOSFET. It is reasonable to assume that the switching energies reported in Section VI are accurate to within ±5% or ±10 μJ, whichever is larger.

VI. DPT RESULTS FOR THE FOUR TRANSISTORS

The four transistors were tested under all combinations of:

1) Current flowing into and out of the half bridge.
2) 50/75/100/125/150 °C case temperature.
3) RR/ZR: Manufacturer recommended external gate resistance / zero external gate resistance.
4) ZV/NV: Zero voltage / negative voltage off-state v_{gs}, as shown in Table 1.

For the SiC MOSFET, the manufacturer recommends zero gate resistance, so RR and ZR are the same. For the Si SJM, ZR caused very large reverse recovery currents and resulted in transistor failure at $V_{dc} = 300$ V, so only RR tests are reported. For the Si IGBT and GaN HEMT, ZR reduces switching loss in all cases, without causing significantly larger voltage or current overshoots during switching. Therefore, ZR results are shown for all transistors except the Si SJM, as this represents 'best' possible operation (lowest loss).

A single DPT takes approximately 14.5 μs to complete and is repeated infrequently (4 Hz) and so both transistors experience very low average power dissipation. The energy dissipated in the transistor in a single DPT causes negligible temperature rise due to the inherent heat capacity and thermal diffusivity of the transistor die [6]. As a result, the junction temperature is assumed to be equal to the case temperature at all times.

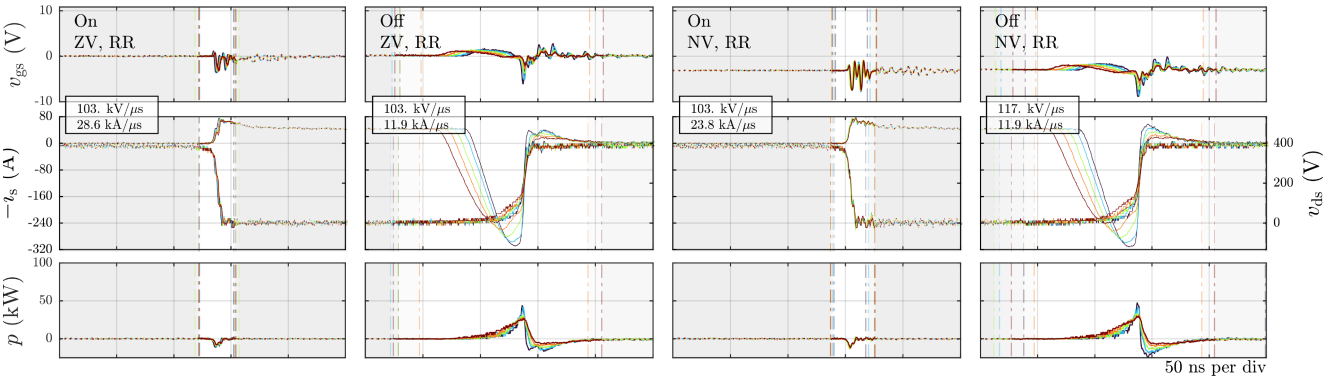
Figs. 9 and 10 show turn-on and turn-off v_{gs}, i_s and v_{ds} waveforms, along with the corresponding instantaneous power waveform, for each transistor type over the full temperature range (temperatures as per the colour bar on Fig. 11). Maximum rates-of-change of v_{ds} and i_s are also indicated. The vertical dotted lines in the Figures indicate the integration framing $t \in [t_0, t_1]$ for each temperature. Note that the Si IGBT waveforms have a longer timebase than the others.

Fig. 11 compares the switching losses calculated using (1) applied to the waveforms of Figs. 9 and 10. It also includes losses for the Si IGBT and GaN HEMT operated with the manufacturer recommended gate resistance. Three major trends are visible: Switching losses increase with temperature; switching losses decrease when the transistors are driven with a zero gate resistance (ZR); and switching losses decrease when a negative off-state voltage is used (NV). The Si IGBT is the most temperature-sensitive transistor (60% increase in switching losses from 50 to 150 °C). The GaN HEMT switching losses are almost halved by using zero gate resistance.

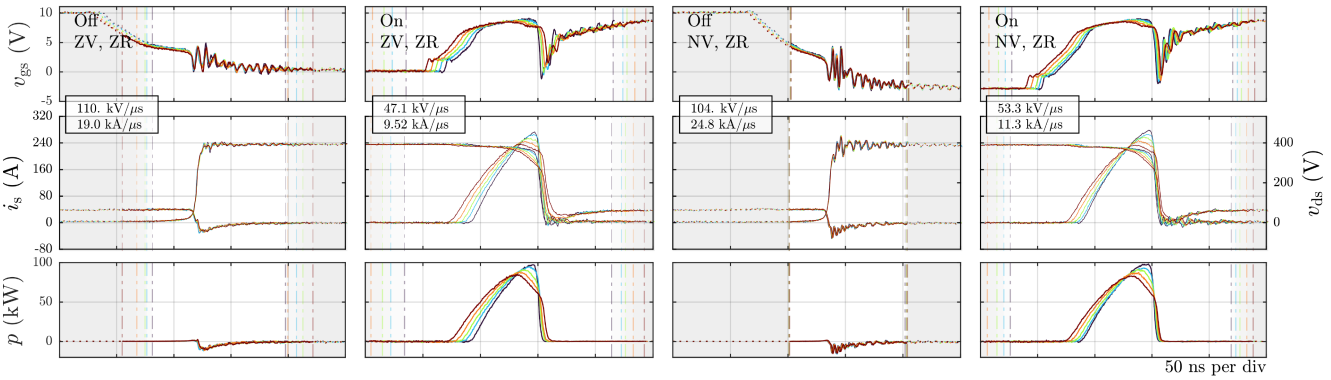
A. DISCUSSION ON SWITCHING BEHAVIOUR

A detailed analysis of the waveforms of Figs. 9 and 10 follows:

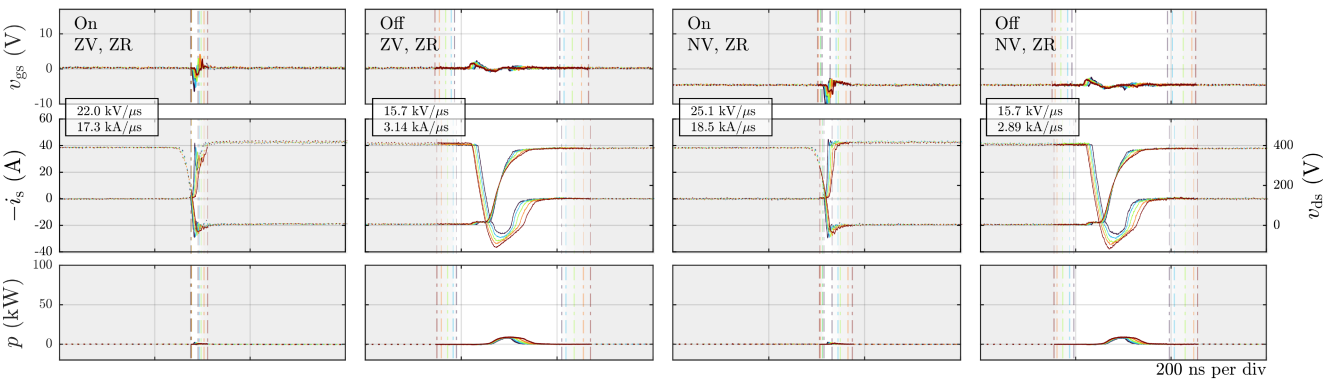
- The lower transistor behaves as a diode for current flowing out of the bridge (Figs. 9(a), (c), and 10(a), (c): current commutates as the upper transistor switches and switching loss in the lower transistor is small). The lower transistor undergoes hard-switching for current flowing into the bridge (Figs. 9(b), (d), and 10(b), (d): current commutates as the lower transistor switches and switching loss in the lower transistor is large).
- The SiC MOSFET and GaN HEMT exhibit peaks in the current at ZV turn-on only (Fig. 10(b) and (d)). We interpret these peaks as evidence of shoot-through (transient turn-on of the opposing transistor) in addition to capacitive charging, because NV eliminates this peak for the SiC MOSFET and reduces it significantly for the GaN HEMT.
- Turn-on for the Si SJM is dominated by the very large reverse recovery charge of the body diode (Fig. 9(a) and (b)), related to the superjunction voltage blocking mechanism [25]. This large peak current necessitated the use of a lower-value i_s current sense resistor to avoid signal chain saturation (1.0 mΩ instead of 3.3 mΩ). No Si SJM failures occurred for RR (failures did occur for ZR). The Si IGBT turn-on is similarly dominated by the reverse recovery of the anti-parallel PiN diode (Fig. 9(c) and (d)).
- Gate plateaus are evident in the v_{gs} hard-switching plots for all transistors at turn-on as expected from basic switching theory [26], noting that the Si IGBT has MOSFET like characteristics at turn-on [27] and it is typically assumed that the GaN HEMT has MOSFET-like gate characteristics [28], despite a Schottky diode gate structure [29]. The turn-on gate plateau for the GaN HEMT corresponds to the fast dv_{ds}/dt of 100–113 kV μs^{-1} (Fig. 10(c) and (d)).
- At turn-off the observed gate plateau voltages are lower than anticipated by [26] for all transistors except the



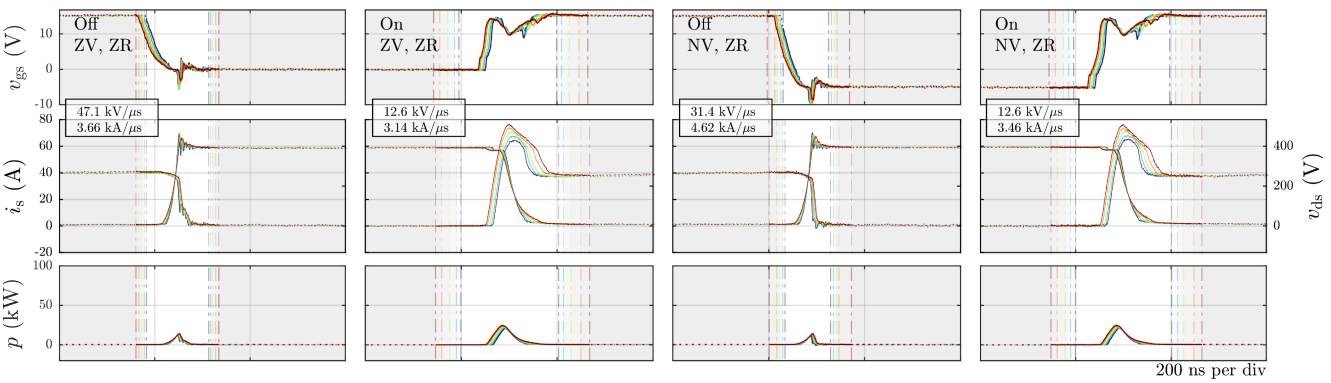
(a) Si SJM, current out of bridge (lower transistor diode switching).



(b) Si SJM, current into bridge (lower transistor hard switching).

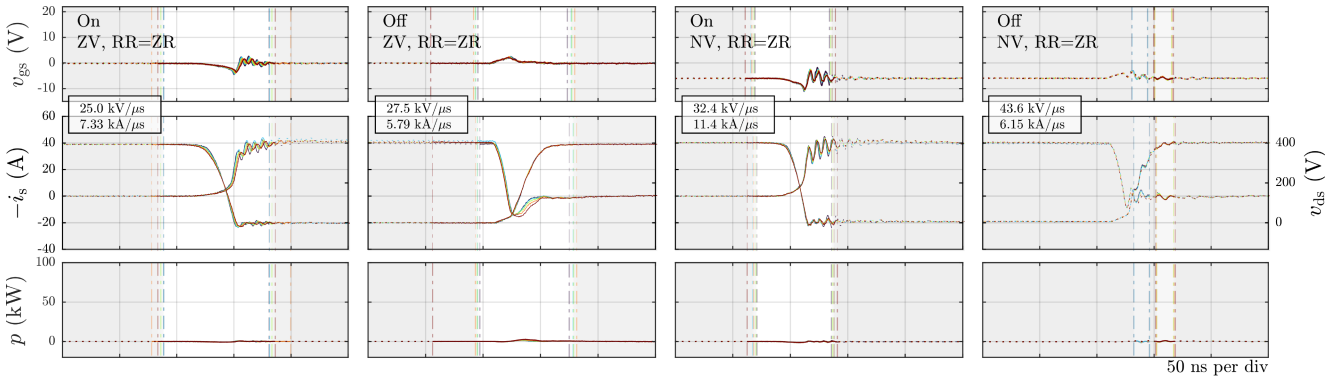


(c) Si IGBT, current out of bridge (lower transistor diode switching).

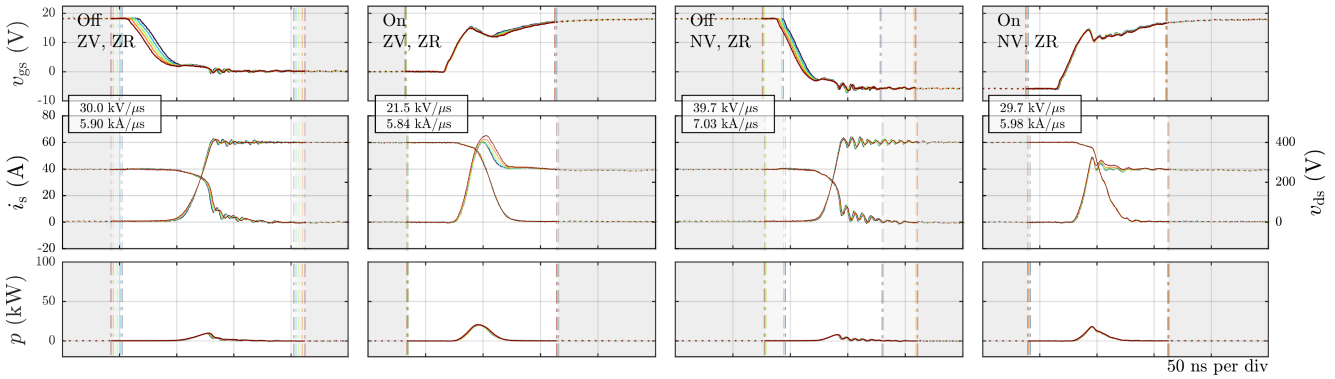


(d) Si IGBT, current into bridge (lower transistor hard switching).

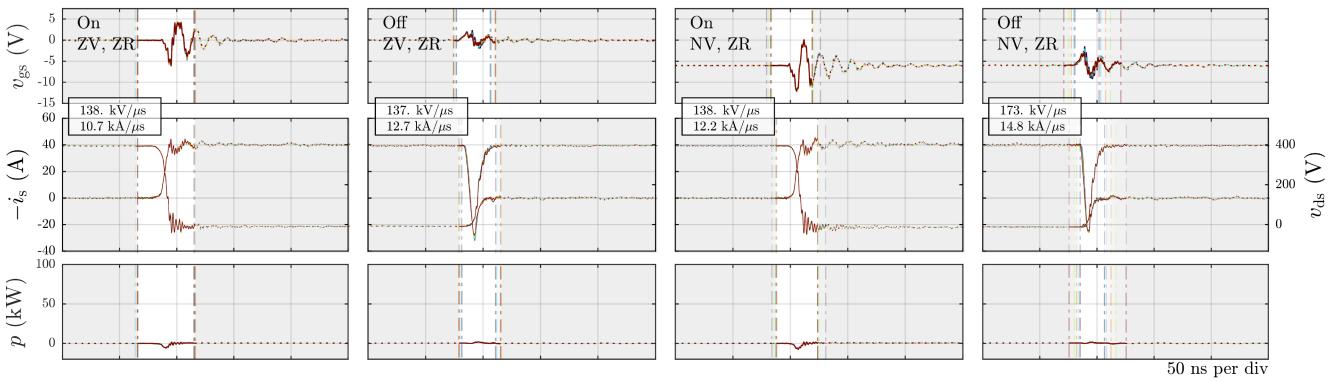
FIGURE 9. **Si SJM and Si IGBT switching waveforms. The white regions and vertical lines indicates the integration frame for each temperature.**



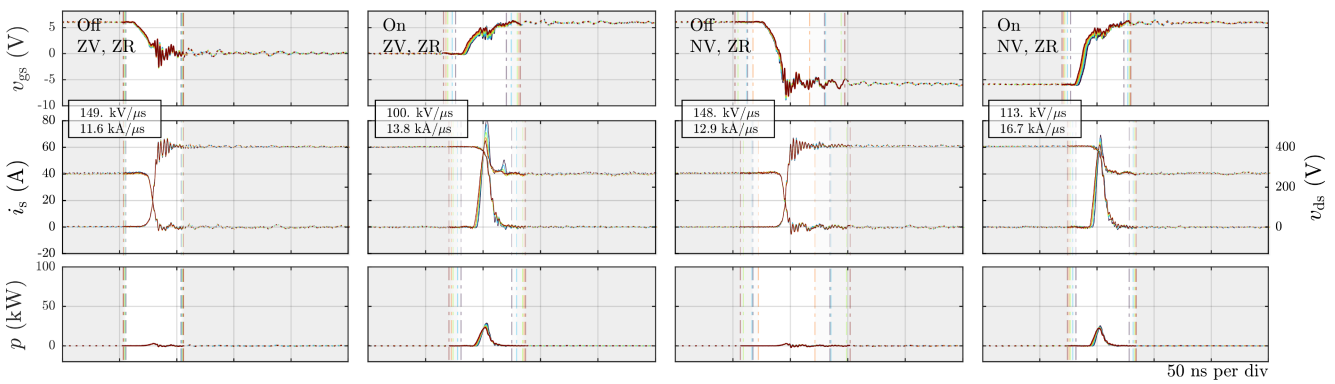
(a) SiC MOSFET, current out of bridge (lower transistor diode switching).



(b) SiC MOSFET, current into bridge (lower transistor hard switching).



(c) GaN HEMT, current out of bridge (lower transistor diode switching).



(d) GaN HEMT, current into bridge (lower transistor hard switching).

FIGURE 10. SiC MOSFET and GaN HEMT switching waveforms. The white regions and vertical lines indicates the integration frame for each temperature.

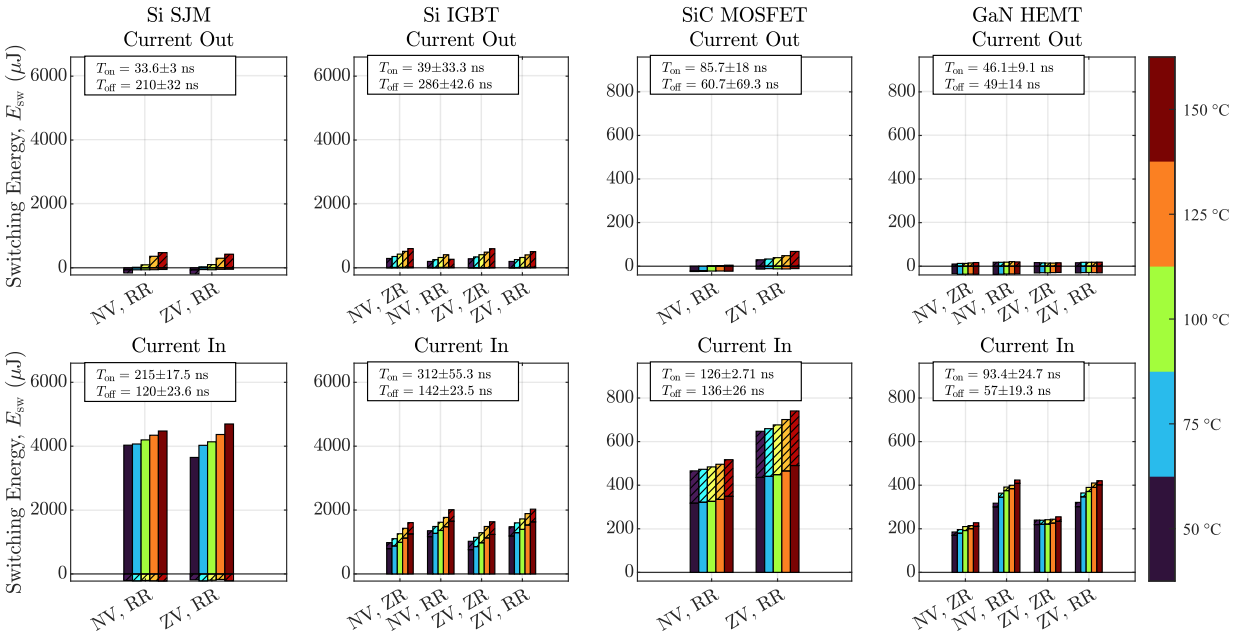


FIGURE 11. Switching losses in the lower transistor for current flowing in and out of the half-bridge. The hatched portion of each bar denotes the turn-off loss and the unhatched portion the turn-on loss.

Si SJM. In the case of the SiC MOSFET, the internal gate resistance of 7 Ω (Table 1) slows the switching and 'hides' the true Miller plateau from the external measurement of v_{gs}, giving a value which is lower at turn-off and higher at turn-on. The SiC MOSFET gate plateau corresponds to a dv_{ds}/dt of 20–40 kV μs^{-1} and results in a fairly symmetrical split of losses for turn-on and turn-off [26] (Fig. 10(a) and (b)).

- The Si SJM has strongly non-linear gate-drain and drain-source capacitances [25], [30] leading to the exceptionally fast dv_{ds}/dt of 282–332 kV μs^{-1} towards the end of turn-off. The turn-off loss is very small for current-in (Fig. 9(b)). The turn-on dv_{ds}/dt of 108–130 kV μs^{-1} is also fast (Fig. 9(a)).
- There are two distinct turn-off behaviours. In most cases of inductive load switching, v_{ds} rises before i_s falls, as for the Si IGBT (Fig. 9(c) and (d)) and SiC MOSFET (Fig. 10(a) and (b)). In contrast, for the Si SJM (Fig. 9(a) and (b)) and GaN HEMT (Fig. 10(c) and (d)), there is significant overlap. Deboy [25] notes that C_{oss} and $C_{ds} + C_{gs}$ is capable of absorbing the whole inductive load current, and so the channel can be shut off rapidly. Because the circuit node capacitance (including the upper transistor) is similar in magnitude to C_{oss} for the Si SJM, the load current may drop early giving an overlap. A similar circuit analysis is possible for the GaN HEMT and in both cases the turn-off loss is very small. The Si IGBT gate behaviour at turn-off also shows that the MOS channel is off before the transistor switches, due to the large conductivity modulated charge which must be swept out by the load current as the voltage rises [27].

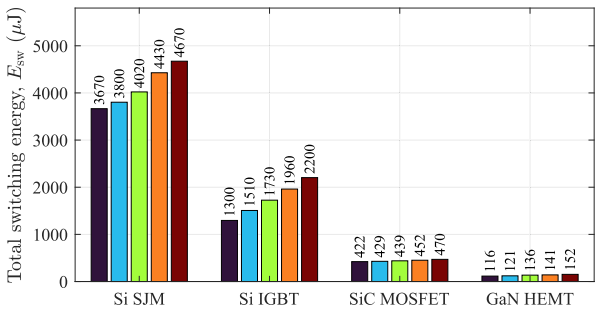


FIGURE 12. Total switching loss in a half-bridge at different temperatures.

- The use of a negative gate off-state voltage (NV) increases dv_{ds}/dt and di_s/dt, particularly for the SiC MOSFET by helping to overcome its internal gate resistance. Zero resistance switching (ZR) significantly improves performance of the GaN HEMT, speeding up turn-on and reducing turn-on losses.
- The Si IGBT, Si SJM and GaN HEMT all exhibit slightly slower overall switching times at higher temperatures, giving greater losses, while the SiC MOSFET is insensitive to temperature, particularly with NV switching.

B. TOTAL SWITCHING LOSSES IN A HALF-BRIDGE

Fig. 12 compares the lowest-loss operation of a half-bridge operating at 400 V and 40 A, i.e., the summation of current-in-turn-on, current-in-turn-off, current-out-turn-on and current-out-turn-off losses from Fig. 11. Lowest-loss operation for all transistors is achieved using NV and ZR, except for the Si SJM which requires RR to avoid failure.

VII. CONCLUSION

When operated without a gate resistor, the GaN HEMT delivers the lowest switching loss: At junction temperatures that are likely to be found in many end applications ($>100\,^{\circ}$C), the switching loss of the SiC MOSFET, Si IGBT and Si SJM transistors are approximately $3.2\times$, $14\times$ and $31\times$ greater than the GaN HEMT, respectively. It is notable that at current market prices, the Si IGBT is roughly one tenth of the price of the WBG transistors, meaning that the decision to select a WBG transistor (or not) is likely to be highly dependent on the switching frequency and overall efficiency required in the end application.

We note that all the transistors studied in this article operated successfully with a zero off-state v_{gs}, which allows simplification of the gate drive circuit in the end application. However, the behaviour of the SiC MOSFET (and to a lesser extent, the GaN HEMT) is improved significantly by a negative off-state v_{gs} as it reduces shoot-through current and speeds up turn-off.

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