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Floating Capacitor Integrated DAB for Single-Phase, Single-Stage PFC in Wireless Battery Charging Application

ITZIAR ALZUGUREN [1,2] (Member, IEEE), ASIER GARCIA-BEDIAGA [1] (Member, IEEE), ANDER AVILA [1], ALEJANDRO RUJAS [1], AND MIROSLAV VASIĆ [2] (Senior Member, IEEE)

[1]Power Electronics Area, Ikerlan Technology Research Centre, Basque Research, Technology Alliance, 20500 Mondragon, Spain
[2]Centro de Electrónica Industrial, Universidad Politécnica de Madrid, 28006 Madrid, Spain

CORRESPONDING AUTHOR: ITZIAR ALZUGUREN (e-mail: ialzuguren@ikerlan.es)

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ABSTRACT In this article, a novel active power decoupling topology called Floating Capacitor Integrated Dual Active Bridge (FCI-DAB) for single-phase, single-stage AC-DC solutions is introduced. The main point of the circuit is an active energy buffer that compensates the power fluctuation at double the grid frequency. The power decoupling filter is composed by a floating capacitor and a full-bridge; and is connected to the high-frequency link of a resonant DAB |AC|-DC converter. Compared to state-of-the-art two-stage solutions, it dispenses with the bulky electrolytic storage capacitor, with high ESR and low reliability, whose function is to create a constant DC bus. Unlike typical single-stage converters, filtering the fluctuating instantaneous power in the primary-side of the converter brings advantages such as reducing the RMS current in the secondary-side of the circuit, which results on a 50% of savings in the secondary-side resistive conduction losses. This is considered a key point, specially in Electric Vehicle (EV) wireless battery charging applications, facilitating the refrigeration of secondary-side circuit that is located on-board the vehicle. The article presents the novel FCI-DAB circuit and proposes a control strategy based on duty-cycle modulation which enables the realization of the PFC in the grid-side and the compensation of the power fluctuation with the active buffer in the primary-side. The FCI-DAB concept is verified by experimental results, obtained from an GaN-based IPT 1.5 kW battery charger, with 93% of efficiency and PF = 0.99.

INDEX TERMS Active filter, power pulsation buffer, PFC, floating capacitor, FCI-DAB, single-phase, single-stage, AC-DC, inductive power transfer, electric vehicle, GaN.

I. INTRODUCTION

Nowadays, single-phase AC-DC converters connected to conventional grid are widely used for numerous applications, such as renewable energy sources or Electric Vehicles (EV). This type of converters must provide the Power Factor Correction (PFC) functionality and power control from AC to regulated DC output.

In conventional, two-stage solutions, the inherent power fluctuation at twice the mains frequency is filtered out by large electrolytic capacitors with high ESR, which apart from penalising the power density, lead to reliability problems that conclude in limited lifetime [1], [2], [3].

An alternative to avoid the electrolytic capacitor are the single-stage chargers that dispense with the DC bus, transferring the harmonic of twice the grid frequency to the output [1], [4], [5]. These chargers tend to be more power-dense and lower in hardware cost. Nevertheless, the control of the converter is more complicated, higher current values appear and the battery can suffer from overheating problems [6], [7], [8], [9]. In [10], a single-stage solution is proposed.

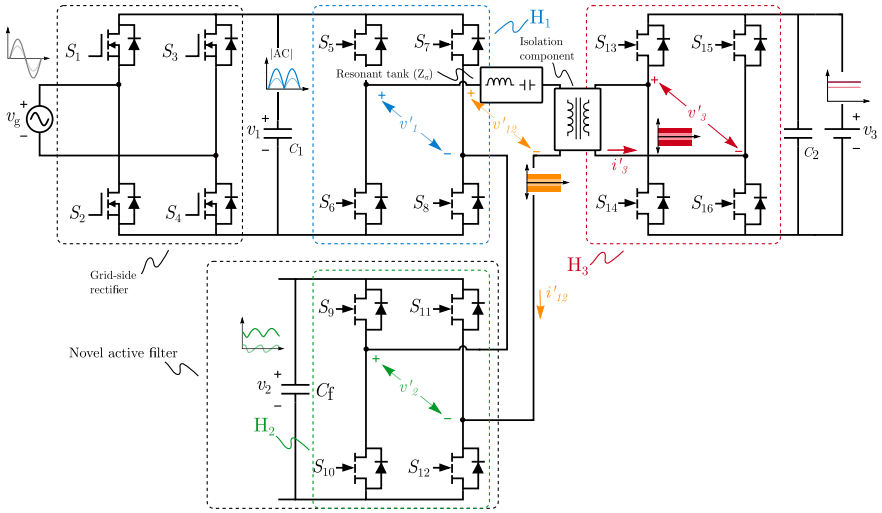

FIGURE 1. Novel circuit for single-phase single-stage AC-DC solutions based on a floating active filter connected to the HF link, called FCI-DAB. It is composed of a grid-connected rectifier, followed by a a rectified sinusoidal voltage bus and a modified resonant DAB converter with an additional active power pulsation buffer connected in series with the isolation component.

However, a big electrolytic capacitor is placed at the output of the converter, thus the problem of the bulky and unreliable electrolytic capacitor is not solved.

Large electrolytic capacitors can also be avoided with active energy buffer circuits with smaller size and longer lifetime energy storage components. A comprehensive review of active power decoupling topologies for single-phase PFC-s is done in [11] and numerous references of active filters connected in parallel with the original converter are included [8], [9], [12], [13], [14].

In [15], an active filter is implemented by a full-bridge inverter connected in series with the input diode rectifier connected to the grid. In the series power decoupling solution in [16], [17], [18], [19], a novel concept by introducing a voltage compensator in series with DC bus lines is proposed. In [20], an active power buffer is integrated into a Three-Level (3L) Flying Capacitor (PFC) PFC circuit. However, the solution does not include galvanic isolation, thus its usage in some applications such as battery chargers is limited, unless a second isolated stage is added to the circuit.

In [21], a generic topology derivation method for single-phase PFCs with integrated active capacitive filter has been proposed, which can derive all existing topologies, and identify a few new topologies. Moreover, a component sizing procedure for benchmarking of these capacitive filters is proposed. In our work we propose a solution which was mapped in [21] as one possible approach for the active filtering. It would be the series connection of the buffer on the AC-side of the original converter.

In this article, the novel active power decoupling topology of Fig. 1 is introduced, called, from now on, Floating Capacitor Integrated Dual Active Bridge (FCI-DAB). The original circuit is a resonant DAB |AC|-DC converter presented in [22], [23] and the novel active power decoupling cell is connected in series to the original circuit, in the high-frequency (HF) AC link.

In [22], [23], an ultra compact system is achieved due to the lack of passive components and a second stage. Therefore, two times the power density of state-of-the-art wireless chargers is achieved. However, the power ripple of twice the grid frequency is transferred to the converter output. In the current work, we add additional circuitry, which is composed of active devices and a capacitor. In this way, we provide added value in terms of system functionality, removing the power ripple of twice the grid frequency at the output completely, thus becoming an industry-accepted solution and still with a high benefits in terms of power density.

In this work, we propose the FCI-DAB as a solution for Wireless Battery Charging application for EV, however, the circuit can be used in different single-phase AC-DC applications. Furthermore, although the resonant variant is analyzed in this article, the modified DAB can be non-resonant, with a transformer and an inductance in series, with its rectangular and linear waveforms.

If we neglect the diode rectifier at the input and look at the three full active bridges, the circuit is a resonant triple active bridge. In [24], [25], [26], circuits consisting of three full bridges, which may or may not be resonant, are analyzed. Compared to the mentioned solutions, in this case, instead of connecting the third bridge to the same transformer via a third winding, the additional bridge is connected in series with the first bridge and the isolation component, thus this magnetic component is less complicated and easier to design. Moreover, the nature or objective of the circuit is not the same. In the aforementioned works, the circuit is proposed as a solution to connect multiple DC energy sources and electrical loads for different applications, such as EV, renewable energy generation or bipolar DC distribution systems. In this

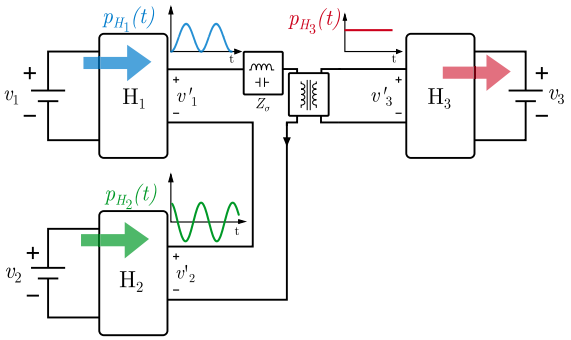

FIGURE 2. Simplified block diagram of the FCI-DAB. The circuit is composed of three full bridges, each one with its power reference. H_1 must fulfill the PFC functionality, H_2 behaves as active power decoupling circuit, thus H_3 transfers constant power to the output.

case, the system is proposed as a single-stage AC-DC solution which incorporates internally the ability to filter out the ripple of the double-the-grid frequency thanks to the floating power decoupling cell connected in series with the original circuit.

Compared to state-of-the-art active filters, FCI-DAB is considered novel due to its series connection to the HF line of a modified DAB. The disadvantage of this circuit is that connecting the filter in series means that all the series current will flow through it, with its consequent conduction losses. Against this disadvantage, the circuit is considered to provide other benefits, which are listed below.

There is no need for a rectification stage that creates a DC bus. i.e. the modified DAB is connected directly after the input diode rectifier, i.e. to a rectified sine bus, with the simplicity and high efficiency that this brings in the AC-DC stage.

The buffer includes only one storage component, which is the floating capacitor that have less capacity than the bus capacitor of two-stage solutions reducing volume and weight and allowing technologies other than electrolytic, such as film or ceramic capacitors. Moreover, it does not need an inductive component, as in the case of a bidirectional buck, improving the power density.

The flying capacitor has a double role of energy accumulation and power shaping. Apart from participating in the filtering of the floating instantaneous power, also participates in the HF operation of the converter and can help in achieving the desired HF waveforms. The circuit can be seen as a multilevel solution and assists in, for instance, achieving higher equivalent voltages or achieving ZVS over all input and output voltage ranges.

The idea of the concept in its non-resonant version was presented in [27] for an OBC application for EV. This time the circuit is presented for a wireless charger application for EV in its resonant version, with the resonant tanks included in series. In this article we wanted to go a step further and analyze where the converter is placed compared to other solutions from academia and industry. We also wanted to analyze the implications of the integration of the active filter and see its weaknesses and advantages. The article also includes studies that go deeper into the circuit design, including the sizing of the floating capacitor and the analysis of the secondary RMS current. The experimental part is further in-depth, including, also, measurements of the efficiencies and RMS currents, apart from the waveforms. A comparative analysis with other solutions from literature, in terms of efficiency and volume, is also performed.

This work is organized as follows. Section II is the presentation of the FCI-DAB, where the control variables and the power references are defined. This is an introduction to the Section III, where a specific control based on the duty-cycle modulation is presented, together with the steady-state HF waveforms and a small description of the regulation strategy. In Section IV, the implications of integrating the active filter in the design and performance of the circuit are analyzed. In Section V, a case study is presented and results obtained from an experimental platform are shown, with the aim of validating the theoretical study. Finally, Section VI draws some conclusions.

II. CIRCUIT, CONTROL VARIABLES AND POWER REFERENCES

The proposed FCI-DAB is shown in Fig. 1. The circuit consists of a grid-side rectifier which may consist of diodes or active switches for unfolding rectification with low conduction losses and bidirectional power flow, followed by a continuous but not constant, rectified sine-shaped bus. Then the modified resonant DAB is connected, which consists of three full bridges (H_1, H_2, H_3). The active filter consists of a floating capacitor or energy storage element (C_f) which is connected in series with the first bridge H_1 via bridge H_2. On the secondary-side of the isolation component is connected bridge H_3.

The circuit of Fig. 1 can be easily simplified in the diagram of the Fig. 2. The basis of the proposed control strategy is to create appropriate power references for each bridge. When a PFC circuit is operating in a single-phase line, the input current follows the same shape of the grid sinusoidal voltage.

As the instantaneous power is the product of voltage and current, the multiplication of these two variables produces a constant active power and a pulsating power at two times of the line frequency. Thus, the power reference of H_1 in steady state is a sine at double the line frequency with positive offset in order to assure the power factor correction (1). The power reference of H_2 in steady state is defined in order to compensate the power fluctuation of the input port in PFC operation (2). The sum of the two powers, which is transferred to the secondary-side of the isolation component (P_{H_3}) is, therefore, constant. This second power reference may also include a constant term, which allows an average power to be transferred or absorbed into the floating capacitor, enabling the regulation of the average floating capacitor voltage and facilitating the capacitor pre-charge process.

$$p^*_{H_1}(t) = P_{H_3} + P_{H_3} sin\left(2\omega t - \frac{\pi}{2}\right) \tag{1}$$

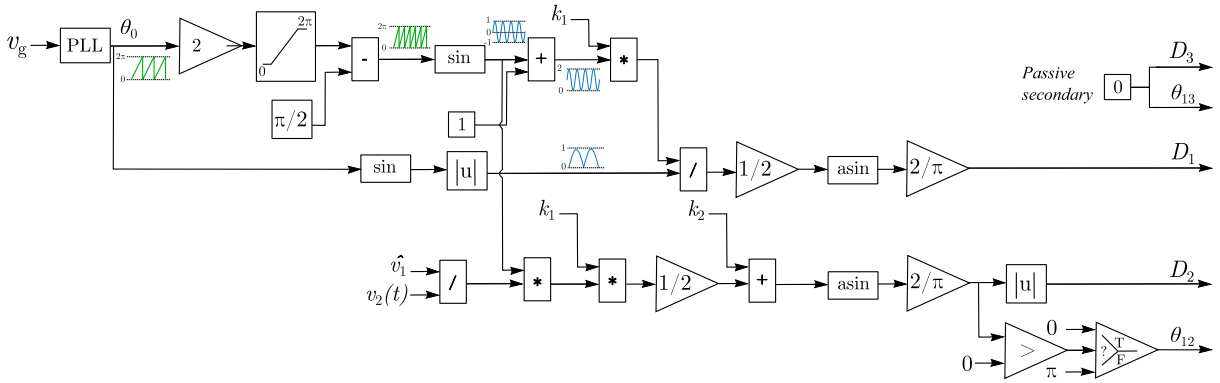

FIGURE 3. Feedforward for duty-cycle modulation: PFC and power fluctuation filtering in the FCI-DAB. Parting from the grid voltage phase (θ_0) obtained by means of a PLL, the control parameters k_1 and k_2 obtained from the regulation, and voltage measurements from the circuit (v_1 and v_2), the duty-cycles of the first two bridges (D_1, D_2) and the phase displacement of the second bridge (θ_{12}) are calculated.

$$p^*_{H_2}(t) = p_{H_2,offset} - P_{H_3} sin\left(2\omega t - \frac{\pi}{2}\right) \tag{2}$$

The power flows can be regulated with the six control parameters, that are: the switching frequency, the phase displacements of the second and third bridges respect to the first one (θ_{12}, θ_{13}) and the duty-cycles of the three bridges (D_1, D_2, D_3), that enable changing the amplitude of the respective equivalent phasor. θ_{12} and θ_{13} are defined as positive when $v'_{2,1}$ is leading $v'_{1,1}$ and $v'_{3,1}$ is leading $v'_{1,1}$, respectively. This gives the possibility to use different modulation strategies, such as a duty-cycle control, a phase-shift control, a hybrid control or an additional frequency-based control. Depending on the selected strategy, the remaining degrees of freedom can be used for the optimization of the performance of the converter.

III. CONTROL STRATEGY BASED ON DUTY-CYCLE MODULATION

As in this article the FCI-DAB is analyzed as Wireless Battery Charger for EV, the frequency band is established by SAE J2954 between 81.39–90 kHz for all light duty vehicle systems and, therefore, a frequency control is avoided because of the small possible range. Moreover, phase shift is not an obvious solution either, due to the complexity of synchronizing both primary and secondary parts. This article proposes a duty-cycle modulation on bridges H_1 and H_2 to fulfil the functions of PFC on the first bridge H_1 and double-grid-frequency filter on the second bridge H_2.

Because of the high non-linearity of the system, a feedforward control of the system is presented, thus the controllers work with continuous control variables. Basically, the grid voltage phase is achieved by means of a PLL. Based on this and the system parameters, a feedforward system is used to obtain the duty-cycles of the first two bridges H_1 and H_2. In this first control strategy proposal, H_3 works as a passive rectifier. The feedforward strategy is explained below in more detail and summarised in Fig. 3.

A. FEEDFORWARD FOR DUTY-CYCLE MODULATION

Considering a switching frequency perfectly tuned at resonant-frequency, primary-side voltage and current will be in phase. An uncontrolled secondary rectifier fixes a square voltage waveform in the secondary-side, which means that the primary-side current can be considered as a constant amplitude signal which depends on the battery voltage and the IPT coupling factor.

Consequently, the power flow of the first and second bridges (H_1, H_2) can be regulated with the duty-cycle of the respective bridge, that are obtained parting from the voltage phasor references. The voltage phasor reference of the first bridge H_1 is defined as follows (3).

$$v'^*_{1,1}(t) = \frac{2}{\pi} k_1 V_g \left[1 + \sin\left(2\omega_0 t - \frac{\pi}{2}\right)\right], \tag{3}$$

where ω_0 is the angular frequency of the grid and V_g is the peak value of $v_1(t)$, being $v_1(t)$ the grid rectified voltage ($v_1(t) = V_g|\sin(\omega_0 t)|$). k_1 is a control parameter between 0 and 1, and with this parameter we can adjust the amplitude of the first harmonic of the created HF output voltage. This amplitude directly impacts the magnitude of the transferred power.

Parting from that reference, the duty-cycle that is applied to the first bridge H_1 is obtained (4).

$$D_1(t) = \frac{2}{\pi} \text{asin}\left[\frac{k_1}{2} \frac{\left(1 + \sin\left(2\omega_0 t - \frac{\pi}{2}\right)\right)}{|\sin(\omega_0 t)|}\right] \tag{4}$$

The second bridge H_2 is controlled to compensate the power fluctuation of the first bridge H_1 and transmit a constant power to the secondary. As H_1 and H_2 are in series, they have the same HF AC current, and thus, to compensate the fluctuating power, the steady-state fluctuating amplitudes of $v'^*_{1,1}$ and $v'^*_{2,1}$ have to be equal but with opposite sign. The voltage reference of this second bridge can also include another constant term that allows to control a constant power apart from the fluctuation, in the case of charging or discharging the floating capacitor.

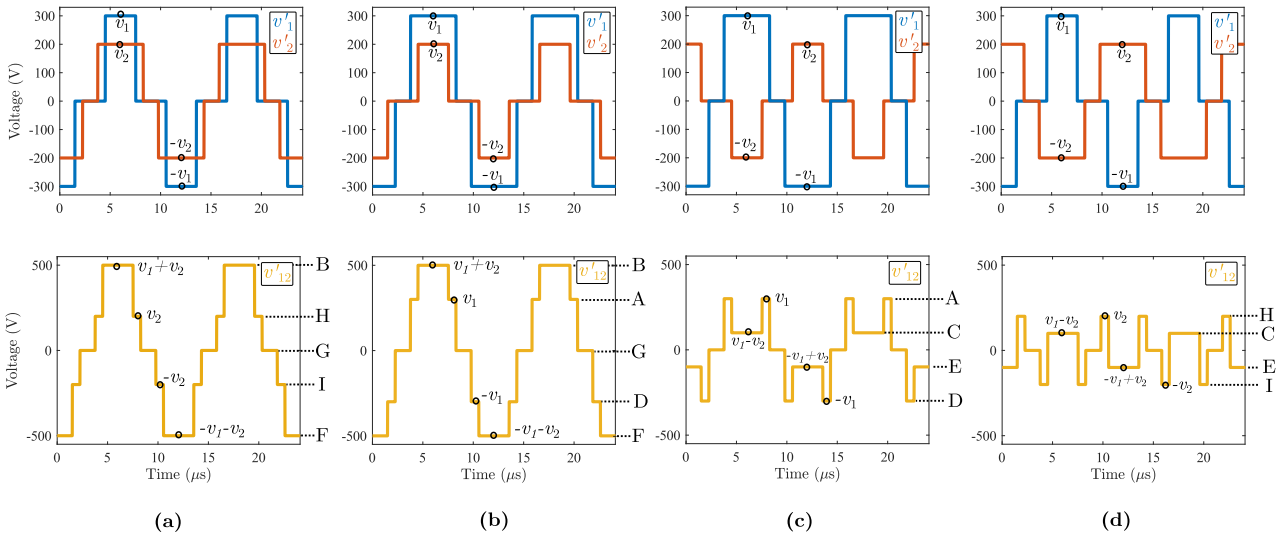

FIGURE 4. High-frequency waveforms in the primary-side of the FCI-DAB. Depending on the grid period point, the output voltages of the first two inverters (H_1, H_2) may be adding or subtracting. (a) $\theta_{12} = 0°$ and $D_2 > D_1$. (b) $\theta_{12} = 0°$ and $D_1 > D_2$. (c) $\theta_{12} = 180°$ and $D_1 > |D_2|$. (d) $\theta_{12} = 180°$ and $|D_2| > D_1$. The voltage levels of v'_{12} are marked with letters, referring to Table 1.

For a correct compensation of fluctuating power, a negative instantaneous power of the active filter could be required. This negative power can be reached with a negative reference $v'^{*}_{2,1}$, that can be achieved with a 180° phase-shift (i.e. a half of the switching period) of this second bridge H_2 respect to the first one. In other words, the second bridge changes from adding voltage to the first bridge to subtracting it, when the power reference changes from being positive to negative. The voltage reference phasor of this second bridge is defined as (5).

$$v'^{*}_{2,1}(t) = \frac{4}{\pi} v_2(t) k_2 - \frac{2}{\pi} k_1 V_g \left[\sin\left(2\omega_0 t - \frac{\pi}{2}\right) \right], \quad (5)$$

where the first term of the sum is related to the aforementioned power offset and can be regulated with the control variable k_2 defined between 0 and 1. $v_2(t)$ is the floating capacitor voltage. Parting from the voltage reference, the duty-cycle applied to the second bridge is the following (6).

$$D_2(t) = \left| \frac{2}{\pi} \operatorname{asin}\left[k_2 + \frac{k_1}{2} \frac{V_g}{v_2(t)} \sin\left(2\omega_0 t - \frac{\pi}{2}\right) \right] \right|, \quad (6)$$

The phase-shift applied to this H_2 bridge being (7).

$$\theta_{12} = \begin{cases} 0° & k_2 + \frac{k_1}{2} \frac{V_g}{v_2(t)} \sin\left(2\omega_0 t - \frac{\pi}{2}\right) \geq 0 \\ 180° & k_2 + \frac{k_1}{2} \frac{V_g}{v_2(t)} \sin\left(2\omega_0 t - \frac{\pi}{2}\right) < 0 \end{cases} \quad (7)$$

In [27], θ_{13} was used as a control variable to regulate the transferred power. In this case, the secondary-side bridge is passive and its phase-shift is not controlled. Instead, using PI regulators, we can adjust the value of k_1 and k_2, which allows us to regulate both the power that we are transferring to the output (P_{H_3}) and the mean value of the floating capacitor voltage ($\bar{v}_2$). This is detailed in the Section III-C.

B. HIGH-FREQUENCY THEORETICAL WAVEFORMS WITH THE PROPOSED MODULATION STRATEGY

Applying the duty-cycle control strategy previously explained, the resultant HF voltage on the primary-side is actually a multilevel voltage, as it can be seen in Fig. 4. We can distinguish four different states which occur throughout the grid period. The output voltages of bridges H_1 and H_2 (at the top of the Fig. 4) and the sum of the two voltages, i.e. the voltage applied to the left side of the resonant tank (at the bottom of the Fig. 4), are shown for each of them.

The first two figures (Fig. 4(a) and (b)) are given when the power reference of second bridge H_2 is positive, i.e. when this bridge has to provide power to the output. This is obtained by applying a positive voltage to the first bridge H_1, i.e. by adding its voltage or by applying 0° of phase shift.

We have the waveforms in Fig. 4(a) when the duty-cycle of H_2 (D_2) is greater than the duty-cycle of H_1 (D_1). Thus, we can observe three voltage levels in the first half of the switching period, which are 0, v_2 and $v_1 + v_2$. In the second half of the switching period, 0, $-v_2$ and $-(v_1 + v_2)$.

The Fig. 4(b) is similar to the previous one, nevertheless, in this case $D_1 > D_2$, so that the voltage levels are 0, v_1 and $v_1 + v_2$ in the first half of the switching period and 0, $-v_1$, $-(v_1 + v_2)$ in the second half of the switching period.

In Fig. 4(c) we see the case where the second bridge H_2 subtracts voltage from the first one H_1, in order to absorb instantaneous energy. The duty-cycle of the first bridge H_1 is greater than the absolute value of the duty-cycle of the second bridge H_2 ($D_1 > |D_2|$). The resultant voltage levels are 0, v_1 and $v_1 - v_2$ in the first half of the switching period and 0, $-v_1$, $-v_1 + v_2$ in the second half of the switching period.

Finally, Fig. 4(d) shows a similar case of the previous one, where the second bridge is 180° out of phase, but the absolute value of the duty-cycle of the second bridge H_2 is greater than

TABLE 1. Different Voltage Levels Applied on the Primary-Side of the FCI-DAB. These Voltage Levels are Created From the Sum or Subtraction of the Output Voltages of Inverters H_1 and H_2. There are Redundant States, I.e., the Same Voltage Level Can Be Created by Activating Different Set of Switches. These Cases are Highlighted in Blue

	H_1				H_2				
V_{12}	S_5	S_6	S_7	S_8	S_9	S_{10}	S_{11}	S_{12}	N_{level}
v_1	1	0	0	1	0	1	0	1	A
$v_1 + v_2$	1	0	0	1	1	0	0	1	B
$v_1 - v_2$	1	0	0	1	0	1	1	0	C
$-v_1$	0	1	1	0	0	1	0	1	D
$-v_1 + v_2$	0	1	1	0	1	0	0	1	E
$-v_1 - v_2$	0	1	1	0	0	1	1	0	F
0	0	1	0	1	0	1	0	1	G
v_2	0	1	0	1	1	0	0	1	H
$-v_2$	0	1	0	1	0	1	1	0	I

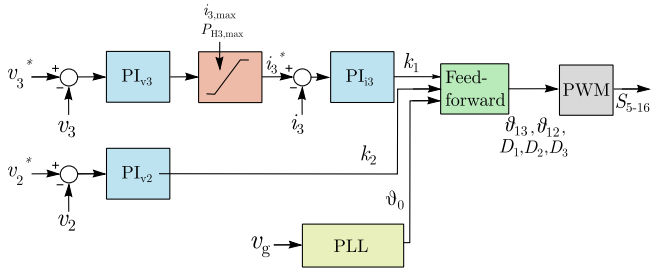

FIGURE 5. Control diagram of the FCI-DAB. A CC-CV control of the output battery is done and an additional control loop for floating capacitor voltage (v_2) is also integrated. The regulators are followed by a feedforward stage, presented previously and simplified in Fig. 3.

the duty-cycle of the first bridge H_1 ($|D_2| > D_1$). The resultant voltage levels are 0, v_2 and $v_1 - v_2$ in the first half of the switching period and 0, $-v_2$, $-v_1 + v_2$ in the second half of the switching period.

Table 1 shows the combinations of activated/deactivated switches for the creation of the voltage levels shown in Fig. 4. The blue numbers mean that although such voltage level can be created with the defined switch combination, it also has another redundant combination. This happens when the bridge has to give 0 V to the output. To achieve this, either the two devices above of the bridge or the two devices below of the bridge can be turned on.

C. REGULATION

Fig. 5 shows the simplified control diagram used in this converter. The feedforward part explained above allows the controllers to work with continuous variables. In a first control loop, Constant Current- Constant Voltage (CC-CV) control of the output battery is done by means of an external voltage loop (v_3), whose output is limited or saturated by the maximum output power and current, and an internal current loop to control the battery charging current (i_3). A second voltage loop is responsible for regulating the mean value of the floating capacitor voltage ($\bar{v_2}$). The phase of the grid voltage (θ_0) necessary to realise the PFC in the feedforward section is achieved by reading the grid voltage (v_g) and using a PLL.

IV. FILTER IMPLICATIONS ON CONVERTER DESIGN AND PERFORMANCE

This section shows two analyses carried out in relation to the integration of the filter in the converter. First, the floating capacitor is studied. Based on the energy that it must provide to the system, the sizing process of the capacitor is done. Then, a study is carried out on the current flowing through the secondary-side of the coil. This study concludes a clear advantage of the proposed circuit respect to a non-filtered circuit, relating to a reduction in the conduction losses of the secondary-side of the converter.

A. FLOATING CAPACITOR SIZING

The floating capacitor C_f is the power decoupling element, i.e., it is in charge of giving or receiving the instantaneous energy to the circuit so that we transmit constant power to the output, free of harmonics of double the grid frequency.

Since in this circuit, the filter is directly involved in the operation of the circuit, as an equivalent extra source of voltage, the voltage of this capacitor must be controlled and within voltage limits. The following analysis is related to that issue.

For the duty-cycle modulation presented above, if we take the (6), it can be derived that what is inside the arcsine must be within the limits [-1,1]. Thus, the voltage level of the floating capacitor must fulfill the following condition (8).

$$v_2(t) \geq \frac{k}{2} V_1 \sin\left(2\omega_0 t - \frac{\pi}{2}\right) \tag{8}$$

If we take a deeper look into this equation, it means that, as this filter acts as an equivalent voltage source and we achieve the compensation of the fluctuating instantaneous power by applying a complementary harmonic to the input bridge, the voltage of this auxiliary source should always be above a low voltage limit.

The average voltage of this capacitor can be regulated by means of control strategies. However, its voltage ripple will depend on the instantaneous power it must supply to the circuit and its capacitance value.

The instantaneous power of the floating capacitor can be expressed as a differential equation.

$$p_{H_2}(t) = v_2(t)\, i_2(t) \Rightarrow p_{H_2}(t) = v_2(t)\, C_f \frac{d_{v_2}(t)}{d_t} \tag{9}$$

We also know the instantaneous power this capacitor will manage, in order to compensate the power fluctuation of twice the grid frequency,

$$p_{H_2}(t) = -P_{H_3} sin\left(2\omega_0 t - \frac{\pi}{2}\right) \tag{10}$$

where P_{H_3} is the mean power we are transmitting to the output of the converter.

Combining (9) and (10) and solving the differential equation, the voltage expression of the floating capacitor can be obtained.

$$v_2(t) = \sqrt{\bar{v_2}^2 + \frac{P_{H_3}}{C_f\, \omega_0} \sin\left(2\,\omega_0\, t\right)}, \tag{11}$$

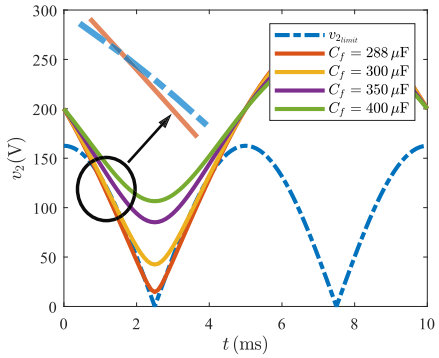

FIGURE 6. Case study example of temporal voltage waveform in the capacitor ($v_2(t)$) depending on the capacitance value (C_f), for a fixed mean voltage value of 200 V. In dotted-dashed blue line, the minimum voltage requirement defined by modulation strategy ($v_{2_{limit}}$) is drawn. The first two capacitance values (288μF, 300μF) do not meet the requirement, since in the two sides of the valley, the instantaneous voltage value is below the voltage requirement defined by the modulation strategy. The following two capacitance values are considered valid (350μF, 400μF).

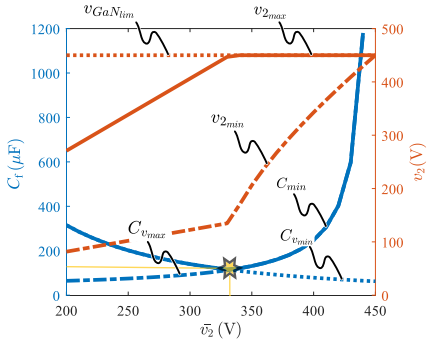

FIGURE 7. Floating capacitor (C_f) sizing analysis in the FCI-DAB taking into account both modulation requirements and semiconductors voltage limit. In dotted blue ($C_{V_{min}}$), the required minimum capacitance to fulfill the minimum voltage requirement for correct duty-cycle based modulation. In dotted-dashed blue ($C_{V_{max}}$), the required minimum capacitance for semiconductor devices maximum blocking voltage requirement. In continuous blue line (C_{min}), the overall capacitance requirement, i.e., the maximum value of the previous two requirements. In continuous red ($v_{2_{max}}$), the maximum voltage value for each $\bar{v_2}$ mean value, together with the voltage limit defined by semiconductors ($v_{GaN_{lim}}$) in dotted red and the minimum voltage value for each $\bar{v_2}$, in dotted-dashed red ($v_{2_{min}}$). The maximum and minimum voltage values are calculated for the required minimum capacitance value (C_{min}).

where $\bar{v_2}$ is the mean voltage of this floating capacitor. This floating capacitor will not provide an average power to the circuit, so that, in steady state, its average voltage can be assumed constant.

If we combine (8) and (11), we can obtain (12).

$$\sqrt{\bar{v_2}^2 + \frac{P_{H_3}}{C_f\,\omega_0}\,\sin\left(2\,\omega_0\,t\right)} \geq \frac{1}{2}V_1 \sin\left(2\omega_0 t - \frac{\pi}{2}\right) \tag{12}$$

We see that, for a given converter power, we can play with the average value $\bar{v_2}$ and the value of the ripple of this capacitor to get a correct operation of the converter. This ripple is directly related to the capacitance of the capacitor (C_f).

To better understand this, the temporal voltage waveform of the capacitor is shown in Fig. 6 for different capacitance values. Here we can see that the smaller the capacitance, the wider the voltage ripple. Thus, there is a limit where the instantaneous value of the voltage goes below the limit fixed by the modulation strategy.

To find the capacitor limit value to guarantee the modulation condition, we solve C_f from this equation, getting the following expression (13).

$$C_f \geq \frac{4\,P_{H_3}\,\sin\left(2\,\omega_0\,t\right)}{\omega_0\left(\left(V_1\,k\,\cos\left(2\,\omega_0\,t\right)\right)^2 - 4\,\bar{v_2}^2\right)} \tag{13}$$

The equation shows that the value of the minimum capacitance required is time dependent through a time window of a grid period. That is, the required minimum C_f value changes over the grid period. For this reason, to ensure the minimum capacitance value for all cases, the worst case must be chosen. For this, we will choose the maximum value that gives this equation during the grid period.

This maximum value is obtained by deriving the function and equaling zero. Although this operation has been done, it is not considered interesting to show the analytical result, since it is a long expression and difficult to interpret at a glance.

The analysis so far, however, only serves to take into account the minimum voltage that this floating capacitor must have in order to work properly with the duty-cycle modulation. However, there is also another condition and that is the maximum voltage that the semiconductors can withstand. This constraint also, of course, limits the choice of the average capacitor voltage and the maximum ripple.

In the result shown in Fig. 7, both limitations are taken into account. On the one hand, in blue, the minimum capacitance that this capacitor must have in order to fulfil the minimum (dotted blue) and maximum (dotted-dashed blue) voltage condition is shown. Since both conditions must be met, i.e. the voltage must be maintained between the aforementioned limits, the capacitor chosen must always have the higher of the two (continuous blue). At low average voltages, the most restrictive condition is the minimum voltage, that is related to the modulation condition. Above a certain voltage, we reach the voltage limit set by the semiconductors, which is where this condition begins to predominate.

The continuous red line ($v_{2_{\max}}$) shows the maximum voltage that the capacitor will have for each capacitor mean value and the capacitance value of the continuous blue line ($C_{\min}$), that is always below the voltage limit defined by semiconductors ($v_{GaN_{lim}}$) in dotted red line. The minimum voltage value that the capacitor will take for each C_f-$\bar{v_2}$ pair is drawn in dotted-dashed red.

To conclude, in the case study set, and for an average capacitor voltage of 340 V, a 150 μF capacitor would be adequate. This capacitance value is far below the mF range of standard two-stage solutions. This allows to go to ceramic or film capacitor solutions, reducing considerably the volume and losses of the DC-link components.

B. COIL DESIGN IMPROVEMENTS RELATED TO FILTER INTEGRATION

The fact of filtering the power fluctuation in the primary-side of the coil and transmitting constant power to the output brings another distinctive aspect to this circuit.

The primary-side current is the same as in the single-stage DAB | AC|-DC converter of [22], however, in the secondary-side of the coil we have a fluctuating power that can be expressed in the same way as (1), since we do not have a buffer or decoupling circuit of power. Having a passive rectifier at the output, a rectangular voltage shape is created in the AC part of this output bridge, which means a constant amplitude voltage harmonic. In this way, the power fluctuation will be reflected in the current harmonic. This means that the amplitude of the current harmonic will have an offset and a sine at twice the mains frequency, which can be expressed simplified as follows (14).

$$i'_{3,1,nofilter}(t) = I'_{3,1} + I'_{3,1}\, sin\left(2\omega_0 t - \frac{\pi}{2}\right), \tag{14}$$

where $I'_{3,1}$ is the mean amplitude value of this current harmonic at the switching frequency.

On the contrary, our system is able to filter the power fluctuation, so that the harmonic of this current in the secondary-side of the converter is constant (15).

$$i'_{3,1,filter}(t) = I'_{3,1} \tag{15}$$

It can be seen that the integration of the filter in the primary-side contributes to the reduction of the peak current in the secondary-side of the coil. This is a clear advantage in coil design, since it can be designed for less current rating, exactly, it will have to withstand currents of half of amplitude. Moreover, this higher current peaks result on both higher voltage peaks in the resonant tank and higher magnetic fields in the coil, in case of the unfiltered circuit. Thus, the power fluctuation compensation in the primary-side smooths the design requirements of the coil and resonant tank.

Considering perfect sinusoidal waves at switching frequency, the RMS current at that frequency can be considered, therefore, as follows (16), (17).

$$i'_{3,1,RMS,nofilter}(t) = \frac{I'_{3,1}}{\sqrt{2}} + \frac{I'_{3,1}}{\sqrt{2}}\, sin\left(2\omega t - \frac{\pi}{2}\right) \tag{16}$$

$$i'_{3,1,RMS,filter}(t) = \frac{I'_{3,1}}{\sqrt{2}} \tag{17}$$

With these current expressions, the power dissipated in a resistor located in the secondary-side of the coil in a time window of a switching period can be expressed in the following way (18), (19).

$$P_{R,sec,nofilter}(t) = \left[\frac{I'_{3,1}}{\sqrt{2}} + \frac{I'_{3,1}}{\sqrt{2}}\, sin\left(2\omega t - \frac{\pi}{2}\right)\right]^2 R_{sec} \tag{18}$$

$$P_{R,sec,filter}(t) = \left(\frac{I'_{3,1}}{\sqrt{2}}\right)^2 R_{sec}, \tag{19}$$

where R_{sec} can be any resistor in series in the secondary-side of the coil, for example the parasitic resistance of the resonant tank components. From this equations above we can conclude that the instantaneous conduction losses of a resistor located in the secondary-side of the coil, in the peak power transfer instant, is four times bigger in the case of a unfiltered circuit. Thus, the coil must be able to dissipate these four times bigger heat peaks.

The mean value of these expressions over a grid period (T_0) is the following (20), (21).

$$P_{R,sec,nofilter} = \frac{3}{2}\left(\frac{I'_{3,1}}{\sqrt{2}}\right)^2 R_{sec} \tag{20}$$

$$P_{R,sec,filter} = \left(\frac{I'_{3,1}}{\sqrt{2}}\right)^2 R_{sec} \tag{21}$$

This result clearly concludes other advantage that can bring the integration of the filter in the primary-side of the converter, reducing 1.5 times the mean conduction losses in the resistive part of resonant capacitors, active devices, or tracks located in the secondary-side. An improvement in conduction losses in the output battery is also obtained, which, depending on the technology, can be considerable, in addition to facilitating its cooling for proper maintenance to avoid degradation.

It has been decided to run a simulation to see what impact this may have on the system. For this purpose, the FCI-DAB and the same circuit without the integrated active filter, i.e., an |AC|-DC DAB, equivalent to [22], have been simulated.

Below is a figure of the power loss breakdown obtained from simulation (Fig. 8), where both topologies are compared.

On the one hand, it can be seen that, in the FCI-DAB, the conduction losses in the secondary-side are minimized. However, the power losses generated by including the active filter in the primary-side, compensate for the aforementioned improvement.

Although the total sum of losses is higher in the FCI-DAB, the distribution of losses is equally important. In the FCI-DAB we minimize the power losses in the secondary-side of the converter, which is the part that is on-board the vehicle, thus facilitating its cooling strategy and giving the possibility of using a natural convection cooling system.

V. CASE STUDY: EXPERIMENTAL RESULTS

A 1.5 kW proof-of-concept prototype employing Gallium Nitride (GaN) semiconductors with a blocking voltage of 600 V (IGOT60R070D1) has been used to validate the operation of the FCI-DAB. The prototype of the Fig. 9 has been tested under the conditions specified in the Table 2.

The same prototype has been used to test both the FCI-DAB and an |AC |-DC DAB. For the | AC|-DC DAB configuration

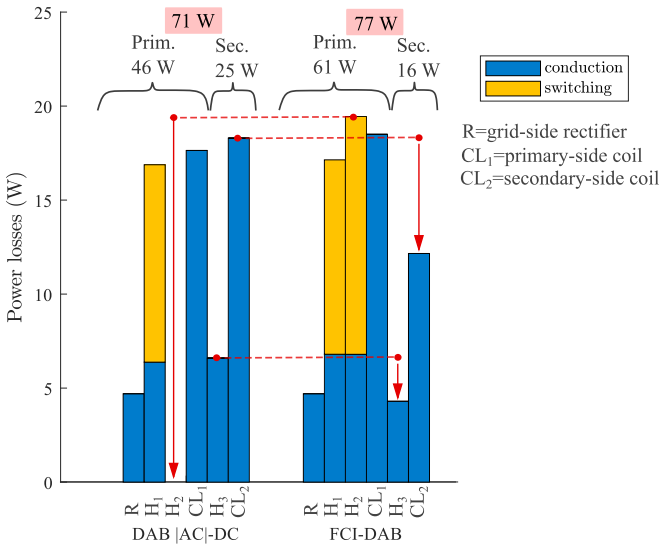

FIGURE 8. Comparison of power losses breakdown for a |AC|-DC DAB and FCI-DAB. It has been simulated for a power of 1.5 kW and a battery voltage of 200 V to emulate a discharged battery, thus better appreciating the analyzed effect.

FIGURE 9. Low-profile battery charger based on FCI-DAB. Housing, coil and power boards.

TABLE 2. FCI-DAB Case Study Specifications

Description	Value	Unit
Output power - P_{H3}	1.5	kW
Grid peak voltage- - $\hat{v}_g$	$230\sqrt{2}$	V
Grid voltage frequency -f_0	50	Hz
Output nominal voltage - V_3	400	V
Floating nominal voltage- V_2	180	V
Floating capacitor capacitance value- C_f	300	μF
Resonance frequency- f_o	85	kHz
Coupling factor- k_f	0.2-0.4	
Primary coil inductance- L_p	116	μH
Secondary coil inductance- L_s	116	μH
Primary resonant capacitor- C_p	31	nF
Secondary resonant capacitor- C_s	31	nF

the same circuit but with the filter disabled is evaluated, equivalent to [22]. This |AC|-DC DAB transmits to the secondary, and consequently to the output, the ripple of the double the grid frequency that comes from the fact of the realization of PF in the grid connection.

The fundamental experimental waveforms for both topologies under test obtained in ports 1, 2 and 3 are shown in Fig. 10.

Subfigure (a) of Fig. 10 shows the grid voltage and current (v_g, i_g), while subfigure (b) of Fig. 10 shows the output signals, from port 3. In the |AC|-DC DAB, the output current (i_3) contains the fluctuation at twice the mains frequency, in contrast to FCI-DAB, which contains a constant output current, free of low-frequency ripple.

Subfigure (c) of Fig. 10 shows the powers of the three bridges (p_{H1}, p_{H2}, p_{H3}). In the first case, the second bridge (H_2) is disabled, so its power remains at 0. The power of the first bridge (p_{H1}), the one absorbed from the grid, is a sine at twice the grid frequency, characteristic of single-phase PFC-s converters. As there is no power decoupling in the primary side of circuit, this fluctuation is transmitted to the output (p_{H3}).

However, in FCI-DAB, the second bridge (H_2) works correctly, compensating the power fluctuation of the first bridge, thus converting the sum of the two a constant power, which is transmitted to the output (p_{H3}).

Fig. 11 shows the waveforms of the HF AC part. Subfigure (a), in blue, shows in the first case (1_a), the choked voltage of the first bridge (v_1'), as the voltage of the second bridge v_2' is 0. while in the second (2_a), the same choked voltage plus the choked voltage of the second additional bridge (v_{12}'). Although this sum of voltages has a variable amplitude, the mean value of this voltage waveform in a HF time window does not change throughout the grid period.

For that reason, in subfigure (b) of Fig. 11, one can see the difference of the secondary resonant current (i_3') in both cases, which is a direct reflection of the primary voltage (v_{12}'). While in the |AC|-DC DAB (1_b), this resonant current has a variable amplitude, FCI-DAB (2_b) follows a resonant current with constant amplitude. The shape of this current reflects the power transmitted to the output, variable in one case and constant in the other.

In addition, an interesting effect has been identified in these results, which can be solved by the FCI-DAB. In DAB | AC|-DC circuit, the zero crossings of the grid voltage (v_g) result in moments of zero transferred power. The voltage induced in the primary does not reach a sufficient level to polarize the diodes of the secondary, thus not transferring power. This effect is studied in [28], [29], is related to the voltage drop on the resonant tank and depends on the difference between the resonance and switching frequency, resulting in the distortion of the grid current (i_g).

The integration of the active filter in series results in a higher induced voltage, which means that, even at zero crossings, the secondary diodes are biased. In this way, there is no

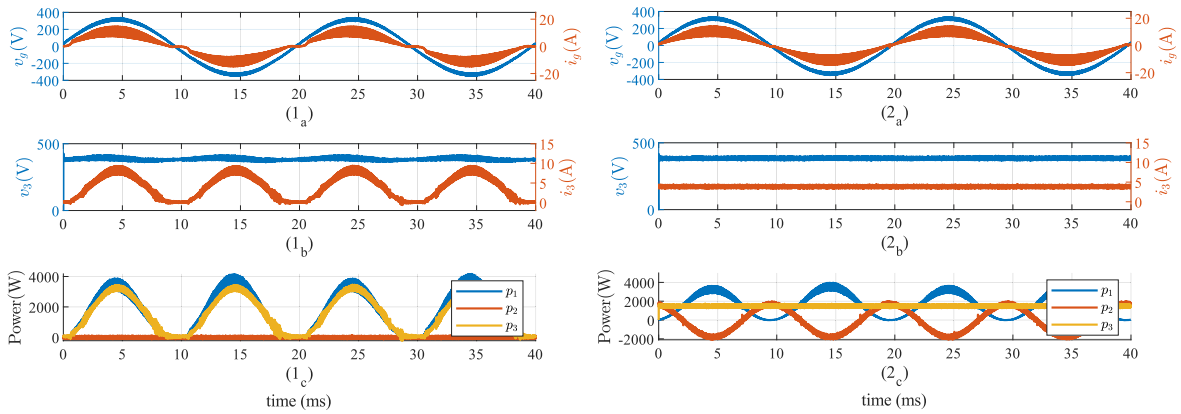

FIGURE 10. Experimental waveforms of the DAB | AC|-DC (case 1) and FCI-DAB (case 2) ports. (a) Grid-side voltage and current. (b) Output voltage and current. (c) Powers of the three ports.

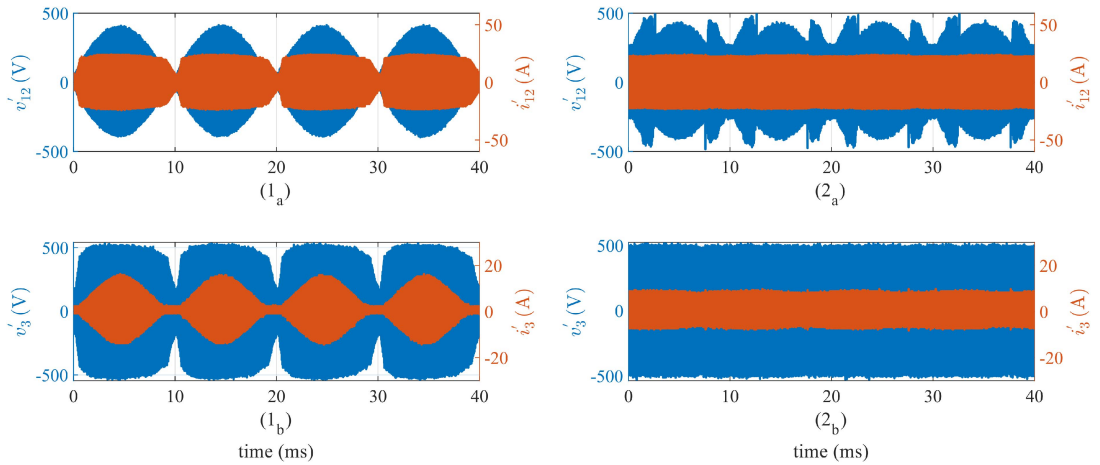

FIGURE 11. Switched experimental waveforms of the DAB | AC|-DC (case 1) and FCI-DAB (case 2) ports. (a) Primary-side voltage and current. (b) Secondary-side voltage and current.

zero transferred power and the distortion in the grid current is minimized.

In order to have a more quantitative knowledge of the fact of integrating the active filter in the circuit, FCI-DAB has been tested in laboratory at different operating points, in which the efficiency and the quality of the grid current have been measured experimentally (Fig. 12).

The integration of the converter in the circuit penalizes the efficiency of the converter by about 2% respect to DAB | AC|-DC but is still close to the state-of-the-art solutions with two stages, which is around 93% [30].

Compared to DAB | AC|-DC, the quality of the input current is improved. Previously seen in Fig. 10(a), the effect that causes the current to distort at zero-crossings is solved by the proposed filter. In this way, the THD of this grid current is significantly improved.

Following with the comparison with the DAB | AC|-DC, it is also shown the value of the square of the RMS current in the secondary for both cases. It verifies the theoretical analysis performed previously, in which it was shown that the square of the RMS current value is reduced by 1.5, which directly affects the conduction losses in the resistive part of the devices placed in the secondary side. This would also happen in state-of-the-art two-stage solutions, but here we achieve that functionality with a single-stage solution with higher power density.

Regarding the volume of the converters, [22], [23] discuss the volume reduction of the DAB | AC|-DC (named as Bidirectional Back-End PFC) compared to state-of-the-art Front-end PFC IPT solution by removing passive components. The FCI-DAB is considered a new version of the DAB | AC|-DC, which allows improvements in functionality, but still maintaining the volume reduction improvements compared to the state-of-the-art solutions, due to the low volume added by the four active devices and the low profile ceramic capacitors. In Table 3 the volume comparison of both topologies from [22], [23], together with the FCI-DAB is shown.

In addition, we have also added an active filter solution from the literature in the comparison table. This active filter is a bidirectional buck/boost [9] whose sizing for this case study has been done based on the reference [31] and the volume

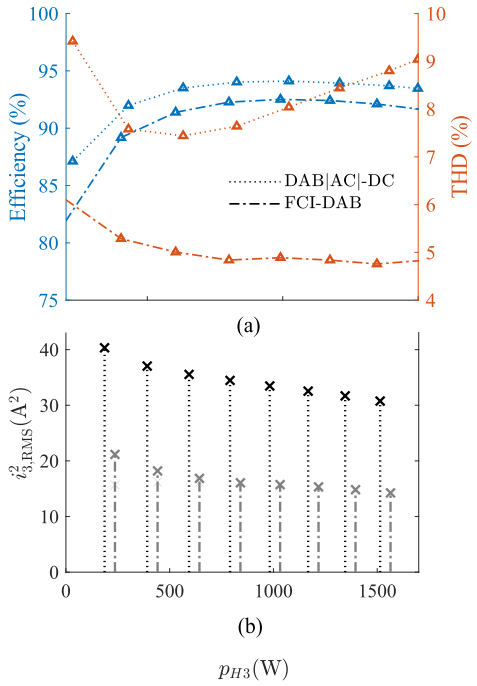

FIGURE 12. Quantitative comparison of DAB | AC|-DC and FCI-DAB. Efficiencies and THD of the input current (i_g) (a), and the square of the output RMS current (b).

TABLE 3. Comparative Table of the FCI-DAB With Other Solutions of the Literature. P.d.= Power Density and P.l.s.= Power Losses on the Secondary-Side of the IPT Converter. * in the DAB | AC|-DC* [23] the Volume and the Power Losses of the Output Storage Capacitor Have Been Taken Into Account

Converter	P (kW)	P.D. (kW/cm^3)	Eff. (%)	P.L.S. (W)
Front-end PFC IPT [23]	3.2	3.22	94.1	30
DAB|AC|-DC* [23]	3.2	3.91	94.96	39
DAB|AC|-DC w/ buck [9]	3.6	5.40	94.6	46
FCI-DAB [27]	3.6	5.73	93.34	30

of the passive components has been obtained following the procedure of [32].

It should be noted that in this case, the volume that an electrolytic capacitor would have at the output bus has been added to the DAB | AC|-DC, so that all the topologies compared in this table have the ability to filter the LF ripple. In this case, the added capacitor has been calculated for a 400 V bus and a ripple of 5%.

The FCI-DAB losses a couple of efficiency points as seen above. However, it increases the power density by 1.78 over the Front-end PFC IPT and 1.47 over a DAB | AC|-DC with a storage capacitor at the output.

If the FCI-DAB is compared to the DAB | AC|-DC with the auxiliary buck/boost, the FCI-DAB loses slightly more than 1% of efficiency. However, it has been seen that the circuit added to the DAB | AC|-DC can be reduced by about 50% compared to a bidirectional buck/boost, due to the lack of an inductance.

In addition, it can be seen that the FCI-DAB converter stands out for having less power losses on the secondary-side. This helps to lighten the equipment on-board the EV, as well as opening up possibilities for natural convection cooling.

VI. CONCLUSION

In this article, a novel active power decoupling topology named FCI DAB is introduced. The original circuit is a resonant DAB |AC|-DC converter and the active power decoupling cell is connected in series to the original circuit, in the HF AC link. The circuit is proposed as a solution for Wireless Battery Charging application for EV, however, the circuit can be used in different AC-DC applications. Moreover, the article proposes a duty-cycle modulation to fulfil properly the functions of PFC and double-grid-frequency filtering. Analysed topics has been validated by means of an ultra-compact IPT low-profile 1.5 kW battery charger, based on last generation GaN devices.

The main distinctive of this solution is the ability to get rid of the double-the-grid-frequency ripple in the primary-side of the converter, without the need of the typical large electrolytic capacitor of two-stage solutions.

In this case, the instantaneous power fluctuation is decoupled to a floating capacitor, whose capacitance value can be reduced significantly compared to the double-stage solution bus capacitor. This, apart from reducing the capacitor volume, also allows a change of technology, using, for example, film or ceramic capacitors, improving reliability and ability to handle high currents, as well as lower ESR values and a wider range of operating voltages.

Compared to single-stage solutions without decoupling filter in the primary side, FCI-DAB also allows to decrease the RMS current of the secondary-side, thus reducing the resistive conduction losses 1.5 times and allowing a coil design with lower current capability.

Compared to other state-of-the-art active decoupling filters, our solution is considered novel due to its series connection to the HF line of a modified DAB. In addition, the lack of need for a high-frequency grid-side active rectifier is considered to provide interesting benefits, such as the non-necessity of the creation of a DC bus, thus improving the efficiency of the AC-DC stage and, consequently, the overall converter efficiency. The modified DAB is connected directly after the input diode rectifier, i.e. to a rectified sine bus. In addition, it does not need an inductive component, as in the case of a bidirectional buck that works as a equivalent current source.

Finally, the active filter, apart from participating in the filtering of the floating instantaneous power, also participates in the HF operation of the converter. The circuit can be seen as a multilevel solution and assists in, for instance, achieving higher equivalent voltages or achieving ZVS over all input and output voltage ranges.

In summary, this article has presented a novel circuit that integrates a fluctuating instantaneous power decoupling circuit, together with a control proposal for correct operation and the analysis of the advantages it can provide respect to SoA

solutions. The correct functionality of the proposed circuit has been demostrated with a GaN-based IPT battery charger that was processing 1.5 kW with 93% of efficiency and PF = 0.99.

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ITZIAR ALZUGUREN (Member, IEEE) received the B.S. degree in energy engineering from the University of Mondragón, Mondragón, Spain, in 2019, and the M.Sc. degree in industrial electronics from the Universidad Politécnica de Madrid (UPM), Madrid, Spain, in 2020. Since 2020, she has been a Researcher with the Ikerlan Technology Research Centre, Mondragón, where she is currently working toward the Ph.D. degree in collaboration with the Centro de Electrónica Industrial, UPM. Her research interests include design and optimization of power converters for electrical traction, renewable energy, inductive power transfer, and energy storage applications, based on wide-bandgap devices.

ASIER GARCIA-BEDIAGA (Member, IEEE) received the B.Sc. degree in electronics from the University of Mondragón, Mondragón, Spain, in 2007, the M.Sc. degree from the Electrical, Electronics, Computer Science, Hydraulics and Telecommunications Engineering School, Toulouse, France, in 2009, and the Ph.D. degree from the Swiss Federal Institute of Technology Lausanne, Lausanne, Switzerland, in 2014. Since 2014, he has been a Researcher in power electronics area with Ikerlan Technology Research Centre, Mondragón. His research interests include wide-bandgap power electronics devices and the design, control and optimization of hard and soft-switching power converters for railway, renewable energy, storage systems, and inductive power transfer applications.

ANDER AVILA received the B.Sc. degree in industrial electronics and the M.Sc. degree in energy and power electronics from the University of Mondragón, Mondragón, Spain, in 2013 and 2015, respectively, and the Ph.D. degree in power electronics from the University of Oviedo, Gijón, Spain, in 2019. Since 2015, he has been a Researcher in power electronics area with Ikerlan Technology Research Centre, Mondragón, Spain. His research interests include wide-bandgap semiconductors and the design, control and optimization of hard and soft-switching power converters for railway, storage systems, and inductive power transfer applications.

ALEJANDRO RUJAS received the B.Sc. degree in electronics from the University of Mondragón, Mondragón, Spain, in 2004, the M.Sc. degree in electrical engineering from the Swiss Federal Institute of Technology, Lausanne, Switzerland, in 2007, and the Ph.D. degree from the University of the Basque Country UPV/EHU, Leioa, Spain, in 2023. He has been a Researcher in power electronics area with the Ikerlan Technology Research Centre, Mondragón, since 2007, and the Leader of the Power Converter Team, since 2016. His research interests include design and control of power electronics converters for electrical traction, renewable energy, aeronautics, and energy storage applications.

MIROSLAV VASIĆ (Senior Member, IEEE) was born in Serbia, in 1981. He received the B.S. degree from the School of Electrical Engineering, University of Belgrade, Belgrade, Serbia, in 2005, and the M.S. and Ph.D. degrees from Centro de Electrónica Industrial, ETSII, Universidad Politécnica de Madrid (UPM), Madrid, Spain, in 2007 and 2010, respectively. Since then he has been working with Centro de Electrónica Industrial, ETSII, UPM. Since 2019, he has been an Associate Professor with UPM. He has authored or coauthored more than 70 peer-reviewed technical papers at conferences and in IEEE journals and he advised five Ph.D. thesis and holds six patents. In the recent years great part of his research activities has been related to the research of new semiconductor devices based on GaN and their impact on power electronics. His research interests include application of power converters and their optimization. In 2012, he was the recipient of the Semikron Innovation Award for the teamwork on RF Power Amplifier with Increased Efficiency and Bandwidth. He was also the recipient of a medal from Spanish Royal Academy of Engineering as a recognition of his research trajectory in 2015 and UPM Research Projection Award for the best young Researcher at Universidad Politécnica de Madrid in 2016. He is an Associated Editor for IEEE JOURNAL OF EMERGING AND SELECTED TOPICS IN POWER ELECTRONICS and IEEE TRANSACTIONS ON VEHICULAR TECHNOLOGY. From 2021 to 2023, he was one of the co-founders of IEEE PELS TC 10- Design Methodologies and acted as the Vice-chair.