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Overvoltage Suppression in Initial Charge Control for DC Capacitor Using Multiple Leg Short-Circuits With SiC-MOSFETs in Power Converters

TOMOYUKI MANNEN [1] (Member, IEEE), AND KEIJI WADA [2] (Senior Member, IEEE)

[1]Department of Applied Physics, University of Tsukuba, Tsukuba 305-8577, Japan
[2]Department of Electrical Engineering and Computer Science, Tokyo Metropolitan University, Tokyo 191-0065, Japan

CORRESPONDING AUTHOR: TOMOYUKI MANNEN (e-mail: mannen@ieee.org)

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ABSTRACT This article proposes an improved overvoltage suppression method for the initial charge of the dc capacitor in voltage source power converters. The proposed method makes multiple short-circuits in each leg, utilizing power devices in the converter. These short-circuits discharge the dc capacitor and suppress overvoltage caused by resonant effects during the initial charge. The utilization of short durations of short-circuits multiple times in each leg reduces the power consumption in the power devices and results in a decrease in the peak junction temperature. Experimental verification using a 200-V, 5-kVA three-phase converter demonstrates that the proposed multiple short-circuit method reduces power consumption by 6% and suppresses device degradation by more than 40 times compared to the previously proposed single short-circuit method. The experimental results exhibit the effective overvoltage suppression capability of the proposed method with modest device degradation. As a result, the proposed method allows for the elimination of the initial charge circuit, leading to reductions in the size and cost of power converters, particularly in PWM rectifiers.

INDEX TERMS Electrolytic capacitorless power converter, initial charge, short circuit, SiC-MOSFET.

I. INTRODUCTION

Power density of power converters has been increasing in the recent decade [1], [2], [3]. Improvements in power semiconductor devices and the adoption of wide-band-gap (WBG) semiconductor devices have contributed to reducing power device losses and, consequently, the size of heat sinks in power converters [3]. WBG devices, such as SiC and GaN, offer the advantage of higher switching frequencies, enabling the reduction of passive components [4]. As power converters increase their power density, it becomes crucial to reduce losses not only in power devices but also in passive components, as small converters face challenges in heat dissipation [5]. However, conventional power converters usually employ electrolytic capacitors due to their high power density and low cost, but the electrolytic capacitors contain large parasitic resistors that become more remarkable, especially during high-frequency operations. Therefore, high power density converters are increasingly utilizing film or ceramic capacitors instead of electrolytic capacitors, even for the dc link capacitors [6], [7], [8].

In addition, many researchers have proposed circuit topologies and control methods aimed at reducing the capacitor and achieving electrolytic capacitorless power converters [9], [10], [11], [12], [13], [14], [15], [16], [17]. Since electrolytic capacitors have a shorter lifetime, particularly in high-temperature operations, compared to other components, they become a limiting factor in the overall lifetime of power converters [18], [19], [20]. Consequently, electrolytic capacitorless power converters are attractive because they offer increased lifetime and reduced maintenance costs. However, electrolytic capacitorless power converters require a significant reduction in

capacitance to avoid becoming bulky, as film and ceramic capacitors have lower energy density compared to electrolytic capacitors. Reference [15] proposed a control method for an interior permanent magnet (IPM) motor to achieve power factor correction (PFC) in its single-phase diode rectifier connected to the ac mains. This method utilizes the inertia of the motor to absorb power ripple from the single-phase ac power source, leading to a great reduction in passive components within power converters.

However, power converters generally include not only the main circuit but also auxiliary components such as sensors, controllers, and protection elements. Grid connection converters, for example, integrate an initial charge circuit alongside the typical auxiliary components. The conventional initial charge circuit consists of a resistor and a mechanical contactor connected in parallel, which is connected in series with the converter [21]. The resistor serves to limit the source current flowing into the dc capacitor when its voltage is lower than that of the ac mains. Once the dc capacitor voltage reaches the set value, the mechanical contactor turns on, bypassing the resistor and allowing the converter to start operation. Therefore, the resistor of the initial charge circuit is only used during the initial charge period. However, since the converter current constantly flows through the mechanical contactor, the contactor must be designed to handle the rated power of the power converters. Consequently, even with the implementation of smaller passive components and heat sinks, the initial charge circuit is a challenge for increasing converter power density.

Here, in an electrolytic capacitor-less converter, a small capacitor needs to be employed as the dc capacitor, which increases the characteristic impedance of the ac inductors and dc capacitor, thereby reducing the inrush current. Consequently, even when the converters start up without the initial charge circuit, the inrush current is less likely to cause damage to the power devices. However, due to resonance between the ac inductors and the dc capacitor, the dc capacitor voltage increases to double the source voltage. Since the rated voltage of a dc capacitor is typically designed to be lower than 150–160% of the supply voltage, an increase to double the supply voltage results in an overvoltage condition in the dc capacitor.

Reference [22] proposed a method to suppress overvoltage in the power converter by using a leg short circuit. This short circuit discharges the dc capacitor when its voltage reaches the set value, preventing the power converter from overvoltage. During the short-circuit operation, the short-circuit current is limited by both the parasitic elements of the power converter [23] and the current saturation in the power devices, resulting in a gradual discharge of the dc capacitor voltage. Many papers have reported the results of short-circuit tests [24], [25], [26], [27], [28], [29], and it has been shown that short-circuits cause significant losses and heat generation in power devices. As a result, a single short-circuit may cause destructive damage [30], and repetitive short-circuits can also lead to the degradation of power devices [31], [32]. However, the overvoltage suppression method proposed in [22] can be applied several hundred times without causing specific damage to the power devices [33]. Considering that the start-up sequence occurs only when the converter is connected to the ac mains or when the ac mains are restored after a blackout, it is assumed that the converter performs overvoltage suppression control a maximum of three times per day. However, since the designed lifetime of the power converter is longer than 10 years, it is necessary to perform the initial charge more than 10000 times over its lifetime. Therefore, the overvoltage suppression method proposed in [22] reduces the lifetime of the power converter and lacks sufficient characteristics for practical system utilization.

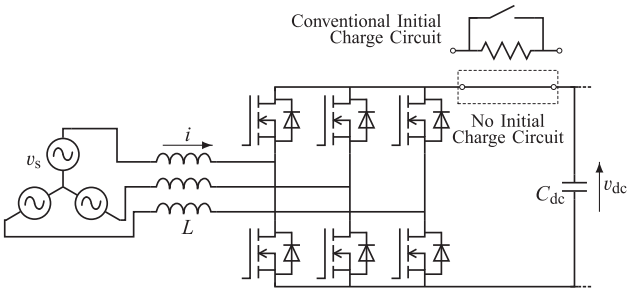

FIGURE 1. Circuit diagram of a voltage source converter.

This article proposes an improved control method for suppressing overvoltage across the dc capacitor in the power converter. The proposed method utilizes the power devices in the converter to make multiple short circuits in each leg, effectively reducing the peak voltage across the dc capacitor [34]. In this multiple short-circuit method, each short circuit has a short duration, and there are intervals between the short-circuit periods for each power device. Consequently, the maximum temperature of the power devices is lower compared to the single short-circuit method proposed in [22]. Furthermore, theoretical analysis in this article clarifies that the total power loss in the multiple short-circuit method depends on the total number of short circuits, rather than the duration of each individual short circuit. Experimental verification confirms that the multiple short-circuit method results in smaller voltage fluctuations in the dc capacitor during the initial charge and lower energy consumption in the power devices. The experimental results exhibit a good capability of the multiple short-circuit method for suppressing the peak voltage across the dc capacitor during the initial charge. Therefore, the proposed multiple short-circuit method in this article is suitable for practical utilization in power converters without compromising their lifetime.

II. CIRCUIT CONFIGURATION

Fig. 1 shows a circuit configuration of the power converter and its circuit parameters used for the following experiments are listed in Table 1. Fig. 2 also shows a picture of the experimental setup. This configuration assumes the rectifier part of an electrolytic-capacitorless power converter for a

TABLE 1. Circuit Parameters of the Converter Used in the Experiments

Source Voltage	V_s	200 V	
Source Frequency	f_s	50 Hz	
Rated Power	S	5 kVA	
AC Inductor	L	0.43 mH	(1.7%)
DC Capacitor	C_{dc}	50 μF	(0.5 ms)

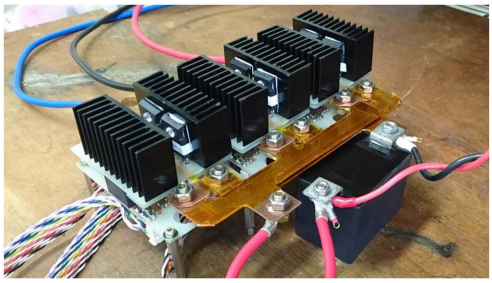

FIGURE 2. Picture of the experimental setup.

5-kVA three-phase motor drive system. The converter circuit is a three-phase voltage source converter consisting of SiC-MOSFETs (Cree C2M0040120D) and SiC-SBDs (Cree C4D10120D). The power converter has ac inductors L as a switching ripple filter on its ac side. Only a small film capacitor C_{dc} is installed on its dc side as a dc capacitor. No initial charge circuit is included in the converter, for example, a resistor and contactor. The circuit parameters are designed enough to operate the power converter at a switching frequency of 20 kHz [13], [14], [15], [16], [17].

After the converter without an initial charge circuit connects to the ac source, the dc capacitor charges through the ac inductors. If there is no control, the dc capacitor voltage finally reaches double the ac source voltage.

III. OVERVOLTAGE SUPPRESSION METHOD USING LEG SHORT-CIRCUITS IN THE CONVERTER

A. SINGLE SHORT-CIRCUIT IN EACH LEG

The overvoltage suppression method proposed in [22] performs a single short-circuit in each leg using power MOSFETs in the converter. This short circuit discharges the dc capacitor and suppresses its peak voltage.

Fig. 3 shows an operation principle of the overvoltage suppression method using a single short-circuit proposed in [22]. When the dc capacitor voltage reaches the set value in the initial charge, both upper and lower MOSFETs in one of three legs turn on simultaneously. In the leg short-circuit duration, the dc capacitor voltage steeply decreases as if a small resistor is connected to the dc capacitor in parallel. After a several-μs, the MOSFETs turn off to finish the short circuit duration and the dc capacitor voltage starts to increase again. It is important to note that the short-circuit current flows only in the dc side, involving the power devices and the dc capacitor. Therefore, the short-circuit current has no effect on the ac mains. Furthermore, since the short-circuit method is only used for the

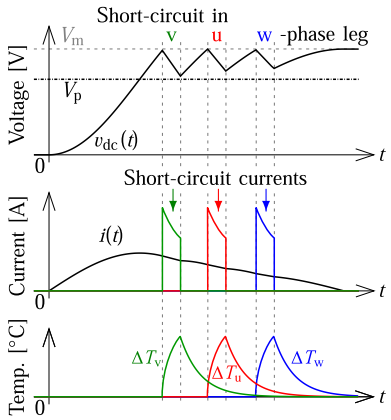

FIGURE 3. Operation principle of the overvoltage suppression method proposed in [22].

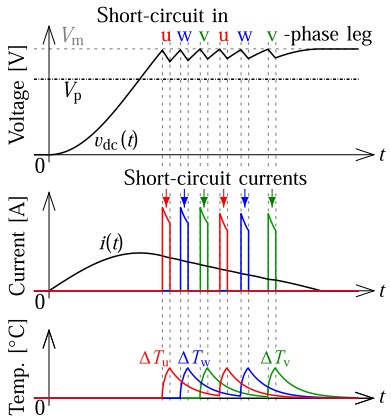

FIGURE 4. Operation principle of the overvoltage suppression method using multiple short-circuits in each leg.

initial charge, it does not disturb the normal operation, and the power loss during the short-circuits has no impact on the overall efficiency of the power converter.

The single short-circuit method for overvoltage suppression makes a short-circuit only once in each leg. In this case, each short circuit has a long time duration and consumes a large amount of energy to achieve overvoltage suppression because the total number of short-circuit is limited to no more than three, corresponding to the number of legs in the converter. The large energy consumption may potentially damage the MOSFETs and/or reduce their lifetime, even though the energy is less than the short circuit capability [33].

B. MULTIPLE SHORT-CIRCUITS IN EACH LEG

This article proposes an overvoltage suppression method using multiple short-circuits in each leg to reduce the damage to the MOSFETs. Fig. 4 shows an operation principle of the multiple short-circuits method. In this method, the short-circuit duration in each leg is split into several times. Each short-circuit has smaller energy consumption compared to the single short-circuit method due to the reduced short-circuit

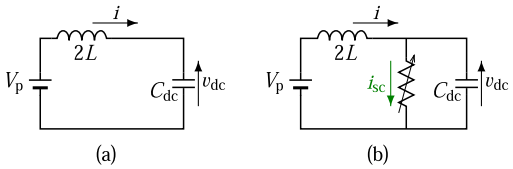

FIGURE 5. Equivalent circuit diagram of the power converter under (a) charging mode and (b) short-circuit mode.

time duration. In addition, intervals between short circuits in each leg facilitate cooling of the MOSFETs and allow them to recover their initial conditions. As a result, the multiple short-circuit method can reduce the maximum junction temperature of the MOSFETs and the thermal stress on them.

However, the multiple short-circuit method offers significant flexibility, particularly regarding the timing and duration of the short-circuits, which significantly influence energy consumption and the peak junction temperature in the MOSFETs. If the multiple short-circuit method employs inappropriate timings and durations, it may damage and/or degrade the MOSFETs, leading to a shorter lifetime. Therefore, the multiple short-circuit method requires an appropriate design of the timing and duration of short-circuits.

IV. CIRCUIT ANALYSIS OF THE INITIAL CHARGE

A. CHARGING MODE BEFORE SHORT CIRCUIT

When the ac voltage source connects to a voltage-source converter equipped with no initial charge circuit, the dc capacitor may begin to be charged from the ac voltage phases having maximum and minimum potential through the ac inductors due to the anti-parallel diodes. For the sake of simplicity, assuming that the charging time of the dc capacitor is sufficiently short, the following analysis regards the source voltage as a constant value V_p during the initial charge, which is the peak of the line-to-line ac voltage. Fig. 5 shows an equivalent circuit diagram used for the analysis. In this case, the dc capacitor C_{dc} is connected with the two ac inductors L and voltage source V_p in series during the initial charge.

The source current $i(t)$ and dc capacitor voltage $v_{dc}(t)$ are derived from the following differential equations:

$$2L\frac{d}{dt}i(t) = V_p - v_{dc}(t), \tag{1}$$

$$C_{dc}\frac{d}{dt}v_{dc}(t) = i(t). \tag{2}$$

Here, the characteristic angular frequency ω and characteristic impedance Z are defined as

$$\omega = \frac{1}{\sqrt{2LC_{dc}}}, \tag{3}$$

$$Z = \sqrt{\frac{2L}{C_{dc}}}. \tag{4}$$

The source current $i(t)$ and dc capacitor voltage $v_{dc}(t)$ are obtained by solving differential equations (1) and (2) at the same time, and are given by

$$v_{dc}(t) = A\cos(\omega t - \phi) + V_p, \tag{5}$$

$$i(t) = -\frac{1}{Z}A\sin(\omega t - \phi), \tag{6}$$

where A and ϕ are the amplitude and phase angle of the resonant. When considering an initial condition at $t = T_{init}$, A and ϕ are given by the dc capacitor voltage V_{init} and source current I_{init} as follows:

$$A = \sqrt{(V_{init} - V_p)^2 + Z^2 I_{init}^2}, \tag{7}$$

$$\phi = \omega\frac{T_{init}}{2} + \operatorname{atan}\frac{(V_{init} - V_p)\sin\frac{\omega T_{init}}{2} + ZI_{init}\cos\frac{\omega T_{init}}{2}}{(V_{init} - V_p)\cos\frac{\omega T_{init}}{2} - ZI_{init}\sin\frac{\omega T_{init}}{2}}. \tag{8}$$

Note that the source current $i(t)$ should be positive during the initial charge due to diodes in the converter.

When the voltage source connects to the converter at $t = 0$, both the dc capacitor voltage and source current at $t = 0$, V_0 and I_0, are zero due to the initial charge. Therefore, the amplitude and phase angle at $t = 0$ are $A_0 = V_p$ and $\phi_0 = \pi$, respectively, which are derived from $V_{init} = V_0 = 0$, $I_{init} = I_0 = 0$, and $T_{init} = T_0 = 0$. After that, the dc capacitor voltage and source current increase according to (5) and (6). The source current takes its peak value $I_{max} = V_p/Z$ at $t = \pi/2\omega$, and the current charges the dc capacitor until the current becomes zero. As a result, the dc capacitor voltage finally reaches $V_{max} = V_p + A$. For example, if the converter operates without any initial charge control, the maximum dc capacitor voltage is $V_{max} = 2V_p$. Therefore, it is necessary to reduce the amplitude A in order to suppress the maximum dc capacitor voltage.

B. CHARGING MODE AFTER SHORT CIRCUITS

After the short-circuit duration, the circuit immediately switches to the charge mode and the dc capacitor voltage and source current follow (5) and (6) again, respectively. Here, the dc capacitor voltage and the source current at the end of the n-th short-circuit duration $t = T_{ne}$ are defined as V_{ne} and I_{ne}, respectively. After the n-th short-circuit duration, the dc capacitor voltage v_{dcn} and source current i_n are given by

$$v_{dcn}(t) = A_{ne}\cos(\omega t - \phi_{ne}) + V_p, \tag{9}$$

$$i_n(t) = -A_{ne}\frac{1}{Z}\sin(\omega t - \phi_{ne}), \tag{10}$$

where the amplitude A_{ne} and phase angle ϕ_{ne} are calculated as follows:

$$A_{ne} = \sqrt{(V_{ne} - V_p)^2 + Z^2 I_{ne}^2}, \tag{11}$$

$$\phi_{ne} = \omega\frac{T_{ne}}{2} + \operatorname{atan}\frac{(V_{ne} - V_p)\sin\frac{\omega T_{ne}}{2} + ZI_{ne}\cos\frac{\omega T_{ne}}{2}}{(V_{ne} - V_p)\cos\frac{\omega T_{ne}}{2} - ZI_{ne}\sin\frac{\omega T_{ne}}{2}}. \tag{12}$$

C. MODELING OF THE SHORT-CIRCUIT CURRENT WAVEFORM

The proposed initial charge method uses short-circuit operation for discharging the dc capacitor. However, the short-circuit current waveform has various shapes which depend on the power devices, applied voltage, stray inductance, and

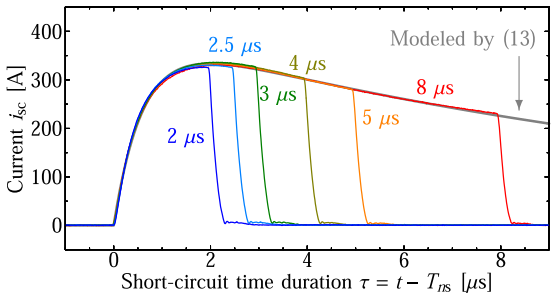

FIGURE 6. Measured short-circuit current waveforms of the proposed method in various time durations and a modeled short-circuit waveform using (13).

so on. The dependence on power devices is not solely based on the internal structure and chip size, but also on individual differences. Since it is quite difficult to analytically represent the short-circuit waveforms, this article uses two approximate functions based on the waveforms measured in experiments for the following analysis.

Fig. 6 shows measured short-circuit waveforms during the initial charge. When both the gates turn on at $t = T_{ns}$, the short-circuit current starts to increase slowly due to stray inductance in the circuit. After several-μs, the short-circuit takes its peak and starts to decrease slowly, because large power loss in the devices heats themselves and increases their equivalent resistance. After the gates turn off at $t = T_{no}$, the short-circuit current steeply decreases and reaches zero at $t = T_{ne}$.

The applied voltage for the devices can be assumed as a constant during the short-circuit operation because the short-circuit always starts at the same dc-capacitor voltage, $v_{dc} = V_m$, and the dc-capacitor voltage slightly decreases in the proposed method. Therefore, it can be assumed that the short-circuit current waveform in the proposed method always follow the same line while both the gates are on.

This article assumes that the short-circuit waveform consists of two parts: an exponential function while the gates are on and a quadratic function after the gates turn off. This article employs

$$i_{sc}(t) = \begin{cases} K_R\left(1-e^{-K_L(t-T_{ns})}\right)\left(e^{-K_T(t-T_{ns})}+K_S\right) & (T_{ns} \le t < T_{no}) \\ K_O\,(t-T_{ne})^2 & (T_{no} \le t < T_{ne}) \\ 0 & (\text{others}) \end{cases} \tag{13}$$

as a current waveform model during a short-circuit, where the static parameters K_X decide the short-circuit current waveform. K_R is related to the equivalent resistance of power devices during the short-circuit under a constant temperature. K_L is a coefficient caused by stray inductance in the circuit. K_T is from the temperature change in power devices caused by the power loss in the short-circuit. K_S shows a factor of the short-circuit current in steady states, if possible. K_O is related to the turn-off speed of the power devices. This article employs the static parameters K_X extracted from and fitted to the short-circuit waveforms measured at $v_{dc} = V_m$ in the power converter in order to minimize the error.

Since the short-circuit current i_{sc} should be a continuous function, the turn-off duration $T_{ne} - T_{no}$ is calculated by using K_O as follows:

$$T_{ne} - T_{no} = \sqrt{\frac{I_{scno}}{K_O}}, \tag{14}$$

where I_{scno} is the short-circuit current at $t = T_{no}$, $I_{scno} = i_{sc}(T_{no})$.

D. IN THE SHORT-CIRCUIT DURATION

The source current and dc capacitor voltage during the short-circuit duration, $i(t)$ and $v_{dc}(t)$, are derived from the following differential equations:

$$2\,L\frac{d}{dt}i_n(t) = V_p - v_{dcn}(t), \tag{15}$$

$$C_{dc}\frac{d}{dt}v_{dcn}(t) = i_n(t) - i_{sc}(t). \tag{16}$$

Substituting (13) into (15) and (16), the current and voltage while the gates are on are given by

$$i_{ns}(\tau) = A_{ns}\sin(\omega\tau + \phi_{ns}) + K_S K_R\left(1 - \frac{\omega^2 e^{-K_L\tau}}{\omega^2 + K_L^2}\right) + K_R\omega^2 e^{-K_T\tau}\left(\frac{1}{\omega^2 + K_T^2} - \frac{e^{-K_L\tau}}{\omega^2 + (K_T + K_L)^2}\right), \tag{17}$$

$$v_{dcns}(\tau) = -A_{ns}Z\cos(\omega\tau + \phi_{ns}) - K_R Z\omega\frac{(K_T + K_L)e^{-(K_L+K_T)\tau}}{\omega^2 + (K_T + K_L)^2} + K_R Z\omega\left(\frac{K_T e^{-K_T\tau}}{\omega^2 + K_T^2} - \frac{K_L K_S e^{-K_L\tau}}{\omega^2 + K_L^2}\right) + V_p, \tag{18}$$

where τ is the time since the short-circuit started, $\tau = t - T_{ns}$. Here, I_{ns} and V_{ns} represent the current and voltage when the n-th short-circuit starts at $\tau = 0$. The amplitude and phase angle of the resonant at $\tau = 0$, A_{ns} and ϕ_{ns}, are given by

$$A_{ns} = \sqrt{\left\{-\frac{(K_T+K_L)K_R\omega}{\omega^2+(K_T+K_L)^2} + \frac{K_T K_R\omega}{\omega^2+K_T^2} - \frac{K_L K_S K_R\omega}{\omega^2+K_L^2} + \frac{V_p - V_{ns}}{Z}\right\}^2 + \left\{-\frac{(2K_T+K_L)K_L K_R\omega^2}{(\omega^2+K_T^2)\{\omega^2+(K_T+K_L)^2\}} - \frac{K_L^2 K_S K_R}{\omega^2+K_L^2} + I_{ns}\right\}^2}, \tag{19}$$

$$\phi_{ns} = \operatorname{atan}\frac{-\frac{(2K_T+K_L)K_L K_R\omega^2}{(\omega^2+K_T^2)\{\omega^2+(K_T+K_L)^2\}} - \frac{K_L^2 K_S K_R}{\omega^2+K_L^2} + I_{ns}}{-\frac{(K_T+K_L)K_R\omega}{\omega^2+(K_T+K_L)^2} + \frac{K_T K_R\omega}{\omega^2+K_T^2} - \frac{K_L K_S K_R\omega}{\omega^2+K_L^2} + \frac{V_p - V_{ns}}{Z}}. \tag{20}$$

After the gates turn off at $\tau = T_{no} - T_{ns}$, the short-circuit current decreases steeply to zero. The source current and dc

capacitor voltage are also given by

$$i_{no}(\tau') = \left(\frac{2K_O}{\omega}\sqrt{\frac{I_{scno}}{K_O}} + \frac{V_p - V_{no}}{Z}\right)\sin\omega\tau' + \left(\frac{2K_O}{\omega^2} + I_{no} - I_{scno}\right)\cos\omega\tau' + K_O\left(\tau' - \sqrt{\frac{I_{scno}}{K_O}}\right)^2 - \frac{2K_O}{\omega^2}, \quad (21)$$

$$v_{dcno}(\tau') = Z\left(\frac{2K_O}{\omega^2} + I_{no} - I_{scno}\right)\sin\omega\tau' - Z\left(\frac{2K_O}{\omega}\sqrt{\frac{I_{scno}}{K_O}} + \frac{V_p - V_{no}}{Z}\right)\cos\omega\tau' - Z\frac{2K_O}{\omega}\left(\tau' - \sqrt{\frac{I_{scno}}{K_O}}\right) + V_p, \quad (22)$$

where τ' is the time since the gates turned off, $\tau' = t - T_{no}$, and v_{no} and I_{no} are the dc capacitor voltage and source current at $\tau' = 0$, $V_{no} = v_{dcns}(T_{no} - T_{ns})$ and $I_{no} = i_{ns}(T_{no} - T_{ns})$, respectively. When the short-circuit current reaches zero, the dc capacitor voltage starts to increase again. The end value of the current and voltage in the n-th short-circuit duration are calculated as

$$I_{ne} = i_{no}\left(\sqrt{\frac{I_{scno}}{K_O}}\right) = \left(\frac{2K_O}{\omega}\sqrt{\frac{I_{scno}}{K_O}} + \frac{V_p - V_{no}}{Z}\right)\sin\left(\omega\sqrt{\frac{I_{scno}}{K_O}}\right) + \left(\frac{2K_O}{\omega^2} + I_{no} - I_{scno}\right)\cos\left(\omega\sqrt{\frac{I_{scno}}{K_O}}\right) - \frac{2K_O}{\omega^2}, \quad (23)$$

$$V_{ne} = v_{dcno}\left(\sqrt{\frac{I_{scno}}{K_O}}\right) = Z\left(\frac{2K_O}{\omega^2} + I_{no} - I_{scno}\right)\sin\left(\omega\sqrt{\frac{I_{scno}}{K_O}}\right) - Z\left(\frac{2K_O}{\omega}\sqrt{\frac{I_{scno}}{K_O}} + \frac{V_p - V_{no}}{Z}\right)\cos\left(\omega\sqrt{\frac{I_{scno}}{K_O}}\right) + V_p. \quad (24)$$

Therefore, the amplitude and phase angle of the resonant after the n-th short circuit, A_{ne} and ϕ_{ne}, are derived from substituting (23) and (24) into (11) and (12). Only the short-circuit duration can change the amplitude of the resonant and suppress the peak voltage of the dc capacitor voltage.

E. ANALYSIS-BASED OPERATING WAVEFORMS IN THE INITIAL CHARGE METHOD

Fig. 7 shows calculated waveforms of the resonant amplitude, the dc capacitor voltage, and the source current during the initial charge using a multiple short-circuit method. Fig. 8 is the time-expanded waveforms of Fig. 7, which focuses on short-circuit durations. At the start of the short-circuit durations, around T_{ns}, the dc capacitor voltage slightly increases because the source current is still larger than the short-circuit current due to its slow increase. And then, the dc capacitor voltage decreases until the gates of the inverter are turned off. After that the short-circuit current steeply decreases and the dc capacitor voltage increases again. Each short-circuit duration decrease the resonant amplitude and dc capacitor voltage. On the other hand, the source current exhibits a more gradual slope after the short circuit than before, which means that the resonant takes longer to complete. This is because the applied voltage to the ac-side inductors becomes smaller according to the suppression in the dc capacitor voltage.

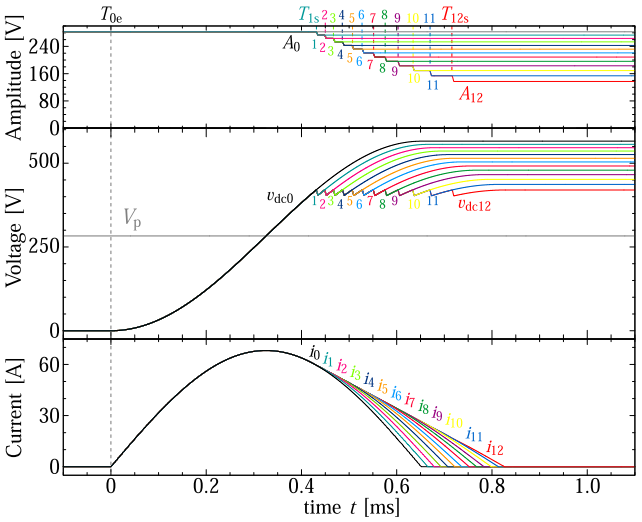

FIGURE 7. Calculated values of the amplitude A, the dc capacitor voltage v_{dc}, and the source current i.

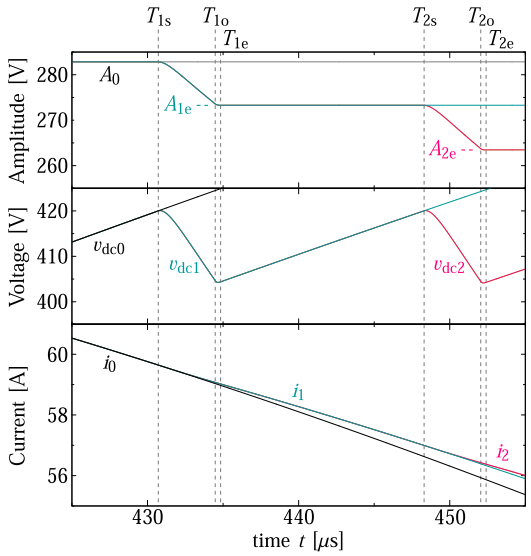

FIGURE 8. Time-expanded waveforms of Fig. 7 focusing on the first short-circuit.

In the single short-circuit proposed in [22], each leg can make only one short-circuit and only three short-circuits should suppress the peak voltage. As a result, each short-circuit causes large power consumption in the devices and damages them. On the other hand, the multiple short-circuit method proposed in this article can make many short-circuits in each leg, which may reduce the power consumption in each short-circuit and damage in each device. However, the multiple short-circuit method increases the degree of freedom such as the number of short-circuits, duration of each short-circuit, and start timing of them, compared with the single short-circuit, method which has only three variables for controlling the initial charge behavior.

V. CONTROL STRATEGIES OF THE MULTIPLE SHORT-CIRCUIT METHOD

A. POWER LOSS IN THE INITIAL CHARGE

The voltage source provides energy to the dc capacitor through the initial charge current. Since the analysis in this article assumes the source voltage is a constant during the initial charge, the total amount of provided energy from the source, W_s, is given by

$$W_s = \int_0^{T_f} V_p i(t) \mathrm{d}t, \tag{25}$$

where T_f is the finishing time of the initial charge. The source current $i(t)$ reaches zero at $t = T_f$. The stored energy after the initial charge, W_f, is calculated as

$$W_f = \tfrac{1}{2} C_{dc} V_f^2, \tag{26}$$

where V_f represents the dc capacitor voltage reached after finishing the initial charge. The energy difference between W_s and W_f is considered to be consumed in the power devices during the short-circuit duration. The final voltage V_f is usually set to the peak voltage V_m to reduce unnecessary energy consumption. The stored energy in the dc capacitor, W_f, depends on the peak voltage V_m and remains constant for each peak voltage. Therefore, the provided energy from the voltage source, W_s, needs to be reduced to minimize the consumed energy.

Equation (25) indicates that if the source current $i(t)$ decreases rapidly and for a short time to reach zero, the energy provided from the voltage source, W_s, will be reduced. Assuming that the dc capacitor voltage can be fixed at the peak voltage V_m once it reaches that level, the source current decreases linearly at the maximum rate of decrease and achieves the minimum finishing time T_f for a certain peak voltage. In this case, the minimum value of the energy provided from the voltage source, W_s, is given by

$$\begin{aligned} W_s &= V_p \left\{ \int_0^{T_{1s}} i_0(t)\,\mathrm{d}t + \int_{T_{1s}}^{T_f} \left(I_{1s} + \tfrac{(V_p - V_m)(t - T_{1s})}{2L} \right) \mathrm{d}t \right\} \\ &= \frac{C_{dc} V_p V_m^2}{2(V_m - V_p)}. \end{aligned} \tag{27}$$

Therefore, the energy consumption in the power devices is theoretically higher than the value given by

$$W_{loss} = W_s - W_f = \frac{C_{dc} V_m^2 (2V_p - V_m)}{2(V_m - V_p)}. \tag{28}$$

Fig. 9 shows the minimum energy consumption at a certain peak voltage. As the peak voltage increases, the energy consumption reduces. However, it is impossible for v_{dc} to keep the peak voltage V_p because the short-circuit waveforms depend on the power devices. The achievable minimum energy consumption is slightly larger than (28) as follows.

The source voltage is assumed to be a constant, V_p, the provided energy W_s is calculated as

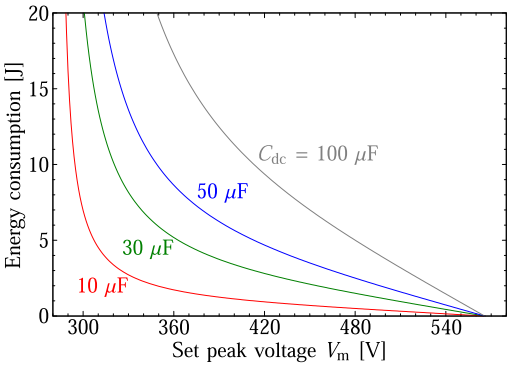

FIGURE 9. Theoretical minimum energy consumption in the short-circuits during the initial charge.

$$\begin{aligned} W_s &= V_p \int i(t)\mathrm{d}t \\ &= \left\{ \sum_{n=1}^{N} \left(\int_{T_{(n-1)e}}^{T_{ns}} i_{(n-1)}(t)\,\mathrm{d}t + \int_{T_{ns}}^{T_{no}} i_{ns}(t)\,\mathrm{d}t + \int_{T_{no}}^{T_{ne}} i_{no}(t)\,\mathrm{d}t \right) \right. \\ &\quad \left. + \int_{T_{Ne}}^{T_f} i_N(t)\,\mathrm{d}t \right\} V_p, \end{aligned} \tag{29}$$

where N is the total number of the short-circuits. Note that T_{0e} can be regarded as $T_{0e} = 0$, the initial condition of the initial charge. Equations (9)–(12) and (17)–(24) indicate that all the current functions, $i_n(t)$, $i_{ns}(t)$, and $i_{no}(t)$, are functions of each other. T_{ns} is determined from the source current and dc capacitor voltage at $t = T_{(n-1)e}$, $i_n(T_{(n-1)e})$ and $v_{dcn}(T_{(n-1)e})$, and the set value to start a short-circuit, V_m. T_{ne} is derived from the time duration and turn-off characteristic of short-circuits. Therefore, only the time duration of both the gates turned on determines the behavior of the proposed multiple short-circuit method.

B. TOTAL NUMBER AND TIME DURATION OF SHORT CIRCUITS

This article discusses the following four strategies for making short-circuits:

(i) Adjust the short-circuit duration individually to achieve the same dc capacitor voltage ripple each time.
(ii) Optimize the duration of each short-circuit individually to minimize the total losses during the short-circuits.
(iii) Minimize the losses by using the same short-circuit duration for every three short-circuits.
(iv) Minimize the losses by setting the same fixed duration for all short-circuits.

Fig. 10 shows the calculated short-circuit time duration for each strategy. Since analytical optimization of the multiple short-circuit method is quite difficult due to the number of variables, the calculated time durations are based on numerical optimization to minimize power loss in the devices at a certain maximum and final voltage, 420 V. In the optimized

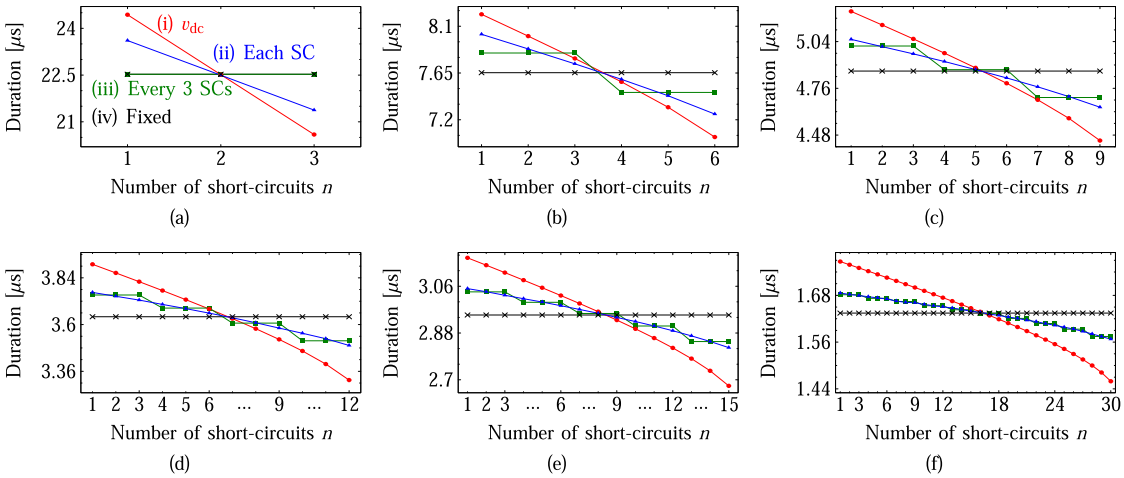

FIGURE 10. Calculated time duration of each short-circuit when the total number of short-circuits is set to (a) 3, (b) 6, (c) 9, (d) 12, (e) 15, and (f) 30.

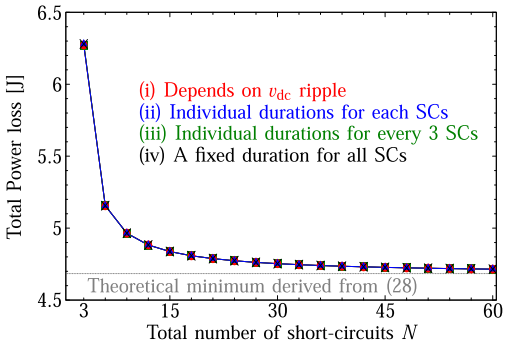

FIGURE 11. Calculated total power loss of the initial charge with the proposed multiple short-circuit method.

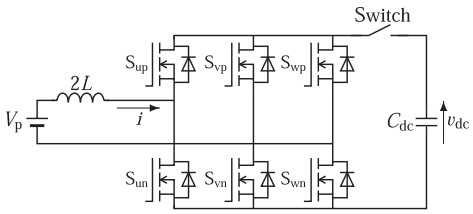

FIGURE 12. Circuit diagram used in the experimental verification.

results, the short circuits start when the capacitor voltage reaches the maximum voltage and end at the optimized time durations for the four strategies.

When short-circuit time is set for each, short-circuit time becomes shorter as the short-circuit order increases. The total number of short-circuits also affects the time duration, with the higher the number of short circuits, the shorter the duration of each short-circuit. Note that the power loss for each short circuit depends on the duration of the short circuit, and a short circuit occurs every three times in each leg. For example, the first, fourth, and seventh short circuits occur in the u-phase leg. As a result, individual duration strategies may result in unbalanced power losses between devices.

Fig. 11 shows the total power loss in the devices during the initial charge. As the number of total short-circuits increases, the total power loss decreases and approaches the theoretical minimum. On the other hand, at a certain number of total short-circuits, the power losses for each strategy are almost the same value. Therefore, it is sufficient to consider and increase only the total number of short-circuits in order to reduce the overall power loss. Since the proposed method can be implemented in the converter without any additional sensors and components, it is easy to employ a fixed short-circuit duration, such as 3 μs for example, and trigger short-circuits when the dc capacitor voltage reaches the set voltage, using a sensor equipped for dc capacitor voltage control.

VI. EXPERIMENTAL VERIFICATION

Fig. 12 shows the experimental circuit configuration for the initial charge. Since the initial charge needs to be tested under the most critical condition, the initial charge always starts at the same phase angle as the ac voltage, which corresponds to the maximum line-to-line voltage. Considering that the output voltage of one phase is zero at this angle, the initial charge current flows through the two phases. In the following experiments, a dc voltage power supply is connected to the ac terminals of the u-phase and w-phase instead of using a three-phase ac power source. The voltage source was set to 283 V, which corresponds to the maximum line-to-line voltage of the ac 200 V. The v-phase leg terminal is excluded from the connection with the voltage source because the initial charge current flows through the other two terminals at this angle. The experiments employed a simple gate driver without any protection for each of the devices to make short-circuits. If the circuit employs gate drivers with any protections, such as DESAT, its protection time constant should be set longer than the short-circuit time duration. An ac inductor $2L$ is installed on the ac side instead of the three-phase ac inductor L. Furthermore, a switch on the dc side controls the connection between the dc capacitor and the power supply, similar to a

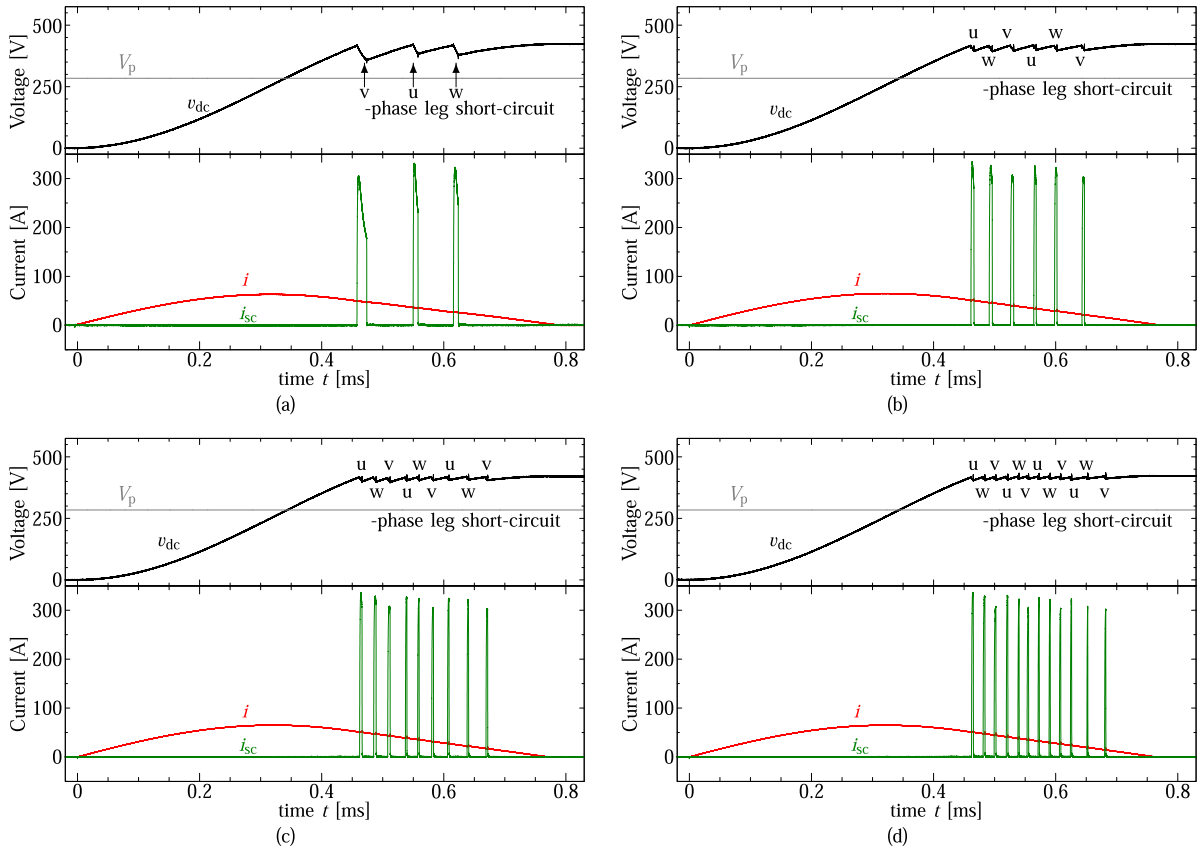

FIGURE 13. Experimental waveforms during the initial charge for the dc capacitor with the overvoltage suppression method when each leg has short-circuits (a) once, (b) twice, (d) three times, and (d) four times, respectively.

circuit breaker on the ac side. The switch turns on at $t = 0$ and starts the initial charge by connecting the dc capacitor to the power supply.

Fig. 13 shows experimental waveforms of the initial charge for the dc capacitor using the overvoltage suppression method. The short-circuit durations were set to achieve the same final voltage based on the number of short-circuits. Fig. 13(a) represents a measurement obtained with the single short-circuit method. In this method, each leg experienced a long-duration short-circuit only once, resulting in a total of three short-circuits during the initial charge. After starting the first short circuit, the peak of the short circuit current reached 332 A, and the dc capacitor voltage fluctuates between 420 V and 355 V. The source current showed no spikes during the short circuit, confirming that the short circuit did not affect the ac mains. Eventually, the source current i becomes 0, and the dc capacitor voltage reached 420 V at $t = 0.79$ ms. Despite the large current flowing through the dc capacitor, the capacitor did not heat up due to the small equivalent series resistance (ESR) in the film capacitor and the short time duration of the short-circuit.

Figs. 13(b)–(d) show experimental waveforms of the proposed overvoltage suppression method using multiple short circuits. Each leg experienced short short-circuits 2–4 times, resulting in a total of 6, 9, and 12 short-circuits in Figs. 13(b)–(d), respectively. The duration of each short circuit was adjusted to achieve a final voltage of 420 V, rather than relying on the calculated time, due to the presence of parasitic resistance in the circuit components and variations in individual SiC-MOSFET parameters.

In the first short-circuit of Figs. 13(b), the proposed method makes a short-circuit in the u-phase leg. The peak of the short-circuit current was 334 A and the dc capacitor discharged to 394 V. Subsequently, short-circuits occurred one by one in the w- and v-phase legs, leading to a discharge of the dc capacitor again and again. And then, the proposed method makes the second short-circuit in the u-phase leg. The peak current during the second short circuit was 326 A, which is lower than that in the first short-circuit due to the higher junction temperature in the MOSFET. In this case, the initial charge was completed at $t = 0.77$ ms. The dc capacitor voltage fluctuation was reduced to 27 V, ranging between 420 V and 393 V.

Similarly, in Figs. 13(c) and (d), the peak short-circuit current in each leg gradually decreased. The initial charge completed at $t = 0.77$ ms in Fig. 13(c) and $t = 0.76$ ms in Fig. 13(d). The voltage fluctuation was 24 V in Fig. 13(c) and 18 V in Fig. 13(d), respectively. Increasing the number of short-circuits in each leg results in a shorter initial charge duration and smaller voltage fluctuation.

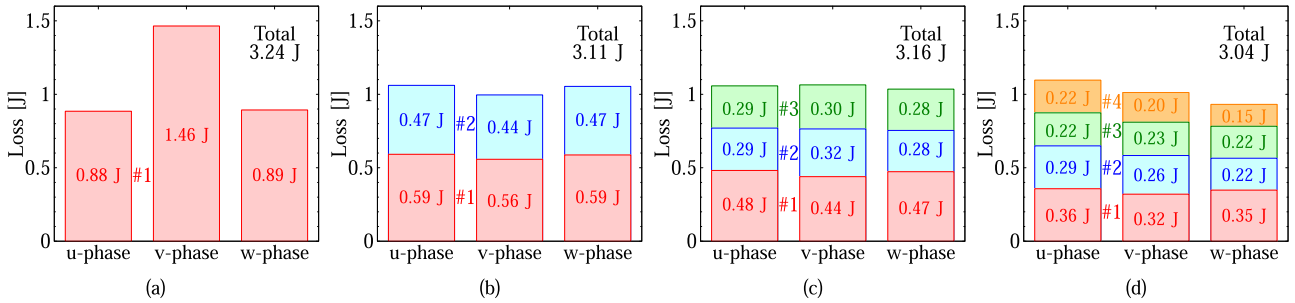

FIGURE 14. Measured power loss during each short-circuit duration in the initial charge when each leg has short-circuits (a) once, (b) twice, (d) three times, and (d) four times, respectively.

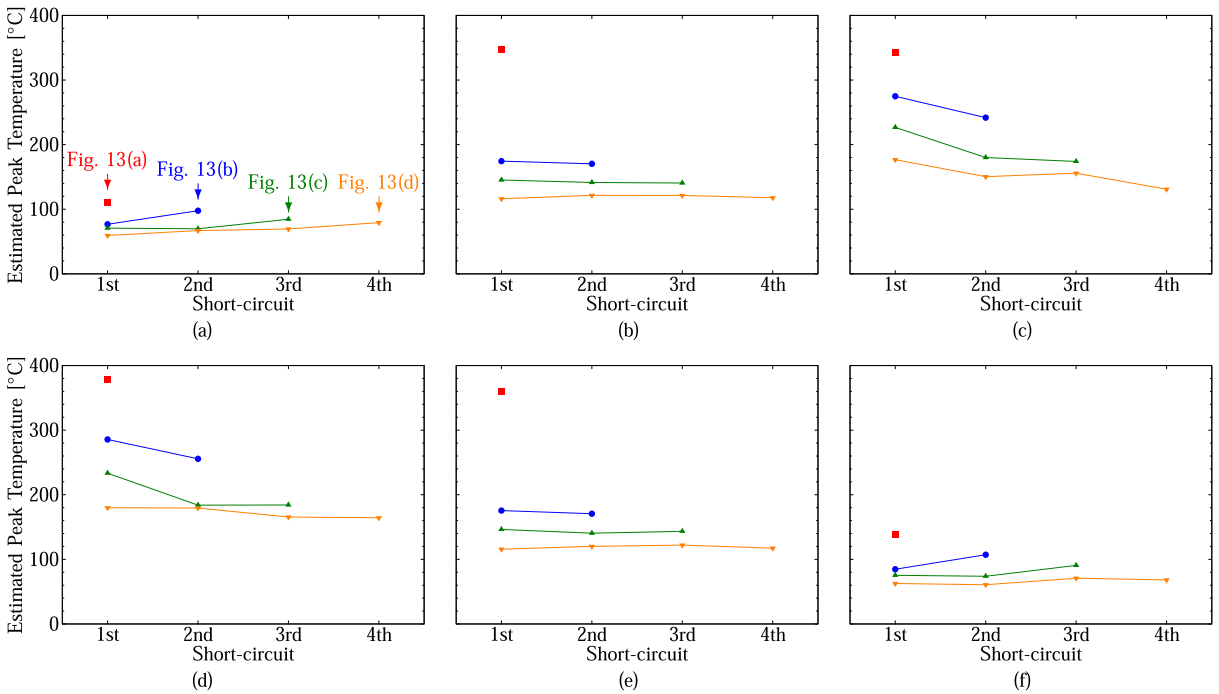

FIGURE 15. Estimated peak junction temperature in each short-circuit duration of MOSFETs used as the switch (a) S_{up}, (b) S_{vp}, (c) S_{wp}, (d) S_{un}, (e) S_{vn}, and (f) S_{wn}.

Fig. 14 shows the measured energy consumption under different conditions. Fig. 14(a) is in a case of using the single short-circuit method. During the short-circuit, the energy consumption was 0.9 J in the u- and w-phase legs, 1.5 J in the v-phase leg, and 3.2 J in total. The short-circuit capability of the SiC-MOSFETs used in the experiments is 1.4 J [24]. Therefore, the energy consumption in the u- and w-phase legs during the short-circuit is lower than the capability. Similarly, in the v-phase leg, the energy consumption during the short-circuit is also lower than the capability because the energy consumption is divided between both the lower and upper devices.

Figs. 14(b)–(d) represent the measured results using the overvoltage suppression method with multiple short-circuits. The energy consumption in each leg is divided into 2–4 sections corresponding to each short-circuit duration, similar to those shown in Fig. 10. The maximum energy consumption in each short-circuit duration was reduced to 0.4 J when using 4 short-circuits in each leg, as seen in Fig. 14(d). By increasing the number of the short-circuits in each leg, the energy consumption in each short-circuit duration decreases. The total energy consumption of the proposed method was slightly reduced to 3.0 J in Fig. 14(d). Therefore, as the number of short circuits increases, the total energy consumption decreases similarly to Fig. 11. However, the energy consumption in each device is still approaching the short-circuit capability, resulting in a high junction temperature.

Fig. 15 shows the estimated peak junction temperature of the MOSFETs for each short-circuit duration. Direct measurement of the junction temperature poses a challenge due to the short duration of the short circuit, typically lasting only several-μs [35], [36], [37]. In Fig. 15, the junction

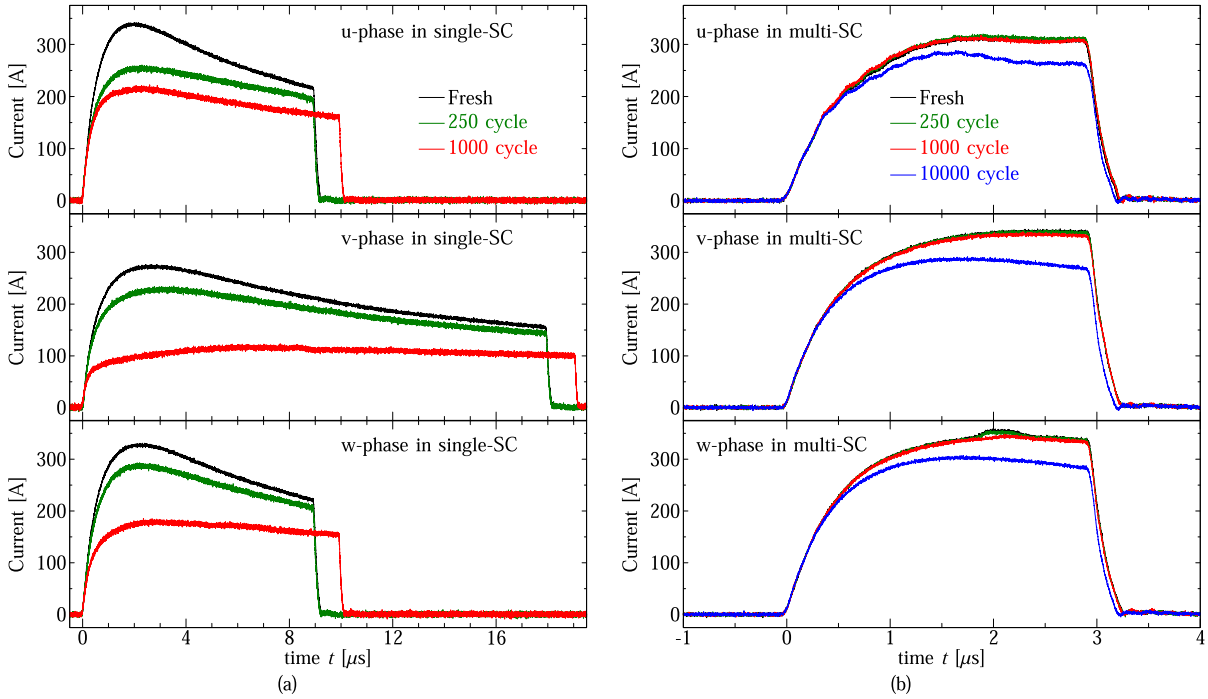

FIGURE 16. Short-circuit current waveforms of the overvoltage suppression method using new devices and after several cycles of operation using (a) the single short-circuit method and (b) the multiple short-circuit method with four short-circuits in a leg.

temperature was estimated through SPICE simulation using the manufacturer-provided SiC-MOSFET device model from Cree. The simulation replicated the same short-circuit duration, timing, and conditions as the experiments.

Figs. 15(a) and (d) show the temperature of the upper and lower MOSFET in the u-phase. The lower MOSFET exhibits a higher junction temperature compared to the upper MOSFET, attributed to its larger device current and the majority of the dc capacitor voltage being applied to the lower MOSFET in the u-phase. Similarly, the upper MOSFET has a higher junction temperature than the lower MOSFET in the w-phase. On the other hand, Figs. 15(b) and (e) show the temperature in v-phase, where the temperature of the upper and lower MOSFETs are balanced due to the balanced voltage across and the same current through the upper and lower devices.

The maximum junction temperature in each case was 378 °C, 286 °C, 233 °C, or 180 °C in Figs. 14(a)–(d), respectively. By increasing the number of short-circuits in each leg, the peak junction temperature in each short-circuit duration was reduced. Additionally, a further increase in the number of short-circuits in a leg may suppress the peak junction temperature to lower than 175 °C. The multiple short-circuit method can effectively suppress the peak junction temperature due to both the small energy consumption in each short-circuit duration and the intervals between the short-circuits. Focusing on the u-phase leg, the total energy consumption in the single short-circuit method was 0.9 J, while it was 1.1 J in the 4 short-circuits method. Despite the higher energy consumption in the multiple short-circuit method compared to the single short-circuit method, the peak junction temperature in the multiple short-circuit method is lower. Even though the energy consumption in the multiple short-circuit method is larger than that in the single short-circuit method, the peak junction temperature in the multiple short-circuit method is lower than that in the single short-circuit method. Even though the intervals between the multiple short-circuits were several tens of μs, they had the capability to effectively cool the MOSFETs. Therefore, the proposed multiple short-circuit method can reduce the thermal stress on the MOSFETs.

Fig. 16 shows experimental waveforms of the initial charge obtained after several cycles of the overvoltage suppression control. Since the short-circuit may affect the long-time reliability of the power devices, this article conducted repetitive tests of the initial charge to evaluate the effect of short-circuits. The initial charge is required only when the power converter is connected to the ac mains or after a blackout event, and it is assumed to occur up to three times per day. Considering the typical lifetime of inverters is 8–10 years, the repetitive test focuses on device degradation up to 10000 cycles ($\approx$ 3 times/day $\times$ 365 days/year $\times$ 10 years).

Fig. 16(a) is measured with the single short-circuit method. The peak of the short-circuit current decreased by 12–25% after 250 cycles and 36–57% after 1000 cycles compared to the initial condition. Hence, the single short-circuit method clearly resulted in degradation of the power devices with increasing number of initial charge cycles. On the other hand, Fig. 16(b) is measured with the proposed multiple short-circuit method, which employs four short-circuits in each leg. The short-circuit current waveforms of 250 and 1000 cycles closely resembled those of the initial condition. After 10000

cycles, the peak of the short-circuit current only decreased by 8–15% compared to the initial condition. Even though the multiple short-circuit method operated more than 40 times as many times as the single short-circuit method, the peak current change in the multiple short-circuit method was smaller than that in the single short-circuit method. Consequently, the multiple short-circuit method can extend the lifetime of the power converter.

VII. CONCLUSION

This article proposed an overvoltage suppression method for the initial charge of power converters, utilizing multiple short-circuits in each leg. The proposed method employs several brief short-circuits in each leg to effectively suppresses overvoltage during the initial charge. The multiple short-circuit method demonstrates the capability to reduce voltage ripple across the dc capacitor and decrease energy consumption in the MOSFETs during the initial charge. Additionally, the intervals between the short-circuits contribute to lowering the temperature of the MOSFETs, thus reducing overall stress.

Experimental verification revealed that the multiple short circuit method reduced voltage ripple across the dc capacitor from 15% to 4%. Simulation results estimated a significant decrease in the peak junction temperature of the MOSFETs, from 378 °C to 180 °C, when employing four short-circuits in each leg. Despite only a 6% reduction in total energy consumption during the short-circuits, the repetitive test of the initial charge indicated that the power device degradation, as indicated by the peak current, was limited to 8–15% after 10000 cycles of the four short-circuits method. This degradation was lower than that observed after 250 cycles of the single short-circuit method.

Therefore, the multiple short-circuit method enables effective overvoltage suppression for the dc capacitor, leading to reduced MOSFET degradation and an extended lifetime of the power converter compared to the single short-circuit method. The multiple short-circuit method can contribute to reducing costs and volume in power converters, particularly in PWM rectifiers.

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TOMOYUKI MANNEN (Member, IEEE) received the B.S., M.S., and Ph.D. degrees in electrical engineering from the Tokyo Institute of Technology, Tokyo, Japan, in 2012, 2014, and 2017, respectively. They joined Tokyo Metropolitan University, Tokyo, Japan, as a Postdoctoral Researcher in 2017, and moved to Tokyo University of Science, Tokyo, as an Assistant Professor in 2018. Since 2019, they have been an Assistant Professor with the Department of Applied Physics, University of Tsukuba, Tsukuba, Japan. Their research interests include grid-connection converters, especially in current unfolding strategies, active power filters, and control methods, as well as optimum switching behavior and extreme overload operation in power devices. Dr. Mannen was the recipient of the Committee Prize Paper Awards from the IEEE Industry Applications Society Industrial Power Converter Committee in 2016, 2019, and 2021, Conference Presentation Award from the Institute of Electrical Engineers of Japan in 2013, 2015, 2017, and 2019.

KEIJI WADA (Senior Member, IEEE) received the Ph.D. degree in electrical engineering from Okayama University, Okayama, Japan, in 2000. From 2000 to 2006, he was an Assistant Professor with Tokyo Metropolitan University, Tokyo, Japan, and Tokyo Institute of Technology, Tokyo. From 2006 to 2020, he was an Associate Professor with Tokyo Metropolitan University. Since 2021, he has been a Professor with Tokyo Metropolitan University. His research interests include medium-voltage inverters, electromagnetic interference filters, and circuit implementation. He is a Senior Member of IEEJ.