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A Modified Switched-Capacitor Based Seventeen-Level Inverter With Reduced Capacitor Charging Spike for RES Applications

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ABSTRACT This article presents a grid-connected system for renewable energy source (RES) applications. The proposed system consists of a modified switched-capacitor (SC) based multilevel inverter and a DC-DC flyback converter. By using the DC-DC flyback converter the voltages of DC-link capacitors are adjusted to the same values. This modified SC-based multilevel inverter has benefits like limited capacitor charging spike, reasonable size, power density, cost per output power, active and reactive power support, adjusted injected current to the grid, and reduced number of input power DC supplies. Two isolated DC sources are generated using a flyback converter to supply the SC-based inverter and increase the number of voltage levels produced at the output. In this topology, one of the most important problems of the switched capacitor, i.e., the occurrence of the inrush currents during charging capacitors, is solved by using a circuit unit that consists of an inductor with a parallel power diode in the capacitive charging current path. To confirm the performance of the presented structure, comprehensive experiments and comparisons are provided. In the experiments, the peak current control (PCC) method is applied to control both the active and reactive power injected into the grid by the modified 17-levels grid-connected inverter.

INDEX TERMS Multilevel inverter, photovoltaic systems, switched capacitor inverter.

I. INTRODUCTION

Recently, multi-level inverters (MLI) are one of the most popular solutions to improve the performance of electric vehicles, renewable energy systems such as photovoltaic (PV) systems, and other power electronic devices in medium- and high-power applications [1], [2], [3], [4], [5], [6], [7]. Compared to other inverter structures, these inverters benefit from many merits like producing a staircase voltage waveform of the output with lower total harmonic distortion (THD) and higher power quality [8], [9], [10], [11], [12], [13]. The conventional MLIs are divided into three configurations: diode clamped inverters, flying capacitors, and cascaded H-bridge (CHB) topologies [14], [15], [16]. Although these mentioned topologies have a lot of advantages, they use large numbers of power circuit elements (power switches and power diodes) and power dc supplies, and also large capacitor banks. Furthermore, in these kinds of inverters, a charge balancing control strategy is needed since the voltage of their capacitors will be discharged automatically. Up to now, several charge balancing methods along with their circuits have been introduced to control the DC link voltages of these structures [17], [18], [19]. In the structures which are presented in [17], [18], [19], the duty cycle of the dc bus capacitors of flying capacitor multilevel

inverters was adjusted by using the exiting redundancy switching state. In the mentioned topologies the accuracy of the provided process depends on designing a closed-loop control method.

Recently, a large number of multilevel inverters have been presented based on switched-capacitor (SC) circuits [20], [21], [22], [23], [24], [25], [26]. Compared to other inverters, the SC-based MLIs can generate more voltage levels at the output and decrease the number of needed DC supplies [27], [28], [29], [30]. It should be noted that in these kinds of MLIs, the negative half cycle of the output voltage waveform is generated by an H-bridge (HB) inverter. This issue causes an increased number of power electronic components for them and also as a result increases their overall power losses.

Two hybrid MLIs with an improved total standing voltage (TSV) of switches have been introduced in [31]. These topologies are based on a new switched capacitor basic unit. This topology includes two power electronic switches, one diode, and one capacitor. Note that to produce the negative half-cycle of the output voltage waveform, both of these topologies require an H-bridge. A new SC multilevel inverter has been introduced in [27]. In this topology, its DC voltage levels are produced by charging and discharging the used capacitors in a binary asymmetrical pattern. In [32], a new multilevel inverter has been introduced based on the SC-based topology presented in [27].

Note that both MLIs of [12] and [16] have been analyzed for an asymmetric DC source topology. In these structures, a large number of output voltage levels can be achieved by using the fewest power circuit elements. A new boost MLI topology with multiple charging and discharging capabilities of the capacitors has been presented in [33]. In this topology to improve the charging capabilities, numerous numbers of bidirectional power switches should be used and this issue is undesirable. Another disadvantage of this structure is that by increasing the number of generated output voltage levels, also its TSV will be increased. A high step-up multilevel inverter structure has been presented in [34]. This topology provides tolerating high TSV in higher output voltage levels.

One of the major defects of the SC-based multilevel inverters is that when the boosting factor of the inverter increases, the voltage stress across the power electronic devices (such as power switches, and power diodes) will increase dramatically. Therefore, the utilized circuit components should be selected with a higher power rating, which will increase the overall cost. To obtain a higher number of generated output voltage levels based on reduced circuit components (power switches and power diodes), a new kind of SC-based MLIs has been presented in [28], [35]. In these MLIs a series-parallel switching strategy has been used. Therefore, these inverters can enhance the system flexibility by switching between several capacitors in series or parallel modes. Also, the overall efficiency of these MLIs can be enhanced.

In this article, a modified grid-connected system is presented which consists of two parts: a flyback-based DC-DC converter, and an SC-based MLI. Compared with other conventional topologies, this MLI can provide a greater number of output voltage levels using the same number of power circuit components and power DC supplies.

One of the major disadvantages of the SC-based topologies is the spike current while charging the capacitors [36]. This can cause harmful current stress on the components. In [37], the quasi-resonant inductor overcomes the instant inrush currents in the series-connected capacitors. Depending on the desired number of output voltage levels, the different number of capacitors is applied to generate multiple outputs by only one dc source. In [22], the capacitors stay in a charge state in every switching cycle and they are not discharged completely. It leads to less severe inrush currents without adding an inductor. Thus, these unwanted currents are not mitigated completely.

The modified topology can solve this vital challenge. The modified MLI consists of fourteen power switches, four capacitors, four diodes, and two inductors. It should be noted four switches of modified topology are bidirectional one. In this case, all of the utilized capacitors will be charged to desired values and will be discharged periodically. It should be noted that these charging and discharging operation modes will be done by utilizing any complex modulation strategy and close loop control system.

Using the modified multilevel inverter, the performance of the presented grid-tied system is improved due to the inherent voltage boosting ability and unipolar PWM strategy. In this presented structure, by applying the modified SC units, the boost factor is provided. In this presented grid-connected system, the DC-DC flyback converter is applied to generate two independent DC voltages with a single input DC source.

Furthermore, to control both injected active and reactive powers to the grid and generated thoroughly sinusoidal injected current to the local grid, a peak current control (PCC) method is applied [17]. Therefore, the presented system can support reactive power. The performance of the modified SC-based MLI is validated by experimental and comparison results when the presented system is connected to the grid. The rest of article can be organized as:

The modified grid-tied system is described in Section III. Section IV presents the operation modes of the modified seven-level inverter. The operation and switching state of the dual output DC-DC converter are described in Section IV. Section V provides the extended version of the modified inverter. Further, design considerations for circuit components are expressed in Section VI. The power loss analysis is considered in Section VII. In order to show the benefits and differences of the modified inverter compared with other recent topologies, a comprehensive comparison is done in Section VIII. To prove the feasibility and accurate performance of the modified inverter, simulation results are provided in Section IX. Finally, to verify the advantages and operation of the modified inverter, the experimental prototype is built at 770 W output power and the obtained results are presented in Section X.

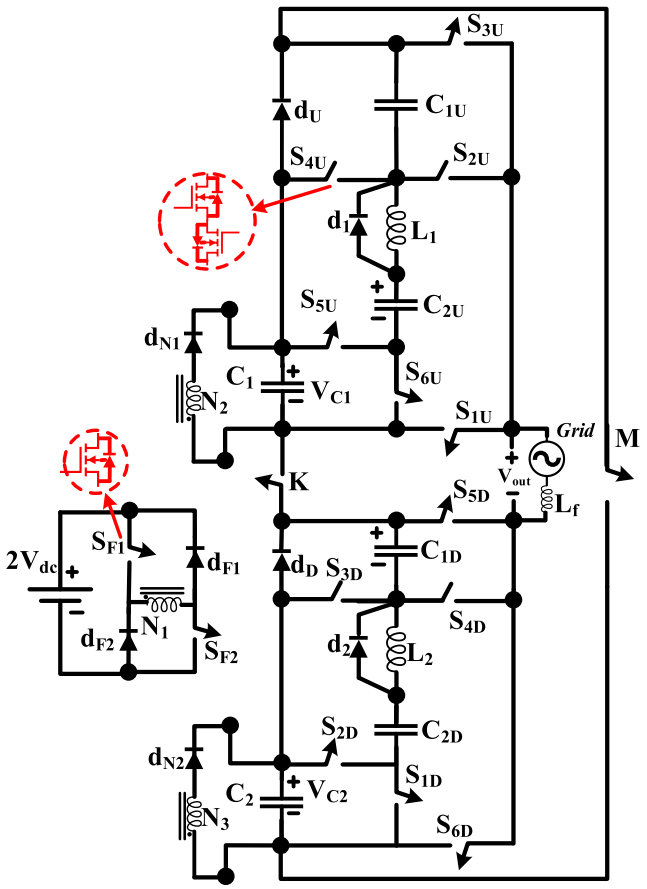


FIGURE 1. Modified grid-tied system.

II. PRESENTED GRID-TIED SYSTEM

Fig. 1 shows the presented grid-tied system which consists of a modified SC-based 17-level inverter and a single-input two-output DC-DC flyback converter. Considering Fig. 1, the modified inverter consists of ten unidirectional switches, four bidirectional switches, and four power diodes. Considering Fig. 1, the aim of using a DC-DC flyback converter is to produce two isolated DC sources with the same values for supplying the modified SC-based inverter. Therefore, a symmetric structure is made that can produce 17-level of the output voltage (even and odd levels).

Capacitor current spike is a major problem in SC-based MLIs. In this topology to reduce the spike current of capacitors during charging modes, two units which consist of inductors (L_1) and (L_2) and power diodes (d_1) and (d_2) are used. It should be noted that, in each of the utilized units inductor and diode will be in parallel positions. According to Fig. 1, when the capacitors C_{1U} and C_{2U} are in charging mode, diode d_1 is in off-state and the capacitor charging current of the mentioned capacitors pass through inductor L_1. Therefore, with the passage of capacitor charging current of capacitors C_{1U} and C_{2U} through inductor L_1, the charging current spike of mentioned capacitors will be decreased.

Also, when the capacitors C_{1D} and C_{2D} are in charging mode, diode d_2 is in off-state and the capacitor charging current of the mentioned capacitors pass through inductor L_2. Therefore, with the passage of capacitor charging current of capacitors C_{1U} and C_{2U} through inductor L_2, the charging current spike of mentioned capacitors will be decreased. Due to the standing voltage on the four power switches S_{2U}, S_{4U}, S_{3D}, and S_{4D} containing both positive and negative half-cycle, using the bidirectional power switches is necessary.

TABLE 1 Switching States of the Modified SC-Based Inverter

Levels	Involved switches	Capacitor's Mode				V_{out}
		C_{1D}	C_{2D}	C_{1U}	C_{2U}	
1st(P)	S_{4D}, K, S_{1U}, S_{1D}, S_{6U}	↓	↑	↑	↑	V_{dc}
	S_{5D}, K, S_{2U}, S_{1D}, S_{6U}	↑	↑	↑	↓	
2nd(P)	S_{6D}, K, S_{1U}, S_{1D}, S_{6U}	↑	↑	↑	↑	$2V_{dc}$
	S_{5D}, K, S_{3U}, S_{1D}, S_{6U}					
3rd(P)	K, S_{6D}, S_{2U}, S_{1D}, S_{6U}	↑	↑	↑	↓	$3V_{dc}$
	S_{3U}, K, S_{4D}, S_{1D}, S_{6U}	↓	↑	↑	↑	
4th(P)	S_{6D}, K, S_{3U}, S_{1D}, S_{6U}	↑	↑	↑	↑	$4V_{dc}$
5th(P)	S_{6D}, K, S_{3U}, S_{3D}, S_{6U}	↓	↑	↑	↑	$5V_{dc}$
	S_{6D}, K, S_{2U}, S_{1D}, S_{5U}	↑	↑	-	↓	
6th(P)	S_{6D}, K, S_{3U}, S_{2D}, S_{6U}	↓	↓	↑	↑	$6V_{dc}$
	S_{6D}, K, S_{3U}, S_{1D}, S_{5U}	↑	↑	↓	↓	
7th(P)	S_{6D}, K, S_{3U}, S_{3D}, S_{5U}	↓	-	↓	↓	$7V_{dc}$
	S_{6D}, K, S_{2U}, S_{2D}, S_{5U}	↓	↓	-	↓	
8th(P)	S_{6D}, K, S_{3U}, S_{2D}, S_{5U}	↓	↓	↓	↓	$8V_{dc}$
zero	S_{5D}, K, S_{1U}, S_{1D}, S_{6U}	↑	↑	↑	↑	0
	S_{6D},M, S_{1U}, S_{1D}, S_{6U}					
1st(N)	S_{2U},M, S_{6D}, S_{1D}, S_{6U}	↑	↑	↓	↑	$-V_{dc}$
	S_{3U}, M, S_{4D}, S_{1D}, S_{6U}	↑	↓	↑	↑	
2nd(N)	S_{5D}, M, S_{3U}, S_{1D}, S_{6U}	↑	↑	↑	↑	$-2V_{dc}$
	S_{6D},M, S_{1U}, S_{1D}, S_{6U}					
3rd(N)	S_{5D}, M, S_{2U}, S_{1D}, S_{6U}	↑	↑	↓	↑	$-3V_{dc}$
	S_{4D}, M, S_{1U},S_{1D}, S_{6U}	↑	↓	↑	↑	
4th(N)	S_{5D}, M, S_{1U},S_{1D}, S_{6U}	↑	↑	↑	↑	$-4V_{dc}$
5th(N)	S_{5D}, M, S_{1U},S_{1D}, S_{4U}	↑	↑	↓	-	$-5V_{dc}$
	S_{4D}, M, S_{1U}, S_{2D}, S_{6U}	↓	↓	↑	↑	
6th(N)	S_{5D}, M, S_{1U}, S_{2D}, S_{6U}	↓	↓	↑	↑	$-6V_{dc}$
	S_{5D}, M, S_{1U}, S_{1D}, S_{5U}	↑	↑	↓	↓	
7th(N)	S_{1U}, M, S_{2D}, S_{5U}, S_{4D}	↓	↓	↓	↓	$-7V_{dc}$
	S_{1U}, M, S_{5D}, S_{2D}, S_{4U}	↓	↓	↓	↓	
8th(N)	S_{5D}, M, S_{1U}, S_{2D}, S_{5U}	↓	↓	↓	↓	$-8V_{dc}$

III. OPERATION MODES OF THE MODIFIED 17-LEVEL SC-BASED INVERTER

The switching Table and utilized capacitor's states of the modified 17-level SC-based MLI are listed in Table 1. As seen, to produce any voltage level at the output, only five power switches should be turned on. In Table 1, the terms of "↑", "↓" and "-" refer to charging mode, discharging mode, and un-connected mode of each capacitor during each level of the output voltage waveform.

It should be noted that each of the capacitors (C_1 and C_2) in the output of the flyback converter is adjusted to $2V_{dc}$ (100 V). In this section, different operation modes of the 17-level inverter are described. Since the operation modes of the modified inverter during the negative half cycle are similar to the positive half cycle, the negative half cycle details are not presented in this section.

A. ZERO OPERATION MODE

The zero-operation mode of the modified SC-based inverter is indicated by the zero level (zero) in Table 1. Considering this table, during this operation mode, the power switches S_{5D}, K, S_{1U}, S_{1D}, and S_{6U} are in ON-state. So that, the amplitude of the generated inverter's output voltage is equal to zero. In addition, in this mode, all of the utilized capacitors (C_{1U}, C_{2U}, C_{1D}, and C_{2D}) are in charging mode.

B. FIRST OPERATION MODE

The First operation mode of the modified inverter is shown by 1st(P) in Table 1. As seen, here, the switches S_{4D}, K, S_{1U}, S_{1D}, and S_{6U} are in ON-state. During this mode, the voltage of the capacitor C_{1D} is transferred to the output and this makes the output voltage the same as the voltage of capacitor C_1 ($V_{out} = V_{C1D} = V_{dc}$). So that, the first level of the positive half-cycle of the output voltage waveform is generated. It should be noted that in this mode all of the switched capacitors (C_{1U}, C_{2U}, C_{1D}, and C_{2D}) are in charging mode.

C. SECOND OPERATION MODE

Considering Table 1, the second operation mode of the modified inverter during the positive half cycle is indicated by 2nd(P). As seen, here, the switches S_{6D}, K, S_{1U}, S_{1D}, and S_{6U} are in ON-state. During this mode, the stored voltage of the capacitor C_1 (output capacitor of flyback converter) is transferred to the output voltage and this makes the output voltage the same as the voltage of capacitor C_1 ($V_{out} = V_{C1} = 2V_{dc}$). Other utilized switched capacitors are in charging mode.

D. THIRD OPERATION MODE

The switching states of power switches and capacitor's modes of modified inverter during third operation mode in the positive half cycle (3rd(P)) are presented in Table 1. Here, the power switches S_{6D}, K, S_{2U}, S_{1D}, and S_{6U} are in ON-state. So that, the capacitor C_1 is connected in series to the capacitor C_{2U}. Therefore, the sum of the voltage of these capacitors is transferred to output of the inverter.

Therefore, the output voltage of the inverter is equal to $3V_{dc}$. The related equations of this mode can be written as:

$$\begin{cases} V_{out} = V_{C1} + V_{C2U} \\ V_{C1} = 2Vdc, \quad VCU2 = V_{dc} \end{cases} \Rightarrow V_{out} = 3V_{dc}, \tag{1}$$

E. FORTH OPERATION MODE

This operation mode is depicted in Table 1 by 4th(P). In this mode, to generate the output voltage equal to ($+4V_{dc}$), the switches S_{6D}, K, S_{3U} S_{1D}, and S_{6U} are in ON-state.

Here, the output voltage is equal to the sum of voltages of capacitors C_1 and C_2 and can be calculated as follows:

$$V_{out} = V_{C1} + V_{C2} = 4V_{dc}, \tag{2}$$

It should be noted that, during this operation mode all of the switched capacitors are in charging mode. These charging modes of capacitors are happened by turning on of the power switches S_{6U} and S_{1D}.

F. FIFTH OPERATION MODE

Table 1 indicate the fifth operation mode of the 17-level inverter by 5th(P) in which the switches S_{6D}, K, S_{3U}, S_{3D}, and S_{6U} are in ON-state in a way that the output voltage becomes equal to the sum of the voltages across the capacitors C_{1D}, C_1, and C_2. The amplitude of the output voltage of the inverter during this operation mode can be written as:

$$V_{out} = V_{C1D} + V_{C1} + V_{C2} = 5V_{dc}, \tag{3}$$

G. THIRD OPERATION MODE

Table 1 presents the sixth operation mode of the modified multilevel inverter by 6th(P). In this mode, the output voltage with the value of ($6V_{dc}$) is aimed to be obtained. As seen, the switches S_{6D}, K, S_{3U}, S_{1D}, and S_{5U} are in ON-state. So, the desired output voltage is obtained as the sum of the voltages of the capacitors C_1, C_2, C_{1D}, and C_{2D}. So, the output voltage of the inverter can be obtained as:

$$V_{out} = V_{C1} + V_{C2} + V_{C1D} + V_{C2D} = 6V_{dc}, \tag{4}$$

H. SEVENTH OPERATION MODE

The switching states of involved switches and capacitor's modes of the inverter during the seventh level of the positive half cycle are presented in Table 1 by 7th(P). Here, to produce ($7V_{dc}$) at the output, the switches S_{6D}, K, S_{2U}, S_{1D}, and S_{5U} are turned on. As seen, the output voltage is equal to the sum of the voltages across the capacitors C_1, C_2, C_{1D}, C_{2D}, and C_{2U}. So, the output voltage of the inverter can be obtained as:

$$V_{out} = V_1 + V_2 + V_{C1D} + V_{C2D} + V_{C2U} = 7V_{dc}, \tag{5}$$

I. EIGHTH OPERATION MODE

The switching states and capacitor's modes of the eighth operational mode are indicated in Table 1 by 8th(P). In this mode, the output voltage of ($8V_{dc}$) is obtained. Here, the switches S_{6D}, K, S_{3U}, S_{2D} and S_{6U} are turned on leading to a voltage equal to the sum of the voltages of the capacitors C_1, C_2, C_{1U}, C_{2U}, C_{1D}, and C_{2D} at the output. Therefore, the output voltage of the inverter can be obtained as:

$$V_{out} = V_{C1} + V_{C2} + V_{C1U} + V_{C2U} + V_{C1D} + V_{C2D} = 8V_{dc}, \tag{6}$$

In addition, the value of the duty cycle during different operation modes of modified MLI is obtained as follows.

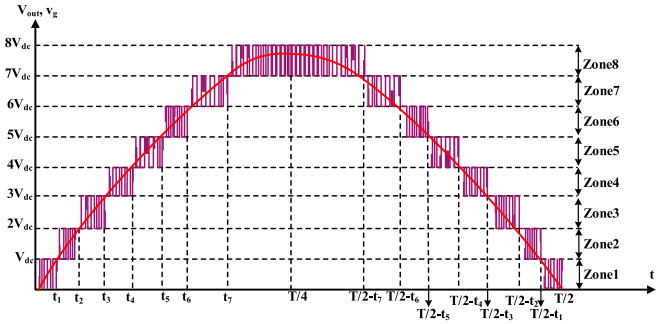


FIGURE 2. The output voltage waveform of the inverter, grid voltage, and eight operation zones of the modified inverter.

Fig. 2 indicates the output voltage waveform of the inverter during the positive half-cycle and a voltage waveform of the local grid with eight operation zones (zone1∼zone8) of the inverter. Considering this figure, the control strategy of the modified inverter can be designed. The maximum switching frequency of the inverter is f_S, also, the sampling frequency is f_{SA}. It is noteworthy that, the maximum switching frequency is half of the sampling frequency ($f_S = 0.5 f_{SA}$). By applying the inductor volt-second balanced (IVSB) law to the voltage across of the inductor filter during a full switching operation period (T_S), the switching duty cycle of the inverter during each mentioned zone is calculated in (9) to (32). It should be mentioned that, in all of the provided equations V_{out} and V_g respectively refer to the output voltages of the inverter and grid. The waveforms of grid voltage and grid current are sinusoidal waveforms with peak values of $V_{g,max}$ and $I_{g,max}$ and the equations of these waveforms can be written as follows:

$$v_g = V_{g,\max} \sin(\omega t), \tag{7}$$

$$i_g = I_{g,\max} \sin(\omega t - \varphi), \tag{8}$$

Where φ denotes the phase difference between the grid voltage and the injected current.

Zone 1:

Regarding Fig. 2, during this zone, the output voltage of the inverter is between 0 and V_{dc}.

By applying the inductor volt-second balanced (IVSB) principle for the voltage across the output inductor during zone 1 for the sampling period, the switching duty cycle of the inverter (D_1) can be obtained as (9)–(11).

$$\int_0^{D_1.T_S} (V_{out} - v_g)dt + \int_{D_1.T_S}^{T_S} (-v_g)dt = 0, \tag{9}$$

$$D_1(t) = \frac{v_g}{V_{out}}, \tag{10}$$

By placing (7) in (10) and considering that the peak value of the output voltage of the inverter during zone1 is equal to V_{dc}, the duty cycle of zone 1 can be written as (11).

$$D_1(t) = \frac{V_{g,\max}}{V_{dc}}.\sin(\omega t); \quad 0 \le t < t_1, \tag{11}$$

Zone 2:

Concerning Fig. 2, it can be seen that during zone 2 the output voltage of inverter is between V_{dc} and $2V_{dc}$. By applying the IVSB rule for the voltage across the inductor filter during zone 2 for the sampling period, the switching duty cycle of the inverter (D_2) can be calculated as (12)–(14).

$$\int_0^{D_2.T_S} (2V_{dc} - v_g)dt + \int_{D_2.T_S}^{T_S} (V_{dc} - v_g)dt = 0; \quad t_1 \le t < t_2, \tag{12}$$

$$D_2(t) = \frac{v_g}{V_{dc}} - 1 = \frac{V_{g,\max}}{V_{dc}} \sin(\omega t) - 1; \quad t_1 \le t < t_2, \tag{13}$$

With respect to (11), the duty cycle of zone2 can be obtained in terms of $D_1(t)$ as follows:

$$D_2(t) = D_1(t) - 1; \quad t_1 \le t < t_2, \tag{14}$$

Zone 3:

Based on Fig. 2, during this operation zone, the output voltage of the inverter is between $2V_{dc}$ and $3V_{dc}$.

$$D_3(t) = \frac{v_g}{V_{dc}} - 2 = \frac{V_{g,\max}}{V_{dc}}.\sin(\omega t) - 2; \quad t_2 \le t < t_3, \tag{15}$$

Due to the (13), the duty cycle of zone3 can be calculated in terms of $D_2(t)$ as follow:

$$D_3(t) = D_2(t) - 1; \quad t_2 \le t < t_3, \tag{16}$$

Zone 4:

Considering Fig. 2, during operation zone 4, the output voltage of the inverter is between $3V_{dc}$ and $4V_{dc}$.

By applying the IVSB rule for the voltage across the inductor filter during this zone for the sampling period, (17) can be written.

$$\int_0^{D_4.T_S} (4V_{dc} - v_g)dt + \int_{D_4.T_S}^{T_S} (3V_{dc} - v_g)dt = 0; \quad t_3 \le t < t_4, \tag{17}$$

the switching duty cycle of the inverter (D_4) can be calculated as (18)–(20).

$$D_4(t) = \frac{v_g}{V_{dc}} - 3 = \frac{V_{g,\max}}{V_{dc}}.\sin(\omega t) - 3; \quad t_3 \le t < t_4, \tag{18}$$

Considering (15), the (18) can be rewritten as follows.

$$D_4(t) = D_3(t) - 1; \quad t_3 \le t < t_4, \tag{19}$$

Zone 5:

In this operation zone, the output voltage of the inverter is between $4V_{dc}$ and $5V_{dc}$. By applying the IVSB rule for the voltage across the inductor filter during zone 5 for the sampling period, the switching duty cycle of the inverter (D_5) can be calculated as (20)–(22).

$$\int_0^{D_5.T_S} (5V_{dc} - v_g)dt + \int_{D_5.T_S}^{T_S} (4V_{dc} - v_g) = 0; \quad t_4 \le t < t_5, \tag{20}$$

$$D_5(t) = \frac{v_g}{V_{dc}} - 4 = \frac{V_{g,\max}}{V_{dc}}.\sin(\omega t) - 4; \quad t_4 \le t < t_5, \tag{21}$$

With respect to (18), the duty cycle of zone5 can be written in terms of $D_4(t)$ as:

$$D_5(t) = D_4(t) - 1; \quad t_4 \le t < t_5, \tag{22}$$

Zone 6:

As seen in Fig. 2, during zone 6 the output voltage of inverter is between $5V_{dc}$ and $6V_{dc}$. By applying the IVSB rule for the voltage across the inductor filter during zone 6 for the sampling period, the switching duty cycle of the inverter (D_6) can be calculated as (23)–(25).

$$\int_0^{D_6.T_S} (6V_{dc} - v_g)dt + \int_{D_6.T_S}^{T_S} (5V_{dc} - v_g)dt = 0;$$
$$t_5 \le t < t_6, \tag{23}$$

$$D_6(t) = \frac{v_g}{V_{dc}} - 5 = \frac{V_{g,\max}}{V_{dc}}.\sin(\omega t) - 5; \quad t_5 \le t < t_6, \tag{24}$$

Considering (21), the duty cycle of zone6 can be written in terms of $D_5(t)$ as:

$$D_6(t) = D_5(t) - 1; \quad t_5 \le t < t_6, \tag{25}$$

Zone 7:

Concerning Fig. 2, it can be seen that during zone 7 the output voltage of inverter is between $6V_{dc}$ and $7V_{dc}$. By applying the IVSB rule for the voltage across the inductor filter during zone 7 for the sampling period, the switching duty cycle of the inverter (D_7) can be calculated as (26)–(28).

$$\int_0^{D_7.T_S} (7V_{dc} - v_g)dt + \int_{D_7.T_S}^{T_S} (6V_{dc} - v_g)dt = 0;$$
$$t_6 \le t < t_7\,, \tag{26}$$

$$D_7(t) = \frac{v_g}{V_{dc}} - 6 = \frac{V_{g,\max}}{V_{dc}}.\sin(\omega t) - 6; \quad t_6 \le t < t_7, \tag{27}$$

Due to the (25), the duty cycle of zone7 can be calculated in terms of $D_6(t)$ as follow:

$$D_7(t) = D_6(t) - 1; \quad t_6 \le t < t_7, \tag{28}$$

Zone 8:

With regard to Fig. 2, it can be seen that during zone 8 the output voltage of inverter is between $7V_{dc}$ and $8V_{dc}$. By applying the IVSB rule for the voltage across the inductor filter during zone 8 for the sampling period, the switching duty cycle of the inverter (D_8) can be calculated as (29)–(31).

$$\int_0^{D_7.T_S} (8V_{dc} - v_g)dt + \int_{D_7.T_S}^{T_S} (7V_{dc} - v_g)dt = 0;$$
$$t_7 \le t < \frac{T}{2} - t_7, \tag{29}$$

$$D_8(t) = \frac{v_g}{V_{dc}} - 7 = \frac{V_{g,\max}}{V_{dc}}.\sin(\omega t) - 7;$$
$$t_7 \le t < \frac{T}{2} - t_7, \tag{30}$$

With regard to (27), the (30) can be rewritten as follows.

$$D_8(t) = D_7(t) - 1; \quad t_7 \le t < \frac{T}{2} - t_7, \tag{31}$$

Considering Fig. 2, the equation of $t_1 \sim t_7$ can be calculated as:

$$t_1 = \frac{1}{\omega}\sin^{-1}\left(\frac{V_{dc}}{V_{g,\max}}\right), \tag{32}$$

$$t_2 = \frac{1}{\omega}\sin^{-1}\left(\frac{2V_{dc}}{V_{g,\max}}\right), \tag{33}$$

$$t_3 = \frac{1}{\omega}\sin^{-1}\left(\frac{3V_{dc}}{V_{g,\max}}\right), \tag{34}$$

$$t_4 = \frac{1}{\omega}\sin^{-1}\left(\frac{4V_{dc}}{V_{g,\max}}\right), \tag{35}$$

$$t_5 = \frac{1}{\omega}\sin^{-1}\left(\frac{5V_{dc}}{V_{g,\max}}\right), \tag{36}$$

$$t_6 = \frac{1}{\omega}\sin^{-1}\left(\frac{6V_{dc}}{V_{g,\max}}\right), \tag{37}$$

$$t_7 = \frac{1}{\omega}\sin^{-1}\left(\frac{7V_{dc}}{V_{g,\max}}\right), \tag{38}$$

Considering Fig. 1, the blocked voltage of each switch in the modified SC-based inverter can be obtained in terms of input dc voltage as follows. It should be noted that the amplitude the of input dc source of the modified SC-based inverter is $2V_{dc}$ ($V_{in} = 2V_{dc}$). The total standing voltage (TSV) of the modified SC-based inverter is equal to the sum of voltage stress of each switch and can be obtained as (39). The per-unit value of TSV (TSV_{PU}) in terms of input dc voltage source (V_{in}) can be obtained as (40).

The logic circuit of the PWM switching gate pulses is illustrated in Fig. 3. Based on Fig. 3, the modified topology has eight operation zones during the positive half cycle (Z_1-Z_8) and negative half cycle (NZ_1-NZ_7). It should be noted that N denotes negative. Fig. 3(a) shows each zone during the positive and negative half cycle. Also, Fig. 3(b) illustrates the generated output voltage levels during positive (L_1-L_8) and negative half-cycles (NL_1-NL_8) and zero level (L_0). Finally, based on Table 1, the switching gate pulses of each switch of the modified inverter are obtained and illustrated in Fig. 4.

$$\begin{cases} V_M = V_K = 4V_{\text{in}} = V_{\text{out}} \\ V_{S1U} = 2V_{\text{in}} \\ V_{S2U} = 1.5V_{\text{in}} \\ V_{S3U} = 2V_{\text{in}} \\ V_{S4U} = 0.5V_{\text{in}} \\ V_{S5U} = V_{\text{in}} \\ V_{S6U} = V_{\text{in}} \\ V_{S1D} = V_{S2D} = V_{\text{in}} \\ V_{S3D} = 0.5V_{\text{in}} \\ V_{S4D} = 1.5V_{\text{in}} \\ V_{S5D} = V_{S6D} = 2V_{\text{in}} \end{cases} \tag{39}$$

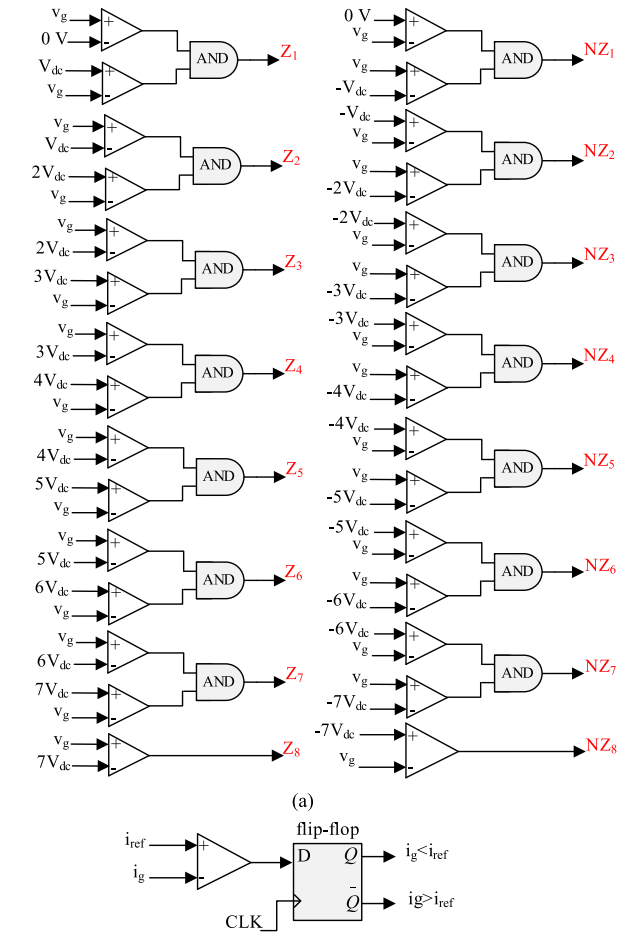


FIGURE 3. (a) Operation zones of modified inverter during positive and negative half-cycles, (b) voltage levels of the output voltage waveform during the positive and negative half cycle.

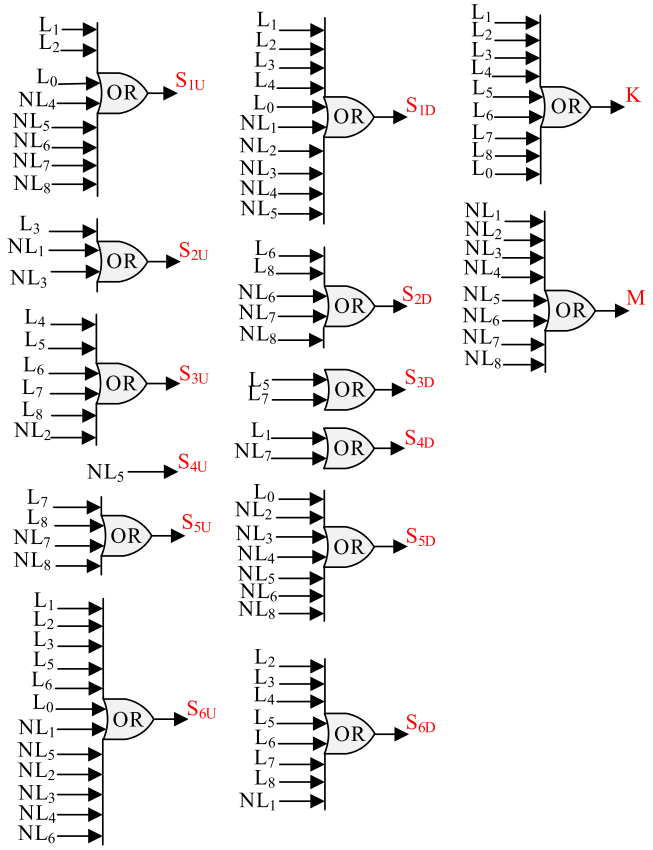


FIGURE 4. Generated switching PWM gate pulses of utilized switches of the modified inverter.

$$TSV = V_{S1U} + \ldots + V_{S6U} + V_{S1D} + \ldots V_{S6D} + V_M + V_K = 24V_{\text{in}} \tag{40}$$

$$TSV_{PU} = \frac{24V_{\text{in}}}{V_{\text{in}}} = 24 \tag{41}$$

IV. OPERATION AND SWITCHING STATES OF THE DUAL-OUTPUT FLYBACK CONVERTER

As mentioned, to generate two isolated DC sources with the same values for supplying the seventeen-level inverter, the dual-output flyback converter is used in the proposed system. In order to obtain to this aim, the switching states of the flyback converter is illustrated in Fig. 5. Based on Fig. 5, the switches S_{F1}, and S_{F2} (see Fig. 1) are turned on together. Also, diodes D_{F1}, and D_{F2} are turned on simultaneously. In addition, when the switches S_{F1}, and S_{F2} are turned on, the secondary and tertiary diodes of flyback (d_{N1}, and d_{N2}) start to conduct. In DC-DC flyback converter, the function of diodes D_{F1}, and D_{F2} is to transfer the energy stored in leakage inductor of transformer, which is turned to the input source.

Note that, the leakage inductance in a transformer is an inductive component that results from the imperfect magnetic linking of one winding to another. It should be mentioned that the absence of diodes D_{F1}, and D_{F2} causes a sharp spike on

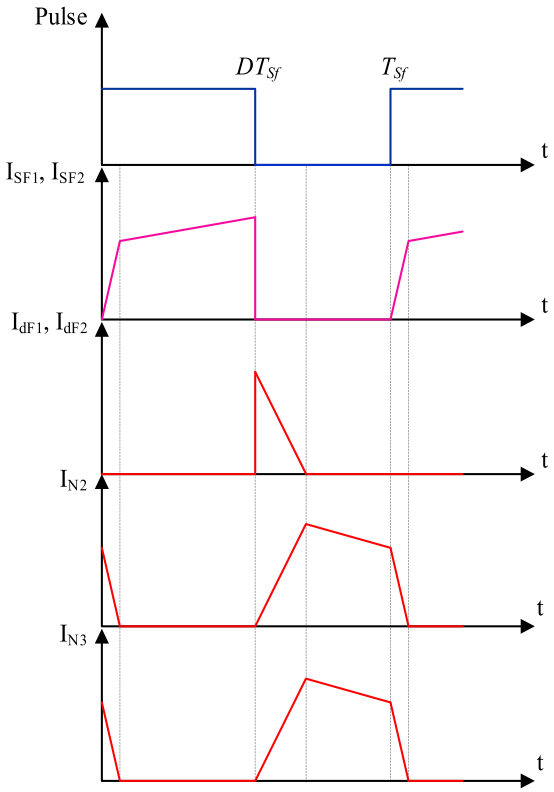


FIGURE 5. Switching states of the dual output flyback converter. (Note that, *D* and T_{sf} are the duty cycle and switching period of the flyback converter.)

the switches S_{F1}, and S_{F2}. So, the power losses of switches S_{F1}, and S_{F2} increase.

The existence of these diodes means that there is no need for snubber for S_{F1}, and S_{F2} to reduce their power losses. In the modified grid-tied system, by adjusting the turns ratio of the used transformer and also the duty cycle of the isolated DC- converter, it is possible to provide flexible voltage boosting performance. In fact, to provide this feature, there are two degrees of freedom such as duty cycle and transformer turn ratio.

As it obvious the flyback converter is used in low power applications. In order to use the modified multilevel inverter in high-power applications the flyback converter can be replaced with another isolated dc-dc converter such as full-bridge isolated dc-dc converter as it is indicated in Fig. 6.

To approach to a high power and use minimum numbers of semiconductors, full-bridge converter, as indicated in Fig. 6, is recommended. Since in high power application the DC-DC flyback in forward converters encounter limitation, it is better to use full-bridge dc-dc converter as shown in Fig. 6 [38].

V. THE EXTENDED OF THE MODIFIED INVERTER

The extended structure of the modified Sc-based inverter can be obtained by integrating more numbers of the SC cells into a packed unit, as illustrated in Fig. 7.

Considering this concept, the number of generated output levels can be enhanced. Considering Fig. 7, the required count

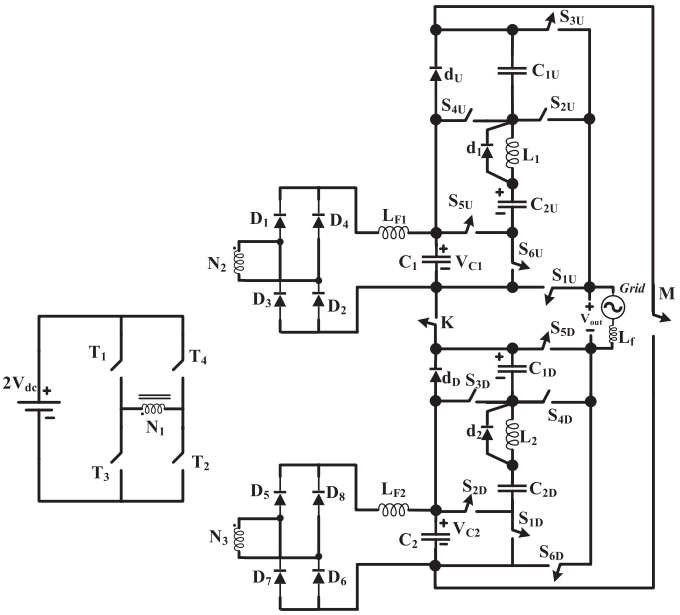


FIGURE 6. Modified grid-tied system for high power applications.

of different circuit elements for proper connection for n numbers of modified SC-based inverter and extended version of modified inverter can be written as follows:

$$N_{SW} = N_{Drive} = 12n + 4 \tag{42}$$

$$N_{Capitor} = 6n \tag{43}$$

$$N_{Diode} = 6n \tag{44}$$

Where, N_{SW}, $N_{Capacitor}$, and N_{Diode} denote number of switches, number of capacitors, and number of diodes, respectively. In this case, in the medium voltage applications, each used bidirectional switch can be made by using a back-to-back connection of two ordinary switches, two IGBTs for each of them are required. Therefore, the total number of needed IGBTs (N_{IGBT}) for the extended version of modified inverter can be expressed as follows:

$$N_{IBGBT} = 16n + 4 \tag{45}$$

Further, if the amplitude of the single input DC source of modified system is assumed as $2V_{dc}$ ($V_{in} = 2V_{dc}$), the maximum value of generated output voltage waveform can be expressed as:

$$V_{out,\max} = 8nV_{dc} \tag{46}$$

Also, the number of generated output voltage levels can be expressed as:

$$N_{level} = 16n + 1 \tag{47}$$

In addition, the per unit value of TSV in terms of input dc voltage source (V_{in}) for the utilized switches in the extended version of modified inverter can be obtained as:

$$TSV_{PU} = 24n \tag{48}$$

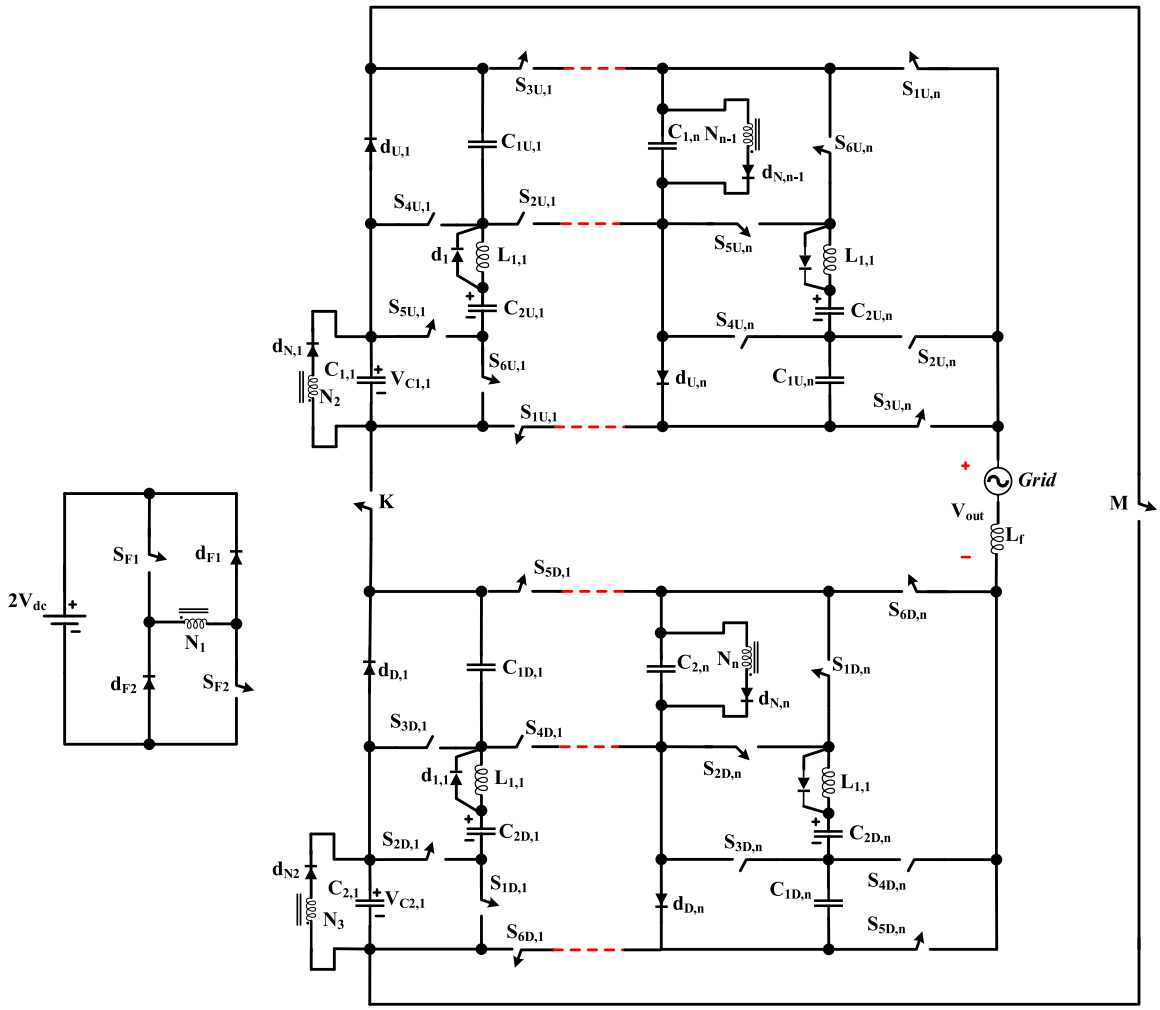


FIGURE 7. The extended version of the modified SC-based system.

VI. CALCULATION OF OUTPUT FILTER INDUCTOR, INDUCTORS L_1, AND L_2 AND UTILIZED CAPACITORS

Concerning Fig. 1, the output filter of the modified grid-tied MLI consists of an inductor with the inductance value of L_f. The voltage across the output filter can be denoted by V_{Lf}. It should be mentioned that, if the power factor is unity and the value of injected grid current is maximum ($t = T/4$), the maximum current ripple value of the output inductor filter happens. At this moment ($t = T/4$), the output voltage is within zone 8 which is equal to $8V_{dc}$ ($V_{out} = 8V_{dc}$). The current equation of the inductor $i_{Lf}(t)$ in a full period of switching can be calculated as follows:

$$i_{Lf} = \frac{1}{L_f}\int_0^t v_{L,f}dt + i_{L,f}(0); \quad t_7 \le t < \frac{T}{2} - t_7, \tag{49}$$

$$\Delta I_{Lf} = i_{Lf}(t = D_8.T_s) - i_{Lf}(0) = \frac{(8V_{dc} - v_g).D_8}{L_f.f_S};$$

$$t_7 \le t < \frac{T}{2} - t_7, \tag{50}$$

Therefore, using (49), the final value of L_f can be calculated as:

$$L_f = \frac{1}{\Delta I_{Lf}.f_S}\left[15V_{g,\max}.\sin(\omega t) - \frac{V_{g,\max}^2}{V_{dc}}.\sin^2(\omega t) - 56Vdc\right], \tag{51}$$

The inductance value of the output filter (L_f) for the maximum value of the inductor current ripple could be obtained as follows:

$$L_f = \frac{1}{\Delta I_{Lf,\max}.f_S}\left[15V_{g,\max} - \frac{V_{g,\max}^2}{V_{dc}} - 56V_{dc}\right], \tag{52}$$

As mentioned, an inductor is used to limit the peak of the charging current. The suggested analysis about the inductor size is presented in this section. In the following, the detailed equations are presented. The equivalent circuit of the charging loop of capacitors C_{1U}, and C_{2U} can be illustrated in Fig. 8. Based on Fig. 8, R_{eq1}, denotes the equivalent resistance of the charging path of capacitors C_{1U}, and C_{2U}.

Also, C_{eq1} represents the equivalent capacitance value of capacitors C_{1U}, and C_{2U}. Considering Fig. 8, by applying the

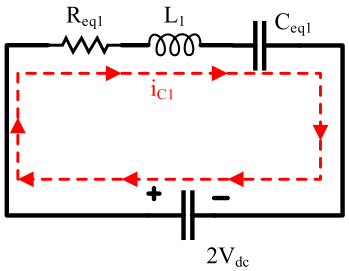


FIGURE 8. The equivalent circuit of capacitors C_{1U} and C_{2U} charging loop.

KVL law in the charging loop of capacitors C_{1U} and C_{2U}, the following equations can be obtained:

$$\begin{cases} R_{eq1} \cdot I_C + L_1 \frac{dI_C}{dt} + \frac{1}{C_{eq1}} \int I_C(t)dt = 0 \\ \frac{d^2 I_C}{dt^2} + \frac{R_{eq1}}{L_1} \frac{dI_C}{L \cdot C_{eq1}} = 0 \end{cases} \tag{53}$$

By solving the above-mentioned equations, the resonance frequency (ω_r) and damping factor (α) can be obtained as:

$$\begin{cases} \alpha = \frac{R_{eq1}}{2L_1} \\ \omega_r = \frac{1}{\sqrt{L_1 \cdot C_{eq1}}} \end{cases} \tag{54}$$

In order to design the optimal size of the inductor L_1 which is used to reduce the capacitor charging current spike, the value of the damping index should be smaller than the resonance frequency, so it can be written as follows:

$$\alpha < \omega_r \Rightarrow \frac{R_{eq1}}{2L_1} < \frac{1}{\sqrt{L_1 \cdot C_{eq1}}} \tag{55}$$

By squaring both sides of (1) and simplifying it, the desired inductance of inductor L_1 is obtained as follows:

$$L_1 > \frac{(R_{eq1})^2 . C_{eq1}}{4} \tag{56}$$

To design the optimal inductance value of the inductor L_2 in order to limit the spike of the capacitor charging current in the charging loop of capacitors C_{1D} and C_{2D}, it should be analyzed as the same as inductor L_1. Therefore, the inductance value of L_2 can be obtained as follows:

$$L_2 > \frac{(R_{eq2})^2 . C_{eq2}}{4} \tag{57}$$

Where, R_{eq1} denotes the equivalent resistance of the charging path of capacitors C_{1U}, and C_{2U}. Also, R_{eq2} represents the equivalent resistance of capacitor charging path of capacitors C_{1D}, and C_{2D}. The both mentioned resistances (R_{eq1}, and R_{eq2}) can be calculated as follows:

$$\begin{cases} R_{eq1} = R_{dU} + 3r_{ESR,C} + r_{L1} + R_{DS} \\ R_{eq2} = R_{dD} + 3r_{ESR,C} + r_{L2} + R_{DS} \end{cases} \tag{58}$$

In addition, the charging current of the capacitors C_{1U}, and C_{2U} can be calculated as follows:

$$i_{C1}(t) = \frac{2V_{dc} - V_{C1U} - V_{C2U}}{\sqrt{\frac{L_1}{C_{eq1}} - \frac{R_{eq1}^2}{4}}} \times e^{-\frac{R_{eq1}}{2L_1}t} \times \sin\left(\sqrt{\frac{1}{L_1 C_{eq1}} - \frac{R_{eq1}^2}{4L_1^2}}\right) t \tag{59}$$

Where, C_{eq1} represent the equivalent capacitance value of capacitors C_{1U}, and C_{2U} and can be obtained as:

$$\begin{cases} C_{eq1} = \frac{C_{1U} \cdot C_{2U}}{C_{1U} + C_{2U}} \Rightarrow C_{eq1} = \frac{C_{1U}}{2} \\ C_{1U} = C_{2U} \end{cases} \tag{60}$$

Also, the charging current of the capacitors C_{1D}, and C_{2D} can be calculated as follows:

$$i_{C2}(t) = \frac{2V_{dc} - V_{C1D} - V_{C2D}}{\sqrt{\frac{L_2}{C_{eq2}} - \frac{R_{eq2}^2}{4}}} \times e^{-\frac{R_{eq2}}{2L_2}t} \times \sin\left(\sqrt{\frac{1}{L_2 C_{eq2}} - \frac{R_{eq2}^2}{4L_2^2}}\right) t \tag{61}$$

Where, C_{eq2} represent the equivalent capacitance value of capacitors C_{1D}, and C_{2D} and can be obtained as:

$$\begin{cases} C_{eq2} = \frac{C_{1D} \cdot C_{2D}}{C_{1D} + C_{2D}} \Rightarrow C_{eq1} = \frac{C_{1D}}{2} \\ C_{1D} = C_{2D} \end{cases} \tag{62}$$

During the time intervals of t_{p1} and t_{p2} the current $i_{C1}(t)$ and $i_{C2}(t)$ reach to their maximum value obtained by the below equation:

$$\begin{cases} t_{P1} = \frac{\pi}{2 \times \sqrt{\frac{1}{L_1 C_{eq1}} - \frac{R_{eq1}^2}{4L_1^2}}} \\ t_{P2} = \frac{\pi}{2 \times \sqrt{\frac{1}{L_1 C_{eq2}} - \frac{R_{eq2}^2}{4L_2^2}}} \end{cases} \tag{63}$$

Now, the maximum values (peaks) of the charging currents during time intervals t_{p1} and t_{p2} can be obtained as:

$$I_{C1,\max} = i_{C1}(t_{p1}) = \frac{2V_{dc} - V_{C1U} - V_{C2U}}{\sqrt{\frac{L_1}{C_{eq1}} - \frac{R_{eq1}^2}{4}}} \times e^{-\frac{R_{eq1} \times \pi}{4L_1 \times \sqrt{\frac{1}{L_1 C_{eq1}} - \frac{R_{eq1}^2}{4L_1^2}}}} \tag{64}$$

$$I_{C2,\max} = i_{C2}(t_{p2}) = \frac{2V_{dc} - V_{C1D} - V_{C2D}}{\sqrt{\frac{L_2}{C_{eq2}} - \frac{R_{eq2}^2}{4}}} \times e^{-\frac{R_{eq2} \times \pi}{4L_2 \times \sqrt{\frac{1}{L_2 C_{eq2}} - \frac{R_{eq2}^2}{4L_2^2}}}} \tag{65}$$

Based on the above equations, it can be able to compromise between inductor size, magnitude of charging current and charging speed.

Supposing the limiting inductor is not present, the charging current of the capacitors were only limited by parasitic resistance of the charging path. The maximum value of the charging current of the capacitors C_{1U}, and C_{2U} ($I'_{C1,\max}$) and C_{1D}, and C_{2D} $I'_{C2,\max}$ without using the inductor in the charging loop can be calculated as:

$$I'_{C1,\max} = \frac{2V_{dc} - V_{C1U} - V_{C2U}}{R_{eq1}} \tag{66}$$

$$I'_{C2,\max} = \frac{2V_{dc} - V_{C1U} - V_{C2U}}{R_{eq1}} \tag{67}$$

Therefore, by using (64) and (66) the percentage of reduction in inrush current of the capacitors C_{1U} and C_{2U} can be figured up by the following equation:

$$\frac{I_{C1,\max}}{I'_{C1,\max}} \times 100 = \frac{R_{eq1}}{\sqrt{\frac{L_1}{C_{eq1}} - \frac{R_{eq1}^2}{4}}} \times e^{-\frac{R_{eq1}\times\pi}{4L_1\times\sqrt{\frac{1}{L_1C_{eq1}} - \frac{R_{eq1}^2}{4L_1^2}}}} (\%) \tag{68}$$

Hence, by using (65) and (67) the percentage of reduction in inrush current of the capacitors C_{1D} and C_{2D} can be figured up by the following equation.

$$\frac{I_{C2,\max}}{I'_{C2,\max}} \times 100 = \frac{R_{eq1}}{\sqrt{\frac{L_2}{C_{eq2}} - \frac{R_{eq1}^2}{4}}} \times e^{-\frac{R_{eq2}\times\pi}{4L2\times\sqrt{\frac{1}{L_2C_{eq2}} - \frac{R_{eq2}^2}{4L_2^2}}}} (\%) \tag{69}$$

It is worth mentioning that using inductor not only limits the inrush current of the capacitors but also it prevents extra power loss which arises from impulsive current charging of the parallel capacitors. This power loss is thoroughly described in [39] however, in order not to make this work copious and tiresome is it not repeated here.

Also, the sizes of the capacitors C_{1U}, C_{2U}, C_{1D} and C_{2D} are calculated. In the following, $I_{g,\max}$ and φ denote the amplitude of the injected current and the phase difference between the grid voltage and the injected current. Note that the output voltage is considered as a staircase waveform. Thus, the maximum discharging value of each capacitor can be expressed in a half-cycle as follow:

$$Q_{Ci} = \int_{t_k}^{(0.5T - t_k)} I_{g,\max}.\sin(\omega t - \varphi); \quad i = 1U, 2U, 1D, 2D, \tag{70}$$

Here, $I_{g,\max}$, T, and ω denote the maximum value of the injected grid current, the periodic time of the grid voltage, and the fundamental angular frequency of the output voltage, respectively. Furthermore, $[t_k, 0.5T - t_k]$ is the time interval related to the longest discharging cycle (LDC) of each capacitor. This time interval will vary for C_{1U}, C_{2U}, C_{1D} and C_{2D} in the modified SC-based MLI. According to Table 1, the LDC for C_{1U}, C_{2U}, C_{1D} and C_{2D} is illustrated in Fig. 9. Thus, by considering the kV_{in} as the maximum allowable voltage ripple, the size of the capacitors can be calculated by using (70).

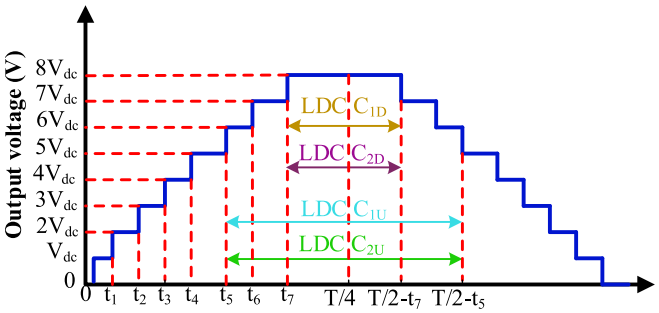


FIGURE 9. The typical output voltage waveform of the modified MLI inverter during positive half-cycle.

$$C_{opt,i} \geq \frac{Q_{C_i}}{kV_{\text{in}}}; \quad i = 1U, 2U, 1D, 2D, \tag{71}$$

VII. POWER LOSS ANALYSIS

In this section, the power losses analysis of the modified 17-level inverter is done. The power losses analysis includes two parts: Switching losses (P_{SW}) and conduction losses (P_{Con}). It should be noted that, other components such as the capacitors only have conduction losses.

A. SWITCHING LOSSES

In this subsection, the switching losses of the power switches are calculated. During the ON and OFF period of the switching state, the switching losses of the switches can be analyzed. To facilitate the analysis process, a linear approximation between the across voltage and the passing current of the power switches is assumed. Therefore, the switching losses of the utilized power switches can be obtained as follow:

$$\begin{aligned} P_{SW_{kth}(on)} &= \frac{1}{T_S}\int_0^{t_{on}} v_{on,k}(t)i(t)dt \\ &= f_S\int_0^{t_{on}} \left(-\frac{I_b}{t_{on}}(t - t_{ON})\right)\left(\frac{V_{on,k}}{t_{on}}t\right)d \\ &= \frac{t_{on}}{6}(f_S V_{on,k} I_k), \end{aligned} \tag{72}$$

$$\begin{aligned} P_{SW_{kth}(off)} &= \frac{1}{T_S}\int_0^{t_{off}} v_{stand,k}(t)i(t)dt \\ &= f_S\int_0^{t_{off}} \left(-\frac{I'_k}{t_{off}}(t - t_{off})\right)\left(\frac{V_{stand,i}}{t_{off}}t\right)dt \\ &= \frac{t_{off}}{6}(f_S V_{block,k} I'_k), \end{aligned} \tag{73}$$

Where, I_k and I'_k refer to the passing current through the kth power electronic switch after turning ON-state and before turning OFF-state, respectively. Furthermore, f_S and T_S denote the switching frequency of the inverter and periodic

time of switching frequency of the inverter, respectively. To calculate the overall power losses of the modified 17-level inverter, the (72) and (73) should be summed together. In this case, the overall power switching losses can be formulated as follows:

$$P_{SW,total} = \sum_{i=1}^{14} \left(\sum_{j=1}^{N_{on}} P_{SW,ON,ij} + \sum_{j=1}^{N_{off}} P_{SW,OFF,ij} \right), \quad (74)$$

B. CONDUCTION LOSSES

Conduction losses are emerged by the ON-state resistance of the utilized power switches (R_{DS}) and power diodes (R_D), forward drop voltage of power diodes ($V_{on,D}$) and the equivalent series resistance of the utilized capacitor (R_{cap}). In this case, the conduction losses of power switches ($P_{con,sw}$) and power diodes ($P_{con,d}$) can be obtained as (75)–(78).

$$P_{con,sw} = \frac{p(t)}{2\pi} \left[\int_0^{2\pi} R_{DS} i^{\alpha+1} d(\omega t) \right], \quad (75)$$

$$P_{con,d} = \frac{q(t)}{2\pi} \left[\int_0^{2\pi} R_D i^2(t).d(\omega t) + \int_0^{2\pi} v_{on,D} i(t).d(\omega t) \right], \quad (76)$$

In the (49) and (50), p(t), q(t) and r(t) present the number of power switches and diodes in the current path. So that, the overall conduction losses of the modified MLI can be obtained as follows:

$$P_{con,total} = P_{con,sw} + P_{con,d}, \quad (77)$$

Therefore, by using (48) and (51) the total power losses of the modified MLI can be calculated as:

$$P_{loss,total} = P_{sw,total} + P_{con,total}, \quad (78)$$

Fig. 10(a) illustrates the pie chart of the inverter switches' power losses distribution. Based on Fig. 10(a), the loss share of each switch from the total switches' power losses is shown in different colors. For example, the share of loss of switch S_{U1} from the total switches power losses is equal to 8%. Further, the pie chart of total switches' power losses, diodes, capacitors, and inductors distributions are shown in Fig. 10(b). From this figure, it can be understood that the share of the switches' total losses from the total power losses of the inverter is equal to 18%. Considering Fig. 10(b), it can be seen that the loss share of capacitor C_{1D} from the total power loss of the inverter is equal to 6%.

The calculation and experimental efficiency curves of the modified inverter versus output power can be illustrated in Fig. 11. Concerning this figure, it can be seen that at output powers of 400 W, the maximum values of experimental efficiency are around 95.5%. Also, at 750 W the experimental efficiency is 94.3%. Also, based on Fig. 11, it can be seen that the experimental efficiency is lower than the calculation efficiency. This is because all of the used components in the topology for the calculation (theoretical) efficiency are assumed ideal. Therefore, the experimental efficiency is always slightly less than the calculation efficiency.

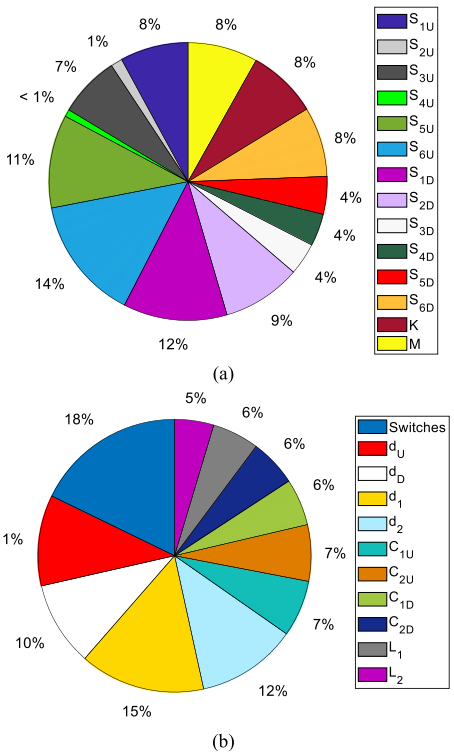


FIGURE 10. (a) Pie chart of the inverters' power switches distribution, (b) pie chart of the inverters' total switches power losses, diodes, capacitors, and inductors distributions.

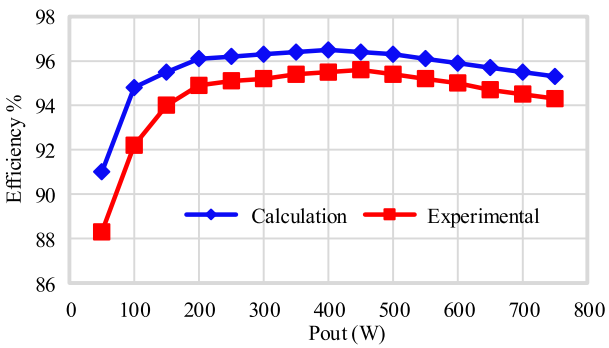


FIGURE 11. The calculation and experimental efficiency curves of the modified inverter versus output power.

VIII. COMPARISON RESULTS

In this part, the modified multilevel inverter is compared with previously presented state-of-the-art multilevel inverters in terms of the number of circuit components, generated output levels, limitation of capacitor spike current, leakage current elimination capability, reactive power support, voltage gain (V.G), total volume (mm^3), power density, cost ($), cost/$P_{out}$, negative half cycle generation based on H-Bridge and also voltage boosting capability. Note that, the power density of the modified topology and other compared topologies are calculated as follows:

$$Power\ density\ (\mathrm{W/mm^3}) = \frac{P_{\mathrm{out}}\,(W)}{Total\ volume\ (\mathrm{mm^3})} \quad (79)$$

TABLE 2 Comparison Between Different Inverters Including the Modified One

Topology	Number of circuit components				Generated output voltage levels	Limitation of capacitor spike current	Leakage current elimination capability	Reactive power supporting	V.G	P_{out}(W)	Total volume (mm^3)	Power density (W/mm^3)	Cost ($)	Cost/P_{out} (P.U.)	H-bridge based	Voltage boosting
	N_{Sw}	N_D	Cap	N_{DC}												
[27]	10	2	2	2	17	No	No	No	2	348	132149.7	2.6×10^{-3}	143.2	0.41	No	Yes
[31]	10	4	2	2	17	No	No	No	2	250	58285.8	4.2×10^{-3}	58.68	0.23	Yes	Yes
[32]	10	12	2	2	17	No	No	Yes	2	513	132149.7	3.8×10^{-3}	143.5	0.28	No	Yes
[40]	10	1	1	2	15	No	No	Yes	1.75	250	251981.3	0.99×10^{-3}	93.89	0.38	No	Yes
[41]	12	1	3	2	17	No	No	Yes	1.6	500	2110876.5	0.23×10^{-3}	159.6	0.32	No	Yes
[42]	18	2	6	2	17	No	No	Yes	4	260	1140977.1	0.23×10^{-3}	295.4	1.14	No	Yes
[43]	12	2	3	1	17	17	No	No	4	600	1168032.5	0.51×10^{-3}	188.74	0.32	No	Yes
[44]	18	0	2	1	17	No	No	No	2	500	356849.8	1.4×10^{-3}	252.9	0.50	No	Yes
[45]	9	0	0	3	15	No	No	No	1	113.75	23400	4.8×10^{-3}	117	1.03	Yes	No
MLI of [46]	24	4	4	4	17	No	No	No	4	500	696934.6	0.72×10^{-3}	372.6	0.75	Yes	Yes
[47]	14	0	4	4	17	No	No	No	2	1330.08	1182639.9	1.1×10^{-3}	402.71	0.31	No	Yes
Modified	14	4	4	1	17	Yes	Yes	Yes	2	777	62055.6	12×10^{-3}	156.3	0.20	No	Yes

Where, Pout and total volume denote the output power and total volume of each topology. To calculate the total volume of each topology, the volume of each of the energy storage components, such as the capacitors and inductors (inductor core), the volume of the used power switches and power diodes, according to the information contained in the datasheet of the mentioned components, have been obtained and added together numerically.

The result of this comparison is presented in Table 2. Considering this table, the modified multilevel inverter uses a flyback converter so, the desired 17-level output voltage waveform can be generated. It should be noted that the modified inverter is the superior one compared to most of the compared 17-levels output voltage with fewer circuit elements and input dc sources. According to Table 2, compared to most of the structures listed in Table 2, the modified structure offers a voltage boosting feature inherently with voltage gain of 2. Therefore, the introduced inverter is a better choice for industrial applications (such as photovoltaic applications).

Compared to other structures listed in Table 2, the capability of limiting the capacitive charging current spike can be highlighted. According to this table, it can be seen that none of the presented structures can provide this important feature. In addition, all of the given topologies haven't the ability of power reactive supporting except topologies [32], [40], [41] and [37].

Based on Table 2, the modified inverter can control both injected active and reactive powers to the grid. However, [45] cannot provide the voltage boosting ability. Therefore, the proposed structure has a higher power density and lower cost ratio (Cost/P_{out}) than the [43], which is economically viable.

Also, the structure presented in [43], unlike the modified structure, cannot limit the capacitor spike current and also the cannot support reactive power.

Compared with previously presented state-of-the-art multilevel inverters, the modified inverter can provide flexible voltage boosting performance by adjusting the turns ratio of the used transformer and also the duty cycle of the isolated DC-DC converter. Furthermore, Since the Modified topology uses an isolated dc-dc converter, it provides a galvanic isolation between the load or grid and dc source.

This can be a beneficial feature to block leakage current in many applications such as grid-connected PV applications. According to Table 2, the rest of the compared structures are not able to eliminate the leakage current. This is one the most important advantages of the modified PV system compared to the other presented PV inverters in Table 2. Considering Table 2, it can be seen that the modified SC-based MLI has the maximum value of the power density between all of the compared topologies.

This means that the modified MLI can transfer more power than other structures to its output. Also, the per-unit value cost (Cost/P_{out}) of the modified MLI is less than other compared topologies. Therefore, it can be concluded from Table 2 that the modified MLI is in good condition in terms of cost, power density, voltage boosting capability, capacitor spike current limiting capability, as well as reactive power capability, and is superior to most of the compared structures.

IX. SIMULATION RESULTS

To verify the limitation capacitor charging current feature of the modified inverter, the simulation results are presented and studied in this section. Also, the voltage stress and current stress of the power switches of inverter are studied. The modified structure is simulated at 777 W output power in a Simulink MATLAB environment. The used circuit elements

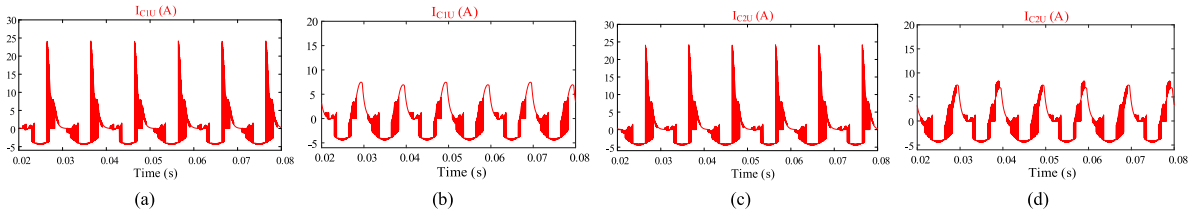


FIGURE 12. Simulation results: the current waveform of capacitor C_{1U}: (a) without inductor, (b) with an inductor, the current waveform of capacitor C_{2U}: (c) without inductor, (d) with an inductor.

TABLE 3 Specifications Used in the SIMULINK Model

Component	Specifications
Output power	777W
Input voltage	100V
C_1, C_2	1000μF
C_{1U}, C_{2U}, C_{1D} & C_{2D}	3300μF
L_f, L_1 & L_2	1mH
Switching frequency	20 kHz
Grid frequency	50Hz
Sampling time	50μs

TABLE 4 Specifications Used in the Experiment Prototype

Element	Type	Value
Input dc source	dc-source	$V_{in}=2V_{dc}=100V$
S_{1U}, S_{2U}, S_{3U}, S_{4U}, S_{5U}, S_{6U}, S_{1D}, S_{2D}, S_{3D}, S_{4D}, S_{5D}, S_{6D}, M & K	C3M0065090D	900V/36A
S_{F1} & S_{F2}	IRFP260N	200V/50A
Gate Driver	TLP 250	IC
d_U, d_D, d_1, d_2, d_{F1} & d_{F2}	RURP3060	600V/30A
Current Transducer	LA55P	Hall effect
Microcontroller	Beagle Bone Black	ARM
Switching frequency	20 kHz	-
Grid frequency	50Hz	-
Sampling time	50μs	-
C_1, C_2	1000μF	150V
C_{1U} , C_{2U}, C_{1D} & C_{2D}	3300μF	75V
L_f, L_1 & L_2	Ferrite Core	1mH

of the modified inverter in the Simulink model are listed in Table 3.

A. SIMULATION RESULTS FOR VALIDATION OF THE LIMITATION OF CAPACITOR CHARGING CURRENT SPIKE

As mentioned, the modified inverter can solve one of the most important problems of the switched capacitor, i.e., the occurrence of the inrush currents during charging capacitors by using a circuit unit that consists of an inductor with a parallel power diode in the capacitive charging current path. To prove the performance of the presented structure, comprehensive simulation results are presented in this section.

Fig. 12(a) and (b) indicate the capacitor charging current waveform of capacitor C_{1U} without and with using an inductor. Based on Fig. 12(a), the maximum value of the capacitor charging current spike of capacitor C_{1U} without using inductor L_1 is around 24 A. Considering Fig. 12(b), it can be seen that the peak value of capacitor charging current spike of capacitor C_{1U} using inductor L_1 is around 7.3 A or less than two times the peak value of injected current to the grid.

Fig. 12(c) and (d) show the capacitor current waveform of capacitor C_{2U} without and with using inductor L_1, respectively. Considering Fig. 12(c)–(d), it can be seen that the maximum value of the capacitor charging current spike of capacitor C_{2U} without using and with using inductor L_1 is around 24 A and 7.3 A, respectively. Fig. 13(a) and (b) show the capacitor current waveform of capacitor C_{1D} without and with using inductor L_2, respectively. Concerning this figure, the amplitude of the capacitor charging current spike of capacitor C_{1D} without inductor and with using inductor L_2 are around 24 A and 7.3 A, respectively. Also, the capacitor charging current waveform of capacitor C_{2D} without and with using inductor L_2 are illustrated in Fig. 13(c)–(d), respectively.

Regarding this figure, it can be seen that the amplitude of capacitor charging current spike of capacitor C_{2D} without and with using inductor L_2 is around 24 A and 7.3 A, respectively. Therefore, it can be concluded from the obtained results that the presence of the inductors L_1 and L_2 in the capacitor charging paths have drastically limited the capacitor charging current spike. Therefore, it can be concluded from the obtained results that the presence of the inductors L_1 and L_2 in the capacitor charging paths have drastically limited the capacitor charging current spike. Considering that the load current is 5 A, and taking into account that with and without the inrush current limiting inductors (L_1 and L_2) the charging current of the capacitors are all 7.3 A, and 24 A respectively, it is understood that these inductors can effectively limit the inrush current by 35%.

B. COMPARE THE CAPACITORS' VOLTAGE RIPPLE, AND OUTPUT VOLTAGE THD WITH AND WITHOUT THE DIODE-INDUCTOR CIRCUITS USING SIMULATION RESULTS

In order to show the effect of the diode-inductor circuits on the capacitors' voltage ripple, and output THD, the simulation results without and with using diode-inductor circuits are presented in this section. Fig. 14(a), and (b) illustrates the voltage ripple of capacitor C_{1U} without using and with using diode-inductor (d_1&L_1) circuit in the capacitor charging loop, respectively.

By comparing Fig. 14(a) and (b), it can be seen that the voltage ripple of capacitor C_{1U} without using diode-inductor circuit is a little bit less than the voltage ripple with using diode-inductor circuit in the capacitor charging loop.

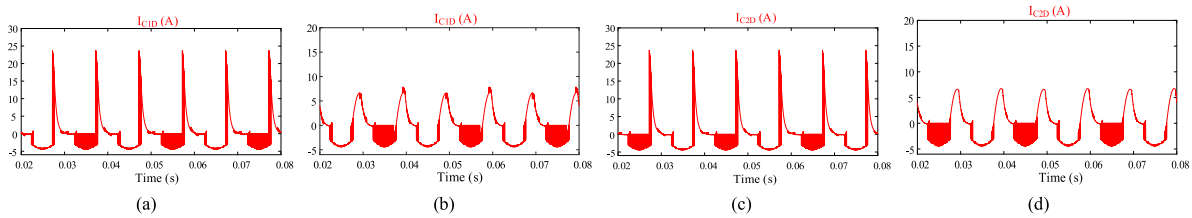


FIGURE 13. Simulation results: the current waveform of capacitor C_{1D}: (a) without inductor, (b) with an inductor, the current waveform of capacitor C_{2D}: (a) without inductor, (b) with an inductor.

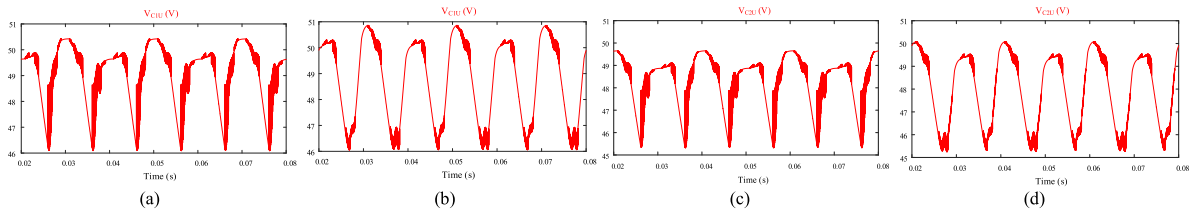


FIGURE 14. Simulation results: capacitors' voltage ripple: (a) capacitor C_{1U} without using diode-inductor circuit, (b) capacitor C_{1U} with using diode-inductor circuit, (c) capacitor C_{2U} without using diode-inductor circuit, (d) capacitor C_{2U} with using diode-inductor circuit.

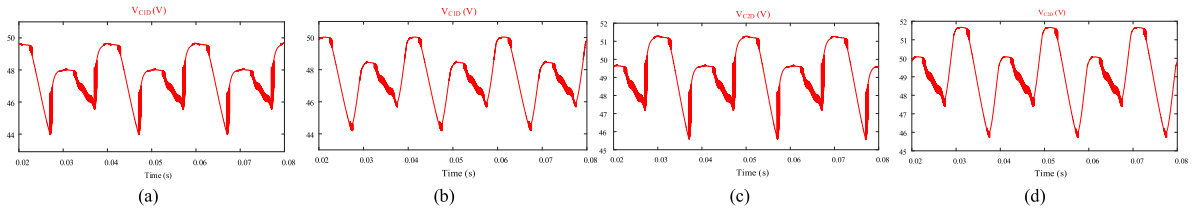


FIGURE 15. Simulation results: capacitors' voltage ripple: (a) capacitor C_{1D} without using diode-inductor circuit, (b) capacitor C_{1D} with using diode-inductor circuit, (c) capacitor C_{2D} without using diode-inductor circuit, (d) capacitor C_{2D} with using diode-inductor circuit.

Meanwhile, regarding Fig. 14, in the case of using the diode-inductor circuit, the capacitor C_{1U} is charged to a greater value than when it is not used.

The voltage ripple of capacitor C_{2U} without and with using the diode-inductor circuit in the charging path of capacitors are indicated in Fig. 14(c), and (d), respectively. Considering this figure, the voltage ripple of capacitor C_{2U} without using diode-inductor circuit is a little bit less than the with using this circuit. However, the capacitor C_{2U} with using diode-inductor can be charged more than state without using diode-inductor circuit.

Fig. 15(a)–(d) show the voltage ripple of capacitor C_{1D} and C_{2D} without and with using the diode-inductor circuits in the charging path of capacitors, respectively. By comparing these figures, it can be concluded that although the voltage ripple of the capacitors increases slightly with the use of diode-inductor circuits, the capacitors can be charged to a greater amount than without the use of the diode-inductor circuits.

The THD of output voltage waveform without and with using diode-inductor circuits are illustrated in Fig. 16(a), and (b), respectively. Based on Fig. 16, the THD value of output voltage is a little bit improved by using diode-inductor circuit.

C. VOLTAGE AND CURRENT STRESS OF THE SWITCHES OF MODIFIED INVERTER

The simulation results of the voltage and current stress of inverter's switches are provided here. The voltage stress of switches S_{1U}~S_{6U} are illustrated in Fig. 17(a)–(f), respectively. Fig. 17(a) shows the voltage stress of switch S_{1U}. considering this figure, the maximum blocked voltage of switch S_{1U} is 200 V or $2V_{in}$. regarding Fig. 17(b), the maximum blocked voltage of switch S_{2U} is 150 V or 1.5 V_{in}. Considering Fig. 17(c), the maximum blocked voltage of switch S_{3U} is 200 V or 2 V_{in}. Also, it can be seen that from Fig. 17(d), the maximum blocked voltage of switch S_{4U} is 50 V or 0.5 Vin. Regarding this figure, the voltage waveform of switch S_{4U} includes both positive and negative cycles. Therefore, for the correct operation of the modified inverter, switch S_{4U} is selected as a bidirectional type. The voltage stress of switch S_{5U} and S_{6U} are illustrated in Fig. 17(e)–(f), respectively. With respect to this figure, it can be seen that the maximum blocked voltage of switch S_{5U} and S_{6U} are 100 V or V_{in}. Fig. 18(a), and (b) shows the voltage stress of switches K and M, respectively.

Regarding this figure, the maximum blocked voltage of switches K and M are equal to 400 V or 2 Vin, respectively.

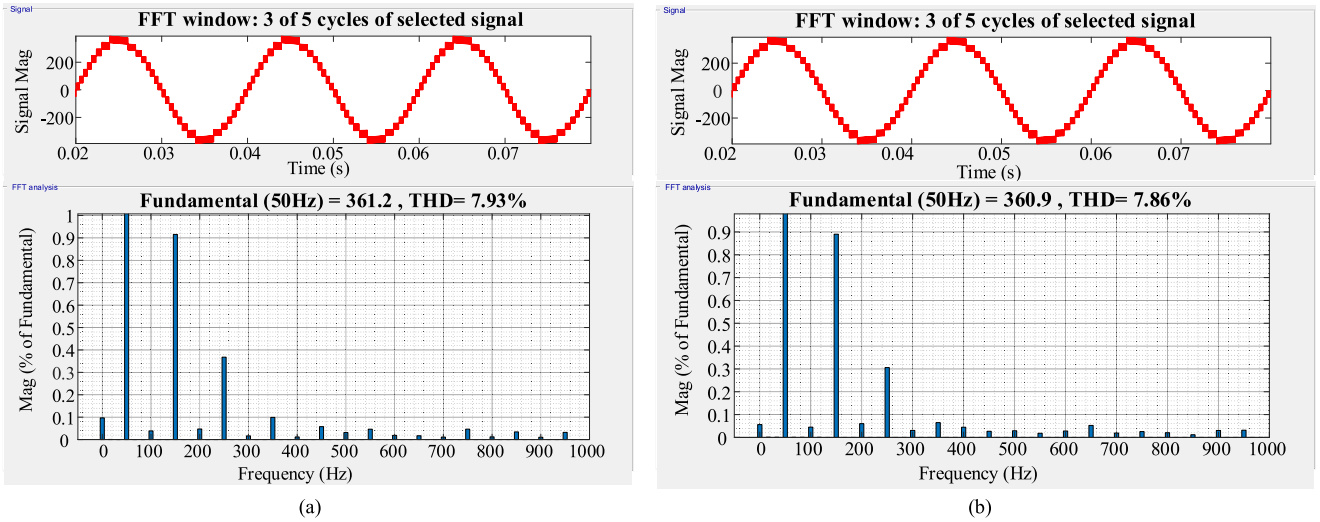


FIGURE 16. Simulation results: output voltage THD: (a) without using diode-inductor circuits, (b) with using diode-inductor circuits.

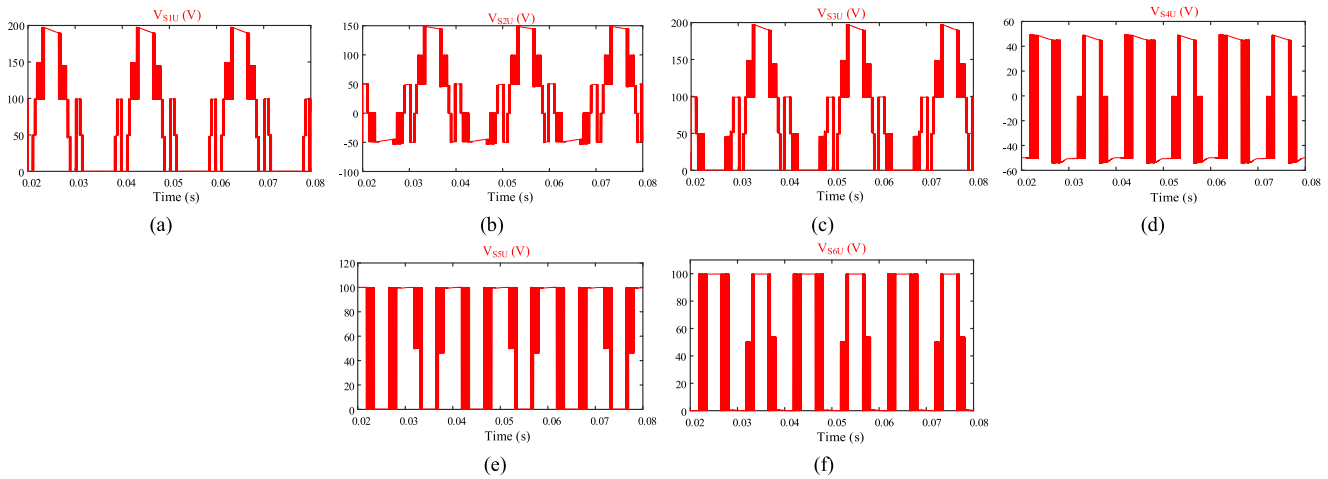


FIGURE 17. Simulation results: voltage stress of switches: (a) switch S_{1U}, (b) switch S_{2U}, (c) switch S_{3U}, (d) switch S_{4U}, (e) switch S_{5U}, (f) switch S_{6U}.

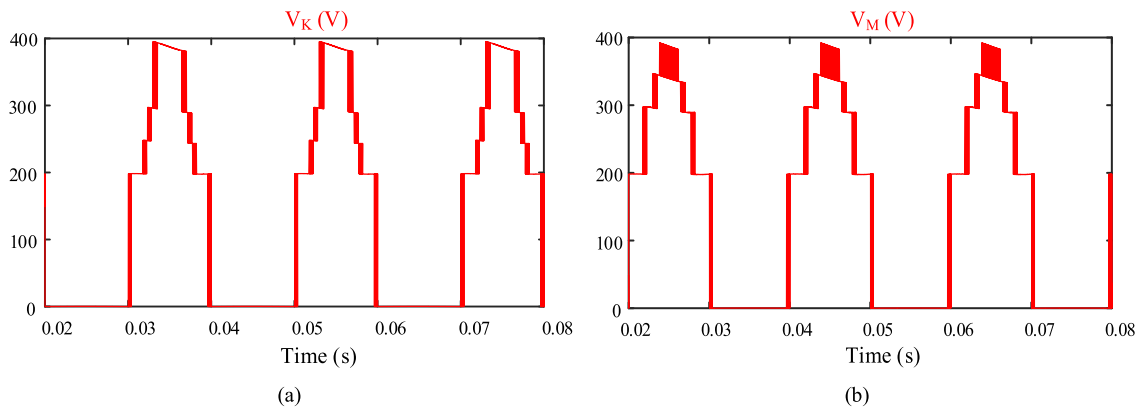


FIGURE 18. Simulation results: voltage stress of switches: (a) switch K, (b) switch M.

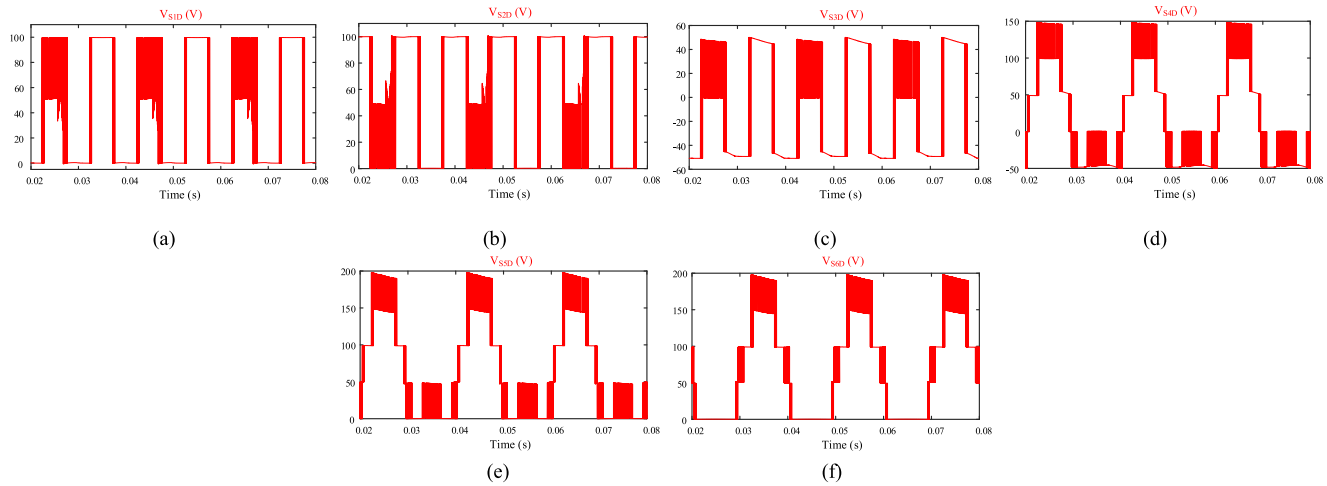


FIGURE 19. Simulation results: voltage stress of switches: (a) switch S_{1D}, (b) switch S_{2D}, (c) switch S_{3D}, (d) switch S_{4D}, (e) switch S_{5D}, (f) switch S_{6D}.

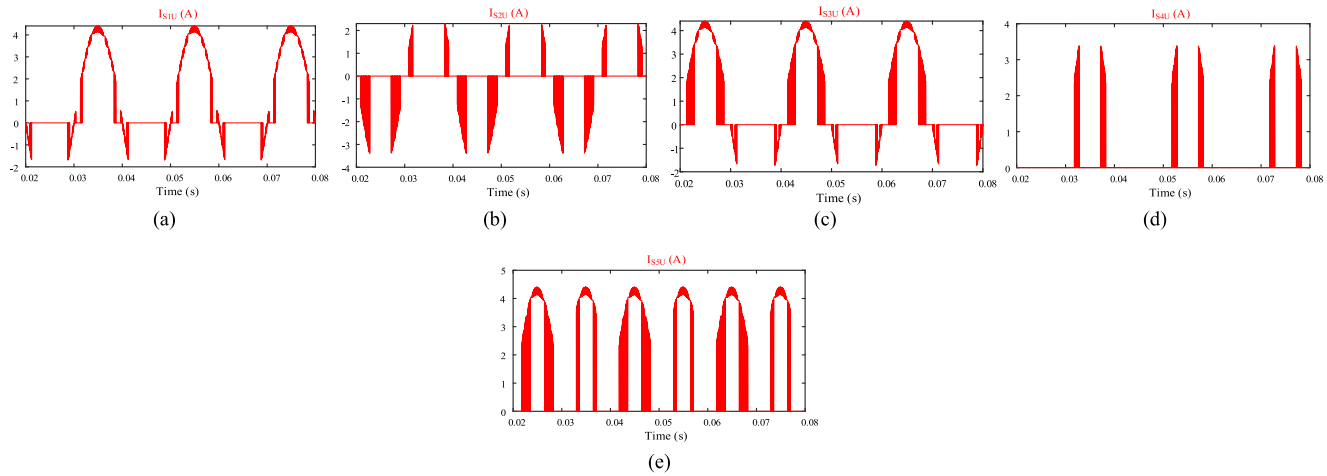


FIGURE 20. Simulation results: current stress of switches: (a) switch S_{1U}, (b) switch S_{2U}, (c) switch S_{3U}, (d) switch S_{4U}, (e) switch S_{5U}.

Further, the voltage stress of switches S_{1D}∼S_{6D} are illustrated in Fig. 19(a)–(f), respectively. The voltage stress of switches S_{1D}, and S_{2D} are shown in Fig. 19(a), and (b), respectively. Regarding this figure, the maximum blocked voltage of switches S_{1D}, and S_{2D} are equal to 100 V or V_{in}. The voltage stress of switch S_{3D} is indicated in Fig. 19(c).

Based on this figure, the maximum blocked voltage is 50 V or 0.5 V_{in}. Also, the voltage stress of switch S_{4D} is shown in Fig. 19(d). Considering this figure, the maximum blocked voltage of switch S_{4D} is 150 V or 1.5 V_{in}. The voltage stress of switches S_{5D}, and S_{6D} are shown in Fig. 19(e)–(f), respectively. Regarding this figure, the maximum blocked voltage of switches S_{5D}, and S_{6D} are 200 V. In addition, the current stress of inverter's switches S_{1U}∼S_{5U} are illustrated in Fig. 20(a)–(e), respectively. Based on Fig. 20(a), the maximum value of current stress of switch S_{1U} is almost equal to 4.2 A. Also, the current stress of switch S_{2U} is shown in Fig. 20(b).

Based on this figure, the maximum value of passing current through the switch S_{2U} is almost equal to 2.2 A. Fig. 20(c) illustrates the current stress of switch S_{3U}. Regarding this figure, the maximum value of current stress of switch S_{3U} is almost equal to 4.2 A. Also, Fig. 20(d) shows the current stress of switch S_{4U} with the maximum value of 3.2 A. The current stress of switch S_{5U} with maximum value of 4.2 A is shown in Fig. 20(e).

Fig. 21(a), and (b) show the current stress of switches K, and M, respectively. Considering Fig. 21, the maximum value of passing current through switches K, and M are almost equal to 4.2 A. In addition, the current stress of switches S_{2D}∼S_{6D} are indicated in Fig. 22(a)–(e), respectively. Based on this figure, it can be seen that the maximum value of passing current through the mentioned switches are almost equal to 4.2 A. As mentioned before, in the modified inverter, by installing an inductor in parallel with a diode in the capacitor charging

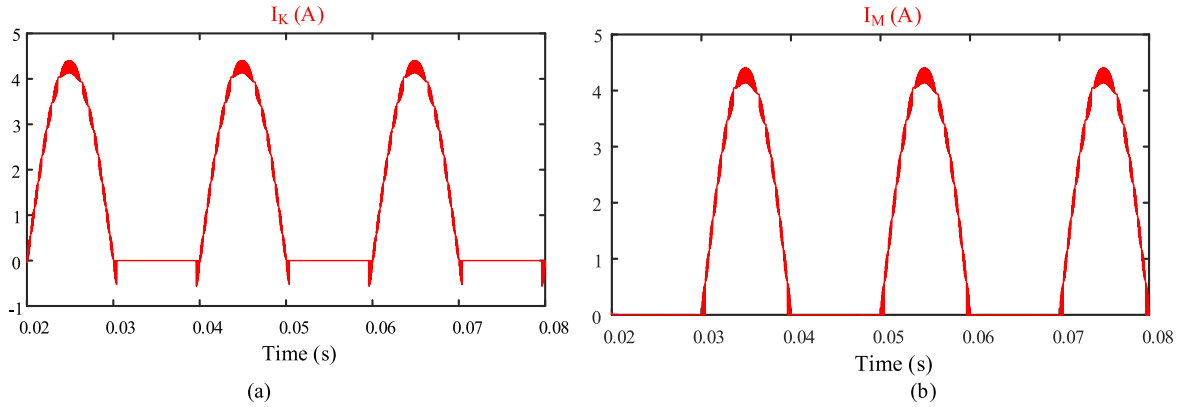


FIGURE 21. Simulation results: current stress of switches: (a) switch K, (b) switch M.

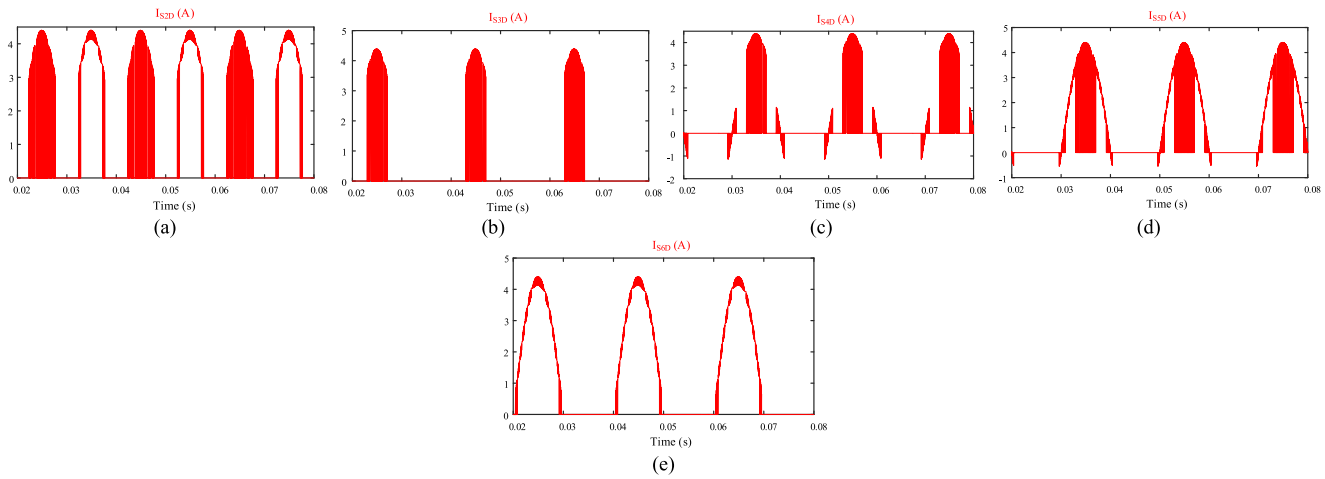


FIGURE 22. Simulation results: current stress of switches: (a) switch S_{2D}, (b) switch S_{3D}, (c) switch S_{4D}, (d) switch S_{5D}, (e) switch S_{6D}.

path, the spike of the capacitor charging current is reduced and the capacitors are charged smoothly.

By reducing the spike of the capacitor charging current, the spike amplitude of the current passing through the switches involved (S_{6U}, and S_{1D}) in the capacitor charging loops is reduced and the current passing through them is softened. In order to verify this issue, the simulation results related to current stress of switches S_{6U}, and S_{1D} are presented in Figs. 23, and 24, respectively. Fig. 23(a) illustrates the current stress of switch S_{6U} without using inductor L_1 in the charging loop. Regarding this figure, the spike amplitude of passing current through the switch S_{6U} is almost equal to 24 A. Fig. 23(b) shows the waveform of passing current trough the switch S_{6U} with using inductor L_1 in the charging loop.

Considering Fig. 23(b), it can be seen that the maximum value of current stress of switch S_{6U} is almost equal to 7.3 A. By comparing Fig. 23(a), and (b), it can be understood that by using the inductor L_1 in the capacitor charging loop, the amplitude spike of passing current passing through the switch S_{6U} which is located in the capacitator charging loop is reduced. The reduction percentage is almost equal to 35%.

Fig. 24(a) illustrates the waveform of passing current through the switch S_{1D} with using inductor L_2 in the capacitor charging loop. Regarding Fig. 24(a), the spike magnitude of passing current through the switch S_{1D} is almost equal to 24 A. Also, the waveform of passing current though the switch S_{1D} with using inductor L_2 in the charging loop is shown in Fig. 24(b). Based on this figure, the maximum value of passing current though the switch S_{1D} is almost equal to 7.3 A. By comparing Fig. 24(a), and (b), it can be seen that by using the inductor L_2 charging pass of capacitors, the amplitude spike of passing current passing through the switch S_{1D} which is located in the capacitator charging loop is reduced. The reduction percentage is almost equal to 35%. Regarding the provided simulation results, it can be concluded that the modified topology has good a feasibility by providing the limitation of capacitor charging spike.

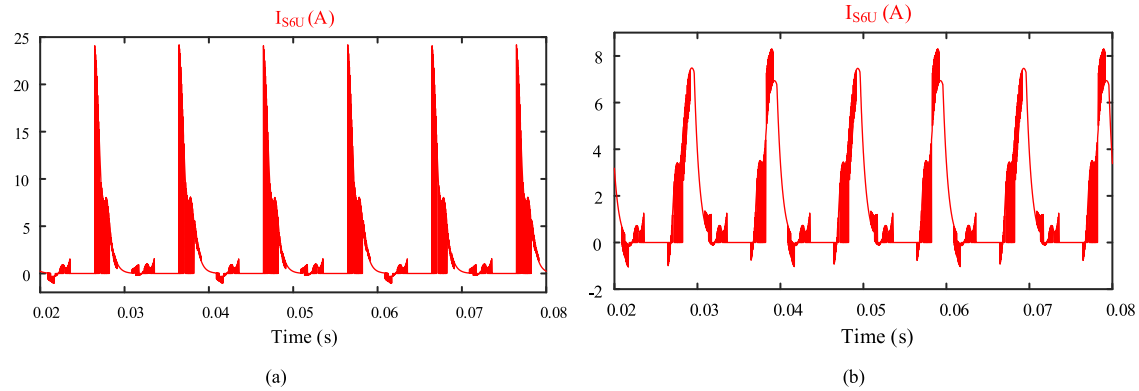


FIGURE 23. Simulation results: current stress of switch S_{6U}: (a) without using inductor L_1 in charging path, (b) with using inductor L_1 in charging path.

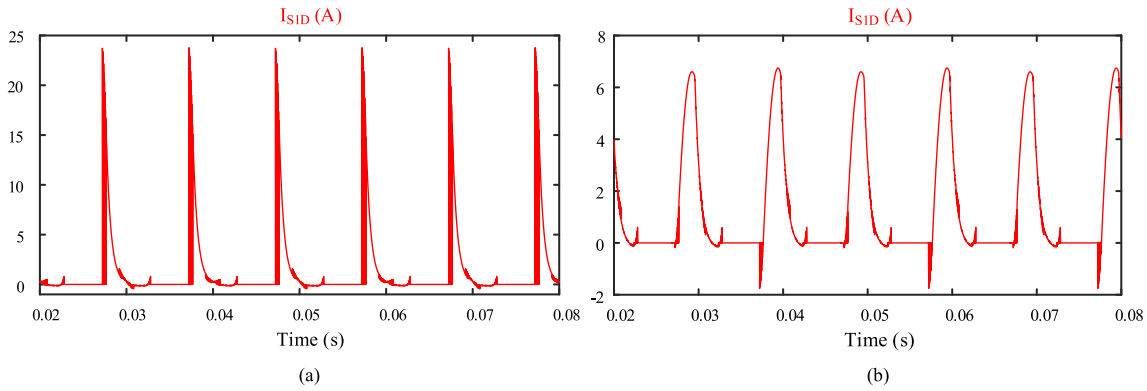


FIGURE 24. Simulation results: current stress of switch S_{1D}: (a) without using inductor L_2 in charging path, (b) with using inductor L_2 in charging path.

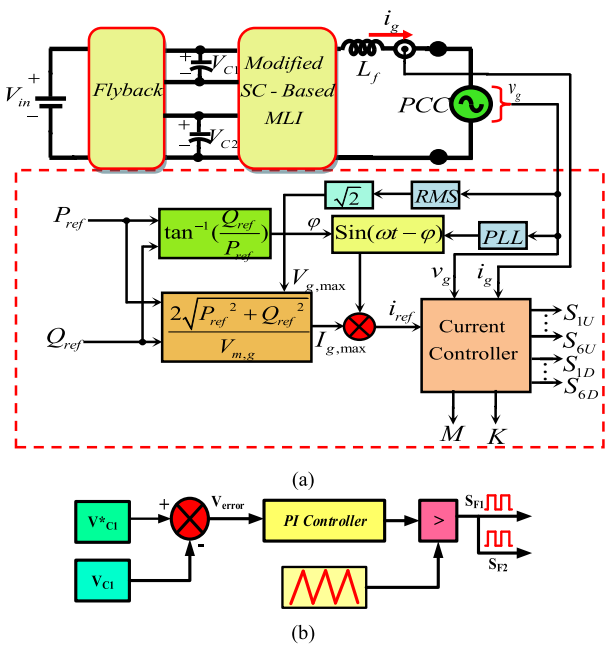
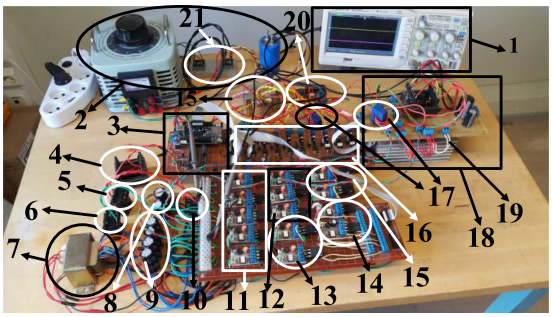


FIGURE 25. Schematic of control system applied for (a) modified SC-based MLI (b) fly back based DC-DC converter.

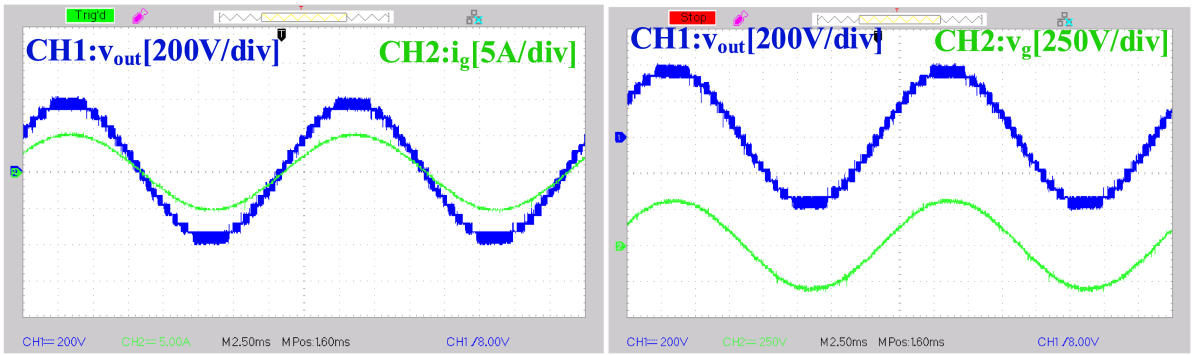


1. Oscilloscope, **2.** Auto transformer for power supply, **3.** Microcontroller board, **4.** Inductor output filter L_f, **5.** Inductor L_1, **6.** Inductor L_2, **7.** Isolated transformer for gate driver circuit of inverter, **8.** Capacitors C_1 & C_2, **9.** Capacitors C_{1U}, C_{2U}, C_{1D} and C_{2D}, **10.** Parallel diodes d_1 & d_2, **11.** Switches S_{1U}, S_{3U}, S_{5U}, S_{6U}, S_{1D}, **12.** Switches S_{2D}, S_{5D} and S_{6D}, **13.** Switches S_{2U} & S_{4U}, **14.** Switches K & M, **15.** Switches S_{3D} & S_{4D}, **16.** Gate driver board of flyback converter, **17.** LEM current sensors, **18.** Power circuit of flyback converter, **19.** Heatsink, **20.** Driver board of current sensors, **21.** Bridge diode.

FIGURE 26. Photo of the experimental prototype of the modified topology.

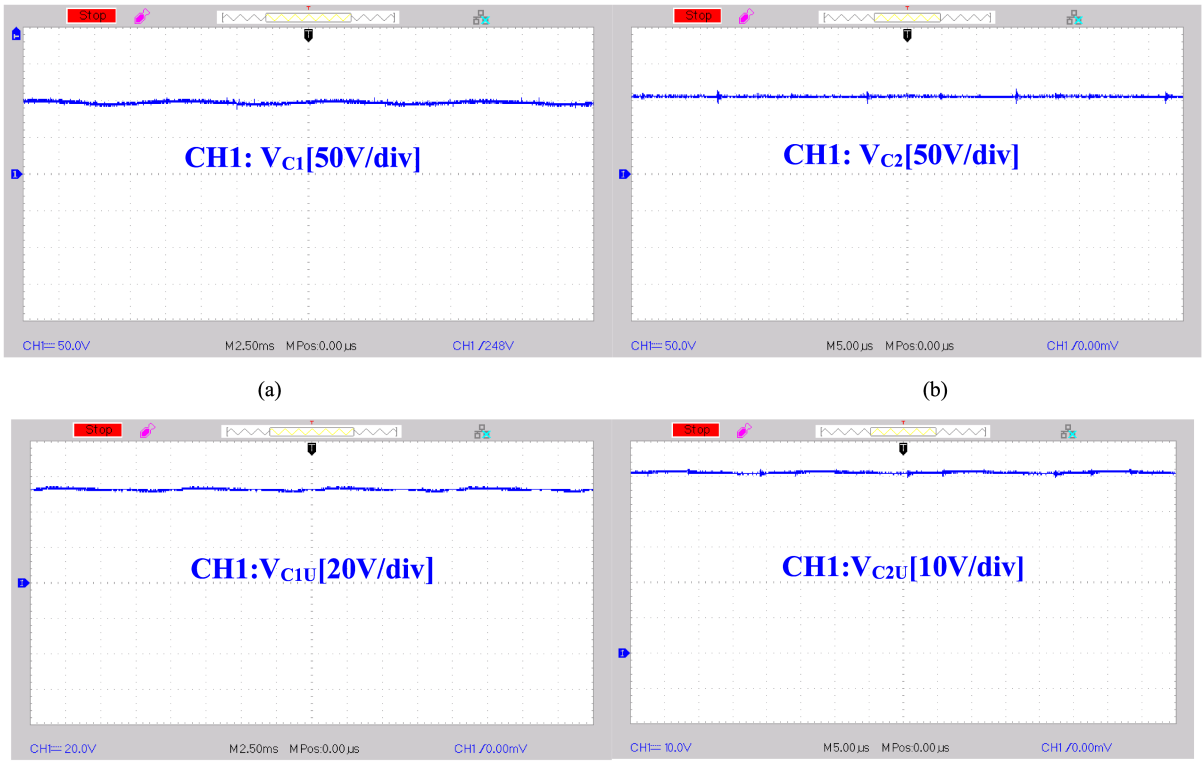
X. EXPERIMENTAL RESULTS

In this section, in order to verify the accurate performance of the SC-based 17-level inverter, some experimental results



(a) (b)

FIGURE 27. The experimental results: (a) the output voltage of the inverter (200 V/div) and the injected current (5 A/div) (b) and the local grid voltage (250 V/div) and injected current to the grid (5 A/div).



(a) (b)

(c) (d)

FIGURE 28. Voltage across (a) the capacitor C_1 (50 V/div) (b) the capacitor C_2 (50 V/div) (c) the capacitor C_{1U} (20V/div) (d) the capacitor C_{2U} (10V/div).

have been obtained at 770W output power in the grid-tied mode of operation. In this case study, to drive the power switches of the inverter, a peak current control (PCC) strategy is applied. By applying this technique, both active and reactive injected powers to the grid are controlled [22], [48], [49], [50].

Fig. 11, illustrates the control system of the modified SC-based MLI and applied flyback-based DC-DC converter. Considering Fig. 25(a), to detect the desired phase and amplitude of the local grid, a phased locked loop (PLL) is applied [22]. Considering the reference values of active and reactive injected powers, the amplitude and phase of the injected current to the grid (i_{ref}) can be obtained. Then, to generate the gate pulses of the utilized switches of the inverter, this obtained reference value (i_{ref}) is delivered to the current control unit. Fig. 25(b) shows the control system of the applied DC-DC converter. Based on this figure, to generate the gate pulse of S_{F1} and S_{F2} the PI controller is used. Fig. 26 illustrates the photo of the experimental prototype of the modified inverter.

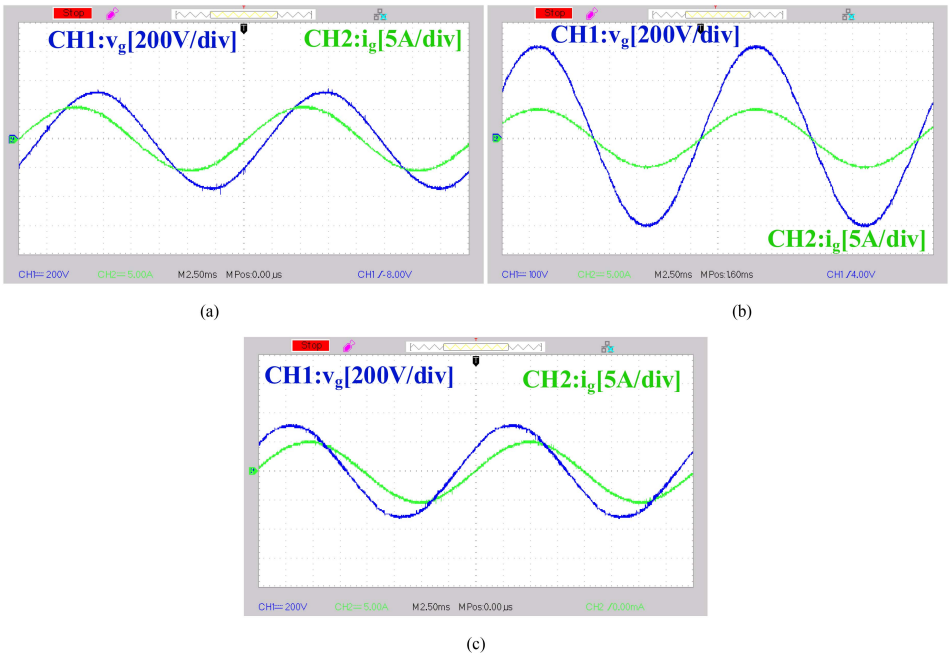


FIGURE 29. The grid voltage and the injected current waveforms under: (a) leading PF (200 V/div & 5 A/div) (b) unity PF (100 V/div & 5 A/div) (c) lagging PF (200 V/div & 5 A/div).

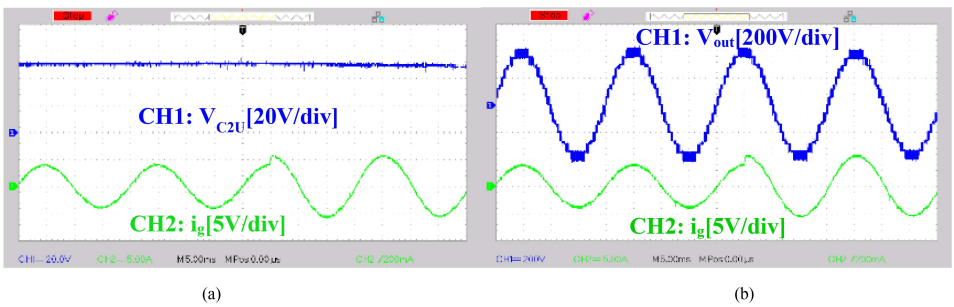


FIGURE 30. The experimental results under the applied step-change: (a) the voltage of the capacitor C_{2U} and the current of the grid (20V/div & 5 A/div) (b) the output voltage of the inverter and injected current to the grid (200 V/div & 5 A/div).

The used circuit elements of the modified grid-tied inverter are listed in Table 3. A 17-level output voltage waveform of the inverter with a magnitude of 400 V is illustrated in Fig. 27(a). Voltage boosting feature of the modified inverter can be verified based on this figure. Concerning this figure, the injected grid current is a sinusoidal waveform with the amplitude of 5 A and unity power factor (PF). With respect to Fig. 27(b), the grid voltage and the inverter output voltage are presented. Based on the results, the desirable performance of the modified MLI along with the presented control method is validated. Also, it can be concluded that the modified inverter is suitable for numerous modern applications where high-quality power is needed to be injected into the grid.

In Fig. 27(b), the maximum values of the inverter output voltage waveform and the grid voltage waveform are equal to 400 *V* and 311 *V*, respectively. Considering these results, both the modified MLI and the applied PCC strategy have proper performances. Fig. 28(a)–(d) respectively show the voltages across the capacitors C_1, C_2, C_{1U} and C_{2U}. Based on this figure, it can be seen that the voltage across of capacitors C_1 and C_2 (output flyback capacitors) which are successfully charged to 100 V. Therefore, it is verified that the applied flyback converter could be generated two isolated voltages with the same values to supply modified MLI.

Also, Fig. 28(c) and (d) show that the voltage across capacitors C_{1U} and C_{2U} are successfully charged to 50 V. Therefore, the performance of the self-balancing the capacitors voltages of SC-based MLI is proved. To verify the supporting active and reactive injected powers feature of the modified MLI, the injected current and grid voltage under three different conditions, i.e., leading, unity, and lagging PF, are illustrated in Fig. 29(a), (b) and (c), respectively. As seen, the amplitude of the injected current to the grid is about 5 A. Hence, the injected power to the grid is 0.77 kW. In Fig. 16, the

experimental results of the modified grid-tied system by applying a step-change in reference current amplitude are shown. In Fig. 30(a), the voltage of the capacitor C_{U2} and the current of the grid are shown. Fig. 30(b) shows the output voltage of the inverter and injected currents to the grid.

As seen, by changing the amplitude of the injected current into the grid from 4 A to 5 A, the output power increases from 622 W to 777 W.

XI. CONCLUSION

In this article, a new 17-levels SC-based MLI is modified by employing the flyback converter which in turn leads to need power elements with lower ratings. This inverter provides the voltage boosting feature with the gain factor of 2. Also, it can pass the reverse current for inductive loads through the exiting power switches. The DC-DC flyback converter is used to generate two independent DC voltages from the single input power supply which is an important economic advantage. The modified inverter uses two circuits, an inductor, and a parallel diode to limit the spike current of capacitors during the capacitor charging mode. This is one of the most important advantages of the modified inverter. Besides, by using the PCC method, the modified inverter can control the amount of the active and reactive injected into the grid. Based on the performed comparison, the modified topology has a lower cost and maximum power density than other topologies. Further, in order to verify the accurate performance of the modified inverter and prove the advantages of this topology such limitation the capacitors charging current spike, simulation results have been presented. Based on the experimental results performed for the modified inverter in grid-connected condition, this SC-based MLI has a desirable performance.

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