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Common DC-Link Multilevel Converters: Topologies, Control and Industrial Applications

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ABSTRACT Multilevel converters (MLCs) are widely recognized for their exceptional benefits and have emerged as the preferred choice for medium- and high-power/voltage applications. Their usage has also been extended to low-power applications to overcome issues associated with high switching frequencies and electromagnetic interference (EMI) commonly encountered in two-level converters. Common dc-link MLCs have received particular attention in industry due to their ability to eliminate the need for bulky and inefficient transformers and rectifiers, making them a compelling option for different applications, primarily medium- and high-power/voltage applications such as wind turbine (WT) power conversion systems. Furthermore, common dc-link topologies are required for back-to-back (BTB) configurations, as they facilitate the use of a shared dc-link between the rectification and inversion stages. Despite their popularity, there is currently no comprehensive review article dedicated to common dc-link topologies. This article addresses this gap by presenting a comprehensive review of common dc-link MLCs, covering their topological evolution, features, topologies comparison, modulation techniques, control strategies, and industrial application areas. Additionally, future perspectives and recommendations are discussed to provide researchers and engineers with a better understanding of the potential applications and advantages of these converters.

INDEX TERMS Multilevel converters, common dc-link, reduced components, modulation, control, high-power applications.

I. INTRODUCTION

The demand for electrical energy from renewable sources has been rapidly increasing in recent years. According to the "Renewables 2022" report by the International Energy Agency (IEA), renewable electricity generation is expected to increase by almost 2400 GW between the years 2022 and 2027, representing an increase of 75% [1]. This upward trend can be attributed to an increasing awareness of the environmental and economic benefits of renewable energies (REs), as well as advancements in power electronics systems, making REs more cost-effective and efficient. This trend is expected to continue as the need for sustainable and clean energy sources increases to meet the growing energy demand and combat climate change.

DC/AC power converters play a critical role in the energy harvesting process from REs. Their ability to optimize the energy generated by these sources, as well as their impact on the efficiency, reliability and cost-effectiveness of these systems, make them an essential component in the integration of RE into the power grid. The employment of conventional two-level converters in medium- and high-power applications is typically limited by the voltage ratings of the power switches available on the market. With these converters, the use of series-connected switches is necessary when commercially available power devices cannot meet the voltage requirements of the application. However, this approach raises the problem of dynamic voltage sharing between the switches [2]. For the sake of solving this issue, the concept of a multilevel converter (MLC) was invented [3], [4]. MLCs use an arrangement of power devices and DC sources to create a staircase output voltage waveform, providing numerous attractive merits compared to conventional two-level converters such as [5], [6], [7], [8], [9]:

1) The ability to deliver higher-quality waveforms with lower harmonic contents at a lower switching frequency, reducing bulky and expensive filter requirements and electromagnetic interference (EMI);
2) The ability to handle medium/high-voltage applications using standard commercial power devices without the need for series-connected switches, eliminating the associated dynamic voltage sharing problem;
3) The operation at a low switching frequency reduces switching losses, increasing the maximum output power and improving system efficiency;
4) Reduction of dv/dt on switches and low/zero common-mode voltage (CMV), which are highly desirable in various applications such as medium-voltage (MV) drive systems to reduce the insulation stress on the machine windings and the bearing failure; and
5) The capability for fault-tolerant operation thanks to the existing redundancies in the switching states, improving the reliability of the power conversion system.

Thanks to their outstanding advantages, MLCs have become the preferred choice for medium- and high-voltage/power applications [9], [10]. Moreover, the use of MLCs has been extended to low-voltage/power applications to avoid the problematic issues of two-level converters associated with the necessary operation at a high switching frequency and the EMI [11], [12], [13]. MLCs offer a compact and efficient solution for low-voltage applications where space constraints and power density are crucial considerations. By generating multiple voltage levels, MLCs can achieve the desired power output while minimizing the size and weight of the system, especially filtering and cooling system requirements. In addition, the remarkable advancements in wide-bandgap devices, such as SiC and GaN power devices, have spurred significant research efforts aimed at leveraging their potential to enhance the power density and efficiency of MLCs in low-voltage applications [14], [15], [16].

Since the inception of the MLC concept, several topologies have been introduced, and some of them are currently mature technologies in the industry for different application fields. Fig. 1 shows the major evolution of MLCs during the last decades. MLC innovation has been started with the cascaded H-bridge (CHB) converter in the 1970s [3], followed by the neutral-point-clamped (NPC) converter in the 1980s [17], [18], [19] and the flying capacitor (FC) converter in the 1990s [20], [21]. These three converters are known as conventional topologies and form the basis for other topologies that were later developed. In the early 2000s, the modular multilevel converter (MMC) [22] and stacked multicell converter (SMC) were introduced with high modularity for high-voltage applications [23]. Combining the robustness of the NPC with the flexibility of the FC topology, the five-level active NPC (5L-ANPC) converter was introduced later in 2005 for industrial MV applications up to 6.9 kV [24], [25]. Over the past decade, several hybrid topologies have been introduced with the aim of reducing the required components. However, only a very few topologies have been employed successfully in industry, such as the 3L T-type (3L-T^{2}C) and 5L packed u-cell (5L-PUC) converters for low-voltage applications [12], [26], [27].

Considering the major evolutionary stages of MLCs, the existing MLC topologies can be categorized into some families, as shown in Fig. 2. The first family includes CHB-based topologies and has been reviewed in [28], [29], [30], [31], [32]. These converters feature high modularity and an optimal number of power switches for output levels [31]. However, multiple isolated DC sources are required, necessitating the use of bulky isolation transformers or limiting their employability to applications that have several isolated DC sources. In addition, uneven power sharing between the cascaded power cells is one of the common challenges in this family [33], [34]. The second family includes NPC-based topologies such as 3L-NPC and 3L-T^{2}C converters. These converters are characterized by robust power circuits and straightforward protection. However, dc-link balancing is an essential requirement in the control design of these topologies. FC-based topologies use capacitors as clamping components to increase the number of levels, forming an MLC family characterized by high flexibility, high redundancies and fault-tolerant operation. Hybrid MLCs are formed by basic cells of the conventional topologies and, therefore, combine several advantages of classical MLCs with the capability to produce a high number of levels. MMC topologies constitute an MLCs family that represents a breakthrough for HV applications due to its high efficiency and high modularity. However, the control problem of MMC is a challenging task due to raising additional issues like circulating current limitation.

The utilization of a common dc-link voltage source converter (VSC) is an essential requirement for some applications, primarily medium- and high-power/voltage applications such as wind turbine (WT) power conversion systems. This is because providing an additional isolated DC source means the use of a bulky and inefficient transformer in conjunction

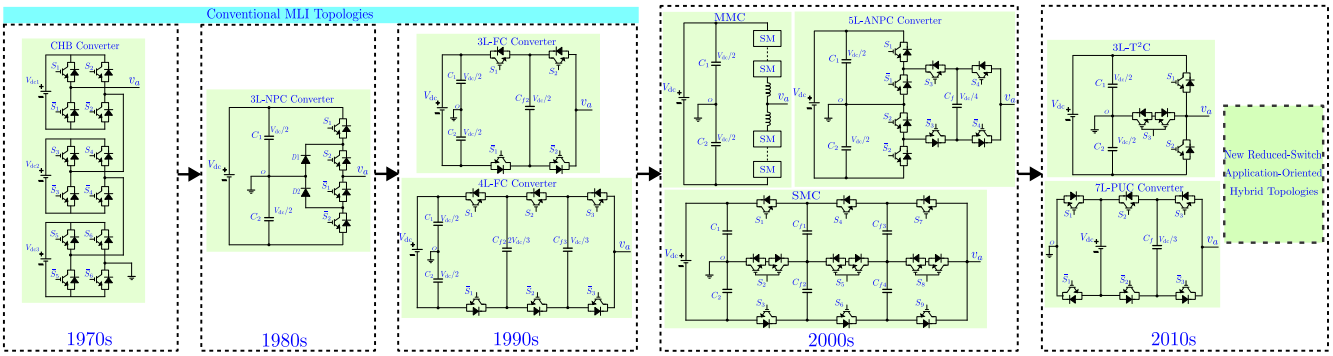

FIGURE 1. Major evolutions of MLC topologies over the past decades.

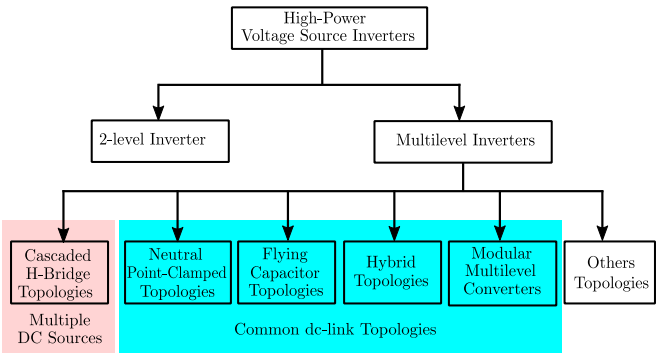

FIGURE 2. Classification of high-power voltage source inverters.

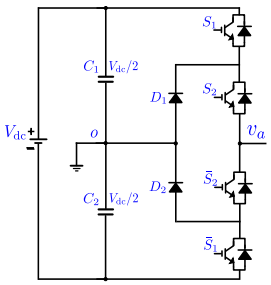

FIGURE 3. One phase-leg of the conventional three-level NPC inverter.

with a diode bridge rectifier, significantly increasing the size and cost of the system. Furthermore, applications that rely on a back-to-back (BTB) configuration utilize a shared dc-link between the rectification and inversion stages, which necessitates the use of topologies featuring a common dc-link for both stages. In addition, common dc-link MLCs can be fully integrated into power conversion systems where traditional two-level converters are already in operation, without the need for modifications on both the DC and AC side, and with minimal adjustments to the controller design, as only one dc-link voltage needs to be regulated [8]. This explains the prevalence of common dc-link topologies in industrial applications. For instance, for battery-powered automotive industry, the voltage levels are on the rise, therefore, MLCs have been proposed to replace the conventional two-level converters. In doing so, common dc-link topologies are recommended as they fit the application requirements [35]. A plethora of reviews on MLC topologies can be found in the literature [6], [7], [8], [28], [32], [36]. However, to date, no comprehensive review article specifically addressing common dc-link topologies has been published yet.

The remainder of this article is organized as follows. The common dc-link topologies are classified, reviewed and discussed in Section II. A detailed quantitative and qualitative comparison is presented in Section III. The common modulation and control methods are discussed in Section IV. Section V covers the industrial applications of the common dc-link MLCs. The recommendations and future trends are provided in Section VI. Finally, the conclusion is drawn in Section VII.

II. COMMON DC-LINK TOPOLOGIES

A. NPC CATEGORY (MID-POINT CLAMPED)

One of the most widely utilized topologies of MLCs is the neutral-point clamped converter (NPC). The three-level NPC structure is used broadly in various industrial, automotive, and drive applications mostly due to its high performance and simplicity. The structure of a basic three-level NPC inverter is shown in Fig. 3. With the basic NPC topology, moving toward a larger number of levels is usually not recommended due to control limitations and the considerable increase in the number of clamping diodes [8].

Although the straightforward structure and control of the three-level NPC look promising, several major limitations have led to extensive research on advanced NPC-based topologies to overcome those limitations. A major issue with the three-level NPC structure is the unbalanced loss distribution in the switches of each leg which leads to a drop in the power density due to the unequal maximum junction temperature in the switches [37]. Another limitation is its use in higher-voltage applications due to the high cost of the converter at higher levels. The most famous NPC-based topologies are introduced in this subsection.

1) ANPC

The three-level Active NPC (ANPC) structure has been able to address the issue of power loss sharing through the use of two different modulation techniques called modulation patterns

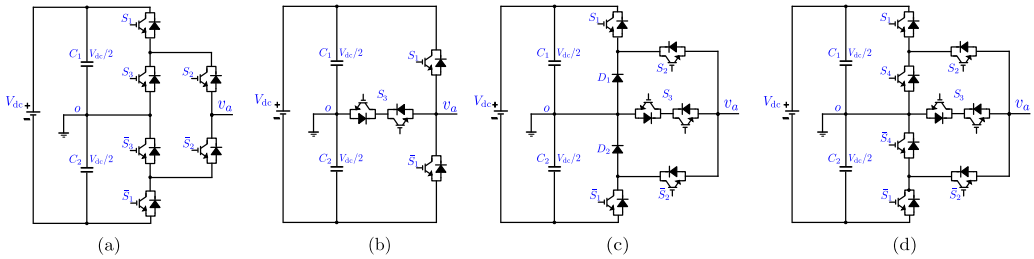

FIGURE 4. One phase-leg of common NPC converters: (a) 3L-ANPC converter, (b) 3L-T^{2}C, (c) 3L-SNPC converter, and (d) 3L-ASNPC converter.

I and II. The topology is shown in Fig. 4(a) in which the two clamping diodes are replaced with two active switches to control the current flow direction in zero states. Modulation pattern I cause most of the switching loss to occur in the outer switches of each leg, while pattern II moves the switching losses to the inner switches. However, using only one of these patterns for the entire period does not balance the loss, so research has looked into ways to use a combination of the two patterns and modify the inverter structure to better balance the loss [37].

A double-frequency (DF) modulation, investigated in [38], can distribute the switching events evenly between the inner and outer switches, resulting in an equal distribution of switching loss. However, as long as there is no algorithm to balance the overall loss, the unequal conduction loss among the switches leads to a junction temperature gap. By taking the converter loss model into account, [39] proposes a more adaptive distribution technique based on the operating point of the inverter. To make this method even more effective, the thermal equivalent model is exploited in another study [40] to equalize both average and peak junction temperatures. However, the computation burden on the microprocessor is considerably large at high switching frequencies. In a recent study [37], the converter's equivalent thermal model is also integrated into the electro-thermal model to account for temperature differences on the heatsink. Additionally, the issue of large computational burden is addressed by introducing the partially averaged electro-thermal model.

Other than the software loss balancing techniques for ANPC converters, hybrid structures propose some power density improvements compared to the basic topology. In hybrid structures, different switch types are exploited where they can minimize the loss [41], [42]. While high-current IGBTs can be used as the inner switches where the majority of conduction loss occurs, wide bandgap MOSFETs can be utilized as the outer/middle switches and withstand switching losses due to their low on/off energy losses.

Higher-level ANPC inverters are also proposed in the literature which will be investigated in detail in Section II-C on hybrid topologies due to the presence of flying capacitors in their structure.

2) T-TYPE CONVERTERS

A three-level T-type converter (3L-T^{2}C) is shown in Fig. 4(b). A T-type structure benefits from some of the advantages of both two-level and three-level inverters. Simple control implementation, low conduction loss, and reduced component count make it a cost-efficient solution while three-level operation results in better waveform quality compared to the conventional two-level inverters [43]. Moreover, this structure mitigates the issue of unbalanced loss distribution in conventional NPC inverters. However, it is worth mentioning that, unlike conventional NPC and ANPC structures, a T^{2}C does not benefit from voltage stress division which limits its use in high-voltage applications [35].

Although the T^{2}C is mostly used in the three-level configuration, a five-level structure is also proposed. This structure is formed by connecting two 3L-T^{2}C inverters sharing a common dc-link [44]. This topology can effectively increase the output voltage levels to 5, while it suffers from more components count and dc-link voltage stress on all the switches.

T^{2}Cs can be combined with other structures like nested NPC (NNPC) and FC to form hybrid structures [45], [46] which will be discussed in more detail in Section II-C.

3) STACKED AND ACTIVE STACKED NPC CONVERTER

In another attempt to address the loss distribution issue of the basic NPC converter, a stacked NPC inverter (SNPC) was proposed in [47] as shown in Fig. 4(c). Similar to the basic NPC, the converter is utilizing two clamping diodes and the voltage stress on semiconductors is equal to $V_{dc}/2$. With an additional path to the neutral point, made by two back-to-back switches, new PWM strategies are achievable. In [47] these PWM strategies have proven to double the apparent switching frequency and therefore, reduce the switching loss stress on the outer switch.

An improvement to this topology is proposed in [48] where the two clamping diodes of SNPC are replaced with two active switches. The structure is shown in Fig. 4(d). The addition of active switches increases the degrees of freedom in achieving the zero-state and therefore, enables a better distribution of the switching losses. By using this topology, the average switching frequency of the power devices has been reduced to half which improves the efficiency and power density of the inverter.

4) OTHER NPC-BASED TOPOLOGIES

NPC-based converter topologies that are commonly found in the market are designed to operate at voltage levels between 2.3–4.16 kV. However, these topologies require significant

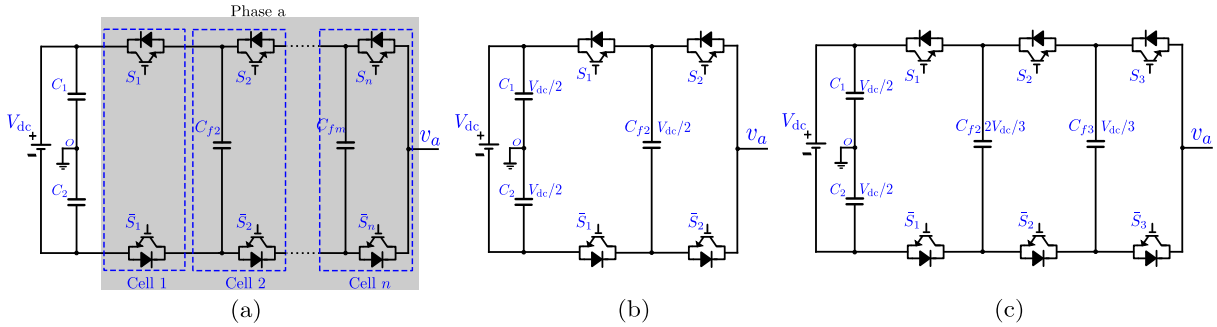

FIGURE 5. One phase-leg of the conventional FC MLC: (a) Generalized *n*-level topology, (b) 3L-FC converter, and (c) 4L-FC converter.

changes in order to be able to handle higher operating voltages, such as those above 6.6 kV. Voltage balancing and control complexity, cost, and fault-tolerance issues are the major limiting factors for moving to higher voltages with a basic NPC-based inverter. In [49], a new power converter, the series-connected multilevel converter (SCMC), is proposed for medium-voltage high-power applications. The five-level operation is achieved by using two series-connected three-level NPC converter modules in each phase. Another NPC-based topology for higher-voltage applications is the NPC/H-bridge structure. However, these structures will not be investigated further here due to the isolated dc-source requirements [50].

TABLE 1. Switching States of Phase *a* for the 3L-FC Converter (↓: Discharging, ↑: Charging, –: No Change)

State	s_1	s_2	v_{ao}	C_f
V_1	1	1	$V_{dc}/2$	–
V_2	1	0	0	↑
V_3	0	1	0	↓
V_4	0	0	$-V_{dc}/2$	–

B. FC CATEGORY

This category includes the topologies that employ FCs without a clamped neutral point and, accordingly, do not bring the issue of dc-link balancing. In these topologies, FCs are used to replace the dc-sources while generating voltage levels. In general, thanks to the modularity, this family has the capability to generate relatively higher levels compared to the NPC family. Moreover, flexibility, fault-tolerant operation, and improved loss sharing between switches are prominent features of these topologies. However, FCs voltage control, pre-charging of capacitors during the start-up process and the large number of employed capacitors are primary challenges associated with this category [10], [51], [52].

The conventional *n*-cell FC-MLC is composed of $2n$ active switches and $n-1$ FCs to generate $n+1$ levels per phase voltage, as shown in Fig. 5(a). For cell-i ($i \in \{1, 2, ..n\}$), two complementary switches ($S_i, \bar{S}_i$) and one FC C_{fi} are used. The exception is cell-1, which has the main dc-link instead of an FC. To produce $n+1$ levels, the voltage V_{fi} of C_{fi} is determined as

$$V_{fi} = \frac{n+1-i}{n} V_{dc} \tag{1}$$

A phase leg of the conventional 3L-FC (2-cell) and 4L-FC (3-cell) converter is shown in Fig. 5(b) and (c), respectively. According to (1), the ratio between the DC voltage source and the FCs voltages is $1:\frac{1}{2}$ in the 3L-FC and $1:\frac{2}{3}:\frac{1}{3}$ in the 4L-FC converter. The switch states of the 3L-FC converter are given in Table 1, where there are four switching states to create three levels in phase voltage. The redundancies available for the zero are exploited to balance the FC at $V_{dc}/2$. The 3L-FC and 4L-FC converters are two mature industrial converters used for electric drives and solar inverters [8].

Several topologies have been derived from the conventional FC-MLC topology to increase the number of voltage levels and/or reduce the required components. One promising topology in this category is the four-level nested NPC (4L-NNPC) presented for MV applications (2.4–7.2 kV) [53], as shown in Fig. 6(a). Similar to the conventional 4L-FC, the 4L-NNPC converter requires six active switches with a blocking voltage of $V_{dc}/3$ and two FCs per phase-leg. The main advantage of this topology is that it limits the sustained voltage of the two FCs to $V_{dc}/3$ instead of $V_{dc}/3$ and $2V_{dc}/3$ in the 4L-FC. However, the 4L-NNPC uses two additional passive diodes. Using an additional cell consisting of two switches and one FC, the 4L-NNPC has been upgraded to the 5L-NNPC converter in [54], as depicted in Fig. 6(b). To generate five levels from the 5L-NNPC converter, the two FCs C_{f1}, C_{f2} are balanced at $V_{dc}/4$ and C_{f3} is balanced at $3V_{dc}/4$ by the available redundant states. Later in [55], the 4L-NNPC in Fig. 6(a) has been operated as a 5L converter without adding any additional passive or active components by balancing C_{f1}, C_{f2} at $V_{dc}/4$ instead of $V_{dc}/3$ in the 4L operation. In doing so, model predictive control (MPC) was adopted to achieve the FCs balance due to the lack of redundant states in the 5L operation mode. However, the voltage stress is not equally distributed among all switches under the 5L operation, where S_1 and S_6 are subjected to double the voltage stress ($V_{dc}/2$) compared to other switches.

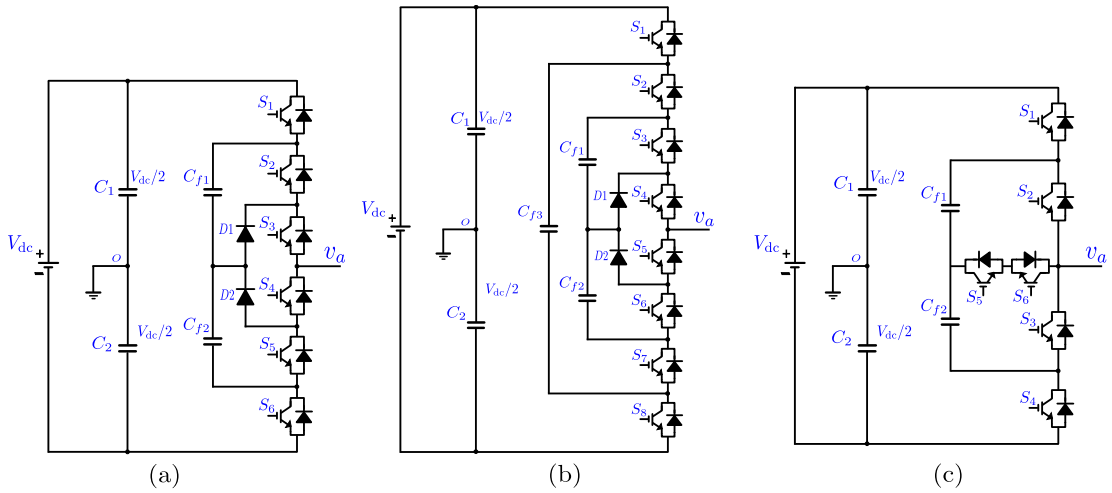

FIGURE 6. One phase-leg of common NNPC converters: (a) 4L-NNPC converter, (b) 5L-NNPC converter, and (c) T-type 4L-NNPC converter.

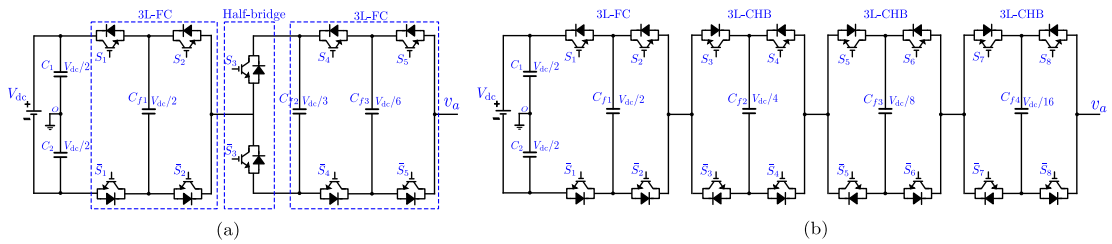

FIGURE 7. Common high-level FC cascaded topologies: (a) 7L cascaded FC converter and (b) 17L cascaded FC converter.

Later, a new T-type 4L-NNPC converter has been proposed in [56] to eliminate the use of clamping diodes, as shown in Fig. 6(c), where only six active switches and two FCs are used in each phase-leg. The operation of this converter is similar to the 4L-NNPC converter as it has the same number of switching states with the same charge/discharge effects on the two FCs. Subsequently, the operation of the T-type 4L-NNPC as a 5L converter with MPC was reported in [46] using switches of different voltage ratings.

Another way to increase the output levels in this category was proposed in [57], where a 7L converter was formed by cascading two units of the conventional 3L-FC with a half-bridge leg, as shown in Fig. 7(a). The FCs are balanced by exploiting the pole redundant states. Moreover, this converter can operate with zero CMV up to the modulation index $M < 0.86$. In [58], a 17L was constructed by cascading a 3L FC unit with three CHB units, as shown in Fig. 7(b). One prominent advantage of this converter is the ability to continue operation with a lower number of levels in the event of a CHB unit failure, improving the reliability of the conversion system.

C. HYBRID MLCS (NPC+FC)

Hybrid multilevel converters (HMLCs) combine multiple fundamental topologies to make use of their respective advantages, while overcoming some of their limitations. Predominantly, hybrid topologies can improve the voltage balancing capabilities for both dc-link and FCs and the power loss distribution across switches, while reducing the number of required active and passive components when compared to NPC and FC topologies [59]. In this section, hybrid topologies which are particularly characterized by featuring both dc-link clamping and FCs as well as a common dc-link are considered. The HMLCs are categorized into the following groups: 1) neutral-point clamped HMLCs, 2) multi-point clamped HMLCs and lastly 3) cascaded HMLCs.

1) NEUTRAL-POINT CLAMPED HMLCS

This subsection presents hybrid multilevel converter topologies which are derived by combining fundamental NPC topologies with FCs. The HMLCs in this category are characterized by clamping to a single dc-link midpoint, which acts as a neutral-point, whereas topologies clamping to multiple dc-link points are presented in the next subsection.

One of the most well-known neutral-point clamped HMLCs is the hybrid five-level active NPC (5L-ANPC), which is derived from connecting a three-level ANPC with a FC power cell connected in series as shown in Fig. 8(a) [24]. Whereas the three-level ANPC can only clamp to three different voltage levels, i.e. $\pm 0.5V_{dc}$ and 0 (V_{dc} being the total dc-link voltage), the FC enables the generation of two additional voltage levels $\pm 0.25V_{dc}$. To achieve this, the voltage across the FC needs to be balanced at $0.25V_{dc}$ and can then be summed on the dc-link

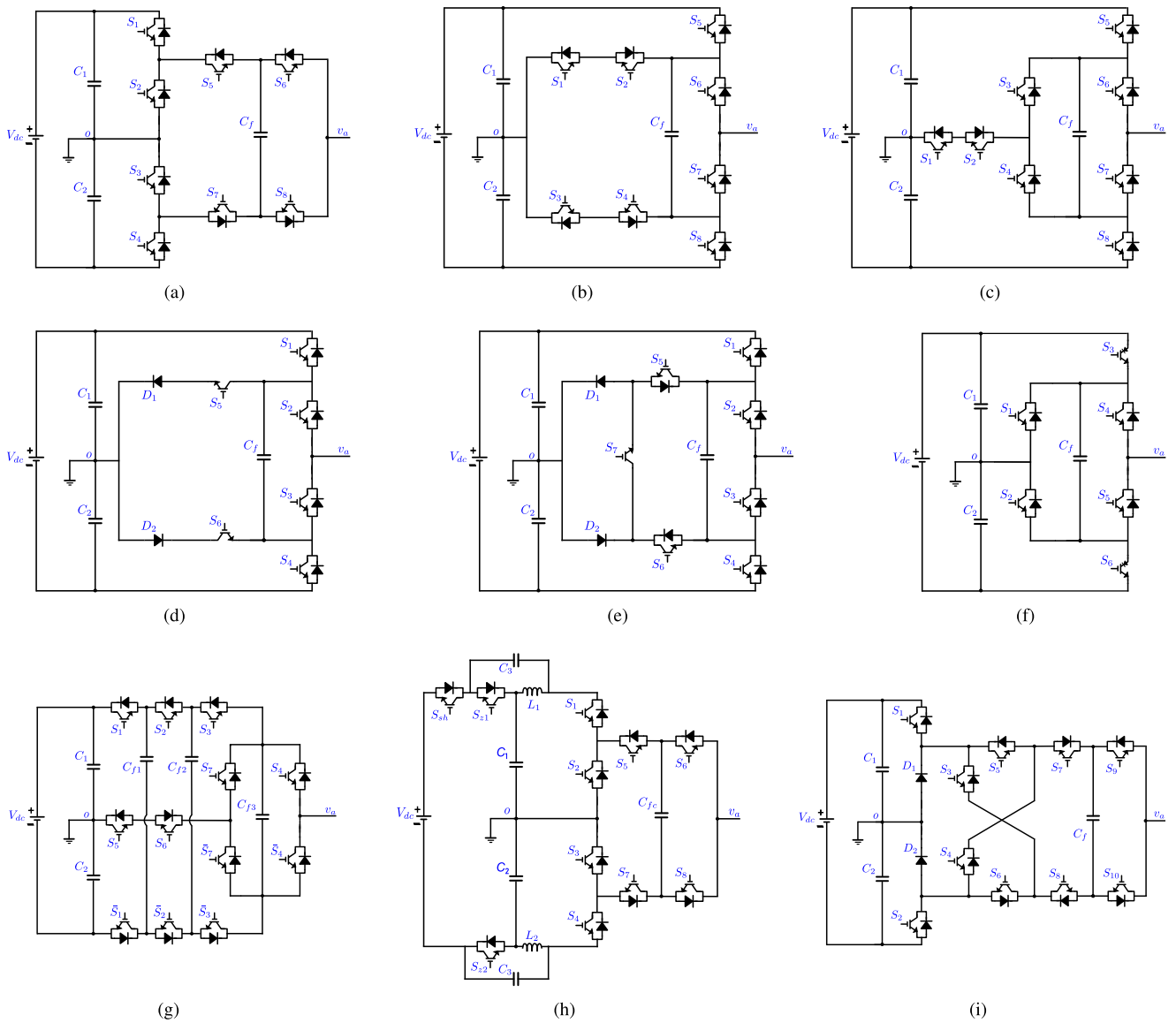

FIGURE 8. 5L-ANPC topologies. (a) 5L-ANPC Type I [24]. (b) 5L-ANPC Type II [60]. (c) 5L-ANPC Type III [61]. (d) Six-switch 5L-ANPC [62]. (e) Seven-switch 5L-ANPC [63]. (f) Six-switch 5L-ANPC with bidirectional switches [64]. (g) 5L-ANPC with auxiliary commutation branches [65]. (h) 5L-ANPC Z-Source Inverter [66]. (i) 5L-ANPC with cross-connected switches [67].

capacitor voltages. For example, a voltage level of $+0.25V_{dc}$ can be generated by switching on the switches S_1, S_5 and S_8. The same voltage level can also be generated by turning on switches S_3, S_6 and S_7. This redundancy of switching states makes it possible to balance the FC at its nominal value. As an additional benefit, it also leads to an even power loss distribution among the switching devices [68].

The topology is composed of eight switches, where switches S_1, S_2, S_3 and S_4 have a maximum voltage stress of $0.5V_{dc}$, while switches S_5, S_6, S_7 and S_8 have a maximum voltage stress of $0.25V_{dc}$. The maximum voltage stress on the switches can be reduced by connecting multiple lower rating switches in series, however this approach introduces dynamic voltage sharing issues, which necessitates the implementation of additional control circuitry [2]. For this reason, the usage of switches with different ratings is a widely adopted alternative strategy.

As the topology has a high number of average switches in the current path, its conduction losses are relatively high at low-voltage applications, making this topology more suitable for medium- and high-voltage applications [69]. Its low cost, volume and control complexity have led to commercially available products for various applications, one of the first being the medium-voltage drive ACS 2000 by ABB rated for voltages up to 6.9 kV [25].

There are two other conventional variants of the 5L-ANPC [60], [61], as shown in Fig. 8(b) and (c), which have the same number of power switches and capacitors, but differ in the number of gate drivers, voltage rating of the switches, total standing voltage (TSV) of switches and number of switches in

conduction paths. The 5L-ANPC Type II reduces conduction losses, but because of the higher maximum voltage stress on the switches it is better suited for low voltage applications. The 5L-ANPC Type III has a reduced TSV, but also has a higher maximum switch voltage [69]. In this subsection, prominent HMLCs derived from these three conventional 5L-ANPC converters are presented, grouped by their number of output levels.

In [62] a reduced switch count five-level ANPC is derived from the conventional 5L-ANPC Type II as shown in Fig. 8(d). Targeting photovoltaic grid-connected applications where output current and grid voltage are usually in phase, the topology removes some reactive current paths in order to reduce the total number of active switches from eight to six. Two additional discrete diodes are still required, however for the inner switches S_5 and S_6 no antiparallel diodes are required, allowing for a further reduction of the system cost [62]. The topology also poses lower conduction losses when compared to the conventional 5L-ANPC Type I, however it suffers from a higher voltage ripple at lower power factors, as the FC voltage drops under the reactive power condition. The HMLC presented in [63] improves reactive power operation capabilities by adding a seventh switch to the aforementioned six-switch 5L-ANPC as depicted in Fig. 8(e), offering similar efficiencies as conventional ANPC topologies under a high power factor.

Another six-switch variant of the 5L-ANPC Type II, shown in Fig. 8(f), uses bidirectional switches to increase its output voltage to unity gain, which is double the relative output voltage when compared to the conventional 5L-ANPC converters [64]. Targeting general-purpose applications, this topology features a similar efficiency as the previously presented six-switch 5L-ANPC from [62], but, in contrast, is able to operate at any power factor. Furthermore, the boosted output voltage can eliminate the need for a dc-dc front-end boost converter. However, a significant disadvantage is the high voltage rating for the FC, which is balanced at the full dc-link voltage V_{dc}, increasing the overall system voume and cost. Furthermore, the outer switches S_3 and S_6 require higher current ratings than the conventional 5L-ANPC topologies as they are burdened by both the capacitor charging current and the load current. [64]

In [65] a new topology is derived from the conventional 5L-ANPC Type III by adding two auxiliary capacitors in order to eliminate the need of additional control circuitry for series connected switches, as shown in Fig. 8(g).

Various converters based on the 5L-ANPC have been proposed in literature for their voltage-boosting capabilities. One such variation involves the inclusion of a Z-source network, as reported in [66], which eliminates the need for an additional boost converter, as depicted in Fig. 8(h). Another variation, discussed in [67], utilizes cross-connected switches to achieve the same outcome, as illustrated in Fig. 8(i).

The conventional 5L-ANPC Type I can also be generalized to produce a higher number of levels by cascading additional FC power cells as show in Fig. 9(a) [24]. This increases the voltage stress on clamping switches, which is usually dealt with by connecting multiple switches in series. With the goal of eliminating the problem of dynamic voltage balancing for these series switches in the generalized topology, a seven-level ANPC with auxiliary commutation branches is presented in [70], as shown in Fig. 9(b). In [71], a nested FC cell is added to the six-switch 5L-ANPC in [78] to produce a seven-level output, as shown in Fig. 9(c). The seven-level T-type ANPC presented in [72] and shown in Fig. 9(d) provides boosting capabilities and can be extended to produce nine or eleven output levels.

Producing nine-levels, the HMLC in Fig. 9(e) cascades an additional FC power cell to the conventional 5L-ANPC Type III [73]. As an alternative to cascading additional cells, another common approach is to increase the number of levels through a split-capacitor T-type cell. In [74] such a split-capacitor ANPC is derived from the conventional 5L-ANPC Type III producing a nine-level output, as depicted in Fig. 9(f). The topology has a low number of active and passive components compared with other nine-level common dc-link HMLCs, leading to lower conduction losses and a lower system cost, while still maintaining the ability of balancing the FC voltage through redundant states. Furthermore, the required voltage rating of the FCs is only $V_{dc}/8$, which reduces the system volume and cost further. A similar nine-level split-capacitor ANPC based instead on the conventional 5L-ANPC Type II is presented in [69] and shown in Fig. 9(g), with the distinction of further reducing the active switch count using the same principle of removing reactive current paths as in the already mentioned six-switch 5L-ANPC from [63].

In [75] and [76], Xu et al. present a generalized split-capacitor ANPC derived from the conventional 5L-ANPC Type I which can produce nine or more levels by cascading multiple such split-capacitor T-type cells as shown in Fig. 9(h). Another nine-level split-capacitor ANPC with unity gain, depicted in Fig. 9(i), is presented in [77].

2) MULTI-POINT CLAMPED HMLCS

The hybrid topologies reviewed so far have had only one dc-link midpoint, however, there also exist some HMLCs that clamp to multiple dc-link points. An early example of this is the P2 converter introduced in [79] and shown in Fig. 10(a), which is a scalable topology deriving its name from the basic two-level FC cell used. Its main advantage is the automatic voltage balancing capability without requiring additional circuitry for both FCs and dc-link capacitors. At the same time, this topology can still be operated for both active and reactive power conversion. Furthermore, all switching devices, diodes and capacitors have the same voltage rating of $1/(N-1)$ times the total dc-link voltage. Despite these advantages, this topology requires a large number of switching devices and capacitors, increasing its cost significantly.

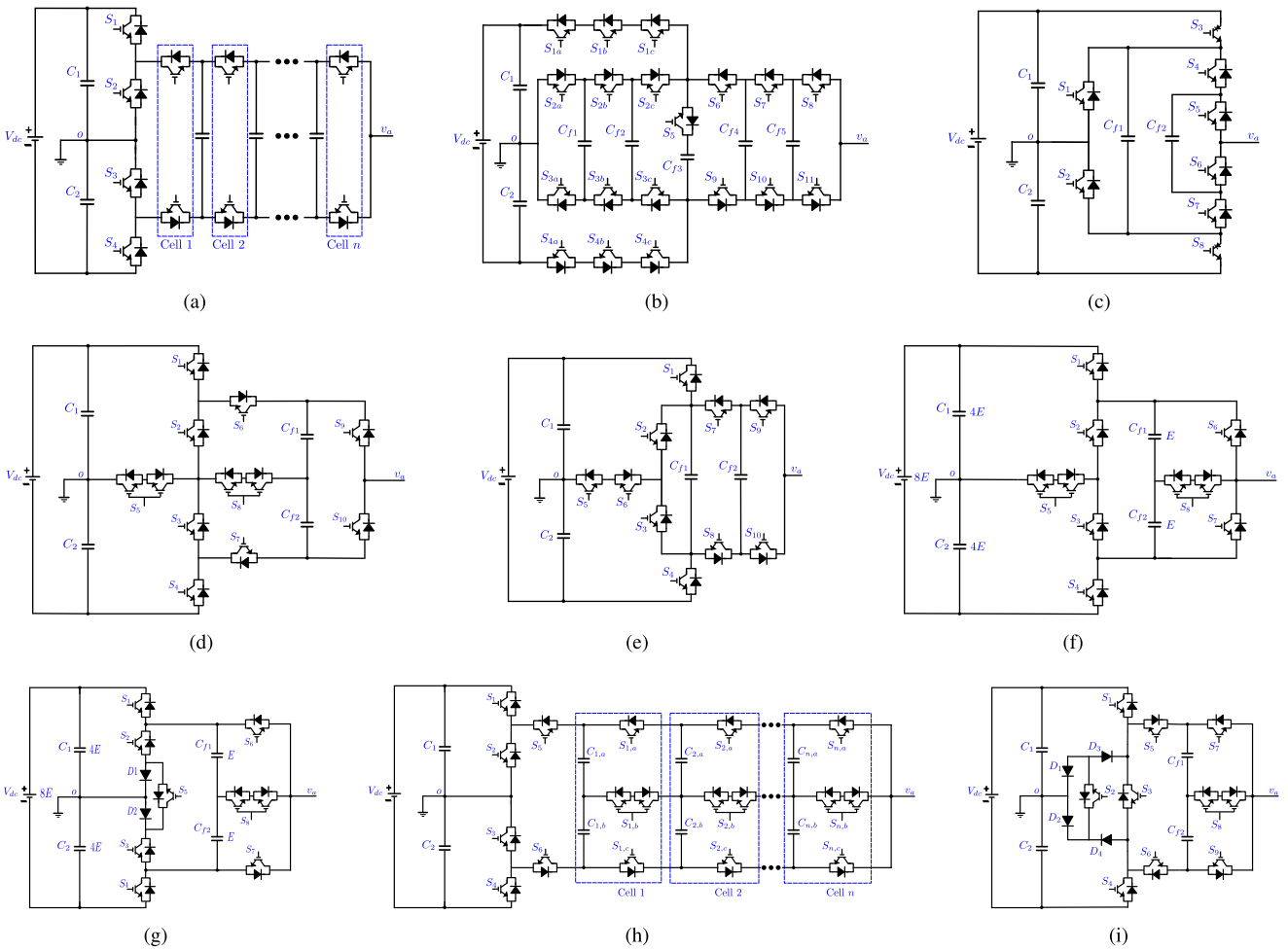

FIGURE 9. Higher level ANPC topologies. (a) Generalized *n*-level ANPC Type I [24]. (b) 7L-ANPC with aux. commutation branches [70]. (c) 7L-8S-ANPC, based on 5L-6S-ANPC [71]. (d) 7L/9L/11L-Boost-ANPC [72]. (e) 9L T-ANPC [73]. (f) 9L split-capacitor T-ANPC [74]. (g) 9L split-capacitor ANPC with reduced count [69]. (h) 9L split-capacitor ANPC [75], [76]. (i) 9L split-capacitor unity gain ANPC [77].

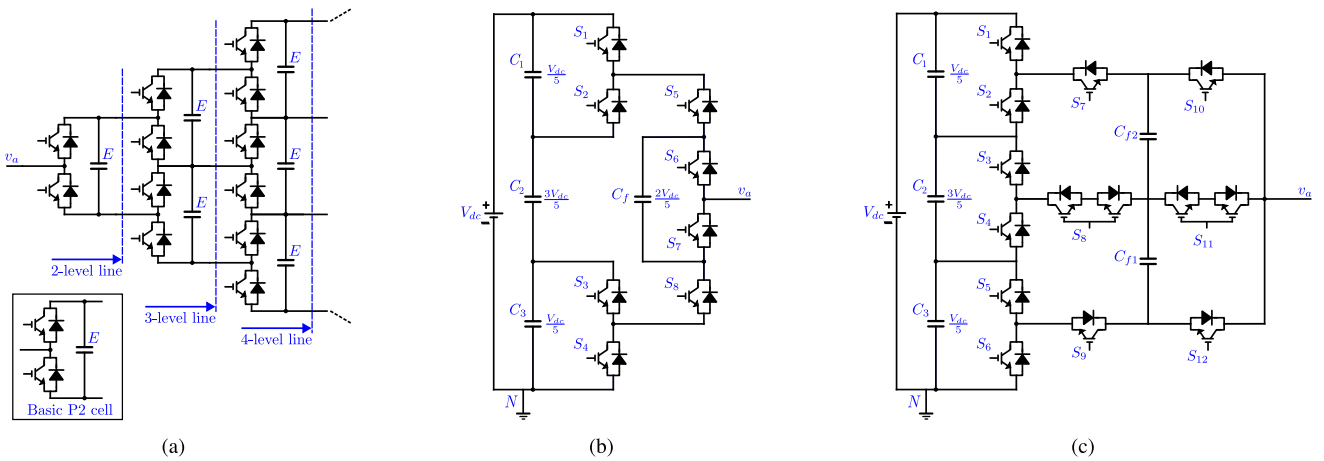

FIGURE 10. Multi-point clamped topologies. (a) General P2 converter [79]. (b) 6L multi-point clamped converter [80]. (c) 7L multi-point clamped converter [81].

Two other multi-point clamped HMLCs, shown in Fig. 10(b) and (c), achieve a reduction of the total device count while maintaining FC voltage balancing capabilities [80], [81]. However, both topologies are limited by their ability of balancing dc-link capacitors, either through a limited operational range or by requiring an auxiliary circuit. At the same time, they still require a relatively high number of capacitors when compared to the ANPC topologies previously presented. In [93], a novel hybrid generalized topology featuring multiple dc-link clamping points is presented. This converter serves as a foundation for deriving various existing and emerging topologies. However, the task of achieving a balanced dc-link is challenging.

3) CASCADED HMLCS

Another possible categorization of HMLCs is to consider those topologies which are derived by cascading one or more types of fundamental cells in parallel or series. Basic cells are typically FC and H-bridge (HB) cells, but can also include more complex cells such as a cross-connected FC cell [59], [92]. The cascaded approach can improve FC voltage balancing characteristics as well as fault-tolerance of the HMLC [59].

A common class of cascaded HMLCs combines a NPC basic cell with a full HB cell in series. Some topologies, such as those in [94] and [95], connect both output phase legs to the HB cell to increase the number of output levels, however this eliminates the possibility of using a common dc-link in three-phase systems as there no longer is a common neutral point. Therefore, within this review only those cascaded HMLCs using a FC-based HB cell are further considered.

An early HMLC using this approach is the converter proposed in [82], connecting a three-level NPC cell with a FC-based HB cell in series, as shown in Fig. 11(a). This topology features a boosted output and can produce up to nine levels, depending on the chosen ratio of FC voltage to dc-link voltage. However, a higher number of output levels eliminates redundant switching states and thus only seven-levels are used to maintain FC voltage balancing capabilities. By using a three-level ANPC cell instead of the NPC, as shown in Fig. 11(b), Pulikanti et al. improve the loss distribution among switching devices in [83]. In another variation, shown in Fig. 11(c), a three-level T-type is cascaded with HB unit to form the seven-level HMLC proposed in [84], resulting in an improved efficiency for low-voltage applications, due to reduced conduction losses, when compared to the NPC. The HMLC presented in [85] and shown in Fig. 11(d) cascades a three-level FC cell to the previous topology to increase the number of output levels to thirteen.

Another possibility of increasing the number of output levels is to use a higher-level NPC cell. The HMLC proposed by [86] and depicted in Fig. 11(e) uses a conventional 5L-ANPC as the NPC cell and can produce nine levels while retaining redundant switching states for FC voltage balancing. A generalized topology is presented in [87] where a generalized ANPC with n cells is cascaded with a HB cell in series as in Fig. 11(f) to produce a total of $4n + 1$ levels.

The cascaded HMLCs discussed so far only used NPC-based cells and HB cells, however other types of basic cells can be used as well. For instance in [88] two parallel FC cells are cascaded with a two-level selector cell in series as shown in Fig. 11(g) to produce a dual FC five-level converter. In [89], Karthik and Loganathan modify this topology to reduce the component count in a three-phase converter by sharing the two FC cells along all three phases and using a three-level NPC as a selector cell in each phase, as shown in Fig. 11(h). In [90], another modification of the dual FC five-level converter with nine output levels is presented. This is achieved by inserting HB cells in between each of the parallel FC cells and the two-level selector switch as depicted in Fig. 11(i). Other cascaded HMLCs combine ANPC and HB cells with a cross-connected FC cell in a seven- and nine-level converter [91], [92]. The seven- and nine-level converters are shown in Fig. 11(j) and (k), respectively.

Lastly the stacked multicell converter (SMC) can also be considered a type of cascaded HMLC, as it is derived by cascading a basic cell both in parallel and in series [23], [97]. Fig. 12(a) illustrates the basic cell for a dual-stack multicell converter. A stacked multicell converter with n such basic cells cascaded in series can produce $2n + 1$ output levels, for example Fig. 12(b) shows a seven-level SMC with three cells in series. The main advantages of this topology are its high modularity and high number of redundant states. However, compared to other hybrid topologies the SMC requires a larger number of FCs, which not only increases system volume and cost, but also reduces its reliability [59].

The stacked multicell can also be cascaded with other fundamental topologies, for instance in [96] a five-level SMC is cascaded with a HB cell, as shown in Fig. 12(c), to produce nine output levels. Compared to the original SMC, fewer FCs are required, while the voltage across the FCs in the SMC cell are balanced at $V_{dc}/4$ and the FC in the HB cell at only $V_{dc}/8$. Proposed for IM drive operation, the topology can also increase the number of output levels to eleven with the goal of increasing the linear modulation range.

D. MMC CATEGORY

The modular multilevel converter (MMC) was originally proposed in 2001 in a German utility model and a German patent by Siemens Company and Prof. Marquardt [22], [98]. Later it was introduced to academia by Prof. Marquardt in 2002 [99], [100]. Since then, the MMC has drawn attention among researchers and become the most promising converter topology for medium and high voltage applications due to its high efficiency, low harmonic distortion, high modularity and scalability [101], [102]. A basic structure of a three-phase MMC is shown in Fig. 13. The three-phase MMC has three legs, and each phase-leg is divided into two halves, called the upper arm (represented by subscript "u") and the lower arm (represented by subscript "l"). Each arm consists of

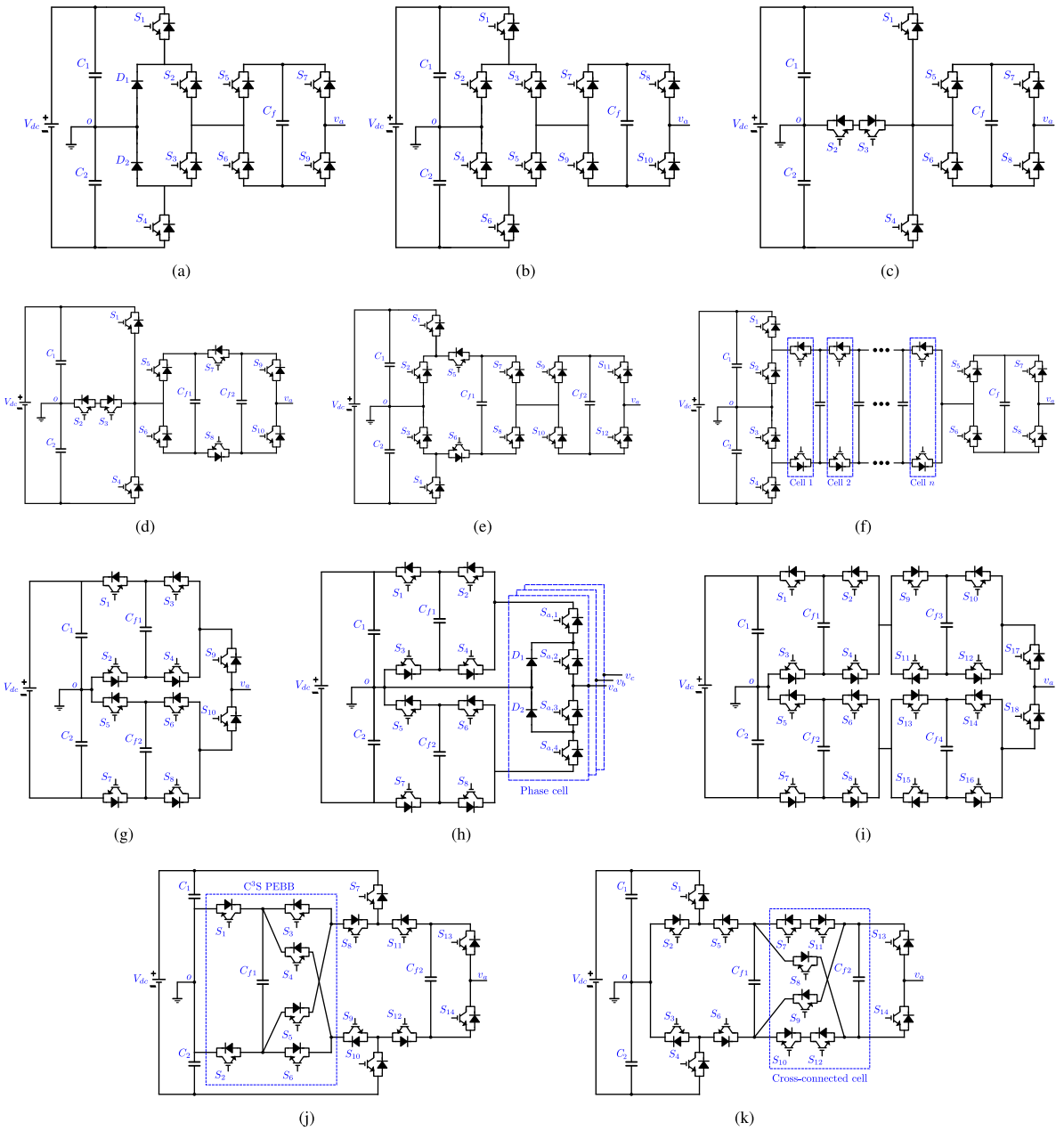

FIGURE 11. Cascaded HMLC topologies. (a) 7L cascaded 3L-NPC with HB in series [82]. (b) 7L/9L cascaded 3L-ANPC with HB in series [83]. (c) 5L/7L cascaded T-type with HB in series [84]. (d) 13L cascaded T-type ANPC with HB in series [85]. (e) 9L cascaded 5L-ANPC with HB in series [86]. (f) Generalized cascaded n-level ANPC with HB in series [87]. (g) 5L cascaded 3L-FC converter [88]. (h) 5L cascaded 3L-FC converter with 3L-NPC [89]. (i) 9L cascaded FC-HB converter [90]. (j) 7L cascaded C3S 5L-ANPC converter [91]. (k) 9L cascaded converter with cross-connected intermediate-level (CCIL) [92].

N series-connected submodules (SMs) and an arm inductor. The arm inductor L_o is used to limit $\frac{di}{dt}$ in the arm currents. The resistor R_o models the power loss within each arm of MMC.

1) BASIC TOPOLOGIES FOR SMs

The most popular and widely used SMs in MMC are half and full bridges, as shown in Fig. 14(a). The half-bridge SM consists of two IGBTs, two diodes and one capacitor. The output voltage v_o of the half-bridge SM has two voltage levels, i.e., "0" (S_1 off, S_2 on) and "V_c" (S_1 on, S_2 off). Depending on the combination of different voltage levels of all the SMs in one leg, the phase output voltage V_s varies from $-\frac{V_{dc}}{2}$ to $\frac{V_{dc}}{2}$. Due to the simple construction, the half-bridge SM is most commonly used in commercial applications such as MMC-HVDC system [103]. Another topology of the SM is the full bridge, also referred to as an H-bridge converter. In the full-bridge SM, the power capacitors can be connected to the terminal at either polarity, hence it can provide three voltage levels, i.e., "$-V_c$", "0" and "V_c". This topology makes it possible to clear DC faults by reversing the DC line voltage

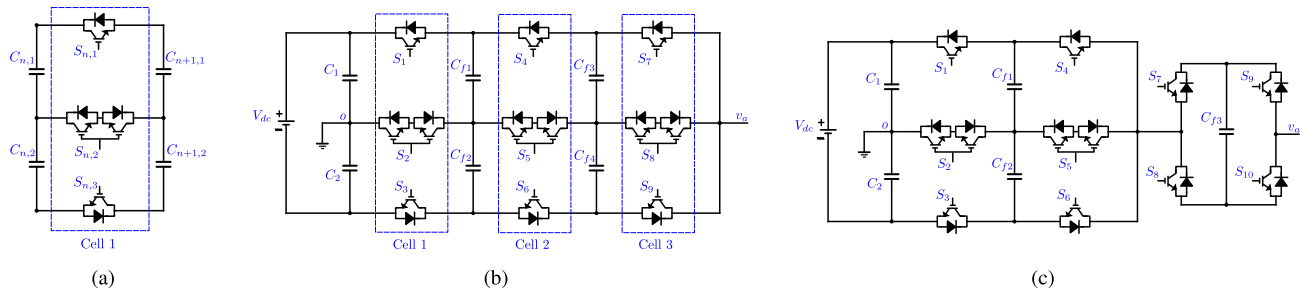

FIGURE 12. Cascaded HMLC topologies based on the Stacked Multicell (SM). (a) Basic cell of the stacked multicell converter [23]. (b) Stacked multicell converter [23]. (c) 9L cascaded SM-HB converter [96].

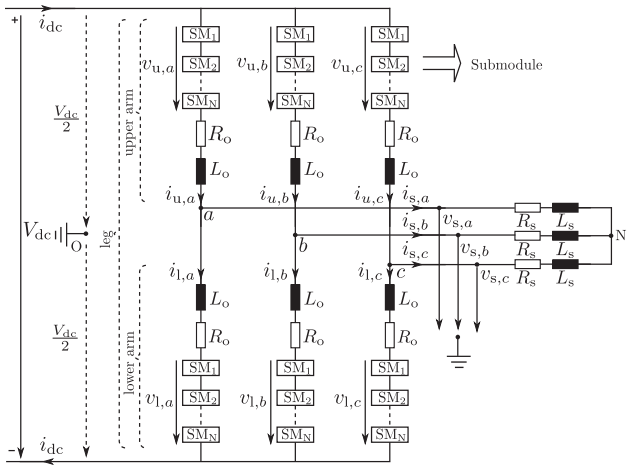

FIGURE 13. Basic structure of a three-phase MMC.

polarity for a short period of time in order to extinguish and de-ionize the electric arc followed by the possibility of multiple restart attempts [104].

2) ADVANCED FULL-BRIDGE SMs

However, the conventional full-bridge SM leads to increased conduction losses since the number of series-connected devices is doubled. The increased conduction losses are not generally acceptable in many high-power systems. Therefore, some advanced full-bridge SMs are introduced, such as semi-full-bridge SM [105] and double-zero full-bridge SM [106], [107].

As shown in Fig. 14(b), the semi-full-bridge SM contains two capacitors which can be connected in series or in parallel, hence it can provide four voltage levels, i.e., "$-V_c$", "0", "V_c" and "$2V_c$". This topology can output a similar voltage level as two conventional full-bridge SM but with fewer semiconductors. Therefore, the conduction losses of semi-full-bridge SM are 25% less than two full bridges. Double-zero full-bridge SM shown in Fig. 14(b) is another advanced SM which combines silicon and silicon carbide. With the additional SiC switch, both the conduction and switching power losses are reduced.

3) MULTILEVEL SMs

The performance of the SMs can be further improved by using multilevel structure [108]. In multilevel SMs, there are more redundancy switching states in MMC, which significantly improve the controllability of SM capacitor voltages. The structure of three-level NPC SM is shown in Fig. 14(c). The three-level NPC MMC has lower semiconductor losses than the full-bridge SM but higher than the half-bridge SM [109]. Besides, the loss is not evenly distributed between the devices, and this SM needs additional voltage balance control. Hence, from the manufacturing and control perspective, the NPC SM is not an attractive solution for MMCs. Another three-level SM is the flying capacitor (FC) SM, as shown in Fig. 14(c). This FC SM has similar semiconductor losses with the half-bridge SM and lower loss than the full-bridge SM. Fig. 14(c) shows the five-level cross-connected SM which consists of two half-bridge SMs and two extra IGBTs with their anti-parallel diodes [110]. This topology provides five-level quadrant operation and DC fault current limitation.

III. COMPARISON OF COMMON DC-LINK TOPOLOGIES

This section compares a selection of the topologies presented in the previous sections based on both quantitative and qualitative factors. The topologies are compared based on the number of output levels, where three, five, seven, and nine-level topologies are considered.

The evaluated quantitative factors include the semiconductor and capacitor count, required voltage ratings and boost factor, as these factors affect the converters characteristics significantly. For instance, a large switch count requires the implementation of a large number of drivers and increases the modulation complexity and failure rates. Limiting the switch count, however, can reduce the number of redundant states which would otherwise be constructive towards FC voltage balancing, loss distribution, and post-fault reconfiguration.

Similarly, the number of voltage sensors and complexity of voltage balancing algorithms increase with the number of FCs employed. Inverters with natural voltage balancing, however, can significantly reduce the complexity of FC voltage balancing algorithms and the computational load. In general, FCs drastically influence the volume and weight of the inverter, thus decreasing the power density as well as increasing the failure rates which is particularly undesirable in transportation

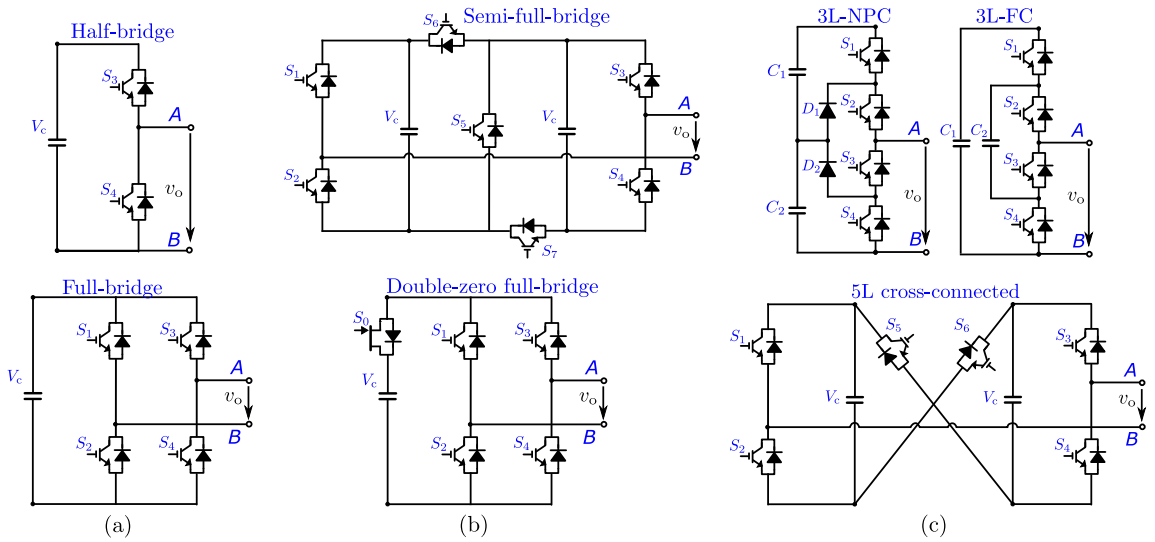

FIGURE 14. Common SM configurations: (a) Basic topologies for SMs, (b) Advanced full-bridge SMs, and (c) Multilevel SMs.

electrification applications and the integrated motor drive configuration [35]. More than two dc-link capacitors will cause similar issues.

The dc-link utilization factor of the inverter is the ratio of peak phase voltage to dc-link voltage. A higher value of this factor means improved efficiency, ease of cable management, and is particularly favorable in traction applications. Furthermore, higher voltages can facilitate faster charging of on-board battery storage systems.

Another factor is the maximum switch blocking voltage, which limits topologies for high-voltage application. A high TSV, on the other hand, exacerbates a converters cost. Lastly, converters which have a structure feasible to be constructed from previously manufactured modules have an advantage in terms of industrial applicability [74].

In order to find an optimal balance between these factors, recently developed topologies follow an application-oriented approach, where the performance of a topology is optimized for the required application voltage and power levels, size, cost, control complexity, loss distribution, reliability and modularity.

For the quantitative comparison, the following parameters are defined: number of unidirectional switches (N_{US}), number of bidirectional switches (N_{BS}), number of diodes (N_D), number of dc-link capacitors (N_{DC}), number of flying capacitors (N_{FC}), and phase peak voltage in per unit respective to the dc-link voltage (V_{OP}). In addition, the maximum switch blocking voltage (V_{MB}) and the total standing voltage (V_{TS}) are calculated in all topologies for the same peak-to-peak value of the output phase voltage ($2V_{OP}$). Per-phase quantities are considered except for the number of common dc-link capacitors. Although the comparison factors provide an estimated overall cost factor, a qualitative assessment is nonetheless instrumental in determining performance regarding specific applications.

TABLE 2. Quantitative Comparison of Common Three-Level Topologies

Topology	N_{US}	N_{BS}	N_D	N_{DC}	N_{FC}	V_{MB}	V_{TS}	V_{OP}
3L-NPC [19]	4	0	2	2	0	0.5	2	0.5
3L-FC [20]	4	0	0	2	1	0.5	2	0.5
3L-T^{2}C [12]	2	1	0	2	0	1	3	0.5

TABLE 3. Qualitative Comparison of Common Three-Level Topologies

Topology	Advantages	Disadvantages
3L-NPC [19]	Simple structure and modulation; equalized voltage blocking; good dynamic response; high efficiency	Unequal loss distribution
3L-FC [20]	Modular structure; fault-tolerance	Complexity of FC voltage balancing
3L-T^{2}C [12]	Simple structure and low losses; no FCs	Higher switch blocking voltages

A. 3L CONVERTERS

Three-level converters have seen extensive commercial adoption, with the 3L-NPC [19] being the most popular variant. The 3L-FC [20] and 3L-T^{2}C [12] offer two alternatives that require no clamping diodes and flying capacitors respectively. A comparison of these three-level topologies based on quantitative factors is given in Table 2. The qualitative assessment of the three-level topologies is presented in Table 3.

TABLE 4. Quantitative Comparison of Common Five-Level Topologies

Topology	N_{US}	N_{BS}	N_D	N_{DC}	N_{FC}	V_{MB}	V_{TS}	V_{OP}
5L-NPC [19]	8	0	6	4	0	0.25	2	0.5
5L-FC [20]	8	0	0	2	3	0.25	2	0.5
5L-NNPC [46]	4	1	0	2	0	0.5	2.5	0.5
5L-ANPC Type I [24]	8	0	0	2	1	0.5	3	0.5
5L-ANPC Type-II [60]	4	2	0	2	1	0.75	3.5	0.5
5L-ANPC Type-III [61]	6	1	0	2	1	0.75	3	0.5
5L-6S-ANPC [62]	6	0	2	2	1	0.75	3.5	0.5
5L-7S-ANPC [63]	7	0	2	2	1	0.75	3.75	0.5
5L-6S-ANPCB [64]	4	2	0	2	1	0.5	2.5	1
5L-ANPC-aux [65]	12	0	0	2	3	0.25	3	0.5
5L-ANPC-CCS [67]	10	0	2	2	1	0.25	3	1
Generalized ANPC [75], [76]	8	1	0	2	2	0.5	3.5	0.5
Cascaded FC [88]	10	0	0	2	2	0.5	3	0.5
Cascaded FC-NPC [89]	6.67	0	2	2	0.67	0.5	2.67	0.5

B. 5L CONVERTERS

The quantitative and qualitative comparisons for selected five-level topologies are presented in Table 4 and Table 5 respectively. Five-level topologies offer a good balance between performance cost and complexity for several applications and consequently five-level topologies are popular among researchers. The topologies proposed in [64] and [67] have unity dc-link utilization, leading to a potentially increased efficiency or requiring half the original dc-link voltage for meeting the same load voltage requirement. The topologies in [60], [61], [62], [63] have higher peak blocking voltages, thus rendering their high voltage applications difficult. Conversely, the lower peak blocking voltages of the topologies in [19], [20], [65] make them preferable for grid-forming, HVDC, FACTS and other high-voltage applications. High number of FCs in [20], [65] will require more sensors and complex balancing schemes. Lower switch count in [46] can be economical but also detrimental in the form of reduced redundant states. Two FCs are used in [89] across all three-phase legs, providing the advantage of simple sensing and balancing control with minimizing the stored energy.

C. 7L CONVERTERS

Table 6 and Table 7 give the quantitative and comparative assessment of seven-level topologies. Topologies described in [71], [72], [83] and [84] perform better in terms of dc-link voltage utilization. The FC count in the 7L-FC limits their feasibility as the sensor requirements and balancing complexities will be sizeable [20]. The double-midpoint ANPC [81] employs three dc-link capacitors leading to balancing complexities. The boost-ANPC topology in [72] has a dc-link utilization of 1.5 with the downside of the charging inrush current and increasing the current stress of the switches.

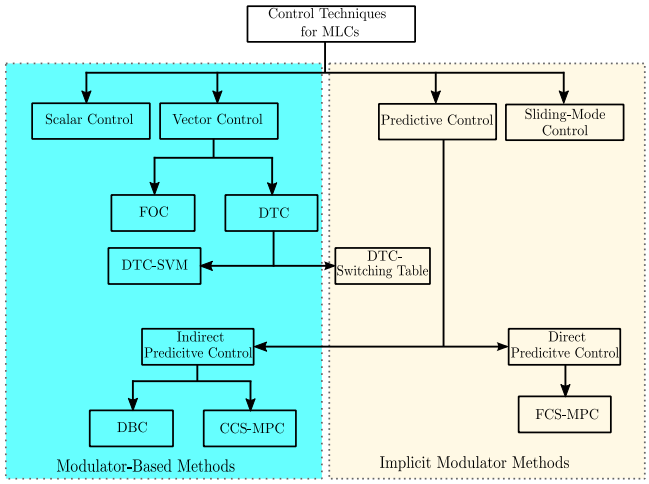

FIGURE 15. Common Control Techniques of Multilevel Converters.

D. 9L CONVERTERS

Nine-level topologies can operate with reduced filter size requirements relative to lower-level topologies while meeting the relevant harmonic standards. Table 8 and Table 9 describe the quantitative and comparative assessment of the topologies. The classical 9L-NPC [19] and 9L-FC [20] topologies have severe challenges because of higher switch and capacitor count. The split-capacitor unity-gain ANPC [77] has unity gain dc-link utilization. The high maximum blocking voltage of the T-ANPC [73] and split-capacitor T-ANPC [74] and the total blocking voltages of generalized series HB-ANPC [90] is undesirable for high-voltage applications. The FC-CHB topology [90] is capable of post-fault operation which is vital for reliability-critical applications, however, the high FC count of the cascaded has a negative impact on the control complexity and power density. The split-capacitor T-ANPC [74] uses only one sensor to balance two FCs, thereby reducing sensors cost and control algorithm complexity.

IV. MODULATION AND CONTROL

Due to the different control objectives and dynamic equations of the load in each application, the control parameters, equations, and priorities vary. In the case of multilevel converter applications, some of the major selection criteria in choosing the suitable controller for the converters are dynamic response, torque ripple, capacitor voltage balancing, equal switch utilization, output waveform quality, simplicity, and cost [111].

A classification of the major control techniques for multilevel converters is shown in Fig. 15. As with the two-level converter, the cascaded control structure usually consists of outer and inner control stages in addition to the modulator block. Although the inner and outer loops are similar in the two-level and multilevel converters, the modulator stage, which is mainly required for scalar and field-oriented control (FOC) techniques, needs to be adapted as the number of levels goes higher. In this section, first, a review of the most popular,

TABLE 5. Qualitative Comparison of Common Five-Level Topologies

Topology	Advantages	Disadvantages
5L-NPC [19]	Simple structure and modulation; equalized voltage blocking; good dynamic response; high efficiency	Unequal loss distribution; more dc-link capacitors
5L-FC [20]	Low peak blocking voltage; lack of clamping diodes; modular structure; fault-tolerance	Capacitor balancing issues; high switch and capacitor count
5L-NNPC [46]	Low component count; low TSV	No redundant states; balancing issues
5L-ANPC Type I [24]	Simple structure; hybrid modulation applicable for lower switching losses, lower harmonics and natural capacitor voltage balancing	Unequal device ratings
5L-ANPC Type II [60]	Low switch count; lower conduction losses compared to Type-I 5L-ANPC	High peak blocking voltage; high TSV; capacitor balancing issues at low power factor; unequal switch utilization
5L-ANPC Type III [61]	High efficiency at high modulation index	High peak blocking voltage; low efficiency at low modulation index
5L-6S-ANPC [62]	Low switch count; optimized performance at high power factor	High peak blocking voltage; limited voltage balancing capabilities at low power factors
5L-7S-ANPC [63]	Improved reactive power capability compared to 6S-5L-ANPC	High peak blocking voltage; limited voltage balancing capabilities at low power factors
5L-6S-ANPCB [64]	Unity gain output; better utilization of dc-link	Requires two reverse blocking switches, high current stress of two switches
5L-ANPC-aux [65]	Low peak blocking voltage; capacitors have snubber-like behavior, thus reducing semiconductor overvoltages; diminished capacitor sizes	High switch and FC count
5L-ANPC CCS [67]	Unity gain output; natural FC balancing	Larger sum of voltage and current stresses; high FCs size
Generalized ANPC [75], [76]	High number of redundant states; fault-tolerance capabilities through post-fault reconfiguration; wide modulation index operation	High switch and capacitor count for 5L operation
Cascaded FC [88]	Even loss distribution; solved transient voltage balancing issues	High active switch count
Cascaded FC-NPC [89]	Minimized energy stored in FC; fault-tolerant operation	High number of conducting switches per level; high conduction loss

TABLE 6. Quantitative Comparison of Common Seven-Level Topologies

Topology	N_{US}	N_{BS}	N_D	N_{DC}	N_{FC}	V_{MB}	V_{TS}	V_{OP}
7L-FC [20]	10	0	0	2	3	0.167	2	0.5
7L-ANPC-aux [70]	18	0	1	2	5	0.167	3	0.5
7L-8S-ANPC [71]	8	0	0	2	2	0.5	2.5	1
Boost-ANPC [72]	7	1	0	2	1	0.33	2.67	1.5
Generalized ANPC [75]	8	1	0	2	2	0.5	3.33	0.5
Double-midpoint ANPC [81]	10	2	0	3	2	0.33	4	0.5
Cascaded HB-ANPC [83]	10	0	0	2	1	0.33	2.67	0.75
Cascaded T-type HB [84]	6	1	0	2	1	0.33	2.67	0.75

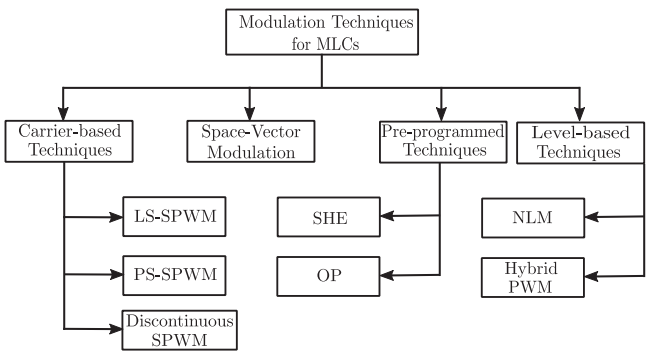

FIGURE 16. Common Modulation Techniques in Multilevel Converters.

as well as advanced modulators, is presented. Also, the control techniques that do not require a separate modulator will be investigated in more detail.

A. MODULATION METHODS

While some control techniques such as direct torque control (DTC) and model-predictive control (MPC) have implicit modulators, other techniques need an independent modulator stage to generate the inverter pulses based on the output of the controller and the operating conditions of the inverter. A general classification of the modulation techniques for MLCs is shown in Fig. 16.

1) CARRIER-BASED PWM TECHNIQUES

The most straightforward modulation techniques for MLCs are carrier-based PWM (CBPWM) techniques. In their most well-known form, level-shifted sinusoidal PWM (LS-SPWM)

TABLE 7. Qualitative Comparison of Common Seven-Level Topologies

Topology	Advantages	Disadvantages
7L-FC [20]	Redundant switching states; low maximum blocking voltage; fault-tolerance	High FCs and switch count
7L-ANPC- aux [70]	Resolves issue of dynamic voltage sharing in series switches and multilevel voltage jumping of phase output voltages	Increased commutation times, high number of FCs and required sensors, and complexity of deadtime compensation algorithm
7L-8S-ANPC [71]	Unity gain output; better utilization of dc-link	Control requirement for capacitor balancing, high current stress of two switches
Boost-ANPC [72]	Boosted dc-link voltage utilization	Charging operation creates significant pulsating current; capacitor voltage ripple, high number of conducting switches increases conduction losses
Generalized ANPC [75]	Ample redundant states; high efficiency	Relatively high number of switches for 7L operation
Double-midpoint ANPC [81]	Low switch voltage stress	High device and capacitor count; complex dc-link balancing
Cascaded HB-ANPC [83]	Relatively high dc-link voltage utilization; FC voltage balancing achievable at higher modulation indices for inductive dominant loads; fundamental frequency modulation possible	High TSV, relatively high size of FC
Cascaded T-type HB [84]	Relatively high dc-link voltage utilization; low number of switches	Complexity of voltage balancing algorithm

TABLE 8. Quantitative Comparison of Common Nine-Level Topologies

Topology	N_{US}	N_{BS}	N_D	N_{DC}	N_{FC}	V_{MB}	V_{TS}	V_{OP}
T-ANPC [73]	8	1	0	2	2	0.75	3	0.5
Split-capacitor T-ANPC [74]	6	2	0	2	2	0.75	3.25	0.5
Reduced-count split-capacitor ANPC [69]	7	1	2	2	2	0.75	3.5	0.5
Generalized ANPC [75]	8	1	0	2	2	0.5	3.25	0.5
split-capacitor unity-gain ANPC [77]	8	1	4	2	2	0.5	2.75	1
CCIL converter [92]	10	2	0	2	2	0.5	3.75	0.5
9L-SMC [23]	8	4	0	2	6	0.25	3	0.5
Series HB-ANPC [86]	12	0	0	2	2	0.5	3.5	0.5
Cascaded FC-CHB [90]	18	0	0	2	4	0.5	4	0.5
Cascaded SM-HB [96]	8	2	0	2	3	0.5	3.5	0.5

and phase-shifted sinusoidal PWM (PS-SPWM) have been constantly used in various applications ranging from industrial to automotive applications. LS-SPWM can be further classified into Phase Disposition (PO), Phase Opposition and Disposition (POD), and Alternative POD (APOD) [112]. These techniques are most appealing due to their lack of complexity since the modulator for high-level MLCs can be simply made by adding carrier waveforms with different phase or level shifts [111].

While the simplicity of LS-SPWM and PS-SPWM techniques is their main advantage, ensuring proper low-frequency operation and voltage balance between the levels is not straightforward. In a comparison between these two techniques, the LS-SPWM shows a better output THD with similar operating conditions while suffering from unequal switch utilization. Therefore, modulating signals need to be swapped periodically to address this issue. This issue and potential solutions to it are discussed in detail in [113].

TABLE 9. Qualitative Comparison of Common Nine-Level Topologies

Topology	Advantages	Disadvantages
T-ANPC [73]	Low device count	High peak voltage stresses on devices
Split-capacitor T-ANPC [74]	Low device count; sensors and losses, configurable through conventional structures	High maximum blocking voltage; high flying capacitor voltage ripple for high modulation indices and unity power factor
Reduced-count split-capacitor ANPC [69]	Low device count; sensors and losses, low conduction loss; high efficiency	High maximum blocking voltage; high flying capacitor voltage ripple for high modulation indices and unity power factor
Generalized ANPC [75]	low number of switches and FCs, high efficiency	Complex control is required to balance the FCs, high voltage ripples in FCs
Split-capacitor unity-gain ANPC [77]	Unity dc-link voltage utilization; capacitor voltage self-balancing	Four clamping diodes required, high conduction losses, high current stress on switches due to capacitor charging
CCIL converter [92]	Ample redundant switching states; simple capacitor voltage balancing mechanism implementation for non-boosting configuration	Addition control and device complexity for boosting configuration
9L-SMC [23]	Ample redundant switching states; high modularity; low-voltage switches and TSV	High number of switches and FCs; high number of conducting switches per level
Series HB-ANPC [86]	Redundant states for balancing FC voltages; operation feasible at all power factors through full modulation index range	High number of conducting switches per level utilization
Cascaded FC-CHB [90]	Fault-tolerance; high modularity, low-voltage switches	Complex capacitor voltage balancing control
Cascaded SM-HB [96]	High dc-link utilization; redundant states	Capacitor balancing at unity power factor

Several modifications have been proposed in the literature for these well-known carrier-based modulators to address their control limitations. In [114], the voltage balancing issue of the FC inverter is addressed by symmetrically arranging the carrier signals in each fundamental period. In [115], the voltage oscillations in low-frequency operation are mitigated at the cost of increased switching frequency by having two modulating signals for each of the converter's three phases. Also, the maximum achievable amplitude of the output waveform is improved. In another study [56], a modified SPWM technique is used for the NNPC inverter structure in which the voltage of the flying capacitor is ensured to remain in the required range.

Other than the mentioned challenges for the SPWM technique in higher number of levels, the limitation posed by hardware and software can deteriorate the effectiveness of the modulator. In [116], the issue of inaccurate synchronization between the carrier signals is discussed and addressed without having a negative impact on the output THD of the inverter.

In addition to the continuous CBPWM techniques that are investigated in this subsection up to now, discontinuous CBPWM techniques are also extended to multilevel structures, offering significant advantages in terms of inverter power loss. This modulating technique avoids switching events when the switch currents are at the peak in their periods. Based on the study in [72], with a switching frequency of 10 kHz, the total power loss of the inverter can be reduced by 10-20% based on the modulation index. However, a slight increase in the THD value of the load current is the downside of the proposed discontinuous CBPWM. Another drawback of this modulation scheme is the voltage balancing issue due to limited switching events at peak currents. This issue is addressed for an NPC inverter in [117] by using different switching patterns based on the operating point of the inverter in terms of modulation index and output waveform frequency.

Finally, hybrid CBPWM methods, in which continuous and discontinuous CBPWM schemes are used together to take advantage of both low THD and low switching losses can be beneficial. The interval that each method is being used determines the trade-off between the two control objectives of the high-quality output waveform and low switching losses.

2) SPACE VECTOR MODULATION (SVM) TECHNIQUES

Space Vector Modulation (SVM) has a superior performance compared with other modulation techniques when it comes to parameters such as voltage balancing, common mode voltage (CMV) reduction, low-harmonic output,dc-link utilization, and transient response [112]. In addition, the complexity of the technique is acceptable when used in three-level inverters. In fact, SVM is the most used modulating technique in applications that require fast dynamic response such as traction applications. However, the main drawback of this technique arises when the number of inverter levels goes higher. The number of available voltage vectors increases from 27 to 125

when moving from a three-level inverter to a five-level structure. Generally, there exists n^3 combination of switching states in an n-level inverter [118].

The implementation of the SVM usually includes several steps. First, using the output of the control stage, the sector that the reference vector lies within is specified by coordinate transformation. Then, the switching times are calculated and the vectors that will be applied are determined. Mapping to two-level SVM techniques can be used to determine the duration of each vector. Finally, the switching sequence will be determined in order to achieve equal switching loss, minimum THD, and minimum voltage imbalance [119].

The additional flexibility in selecting the optimal vector in the SVM scheme addresses many issues in the MLCs that were investigated in the prior sections. Mitigating the fluctuations in the neutral-point voltage (NPV) of NPC-based inverters or the voltage imbalance in FC-based inverters can be accomplished by removing the medium vectors in the space vector diagram (SVD) and introducing virtual vectors in virtual SVM (VSVM) [112], [120]. Another consequence of the added flexibility and redundant vectors in SVM is the capability of the modulator to remove the vectors that cause larger CMV.

As a result of the increased complexity of the controller with SVM scheme in multilevel inverters, many recent studies in the literature have dealt with proposing methods to simplify the modulator. In [119], a generalized method is proposed for multilevel inverters with any number of levels in which a reverse mapping technique from two-level inverter structure is exploited which effectively generates the vectors and pulses for the switches. This scheme has eliminated the need for an additional lookup table. The lookup tables can put a considerable burden on the memory. Similar mapping methods are presented in other studies that can be extended to any number of levels [118].

Several SVM schemes have been also proposed for the four-leg MLCs (FLMLC) which have a wide variety of applications in the four-wire systems. For these structures, a three-dimensional SVM (3DSVM) is used. Although the basics of 3DSVM are similar to that of conventional SVM, a three-dimensional diagram is used for including all the available switching states [121]. Some studies have focused on simplifying 3DSVM. In [121], a generalized 3DSVM is proposed for the FLMLCs that benefit from eliminating the look-up table, voltage balancing scheme, and suitability for any number of levels.

3) PRE-PROGRAMMED SCHEMES

The selective harmonic elimination (SHE) modulation scheme and its variant, optimal pulsewidth pattern (OP), apply the switching transitions at certain pre-programmed angles in order to eliminate certain harmonics from the output waveform [122]. The optimum firing angles in the SHE method is usually driven by solving the harmonic elimination equations using either numerical or intelligent algorithms.

Although SHE method can effectively eliminate low-order harmonics, the overall output THD still remains at high values due to the low effective switching frequency. SHE method is mainly interesting at high-power, high-voltage applications with MMC inverters that operate at low switching frequencies [111].

The low switching frequency in SHE results in high voltage fluctuations on the capacitors or the NP which makes it unattractive for applications that require a high power density with small capacitors. Also, the voltage balancing techniques proposed for the SHE are usually unable to perform at all power factor conditions. In [122], a phase shift is applied to the original firing angles to extend the NP voltage balancing to all power factors.

4) LEVEL-BASED SCHEMES

The nearest level modulation (NLM), which is the main level-based modulation scheme, share some characteristics with the SHE method [123]. Similar to SHE, NLM has the advantage of low switching frequency which makes it suitable for high-power applications which use slower switching devices. On the downside, similar to SHE, they have a poorer output waveform quality and a slower dynamic response when compared to SPWM and SVM techniques. However, unlike SHE, NLM method does not require trigger angle calculations. Instead, at each sampling time, the required number of upper and lower inserted submodules are simply calculated using the reference voltage and a rounding function. Therefore, it benefits from a higher simplicity which makes it a suitable modulation method for high-level MMC inverters in high-voltage applications in which the large number of levels can improve the THD [123].

Some studies have focused on improving the characteristics of the conventional NLM scheme. In [123], the number of output levels has been approximately doubled so the method is applicable to medium-voltage applications. However, this level-increased NLM scheme leads to a higher value of peak-to-peak circulating current. This issue is addressed in [124], in which a deadbeat control is applied to suppress the circulating harmonic currents.

Windowed PWM (WPWM) is another hybrid modulation technique proposed in [125] that combines the NLM and SPWM techniques to benefit from the advantages of both techniques in low-voltage applications. The modulation switches between NLM and SPWM in different intervals based on the operating conditions of the MLC.

B. CONTROL TECHNIQUES WITH IMPLICIT MODULATOR

As mentioned before, certain control techniques are capable of the direct application of pulses to the switches without a need for a modulator stage. In this subsection, some popular controllers with an implicit modulator are investigated.

1) DIRECT TORQUE CONTROL

Direct Torque Control (DTC) is a widely used motor control technique that focuses on controlling the torque and flux directly, rather than through the stator currents. This is achieved through the use of hysteresis controllers for tracking the torque and flux, and a switching table to determine the optimal voltage vector and gating signals. Some of the key benefits of DTC are its fast torque response, robust performance, and straightforward structure that requires minimal computational time. This makes it an ideal choice for a variety of applications, particularly in applications with fast response requirements, such as control of traction motors [111], [126]. The main reason for the simplicity and fast response of the DTC technique is the elimination of the need for current regulators, modulators, and coordination transformations.

While the mentioned advantages make it a potential option for a variety of applications, its drawbacks need to be noted as well. Challenging low-speed control, high start-up currents, and larger torque and current ripple compared to the FOC make it less interesting in some demanding applications. However, as a commercial use of DTC in some demanding multilevel applications, ABB has manufactured an encoderless drive for marine propulsion systems [111].

It is worth mentioning that some studies have made attempt to take benefit of the advantages of both FOC and DTC vector controls by adding a modulator to the DTC controller (DTC-SVM) [127]. Based on a comparison in [111], DTC-SVM has been capable of having the fast response of conventional DTC, while reducing the torque ripple to the level of a FOC controller. However, this improvement is achieved at the cost of decreased simplicity of DTC. It has also been shown that the reference tracking error in a DTC-based drive in standard drive cycles is three times smaller than in FOC-based drives.

2) MODEL PREDICTIVE CONTROL

The principle of MPC is to predict the state variables over a set of future control intervals (prediction horizon) and optimize a designed cost function to achieve the desired performance. MPC has been always considered as an effective control technique for power conditioning systems due to its various benefits such as being a multi-objective control technique (ability to include control objectives and constraints with different natures), the capability of combining the discrete control actions with the continuous behavior of the state variables, faster transient response compared to linear control techniques [128], preserving the nonlinearity of the system (needless model linearization). Two main families of MPC techniques have been discussed in the literature, namely the Finite Control Set MPC (FCS-MPC) and Continuous Control Set MPC (CCS-MPC). In the latter, the use of a modulator is mandatory. However, the discrete control actions that satisfy the switching constraints are directly applied to the converter in FCS-MPC problems. Three main steps characterize the application of FCS-MPC algorithms: 1) Modelling, 2) Calculating the future values of the state variables over the prediction horizon, and 3) Optimizing the designed cost function. FCS-MPC was widely proposed for several common dc-link MLC topologies to mainly control the output current and capacitors' voltages in different applications, such as FC topology with 3L [129], 4L [130], [131], [132], and 8L versions [133], NPC with 3L [134], [135], 4L [136], and 5L versions [137], MMC with 3L [130], [138], 5L [139], [140], and 11L [141].

3) SLIDING MODE CONTROL

The idea of Sliding Mode Control (SMC) is to apply switching control actions (irrespective of the initial conditions) to carry the representative point of the system within a sliding surface (within a finite time) [142], [143], [144]. The sliding surface is typically defined by a linear combination of the state variables or system errors, which leads to a high robustness to parameters mismatch. Moreover, SMC techniques are naturally characterized by a higher dynamic performance compared to PI controllers and reduced computational burden compared to MPC. In the literature, several SMC strategies have been proposed for common dc-link MLC topologies. In [142], the authors proposed an improved SMC technique by including variable weighting factors in the sliding functions. The aim of the proposed technique was to control the common and differential mode currents in MMCs. Based on Gao's reaching law, a sliding mode current controller was applied to a grid-tied 3-phase 3L NPC inverter in [143]. Nevertheless, the classical SMC design might be not appropriate for some topologies like FCIs due to their bilinear structure. In such cases, the switching function could be defined as a combination of state errors.

4) DEADBEAT CONTROL

Feedback compensation techniques, or also called Deadbeat Control (DBC), have been attracting and increased interest in the field of control of common dc-link MLCs. Generally, DBC utilizes the discrete model of the dynamic system to compute the control variables allowing the achievement of a zero steady-state error within a finite settling time [145]. DBC has been successfully applied in multi-objective problems to FCIs [146] and MMCs [147].

V. INDUSTRIAL APPLICATIONS

Nowadays, many common dc-link (NPC, T3, ANPC, FC) and multiple dc-source (CHB) multilevel converter topologies have been increasingly made available in the market to meet the industrial demand for high-power delivery and overcome the voltage/current rating limitation of switches. Historically, CHB inverters are characterized by their modularity, fault tolerance, and ability to generate a high number of voltage levels by cascading cells. However, the requirement of multiple isolated DC sources (rectifier+transformer from the industry point of view) limits their applicability for a vast range of power ratings. Indeed, CHB inverters are mostly employed

TABLE 10. Common Industrial MLC Switch Modules

Company	Module Topology	Voltage Rating	Current Rating	Applications
Vincotech [148]	NPC	1200/1500V	30 to 1800A	Drives Solar Inverters UPS
Vincotech [149]	T3	650/1200V	25 to 1800A	Drives Solar Inverters UPS
Vincotech [150]	ANPC	1200/1500V	150/300/600A	Solar Inverters
Vincotech [151]	FC	1200V	200A	Drives Solar Inverters UPS
Fuji Electric [152]	T3	600/900/1200V	50 to 600A	Drives Power Conditioners UPS
Semikron [153]	NPC	650/1200V	20 to 600A	Wind Turbine Converters Solar Inverters UPS
Semikron [153]	T3	650/1200V	50 to 600A	Wind Turbine Converters Solar Inverters UPS
Infineon [154]	NPC	650/1200V	30 to 400A	High-speed Drives Solar Inverters UPS
Infineon [154]	T3	650/1200V	15 to 600A	High-speed Drives Solar Inverters UPS

in high-power applications (ranging from hundreds of kilowatts to megawatts) where there are no available components for such ratings. On the other side, common dc-link topologies are characterized by the employment of a single DC source making them a good alternative in various applications such as 3-phase industrial systems. Indeed, they can be employed in many configurations such as 3-Leg 3-Wire, 3-Leg 4-Wire, and 4-Leg 4-Wire in motor drives, PV inverters, fast DC chargers, etc. Recently, Vincotech, Semikron, Infineon, and Fuji Electric companies have manufactured switch units for higher efficiency and reduced size ANPC, NPC, and T3 (Table 10) inverters by combining many IGBTs and diodes. Vincotech has also developed other modules like FC and H6.5 for various applications such as PV inverters, drives, UPS, and pumps. In terms of medium voltage applications, FC inverters have been used by Alstom Industry and ALSTOM DRIVES and CONTROLS LTD for the control of synchronous and asynchronous machines of a few megawatts [155]. Moreover, some European locomotives have been using FC inverters to adapt to specific voltages and frequencies of the different European railway networks (1.5-kVDC, 25-kV/50 Hz, 15-kV/16 Hz or 3-kVDC). This adaptation feature makes possible the reduction of the size and cost of the used components. In HVDC applications, MMC topologies are getting an increased interest where they have been used by SIEMENS for the realization of an HVDC transmission system (320 kV/2000MVA) between France and Spain [156]. Nowadays, industries are more interested in using MLCs for high and medium power ratings where 3-phase topologies should be used. It is almost impractical to use topologies with multiple isolated DC sources. Therefore, MLCs with common DC bus have been paid an increased interest in high power applications (pumps, conveyors, fans, traction systems). However, one should note that the increase of active/passive components count will affect the size and cost of the power converter, which is highly undesirable. Thus, market players should find a compromise between the cost, voltage balancing, size, reliability, manufacturing, etc. For instance, Schneider Electric has been using a 3L NPC for motor drives and 4L FCI for UPS applications, while Toshiba has been employing the 3L NPC and 3L/5L PWM converters in high-power drive applications. Recently, Huawei has revealed the employment of the 5L MLC technology in their data centers. Some of the industrial common dc-link MLC products are listed in Table 11.

VI. FUTURE PERSPECTIVES AND RECOMMENDATIONS

MLCs are getting significant attention from industry and play an important role in the new generation of power converters. Although most of the multilevel topologies are used for high-power industrial drives, low-power ranges (above 1 kW) are also taking a significant portion of the market. They can be used as EV chargers or motor drives, residential PV inverters, UPS, etc. In all those applications, a topology with a common DC bus would be very attractive for further development and expansion. Moreover, such an option helps in developing 3-phase configurations to reduce the current in each phase while increasing the power rating. For instance, EV superchargers are connected to the 3-phase network to

TABLE 11. Common DC-Link MLCs in Industry

Company	Product Series	Topology	V/I/P Rating	Applications
Toshiba	T300MVi	NPC	6600V/391A	Drive
Toshiba		MMC	250kV/1200A	HVDC
ABB	ACS6000	NPC	3-3.3kV	Drive
ABB	ACS2000	ANPC	6kV/800kW	Drive
Siemens	SINAMICS GH150	MMC	4-13.8kV	Drive
Schneider Electric	Altivar 1260	NPC	4.16kV	Drive

provide a higher amount of power and charge the EV batteries faster. On the other side, one of the main barriers to the widespread use of MLCs in the industry is design complexity. Although a higher number of voltage levels reduces inherently the harmonic content and reduces the size of output filters, it requires a higher number of switches, auxiliary capacitors, and consequently more gate drivers and complex voltage balancing techniques. Moreover, capacitors are considered points of failure in addition to their significant contribution to the reduction of the reliability and lifetime of the converter. Thus, there should be a trade-off between the high performance and reliability of MLCs. Currently, three-level and five-level NPC, ANPC, and Vienna topologies are considered matured and widely developed/manufactured by companies for many applications. Thus, taking into account that industries are interested in simplicity and high performance for their next generation of power electronic converters and based on the review study performed in this article, the future research and development challenges could be listed as follows:

1) Optimization of the design of the common dc-link MLCs taking into account the recent advances in power device technologies. Exploiting the available variety in the wide-bandgap devices such as SiC and GaN power devices can reduce the cost of the topology and improve the power density and efficiency of the MLC.
2) Designing new common dc-link converter topologies optimized for certain low/medium-power applications such as power supplies, electrified transportation, aerospace and aircraft, residential applications, solid-state transformers, etc.,
3) Developing 5L+ topologies with a reduced component count,
4) Developing bidirectional common dc-link converter topologies for grid-connected and stand-alone modes of operations,
5) Proposing novel voltage balancing strategies/external pre-charging circuits to reduce the capacitors' size and voltage ripples,
6) Reducing the complexity of controllers by proposing new switching strategies with integrated voltage balancing,
7) Increasing efficiency and reducing losses,
8) Investigating new fault-tolerant/modular topologies.

VII. CONCLUSION

The utilization of common dc-link MLCs is a requirement in several application areas due to their numerous benefits, including the elimination of bulky and inefficient transformers and rectifiers. In particular, common dc-link topologies are essential for BTB configurations, where a shared dc-link between the rectification and inversion stages is required. The scope of this article has been to present a comprehensive review of common dc-link MLCs, including their topological evolution, features, comparison of different topologies, modulation techniques, control strategies, and potential application areas. The findings of this article reveal that common dc-link topologies are the dominant choice in industrial applications due to their versatility and compatibility with different power conversion systems. Additionally, the article highlights the fact that most commercialized MLCs utilize common dc-link topologies.

The article demonstrated that common dc-link MLCs have significant potential for further development and implementation. However, there is still a need for further research in areas such as cost-effectiveness, efficiency, fault-tolerant operation and reliability to fully realize their potential. The future perspectives and recommendations discussed in this paper provide valuable insights for researchers and engineers to address these challenges and continue to explore the full potential of common dc-link MLCs.

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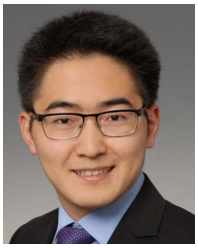

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