Prediction Procedure of Parasitic Parameters Considering Laminated Bus Bar Geometries Based on Online Machine Learning

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ABSTRACT The development of SiC and GaN power devices to achieve high-speed switching operations in power converter circuits is underway. The stray inductance caused by the bus bar geometries between DC capacitors and power devices influences high-speed switching circuits, such as surge voltages and switching losses. Therefore, the evaluation of the parasitic parameters is essential in designing power converter circuits. Currently, parasitic parameters that consider various bus bar geometries are calculated using finite element analysis (FEA) each time, which requires a large calculation time. This article proposes a prediction procedure for the parasitic parameters that easily and quickly consider complex bus bar geometries by performing online machine learning of FEA-based datasets. A laminated bus bar with two apertures to connect DC capacitors or power modules is analyzed, and the parasitic resistance, inductance, and capacitance are predicted. This article describes how large datasets can be obtained from multiple installments and perform online machine learning using XGBoost. To discuss the benefits of online machine learning, the prediction accuracy using test data in multiple machine learning models with different amounts of training data is compared. The mean relative error (MRE) between the predicted and analyzed values improves from 250% to 8% when parasitic parameters are predicted in the frequency range of 50 kHz to 100 MHz.

INDEX TERMS Stray inductance, laminated bus bar, finite element analysis, machine learning, parasitic parameter.

I. INTRODUCTION

Recently, wide-bandgap power devices, such as SiC and GaN devices, to achieve high-speed and high-frequency switching operations in power converter circuits have been developed [\[1\],](#page-7-0) [\[2\],](#page-7-0) [\[3\],](#page-7-0) [\[4\],](#page-7-0) [\[5\].](#page-7-0) Wide-bandgap power devices enable power converter circuits to reduce switching losses and volumes at higher switching frequencies compared with Si-IGBTs [\[6\],](#page-7-0) [\[7\].](#page-7-0) Conversely, stray inductance influences high-speed switching circuits, such as surge voltages, owing to the high rate of current change di_d/dt . Furthermore, stray inductance and capacitance result in oscillations in the switching waveforms, which are sources of noise [\[8\].](#page-7-0) Therefore, the development of bus bar and power module designs to optimize parasitic parameters has been investigated extensively [\[9\],](#page-7-0) [\[10\],](#page-7-0) [\[11\],](#page-7-0) [\[12\],](#page-7-0) [\[13\].](#page-7-0) Reference [\[14\]](#page-7-0) presents a design procedure for an acceptable stray inductance in a high-speed switching circuit, considering the switching period, voltage, and current rating of the circuit. Additionally, Reference [\[15\]](#page-7-0) proposes a design procedure for a laminated bus bar geometry that optimizes the switching waveform by evaluating surge voltages, damped oscillations, and switching losses, which vary according to the parasitic parameters.

Datasheets for power devices and capacitors describe parasitic parameters, such as stray inductance; however, the parasitic parameters of bus bars vary in complexity depending on their geometries. Therefore, the parasitic parameters that consider various bus bar geometries should be calculated using finite element analysis (FEA) for each circuit, which requires considerable calculation time.

Information technology has recently become more generalized, and numerous open-source libraries are presently available. Consequently, machine learning techniques such as neural networks have been utilized in circuit designs [\[16\],](#page-7-0) [\[17\].](#page-7-0) However, studies on machine learning models to

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FIGURE 1. Laminated bus bar with two apertures for terminals.

evaluate the parasitic parameters, considering bus bar geometries have not been conducted.

The authors previously proposed a prediction procedure for parasitic parameters by performing machine learning considering simple bus bar structures [\[18\].](#page-7-0) However, the actual bus bar structures used in power converter circuits have complex topologies, such as bends and terminal holes. Therefore, when preparing datasets, the number of analysis patterns of complex bus bar structures in FEA is enormous, making the implementation of efficient machine learning challenging.

This article proposes a prediction procedure for parasitic parameters that consider laminated bus bar geometries by performing online machine learning. By inputting the variables of the bus bar structure and frequency into the machine learning model using XGBoost, the three parasitic parameters (resistance, inductance, and capacitance) are predicted easily and quickly. After creating a machine learning model, a circuit designer without the skill and knowledge of FEA can predict the parasitic parameters provided the bus bar structure is known. Additionally, the number of analysis datasets required to create a machine learning model that predicts parasitic parameters with sufficiently high accuracy can be validated through online machine learning.

For the target to predict the parasitic parameters, a laminated bus bar with two apertures for the terminals connecting the DC capacitors and power modules is modeled. In actual power converter circuits, laminated bus bars with multiple apertures for terminals are used [\[19\],](#page-7-0) [\[20\],](#page-7-0) [\[21\].](#page-7-0) A laminated bus bar with two apertures for the terminals in this article contains the basic elements of these structures. After performing online machine learning using the analysis datasets, the mean relative error (MRE) between the predicted and analyzed values of the three parasitic resistance, inductance, and capacitance improves to 5.82%, 4.94%, and 8.41%, respectively, in the frequency range of 50 kHz to 100 MHz.

II. TARGET BUS BAR STRUCTURE

Fig. 1 shows a model of a laminated bus bar with two apertures for terminals to connect DC capacitors and power modules.

TABLE 1. Six Variables of Bus Bar Geometries

FIGURE 2. Cross-section of two apertures for terminals.

This is the target to predict the parasitic parameters. This model contains the basic elements of a laminated bus bar with multiple terminal apertures that are used in actual power converter circuits [\[19\],](#page-7-0) [\[20\],](#page-7-0) [\[21\].](#page-7-0) The laminated bus bar consists of a 2-layer FR-4 board with an insulating glass epoxy material laminated with copper foil. Table 1 shows the variables of bus bar geometries. The bus bar length ℓ , width w , conductor thickness*t*, insulator thickness *h*, aperture diameter *d*, and distance from the bus bar edge to the aperture center *c* are defined. To prevent analysis datasets from getting too large from the FEA, the model in Fig. 1 is simplified, and six variables ℓ , w , t , h , d , and c of bus bar geometries are defined. Thus, note that the distance between the two aperture centers *s* is fixed at $w/2$, which varies with *w*. Fig. 2 shows the crosssection of the two apertures for the terminals. The apertures are not penetrated, and the terminals P1 and P2 are set on the upper conductor (positive pole) and the lower conductor (negative pole), respectively. Next, the two terminals, P3 and P4 are set at the bus bar edge and conducted through the flow $P1(+) \rightarrow P3(+) \rightarrow P4(-) \rightarrow P2(-)$. Note that the two terminals, P1 and P2 are assumed to be connected to DC capacitors, and the two terminals P3 and P4 are assumed to be connected to power electronic devices in this model. Fig. [3](#page-2-0) shows a T-type equivalent circuit of the laminated bus bar. The parasitic resistance (R_{bus}) , inductance (L_{bus}) , and capacitance (*C*bus) are defined as the three parasitic parameters. The parasitic resistance (R_{bus}) and inductance (L_{bus}) are defined as follows:

$$
R_{\text{bus}} = R_{\text{a}} + R_{\text{b}} \tag{1}
$$

$$
L_{\text{bus}} = L_{\text{a}} + L_{\text{b}} \tag{2}
$$

 L_{bus} ($L_a + L_b$) influences the surge voltage and oscillation in the switching waveform, whereas C_{bus} influences only

FIGURE 3. T-type equivalent circuit of laminated bus bar.

TABLE 2. Variable Ranges and Number of Analysis Points of Frequency and Bus Bar Geometries to Be Analyzed by FEA

Variable	Min	Max	Number of
			Analysis Points
	50 kHz	100 MHz	32
ł	20 mm	200 mm	
\overline{w}	20 mm	200 mm	9
t.	$35 \mu m$	175 μ m	2
h	1.6 mm	8.0 mm	
\boldsymbol{d}	0 mm	$min(30, w/2, \ell)$ [mm]	9
\mathcal{C}	[mm]	$\ell - d/2$ [mm]	

the oscillation in the switching waveform. Because a T-type equivalent circuit can easily describe these parasitic parameters, it is suitable for evaluating the surge voltage and oscillations in the switching waveform [\[15\].](#page-7-0)

III. FEA SETUP

Datasets are prepared using FEA to create a machine learning model. The software used for analysis is ADS (Keysight Technology). FEA is used to analyze the parasitic parameters by dividing the model to be analyzed into multiple fine tetra-hedral meshes. Only the bus bar shown in Fig. [1](#page-1-0) is modeled. and the boundary condition of FEA is open. S-parameters are output as the format of analysis results by ADS. Therefore, the conversion from S-parameters to Z-parameters is performed, and R_a , R_b , L_a , L_b , and C_{bus} are defined in Fig. 3.

Table 2 shows the variable ranges and the number of analysis points of frequency f and the six variables of the bus bar geometries shown in Table [1.](#page-1-0) The number of analysis points for each variable in Table 2 is determined as the initial target value in machine learning. Online machine learning is expected to optimize these values by considering prediction accuracy and computational cost. Additionally, *d* and *c* are the ranges considering the conditions in which the two apertures do not contact each other or the bus bar edges. The input values that are equally spaced from the minimum to the maximum are analyzed by setting the range of variables and the number of analysis points for each variable. The number of analysis datasets is 831,616 in the setting of Table 2. When $\ell = d$, the minimum and maximum values of *c* are equal, and the number of analysis points of *c* is one.

FIGURE 4. Split acquisition procedure of analysis datasets to realize online machine learning in which the machine learning model is sequentially updated.

Thus, the number of analysis datasets is less than 839,808 (32 \times 9 \times 9 \times 2 \times 2 \times 9 \times 9).

The preparation of all 831,616 datasets by a one-time FEA is computationally costly and requires a long waiting time before machine learning is performed. Therefore, Fig. 4 shows the split acquisition procedure of the analysis datasets by performing multiple FEA while increasing the number of analysis points of ℓ , w , d , and c from two to nine. As the number of analysis points of ℓ , w , d , and c increases from two to nine, the number of analysis datasets increases to 1,920, 9,856, 31,616, 77,952,..., 831,616. This procedure realizes online machine learning in which a machine learning model is sequentially created each time the analysis datasets are acquired. The computational cost of acquiring all 831,616 datasets is divided and machine learning is performed efficiently.

IV. DESIGN OF MACHINE LEARNING MODEL USING XGBOOST

Online machine learning is performed to create and update a machine learning model that predicts the three parasitic parameters R_{bus} , L_{bus} , and C_{bus} . Fig. [5](#page-3-0) shows the algorithm of Gradient Boosting Decision Tree (GBDT) used for machine learning to achieve high prediction accuracy. In GBDT, training datasets must not be pre-processed and it has a fast training time. XGBoost [\[22\],](#page-7-0) an open-source software library in Python, is used to create the machine learning model. Table [3](#page-3-0) shows the variables defined in Fig. [5.](#page-3-0) In GBDT, the algorithm is based on the decision tree that predicts the objective variable *y* of the training datasets (corresponding to *R*bus, *L*bus, and *C*bus) by creating conditional branches for the features x of the training datasets (correspond to f , ℓ , w , t , h , *d* and *c*). In Fig. [5,](#page-3-0) *M* decision trees described in blue graphics are connected in series and trained such that the error between the objective variable *y* and predicted value \bar{v} is small. Thus,

(b) Prediction

FIGURE 5. Algorithm of Gradient Boosting Decision Tree (GBDT) to achieve high prediction accuracy by decreasing the error between the predicted values \bar{y} and objective variable y **.**

TABLE 3. Definition of Variables in GBDT

the weights *Wm* of the predicted value in each decision tree are added to increase the accuracy. The weights *Wm* in each decision tree are trained to decrease as the index increases from 1 to *M*.

Fig. 6 shows the cross-validation, an evaluation method for the machine learning model. The datasets are divided into training data used to train the model and validation data used to evaluate the generality of the model. In the cross-validation, the datasets are divided into four pieces, one of which (25% of the datasets) is used as the validation data, and the remaining three pieces (75% of the datasets) are used as the training data for machine learning. Four machine learning models are created repeatedly such that all four sets of data become validation data sequentially; the average output of each model \bar{y} is used as the predicted value. Multiple training patterns of the machine learning model are executed, allowing for a

FIGURE 6. Cross-validation, an evaluation methods to predict the accuracy of the machine learning model.

highly accurate prediction of various patterns of input data. This validation ensures the reliability of the machine learning model.

Finally, test datasets other than the training datasets are prepared as true unknown data to evaluate the accuracy and reliability of the machine learning model. Table 4 shows the variable ranges of frequency *f* and the six variables of the bus bar geometries shown in Table [1](#page-1-0) in the test datasets. The values of *d* and *c* in Table 4 are selected as the combinations that satisfy the constraints in Table [2](#page-2-0) and the number of test datasets is 1,536.

FIGURE 7. Change in the analysis time of FEA with an increasing number of analysis points.

TABLE 5. Computer Specification Used for FEA

FIGURE 8. Change in MRE and training time of *R***bus with an increasing number of analysis points.**

V. MACHINE LEARNING RESULTS

Fig. 7 shows the change of analysis time for the FEA when the number of analysis points for ℓ , w , d , and c is increased from two to nine. Table 5 shows the specifications of the computer used for the FEA. Notably, the analysis time varies depending on the computer specifications and model to be analyzed. When the number of analysis points is two (the number of analysis datasets is 1,920), the analysis time is 2.90×10^3 s. In contrast, when the number of analysis points is nine (the number of analysis datasets is 831,616), the analysis time is 5.25×10^5 s. As the number of analysis points of ℓ , *w*, *d*, and *c* increases, the analysis time for the FEA increases exponentially.

Figs. 8–10 show the change in the training time with XGBoost and the mean relative error (MRE) between the predicted and analyzed values in the test datasets when the

FIGURE 9. Change in MRE and training time of *L***bus with an increasing number of analysis points.**

FIGURE 10. Change in MRE and training time of *C***bus with an increasing number of analysis points.**

number of analysis points for ℓ , w , d , and c is increased from two to nine. When the number of analysis points is two (the number of analysis datasets is 1,920), the MREs of the predicted and the analyzed values in *R*bus, *L*bus, and *C*bus are 143%, 28.3%, and 252%, respectively. Conversely, when the number of analysis points is nine (the number of analysis datasets is 831,616), the MREs are 5.82%, 4.94%, and 8.41%, respectively. Fig. [11](#page-5-0) shows a detailed comparison of the predicted and analyzed values in *L*bus. In terms of training time, when the number of analysis points is two (the number of analysis datasets is 1,920), the training times for *R*bus, *L*bus, and*C*bus are 0.885, 0.915, and 0.919 s, respectively. In contrast, when the number of analysis points is nine (the number of analysis datasets is 831,616), the training times are 190 sec., 258 sec., and 187 sec., respectively.

Figs. 7–10 describe that there is a trade-off between the prediction accuracy and analysis/training time. The result obtained by online machine learning enables the number of analysis datasets to be optimized by considering the required prediction accuracy of the three parasitic parameters and the analysis/training time.

FIGURE 11. Detailed comparison between the predicted (horizontal axis) and the analyzed (vertical axis) of *L***bus.**

TABLE 6. Size of Bus Bar Geometries for Measurement

Variable	Size
ł.	80 mm
\overline{w}	80 mm
t.	$35 \mu m$
h.	1.6 mm
d.	10 mm
C	30 mm

VI. APPLICATION TO ACTUAL BUS BAR

Using the machine learning model, three parasitic parameters in an actual laminated bus bar with two apertures for terminals are predicted. From the prediction results presented in Section [V,](#page-4-0) the machine learning model with nine analysis points for ℓ , w , d , and c has the highest accuracy and is adopted for the prediction of the actual bus bar. Table 6 shows the values of the six variables that determine the actual bus

FIGURE 12. Laminated bus bar for measurement using the impedance analyzer.

FIGURE 13. Measurement environment for *R***bus and** *L***bus using the impedance analyzer.**

bar geometries. Fig. 12 shows the actual bus bars fabricated by processing 2-layer FR-4 boards. R_{bus} (R_a and R_b) and L_{bus} (L_{a} and L_{b}) are measured with the terminals P1 and P2 shorted, and C_{bus} is measured with the terminals P1 and P2 open from the T-type equivalent circuit shown in Fig. [3.](#page-2-0) The frequency characteristics of the three parasitic parameters are measured using an impedance analyzer (Keysight Technologies E4990 A). Fig. 13 shows a picture of an environment in which only R_{bus} and L_{bus} are measured, with the terminals P1 and P2 shorted and the terminals P3 and P4 connected to the impedance analyzer. Copper pieces are bonded at terminals P3 and P4, as shown in Fig. 12 such that the bus bar can be connected to the impedance analyzer.

Figs. [14–16](#page-6-0) show comparisons of the predicted and the measured frequency characteristics for the three parasitic parameters. The frequency characteristics predicted by the machine learning model are generally consistent with the measured frequency response for all three parasitic parameters in the frequency range of 50 kHz to 100 MHz. Particularly, the increasing trend from low to high frequencies in *R*bus is consistent between the predicted and measured values. Therefore, the machine learning model created by this procedure can predict the three parasitic parameters in the frequency

FIGURE 14. Frequency characteristics of the predicted and measured *R***bus.**

FIGURE 15. Frequency characteristics of the predicted and measured *L***bus.**

FIGURE 16. Frequency characteristics of the predicted and measured *C***bus.**

range of 50 kHz to 100 MHz and can be applied to an actual laminated bus bar.

VII. DISCUSSION

A. BENEFITS COMPARED WITH CONVENTIONAL FEA

In this procedure, the parasitic parameters can be predicted easily and quickly by inputting the values of the bus bar structure and frequency without the FEA, after creating the machine learning model. In the conventional FEA, time and effort are required to set up the analysis software in a complex manner, such as the generation of the meshes and the definition of boundary conditions. With the machine learning model, circuit designers with no FEA skill and knowledge can easily predict the parasitic parameters in bus bars.

B. APPLICATION TO OTHER TYPES OF BUS BARS

The parasitic parameters for other bus bar designs can be predicted, such as multiple apertures or layers, by further increasing the number of variables in bus bar geometries than those in Fig. [1,](#page-1-0) enriching the patterns of the analysis datasets, and creating a more generic machine learning model.

C. PREDICTION FOR PARASITIC PARAMETERS OUTSIDE FREQUENCY RANGE

The machine learning model has a range of applications that can accurately predict them, which is highly dependent on the range of training datasets. In other words, the reliability of the parasitic parameters predicted by the machine learning model is high within the frequency range of 50 kHz to 100 MHz, which is set as the training datasets. However, the error between the predicted and analyzed values can be large outside the frequency range of 50 kHz to 100 MHz. To accurately predict the parasitic parameters outside the frequency range of 50 kHz to 100 MHz, the frequency range set in the training datasets should be expanded and the machine learning model should be updated.

D. EVALUATION OF APPLICABILITY OF MACHINE LEARNING MODEL IN ACTUAL DESIGN

It is evaluated that the machine learning model can be applied to the actual design using the MRE of the parasitic inductance *L*bus as an example. The MRE of *L*bus is 4.94% when the number of analysis points for ℓ , w , d , and c is nine, as shown in Fig. [9.](#page-4-0) The order of magnitude of the analyzed value of L_{bus} is assumed to be 10 nH from Fig. [11,](#page-5-0) and the absolute difference between the predicted and analyzed value is 0.5 nH from the MRE. The switching speed of the SiC-MOSFET rated at 1,200 V is assumed to be 10 A/ns [\[23\].](#page-7-0) Under these conditions, the absolute difference between the predicted and analyzed surge voltage is 5 V. This error in the surge voltage is only 1% of the driving voltage for power converter circuits driven at 500 V, and the surge voltage can be evaluated as a negligible error. Therefore, the machine learning model can be used to evaluate the surge voltage and design laminated bus bars.

VIII. CONCLUSION

This article proposed a prediction procedure for parasitic parameters considering laminated bus bar geometries by performing online machine learning based on analysis datasets. The three parasitic parameters *R*bus, *L*bus, and *C*bus can be predicted in the laminated bus bar by inputting the values of the bus bar structure and frequency into the machine learning model.

The ability to predict the parasitic parameters of a laminated bus bar using machine learning enables the adoption of measures to suppress the surge voltages and oscillations in switching waveforms, which are problems in power converter circuits. Additionally, this procedure can be applied to numerous wiring patterns, including laminated bus bars and modules, by sequentially increasing the number of different types of analysis datasets and performing online machine learning.

REFERENCES

- [1] H.-P. Nee, J. W. Kolar, P. Friedrichs, and J. Rabkowski, "Editorial: Special issue on wide Bandgap power devices and their applications, 2014," *IEEE Trans. Power Electron.*, vol. 29, no. 5, pp. 2153–2154, May 2014.
- [2] H. A. Mantooth, M. D. Glover, and P. Shepherd, "Wide Bandgap technologies and their implications on miniaturizing power electronic systems," *IEEE Trans. Emerg. Sel. Topics Power Electron.*, vol. 2, no. 3, pp. 374–385, Sep. 2014.
- [3] Jerry L. Hudgins, "Power electronic devices in the future," *IEEE Trans. Emerg. Sel. Topics Power Electron.*, vol. 1, no. 1, pp. 11–17, Mar. 2013.
- [4] S. Jahdi, O. Alatise, C. Fisher, L. Ran, and P. Mawby, "An evaluation of silicon carbide unipolar technologies for electric vehicle drive-trains," *IEEE Trans. Emerg. Sel. Topics Power Electron.*, vol. 2, no. 3, pp. 517–528, Sep. 2014.
- [5] S. Abe, K. Fukushima, D. Iioka, and D. Orihara, "Study of the current potential of power converters -applied power semiconductor devices, power density and losses-," in *Proc. IEEJ Int. Power Electron. Conf.*, 2022, pp. 1275–1280.
- [6] Y. Noge and M. Shoyama, "High bandwidth active gate driver for simultaneous reduction of switching surge and switching loss of SiC-MOSFET," *IEEJ J. Ind. Appl.*, vol. 12, no. 3, pp. 384–391, 2023.
- [7] T. -J. Liang et al., "Implementation and applications of grid-forming inverter with SiC for power grid conditioning," *IEEJ J. Ind. Appl.*, vol. 12, no. 3, pp. 244–253, 2022.
- [8] S. Takahashi, K. Wada, H. Ayano, S. Ogasawara, and T. Shimizu, "Review of modeling and suppression techniques for electromagnetic interference in power conversion systems," *IEEJ J. Ind. Appl.*, vol. 11, no. 1, pp. 7–19, 2022.
- [9] S. Tanimoto and K. Matsui, "High junction temperature and low parasitic inductance power module technology for compact power conversion systems," *IEEE Trans. Electron Devices*, vol. 62, no. 2, pp. 258–269, Feb. 2015.
- [10] X. Lin, J. Li, and M. Johnson, "Design and construction of a co-planar power bus interconnect for low inductance switching," in *Proc. IEEE Int. Workshop On Integr. Power Packag.*, 2017, pp. 1–4.
- [11] R. Alizadeh et al., "Busbar design for distributed DC-Link capacitor banks for traction applications," in *Proc. IEEE Energy Convers. Congr. Expo.*, 2018, pp. 4810–4815.
- [12] K. Takao and S. Kyogoku, "Ultra low inductance power module for fast switching SiC power devices," in *Proc. IEEE Int. Symp. Power Semicond. Devices IC's*, 2015, pp. 313–316.
- [13] S. Fukunaga and T. Funaki, "Chip layout optimization of SiC power modules based on multiobjective electro-thermal design strategy," *IEEJ J. Ind. Appl.*, vol. 11, no. 1, pp. 157–162, 2022.
- [14] M. Ando and K. Wada, "Design of acceptable stray inductance based on scaling method for power electronics circuits," *IEEE Trans. Emerg. Sel. Topics Power Electron.*, vol. 5, no. 1, pp. 568–575, Mar. 2017.
- [15] K. Mitsui and K. Wada, "Design of a laminated bus bar optimizing the surge voltage, damped oscillation, and switching loss," *IEEE Trans. Ind. Appl.*, vol. 57, no. 3, pp. 2737–2745, May/Jun. 2021.
- [16] T. Dragičević, P. Wheeler, and F. Blaabjerg, "Artificial intelligence aided automated design for reliability of power electronic systems,' *IEEE Trans. Power Electron.*, vol. 34, no. 8, pp. 7161–7171, Aug. 2019.
- [17] C. M. Bingham, Y. A. Ang, M. P. Foster, and D. A. Stone, "Analysis and control of dual-output LCLC resonant converters with SignificantLeakage inductance," *IEEE Trans. Power Electron.*, vol. 23, no. 4, pp. 1724–1732, Jul. 2008.
- [18] R. Shigetomi and K. Wada, "Prediction procedure of parasitic paramzeters considering laminated bus bar geometries based on machine learning," in *Proc. 11th Int. Conf. Power Electron. - ECCE Asia*, 2023.
- [19] B. Lu et al., "Determination of stray inductance of low-inductive laminated planar multiport busbars using vector synthesis method," *IEEE Trans. Ind. Electron.*, vol. 67, no. 2, pp. 1337–1347, Feb. 2020.
- [20] Y. Wu et al., "Electrothermal-control co-design of an all silicon carbide 2×250 kW dual inverter for heavy-duty traction applications," *IEEE Trans. Ind. Appl.*, vol. 58, no. 1, pp. 505–516, Jan./Feb. 2022.
- [21] Z. Wang, Y. Wu, M. H. Mahmud, Z. Yuan, Y. Zhao, and H. A. Mantooth, "Busbar design and optimization for voltage overshoot mitigation of a silicon carbide high-power three-phase T-type inverter," *IEEE Trans. Power Electron.*, vol. 36, no. 1, pp. 204–214, Jan. 2021.
- [22] XGBoost : "dmlc XGBoost stable," [https://xgboost.readthedocs.io/en/](https://xgboost.readthedocs.io/en/stable/) [stable/](https://xgboost.readthedocs.io/en/stable/)
- [23] ROHM Application Note, "SiC power devices and modules application note Rev.003," p. 60, 2020.

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