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Model Predictive Control for Single-Phase Switched-Capacitor Multilevel Inverters

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ABSTRACT Single-phase switched-capacitor multilevel inverters are an excellent alternative for low-power applications as they provide high voltage gain. However, their control and modulation are not simple due to the particularity of these topologies. Finite Control-Set Model Predictive Control (FCS-MPC) has therefore emerged as an attractive control alternative for these inverters. This article seeks to establish guidelines for the implementation of FCS-MPC in this type of inverter. To that end, FCS-MPC is implemented in two topologies that have previously been described in the literature as well as in a new topology. The results establish excellent methodological guidelines for applying FCS-MPC in this family of inverters, that achieve high dynamic responses.

INDEX TERMS Predictive control, DC-AC power converters, multilevel inverters, switched capacitor circuits.

I. INTRODUCTION

Multilevel inverters (MLIs) are widely applied to renewable energy sources [1], motor drives [2], and micro-grid applications [3] due to their numerous benefits like high power quality, the low voltage rating of the switches, and their ability to handle low-switching frequencies, etc. [4], [5]. In general terms, there are three classical configurations for MLIs: neutral point clamped (NPC), flying capacitor (FC), and cascaded H-bridge (CHB) configurations [6], [7], [8]. These three configurations can be divided into three classes: switched DC-source MLIs (SDC-MLIs) like CHB-MLI, switched-diode MLIs (SD-MLIs) like NPC-MLIs, and switched-capacitor MLIs (SC-MLIs) like FC-MLIs. The limitation of SDC-MLIs is that they require multiple independent DC voltage sources that rely on multiple DC-DC inverters or a big transformer. The weakness of SD-MLIs is their use of multiple discrete diodes, which limits their operation in low power factors. The drawback of SC-MLIs is that they require several capacitors to achieve balanced voltage control [9], [10], [11], [12]. Among all types of the aforementioned topologies, switched-capacitor multilevel inverters have recently become popular among researchers for low-power applications since they use only one or few DC voltage sources [12], [13].

Furthermore, with a good design of the SC-MLI topology, they can boost the input dc-link voltage and self-balance the capacitor voltage. This family of MLIs, like other topologies (SDC-MLI and SD-MLIs), suffers from a high number of components (switching devices) and also capacitors to generate more voltage levels [14]. Additionally, some of the presented SC-MLI topologies require a proper algorithm to balance the capacitor voltage, which makes them more sophisticated and costly [15]. [16], [17] have been offered as five-level topologies for SC-MLIs. [16] utilizes six switches and two extra diodes, which cannot be extended as a generalized topology to generate more voltage levels. The suggested topology in [17] to generate five levels needs more additional

bidirectional switches than in [16], which increases the conduction losses due to the active one diode and one IGBT in on-state mode. Presented topologies [18], [19] use a high number of switches, eight, to make seven levels. In addition, they need a high number of capacitors, four, which increases the power losses and the cost of the inverter. Three seven-level SC-ML topologies have been introduced in [20], [21], [22] using a small number of power switches. Nevertheless, these inverters employ three or more capacitors, except for [22], which uses two. [21] can not boost the voltage, and [22] has high voltage stress on the switches, which affects the power loss and cost of the inverter. [23], [24], [25], [26], [27] have developed SC-MLIs that can boost the output voltage and charge the capacitors in a self-balancing mode, but they need a high number of power switches, ten, some of them are bidirectional. As a result, they lost modularity and experienced increased losses and costs. In addition, most of these topologies require more than two capacitors, which increases the cost and reduces efficiency. Generally, SC-MLIs topologies have been controlled by high-frequency pulse width modulation (PWM) techniques like level-shift, phase-shift, carrier-based PWMs, etc., or by a low-frequency PWM like staircase modulation technique. PWM-based modulation methods have several advantages, including the ability to use extremely high frequencies, independently control the amplitude and frequency, and reduce both load current distortion and filter requirements [14], [15], [16]. Despite these benefits, PWM methods that use a sinusoidal waveform for modulation are not suitable for MLIs because the output inverter frequency must be synchronized with the modulation frequency [17], [18], [19]. In addition, some SC-MLI topologies combine several logical functions with PWM to generate the proper switching pulses, which is more complex to implement [21], [22]. Furthermore, they use a proportional-integral (PI) controller to achieve closed-loop control, which can be complicated due to the difficulty in determining a suitable value [23]. Indeed, the classical PWM methods for the switched-capacitor MLIs create a higher capacitor voltage ripple, which causes high ripple losses [24], [25].

At present, researchers are introducing new SC-MLI topologies almost daily [26], [27]. Since they are controlled by conventional PWM-based methods, they are difficult to implement. Therefore, it is essential that a proper control technique be developed sooner rather than later to ensure that the new topologies that are being developed will be compatible with the state-of-the-art control techniques and that they can be used well into the future. However, lately, with the development of digital control hardware platforms and fast microprocessors, nonlinear control methods such as Slide Mode Control (SMC) [28], Fuzzy Logic Control (FLC) [29], and Model Predictive Control (MPC) have started to appear in the field of multilevel inverter control [30], [31].

Among the above control techniques, MPC is an attractive control alternative for this family of inverters for the following attributes:

1. Fast dynamic response.
2. Ability to control multiple control objectives.
3. Dead-time compensation ability.
4. Easy inclusion of nonlinearities in the model.
5. Ability to handle shifting control objectives.
6. Easy implementation of the resulting controller.

FCS-MPC uses the discrete nature of power electronic inverters to control the current, voltage, power, and torque, etc. In a power electronics inverter, the switches can only be turned on and off in two states, and their combination creates a finite number of states. Using this inherent feature, the inverter switching model can be easily presented, and the prediction can be summarized for the limited situations mentioned. The main elements of this control scheme are the mathematical model of the system and the predefined cost function [32], [33], [34].

The objective of the article is to propose a generalized guideline for applying FCS-MPC to single-phase switched-capacitor MLIs. In order to accomplish this objective, the conventional FCS-MPC technique is applied to two typical single-phase switched-capacitor MLIs to become familiar with the implementation of MPC for this family of inverters. After that, by obtaining the data from these two typical SC-MLI topologies, a generalized FCS-MPC guideline is proposed in order to apply to any single-phase switched-capacitor MLI. To evaluate the correctness of the proposed guideline, a new switched-capacitor multilevel inverter topology is presented. In addition, the power circuit and operation modes of the proposed topology are illustrated in detail, and then, to show the strength and weaknesses of the proposed topology, it is compared to several state-of-the-art SC-MLI topologies. Then, based on the proposed guideline, the FCS-MPC technique is implemented to control the proposed topology. Finally, the experiment results are presented to confirm the correct operation of the proposed topology based on the proposed guideline.

In the following, in Section II, the conventional FCS-MPC technique is applied to two typical single-phase SC-MLI topologies. The proposed generalized FCS-MPC guideline is introduced step-by-step in Section III. The principal operation of the proposed topology and the implementation of FCS-MPC for the proposed topology based on the proposed guideline are described in detail in Section IV. Section V compares the proposed topology with the state-of-the-art SC-MLI topologies in different aspects. The thermal analysis and efficiency assessment of the proposed topology are presented in Section VI. Finally, the experimental results of the proposed topology are presented in Section VII.

II. IMPLEMENTATION OF CONVENTIONAL FCS-MPC TECHNIQUE FOR TWO CLASSICAL SWITCHED-CAPACITOR MLI

The objective of proposing this section is to introduce a generalized FCS-MPC guideline that is applicable to any single-phase switched-capacitor MLI. To accomplish this, the conventional FCS-MPC technique is applied to the two classical single-phase switched capacitor MLI topologies in

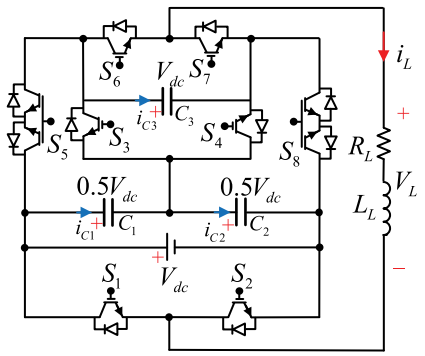


FIGURE 1. First SC-MLI topology.

TABLE 1. Valid Switching States of the First SC-MLI Topology. (↑: Charging, ↓: Discharging, –: No Effect)

States	On-State Switches	C_1	C_2	C_3	i_{C1}	i_{C2}	i_{C3}	V_o	V_L
1	S_1, S_5, S_6, S_8	-	-	↑	0	0	0	0	0
2	S_2, S_5, S_7, S_8	-	-	↑	0	0	0	0	
3	S_2, S_4, S_7	↑	↓	-	0	$-i_L$	0	V_{C2}	$+0.5V_{dc}$
4	S_2, S_5, S_6	-	-	-	0	0	0	V_{dc}	$+V_{dc}$
5	S_2, S_4, S_6	↑	↓	↓	0	$-i_L$	$-i_L$	$V_{dc}+V_{C2}$	$+1.5V_{dc}$
6	S_2, S_3, S_6	↓	↑	-	$+i_L$	0	0	$-V_{C1}$	$-0.5V_{dc}$
7	S_1, S_7, S_8	-	-	-	0	0	0	V_{dc}	$-V_{dc}$
8	S_1, S_3, S_7	↓	↑	↓	$+i_L$	0	$+i_L$	$V_{dc}+V_{C1}$	$-1.5V_{dc}$

this section. Then, in the next section, the proposed generalized FCS-MPC guideline is introduced. In the following, the operation of the topologies as well as the mathematical models of their respective inverters, load currents, and capacitors are described. Finally, both topologies are simulated in MATLAB/Simulink to verify the performance of the control technique.

A. FIRST SC-MLI TOPOLOGY

The power circuit of the first single-phase SC-MLI topology is presented in Fig. 1; this topology was developed by Liu et al. [25]. It consists of ten power switches, six unidirectional switches, two bidirectional switches, and three capacitors (charged in self-balancing mode) and can generate seven voltage levels. Table 1 shows the switching table of this topology.

1) MATHEMATICAL MODEL OF FIRST SC-MLI TOPOLOGY

In this study, the power switches are assumed to be ideal, so they have only two states: ON or OFF. As shown in Table 1, the first SC-MLI topology has eight possible switching states. Therefore, the output voltage of the first inverter V_L can be represented in terms of input DC voltage V_{dc} and the switching function of the inverter as follows:

$$V_L(t) = (F_{S_6} - F_{S_1})V_{dc} + (F_{S_4} - F_{S_3})0.5V_{dc} \tag{1}$$

The power switches are assumed to be ideal. Therefore, $F_{S_1}, \ldots, F_{S_6}$ are the switching function of $S_1, \ldots, S_6$ which have two states ON or OFF.

2) LOAD MODEL

The output voltage of the inverter is given in terms of load current i_L and load parameters (L_L, R_L) as:

$$V_L(t) = R_L i_L(t) + L_L \frac{di_L(t)}{dt} \tag{2}$$

$$\frac{di_L(t)}{dt} = \frac{V_L(t) - R_L i_L(t)}{L_L} \tag{3}$$

The first order derivative of the inverter output current can be represented using the Euler approximation as follows:

$$\frac{di_L}{dt} \simeq \frac{i_L(k+1) - i_L(k)}{T_s} \tag{4}$$

Here, T_s represents the sampling time of the FCS-MPC controller. Meanwhile, $(k+1)$ and (k) represent the $(k+1)th$ and $(k)th$ time intervals of the sampled output current of the inverter, respectively. Therefore, by using (4) in (3), the predicted output current for the $(k+1)$ sample can be represented as follows:

$$i_L(k+1) = \left(1 - \frac{R_L T_s}{L_L}\right) i_L(k) + \frac{T_s}{L_L} V_L(k) \tag{5}$$

In (5), the output current of the inverter is predicted for the $(k+1)th$ time interval using the $(k)th$ sampled current and the predicted output voltage of the inverter using the voltage vectors. The first presented SC-MLI has eight switching states with seven different output voltages and various effects on the capacitor charging/discharging operations. Using all the available switching states, the controller optimizes the inverter's operation by selecting the optimal switching states.

3) CAPACITOR MODEL

The first topology has three capacitors (C_1, C_2, C_3), and their corresponding voltages are (V_{C1}, V_{C2}, V_{C3}); they must maintain $0.5V_{dc}$, $0.5V_{dc}$ and V_{dc}, respectively. The continuous time models of the capacitors' voltages are represented using their initial voltages $(V_{C1}(0), V_{C2}(0), V_{C3}(0))$ and their corresponding currents (i_{C1}, i_{C2}, i_{C3}) as follows:

$$V_{C1}(t) = V_{C1}(0) + \int_0^t i_{C1}(t)dt \tag{6}$$

$$V_{C2}(t) = V_{C2}(0) + \int_0^t i_{C2}(t)dt \tag{7}$$

$$V_{C3}(t) = V_{C3}(0) + \int_0^t i_{C3}(t)dt \tag{8}$$

Then, the discrete-time modeling of the capacitor voltages is determined via Euler approximation as follows:

$$V_{C1}(k+1) = V_{C1}(k) + \frac{T_s}{C_1} i_{C1}(k+1) \tag{9}$$

$$V_{C2}(k+1) = V_{C2}(k) + \frac{T_s}{C_2} i_{C2}(k+1) \tag{10}$$

$$V_{C3}(k+1) = V_{C3}(k) + \frac{T_s}{C_3} i_{C3}(k+1) \tag{11}$$

The capacitors' currents vary based on the applied switching states and the output current direction of the inverter. According to Table 1, the predicted currents of the capacitors are related to the measured output currents of the inverter as follows:

$$i_{C1}(k+1) = (F_{S_3}) i_L(k) \tag{12}$$

$$i_{C2}(k+1) = -(F_{S_4}) i_L(k) \tag{13}$$

$$i_{C3}(k+1) = (F_{S_4} - F_{S_3}) i_L(k) \tag{14}$$

By substituting (12)–(14) in (9)–(11) and measuring the capacitors' voltages, their future voltages can be predicted.

4) FCS-MPC CONTROLLER

The inverter's predicted and reference load current and capacitor voltages are included in the cost function of the FCS-MPC controller as follows:

$$\begin{aligned} G_1(k) = {} & (i_L^*(k) - i_L(k+2))^2 \\ & + \lambda_1[(V_{C_1}^*(k) - V_{C_1}(k+2))^2 \\ & + (V_{C_2}^*(k) - V_{C_2}(k+2))^2] \\ & + \gamma_1[V_{C_3}^*(k) - V_{C_3}(k+2)^2] \end{aligned} \tag{15}$$

where λ_1 and γ_1 represent the weighting factors of the capacitors' voltages (C_1, C_2, C_3) that are required to achieve proper operation of the proposed topology. The weighting factor is calculated in terms of the rated load current and capacitor reference voltages ($\lambda_1 = i_L/V_{C1,2}^*$, $\gamma_1 = i_L/V_{C3}^*$) to compensate for the difference in the nature of the control objectives [30]. The reference values of the capacitor voltages are controlled by the following:

$$V_{C1}^*(k) = V_{C2}^*(k) = 0.5V_{dc} \tag{16}$$

$$V_{C3}^*(k) = V_{dc} \tag{17}$$

B. SECOND SC-MLI TOPOLOGY

The schematic circuit of the second topology is a classical stacked multicell converter (SMC), shown in Fig. 2 [8]. The SMC generates five levels with eight power switches, two DC-link capacitors (C_{21}, C_{22}), and two floating capacitors (C_{11}, C_{12}). The DC-link capacitors are charged to half of the dc-link voltage V_{dc}. The floating capacitors are charged to a quarter of the dc-link voltage. The SMC's power switches operate complementary to ensure the normal operation of the system. The switching pattern of the classical five-level SMC is illustrated in Table 2.

As in the first topology, the output voltage of the SMC (V_L) can be expressed in terms of the DC-link, floating capacitor voltages, and switching function as:

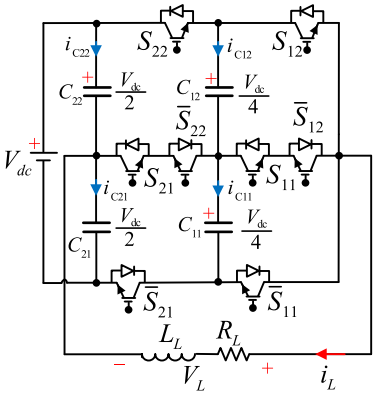


FIGURE 2. Classical 5-level SMC topology.

TABLE 2. Valid Switching States of the Five-Level SMC Topology. (↑: Charging, ↓: Discharging, –: No Effect)

States	On-State Switches	C_{12}	C_{11}	i_{C12}	i_{C11}	V_o	V_L
1	S_{21}, S_{22}	↓	↓	$+i_L$	$+i_L$	$V_{C22} - V_{C12} - V_{C11}$	
2	S_{11}, S_{21}	-	-	0	0	$V_{C12} - V_{C11} - V_{C21}$	0
3	S_{11}, S_{12}	↓	↓	$-i_L$	$-i_L$	V_{C22}	
4	S_{11}, S_{21}, S_{22}	↑	-	$+i_L$	0	$V_{C22} - V_{C12}$	$+0.25V_{dc}$
5	S_{11}, S_{12}, S_{21}	↓	-	$-i_L$	0	V_{C12}	
6	S_{11}, S_{12}, S_{21}, S_{22}	-	-	0	0	V_{C22}	$+0.5V_{dc}$
7	S_{21}	-	↑	0	$+i_L$	$-V_{C11}$	$-0.25V_{dc}$
8	S_{11}	-	↓	0	$-i_L$	$V_{C11} - V_{C21}$	
9	$\overline{S}_{11}$, $\overline{S}_{12}$, $\overline{S}_{21}$, $\overline{S}_{22}$	-	-	0	0	V_{C21}	$-0.5V_{dc}$

$$\begin{aligned} V_L(t) = {} & V_{C11}(F_{S_{11}} - F_{S_{21}}) + V_{C12}(F_{S_{12}} - F_{S_{22}}) \\ & + V_{C21}(F_{S_{21}} - 1) + V_{C22}F_{S_{22}} \end{aligned} \tag{18}$$

Here, $F_{S_{11}}, F_{S_{12}}, F_{S_{21}}, F_{S_{22}}$, are the switching function of $S_{11}, S_{21}, S_{12}, S_{22}$ which have two states ON or OFF.

The model of the load is given by (2)–(5), and the model of the capacitors can be obtained from (6)–(11). As previously stated, the capacitors' currents vary according to the applied switching states and the direction of the inverter's output current. According to Table 2, the predicted current of the capacitor is related to the measured output current of the inverter by the following:

$$i_{C11}(k+1) = (F_{S_{21}} - F_{S_{11}}) i_L(k) \tag{19}$$

$$i_{C12}(k+1) = (F_{S_{22}} - F_{S_{12}}) i_L(k) \tag{20}$$

The inverter's predicted and reference load currents and capacitor voltages, as well as the second SC-MLI's switching frequency reduction, are included in the cost function of the MPC controller as:

$$\begin{aligned} G_2(k) = {} & (i_L^*(k) - i_L(k+2))^2 \\ & + \lambda_2[V_{C_{11}}^*(k) - V_{C_{11}}(k+2)^2 \end{aligned}$$

TABLE 3. Simulation Parameters

Symbol	Parameters	Values
V_{dc}	DC-link voltage	120[V]
$C_1, C_2, C_{11}, C_{12}, C_{21}, C_{22}$	Capacitors	2200[μF]
C_3	Capacitor	1200[μF]
f_L	Load frequency	50[Hz]
R-L	Load	50[Ω], 10[mH]
$\lambda_1, \gamma 1$	Weighting Factors	0.05,0.025
$\lambda 2, \gamma_2$	Weighting Factor	0.03,0.08
T_s	Sample time	100[μs]

$$+ (V^*_{C_{12}}(k) - V_{C_{12}}(k+2))^2] + \gamma_2 G_{sw}(k+2) \quad (21)$$

The reference values of the capacitor voltages are equal to those of the first topology as expressed in (16). The switching frequency reduction in the power inverters refers to commutations between switches that can be easily controlled by MPC. Therefore, as can be seen in (21), another term in the cost function to reduce the number of switches, which change between $S(k)$ and $S(k+1)$, which can be expressed by using (18) as:

$$\begin{aligned} G_{sw}(k+2) = {} & 0.5(F_{S_{11}}(k+1) - F_{S_{11}}(k))^2 \\ & + 0.5(F_{S_{12}}(k+1) - F_{S_{12}}(k))^2 \\ & + 0.5[(F_{S_{21}}(k+1) - F_{S_{21}}(k))^2 \\ & + (F_{S_{22}}(k+1) - F_{S_{22}}(k))^2] \end{aligned} \quad (22)$$

C. SIMULATION STUDY

Both the presented topologies are simulated in MATLAB/Simulink to verify the performance of the proposed FCS-MPC. The inverters feed an R-L load. The input DC-link is set to 120[V]. The simulation parameters are listed in Table 3. The topologies are evaluated for a step change load current at 6.6[ms] to demonstrate the dynamic response of the MPC. The simulation results of the first SC-MLI are shown in Fig. 3, and those of the second topology are shown in Fig. 4. Fig. 3(a) shows the load voltage of the first SC-MLI. As can be seen in the figure, when the reference current is decreased from 3[A] to 2[A] the number of levels reduces from seven to five. The reference and load currents are shown in Fig. 3(b). The load current correctly tracks the reference signal before and after the current change. In addition, it has a fast dynamic response when the reference signal is reduced. The capacitor voltage waveforms are shown in Fig. 3(c). As can be seen, the capacitor voltages are balanced in their references in both: steady state and transient state (after the step change in the reference signal). Fig. 4 shows the simulation results for the 5L-SMC topology. For this inverter, in addition to current control and capacitor voltage balancing, the communication reduction has been included in the cost function. The switching frequency

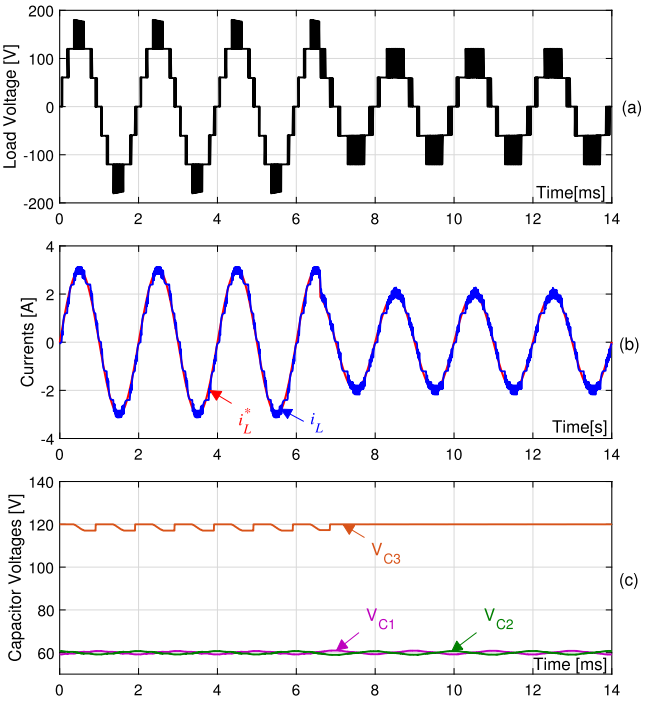


FIGURE 3. Simulation results of the first 7L-SC-MLI: (a) load voltage; (b) load and reference currents; (c) capacitor's voltages.

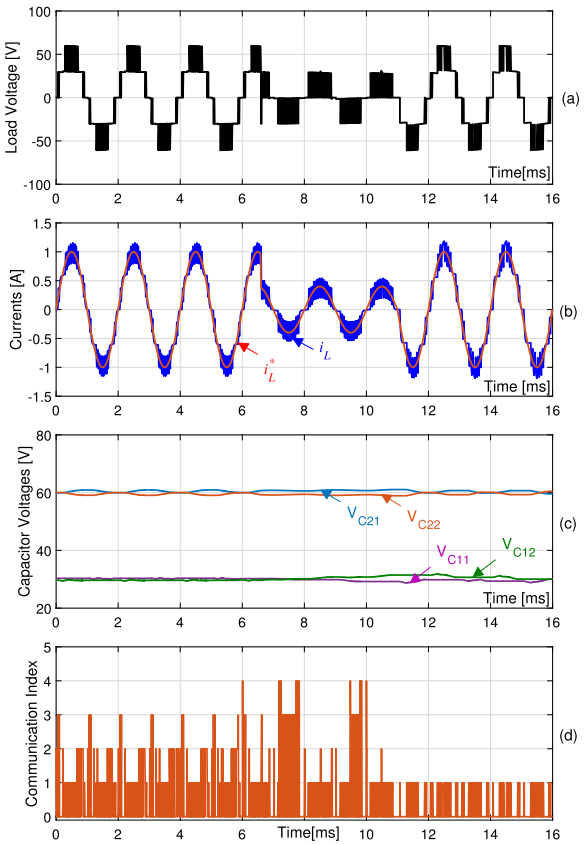


FIGURE 4. Simulation results of second classical 5L-SMC; (a) load voltage; (b) load and reference currents; (c) capacitors' voltages; (d) communication index.

reduction is applied at time 11[ms]. We considered a step change in the weighting factor γ_2, which is initially zero and increases to 0.08 at time 65[ms]. Consequently, as illustrated in Fig. 4(d), the number of commutations is reduced while the capacitors are kept fixed at their reference values and the load current tracks its reference properly.

III. PROPOSED GENERALIZED FCS-MPC GUIDELINE FOR SINGLE-PHASE SC-MLIS

In this section, based on applying model predictive control to two conventional SC-MLI topologies, a generalized FCS-MPC guideline is presented step-by-step to apply for any single-phase switched-capacitor multilevel inverter.

A. GENERAL DESCRIPTION

1) ELECTRICAL SYSTEM IDENTIFICATION

In the first step, all valid switching states of a multilevel inverter are identified through the power circuit of the inverter. They are then summarized in a single table, as shown in Table 1 and Table 2. The identification table is a tool for managing information. In this table, the switching states are included based on the output voltage of the inverter and their effect on the capacitor voltages.

2) PREDICTIVE MODEL

In the second step, the capacitor voltages and currents are written based on the load current i_L and input voltage V_{dc} because they are typically the only measured variables. It is important to consider that the equations will be based on measurements and switching states; the latter can be considered in a mathematical and logical way as expressed by (1)–(14). Because these equations are in discrete time, the multilevel inverter model will be a function of the input DC-link voltage, capacitor voltages, and switching states S. As a result, $V_L = F_1(V_{dc}, V_C, S)$ can be shown. Likewise, the model of the load is a function of the load parameters, expressed as $i_L = F_2(V_L, i_L)$, and the voltage of the capacitors is a function of the capacitors' current, reference voltage, and switching state, i.e., $V_C = F_4(V_C, i_C)$. Therefore, the capacitor current is a function of the load current and the switching states $i_C = F_3(i_L, S)$.

3) COST FUNCTION

After identifying the prediction model, it can be included as a cost function. Weighting factors must be included in the cost function. They are heuristically designed based on the behavior of the objective variables. Furthermore, it is possible to include other control objectives, like switching frequency reduction (see Fig. 4).

B. FCS-MPC ALGORITHM

The FCS-MPC algorithm is shown in Table 4. First, the measurement signals are written for the SC-MLI; these typically include DC link voltage, capacitor voltage, and output current.

TABLE 4. Generalized FCS-MPC Technique for Switched Capacitor Multilevel Inverter Topologies

FCS-MPC algorithm for SC-MLIs	
Input: $[V_{dc}(k), V_C(k), i_L(k)]$	→ Measurements
Input: $[V_C^*(k), i_L^*(k)]$	→ References
j_{opt}=1	
$V_L(k+1) = F_1[V_{dc}(k), V_C(k), S(k, j_{opt-1})]$	
$i_L(k+1) = F_2[V_L(k+1), i_L(k)]$	→ Compensation Delay
$i_C(k+1) = F_3[S(k, j_{opt-1}), i_L(k+1)]$	
$V_C(k+1) = F_4[V_C(k), i_C(k+1)]$	
$G_{opt} = \infty$	
for $j = 1, \ldots, n$	→ Switching States
$V_L(k+2) = F_1[V_{dc}(k), V_C(k), S(k+1, j)]$	→ Inverter's Model
$i_L(k+2) = F_2[V_L(k+2), i_L(k+1)]$	→ Load's Model
$i_C(k+2) = F_3[S(k+1, j), i_L(k+2)]$	→ Capacitor's Model
$V_C(k+2) = F_4[V_C(k+1), i_C(k+2)]$	
$G(k) = [i_L^*(k) - i_L(k+2)]^2 + \sum_{i=1}^{m} \lambda_i [V_C^*(K) - V_C(K+2)]^2$	→ Cost Function
if	
G(j) < G_{opt}	
G_{opt} = G(j)	→ Optimal States
j_{opt} = j	
end	
end	
Output: $S_{opt} = S(j_{opt-1})$	→ Optimal Vector
$j_{opt-1} = j_{opt}$	→ Go to Next Cycle

The capacitor voltage and output current are then added as reference signals, denoted by (k). Then the delay compensation, which is based on the model predictions for one switching state and denoted by (k+1), is incorporated. The compensation delay must be included in the FCS-MPC algorithm due to the time delay between the measurements and actuation. This time delay improves the system's responsiveness. Next, the relationships between the inverter's model with switching states, the load model, and the capacitor's model are written in a control loop, and the last line, i.e., the cost function indicated by (k+2), is written. The value of the cost function is compared with its optimal value. If it is less than its optimal value, the optimal value is chosen. Finally, based on the optimal cost function, the best switching state is chosen and applied to the inverter. This cycle is repeated for all switching states.

IV. PROPOSED 7-LEVEL SC-MLI TOPOLOGY

A. DESCRIPTION

The power architecture of the proposed switched-capacitor multilevel inverter topology is illustrated in Fig. 5. The circuit of this topology requires only one DC power supply and two

TABLE 5. All Switching States of the Proposed Seven-Level SC-MLI. (↑: Charging, ↓: Discharging, –: No Effect)

States	S_1	S_2	S_3	S_4	S_5	S_6	S_7	S_8	C_1	C_2	i_{C1}	i_{C2}	V_o	V_L
1	0	1	1	0	0	1	1	0	↑	↑	i_{dc}	i_{dc}	0	0
2	1	0	1	0	1	0	1	0	↑	↑	i_{dc}	i_{dc}	0	
3	1	0	0	0	0	1	0	1	↓	-	$-i_L$	0	V_{C1}	$+0.5V_{dc}$
4	1	0	0	1	1	0	0	0	↓	-	$-i_L$	0	V_{C1}	
5	1	0	1	0	0	1	1	0	↑	↑	$i_{dc}-i_L$	$i_{dc}-i_L$	V_{dc}	$+V_{dc}$
6	1	0	0	1	0	1	0	0	↓	-	$-i_L$	0	$V_{dc}+V_{C1}$	$+1.5V_{dc}$
7	0	1	0	1	1	0	0	0	-	↓	0	i_L	$-V_{C2}$	$-0.5V_{dc}$
8	0	1	0	0	0	1	0	1	-	↓	0	i_L	$-V_{C2}$	
9	0	1	1	0	1	0	1	0	↑	↑	$i_{dc}+i_L$	$i_{dc}+i_L$	$-V_{dc}$	$-V_{dc}$
10	0	1	0	0	1	0	0	1	-	↓	0	i_L	$-(V_{dc}+V_{C2})$	$-1.5V_{dc}$

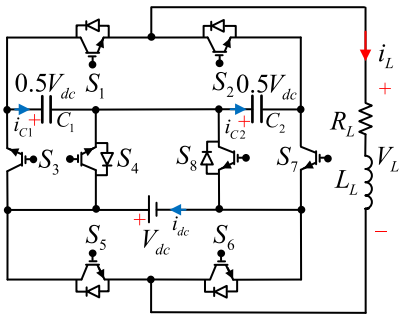


FIGURE 5. Proposed seven-level switched-capacitor multilevel inverter topology.

TABLE 6. Voltage Stress of Each Switch of the Proposed Seven-Level SC-MLI for Generating Each Level

	Switches	S_1	S_2	S_3	S_4	S_5	S_6	S_7	S_8
Voltage Levels	[0]	V_{dc}	0	0	$0.5V_{dc}$	V_{dc}	0	0	$0.5V_{dc}$
	[+1]	0	V_{dc}	$0.5V_{dc}$	V_{dc}	V_{dc}	0	-$0.5V_{dc}$	0
	[+2]	0	V_{dc}	0	0	V_{dc}	0	0	$0.5V_{dc}$
	[+3]	0	V_{dc}	-$0.5V_{dc}$	$0.5V_{dc}$	V_{dc}	0	$0.5V_{dc}$	V_{dc}
	[-1]	V_{dc}	0	$0.5V_{dc}$	V_{dc}	V_{dc}	0	0	0
	[-2]	V_{dc}	0	0	0	0	V_{dc}	$0.5V_{dc}$	$0.5V_{dc}$
	[-3]	V_{dc}	0	$0.5V_{dc}$	V_{dc}	0	V_{dc}	$0.5V_{dc}$	$0.5V_{dc}$

TABLE 7. Current Stress of Each Switch of the Proposed Seven-Level SC-MLI for Generating Each Level

	Switches	S_1	S_2	S_3	S_4	S_5	S_6	S_7	S_8
Voltage Levels	[0]	0	I_L	I_{dc}	0	0	I_L	I_{dc}	0
	[+1]	I_L	0	0	0	0	I_L	0	I_L
	[+2]	I_L	0	$I_{dc}-I_L$	0	0	I_L	$I_{dc}-I_L$	0
	[+3]	I_L	0	0	I_L	0	I_L	0	0
	[-1]	0	I_L	0	0	0	I_L	0	I_L
	[-2]	0	I_L	0	0	I_L	0	$I_{dc}+I_L$	0
	[-3]	0	I_L	$I_{dc}+I_L$	0	I_L	0	0	I_L

capacitors that are connected through the four semiconductor switches (S_3, S_4) and (S_7, S_8).

By paralleling with the input DC source, the voltage of the two selected DC capacitors (C_1, C_2) is charged naturally at half of DC source ($0.5V_{dc}$). Thus, the proposed switched-capacitor inverter does not require any further charge balancing in the control circuits.

Therefore, the proposed inverter provides a stepped waveform with seven different voltage levels ($0, \pm 0.5V_{dc}, \pm V_{dc}$, and $\pm 1.5V_{dc}$). These voltage levels are created by connecting the DC power supply with capacitors in series and in parallel. Consequently, the proposed inverter boosts the DC power supply input by 1.5 times.

In addition to the boost advantage of the proposed inverter, it also mitigates the voltage stress of the power switches because it does not require a conventional H-bridge inverter to change the output voltage polarity.

The voltage and current stress of each power switch during the generation of each voltage level are given in Tables 6 and 7. Since the four switches (S_1, S_2), (S_5, S_6) are operettas in complementary, hence the voltage stress of these pair switches are V_{dc} and their current stress is equal to load current I_L. Similarly, the voltage stress of two switches (S_4, S_8) are equal to V_{dc} and load current is passing from these switches. The voltage stress that two switches (S_3, S_7) endure is equal to half of the input dc-link voltage $0.5V_{dc}$ and the current stress for these switches is the sum of DC current and load current. Therefore, based on Tables 6 and 7, the voltage rating and current rating of (S_1, S_2, S_4, S_5, S_6, S_8) are V_{dc} and I_L, respectively. The voltage and current ratings switches (S_3, S_7) are $0.5V_{dc}$ and ($I_L + I_{dc}$), respectively. The Total Stress Voltage (TSV) of the proposed inverter is obtained from the sum of the maximum voltage stresses on all semiconductor switches. Consequently, the proposed inverter TSV value is $7V_{dc}$, which is low and leads to selecting IGBTs with a low-rating voltage. Hence, in this shape, all semiconductor switches consist of an IGBT along with one anti-parallel diode, except for one pair of IGBTs (S_3, S_7) that do not require anti-parallel diodes.

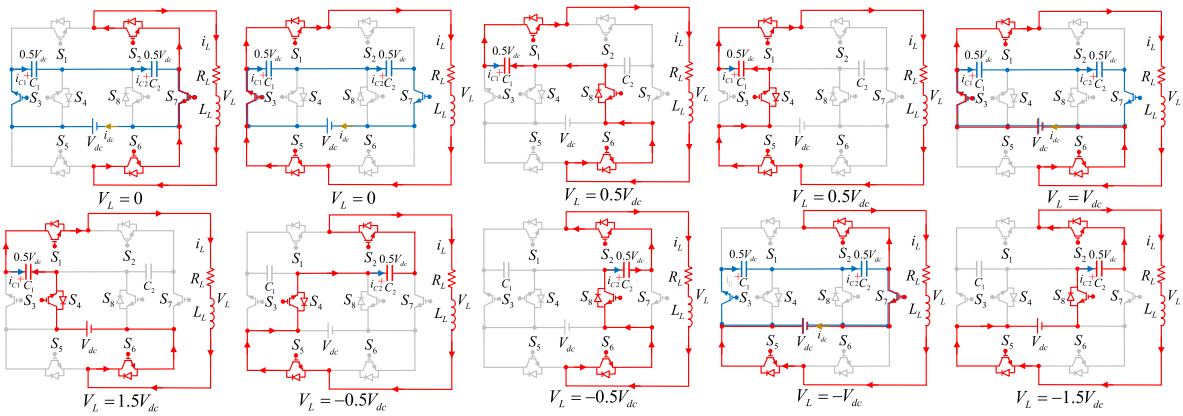


FIGURE 6. All operation modes of the proposed seven-level switched-capacitor topology.

B. OPERATION MODES

All possible switching states, capacitor charge conditions, and output voltages of the proposed sub-module switched-capacitor inverter are shown in Table 5. In this table, "↑" is for charging, and "↓" is for discharging capacitors, and "−" is the neutral mode. As can be seen in Table 1, there is some redundancy in creating voltage levels of $\pm 0.5V_{dc}$ and the zero level. All operation modes used to create the seven voltage levels in the proposed multilevel inverter, as shown in Fig. 6, are explained in detail as follows:

- *First mode:* the first mode has zero levels. For this mode, there are two states. The first state produces zero levels in the output by switching the three switches of (S_2, S_6, S_7). In addition, the power switch S_3 is also turned on so that the capacitors are charged in parallel with the input DC supply. The other state that creates zero levels can be produced by switching the switches (S_1, S_3, S_5) along with S_7 to charge the capacitors.
- *Second mode:* the second mode is $+0.5V_{dc}$. As with the zero-level mode, there are two different states that produce this mode. The first and second states produce $0.5V_{dc}$ by switching three switches, either (S_1, S_6, S_8) or (S_1, S_4, S_5). In this mode, the voltage of the capacitor C_1 is discharged through the load current, and the voltage level of $+0.5V_{dc}$ can be generated.
- *Third mode:* The third mode is $+V_{dc}$. By turning on three power switches (S_1, S_3, S_6), the magnitude of the input DC supply can be generated at the output. Switch S_7 is also turned on to keep the capacitor voltages charged.
- *Fourth mode:* This mode provides the maximum positive level, $1.5V_{dc}$, which is obtained from the sum of the voltage of C_1 and the input DC supply. This voltage level is produced by the switching of three switches (S_1, S_4, S_6).
- *Fifth mode:* In this mode, the output voltage is equal to the capacitor voltage of C_2, that is $-0.5V_{dc}$. As in the second mode, there are two available states that produce this mode. It is created by turning on three switches, either (S_2, S_4, S_5) or (S_2, S_6, S_8).
- *Sixth mode:* In this mode, the output voltage is equal to the negative value of the input DC power supply $-V_{dc}$; it is generated by three switches (S_2, S_5, S_7). In addition, switch S_3 is turned on to charge the capacitors.
- *Seventh mode:* This mode provides the second negative level, $-1.5V_{dc}$, which is obtained from the sum of the capacitor voltage C_2 and the input DC supply. This output voltage level is achieved by the switching of three switches (S_2, S_5, S_8).

C. APPLYING FCS-MPC FOR THE PROPOSED SC-MLI BASED ON PROPOSED GENERALIZED GUIDELINE

The proposed generalized FCS-MPC guideline is implemented for the control of the proposed seven-level SC-MLI. In the two previous subsections (A and B), all operation modes of the proposed topology are described, and all valid switching states based on the output voltage of the proposed inverter and capacitor voltage and currents are described in detail. Therefore, the first step of the proposed guideline, which is electrical system identification, has been completed.

The second step of the proposed guideline is predictive control. This step is about extracting the model of the proposed inverter and load model. Therefore, in the first place, the model of the proposed inverter is derived based on switching states from Table 5. As detailed in Table 5, the proposed topology has ten different switching states. Based on the proposed seven-level inverter in Fig. 5, the output voltage of the inverter V_L can be represented in terms of input DC voltage V_{dc} and the switching function as follows:

$$V_L(t) = (F_{S_1} - F_{S_5})V_{dc} + (F_{S_4} - F_{S_8})0.5V_{dc} \qquad (23)$$

Here, $F_{S_1}, \cdots F_{S_8}$, are the switching function of $S_1, \ldots, S_8$ which have two states ON or OFF.

Then the load model that is a resistive-inductive load is derived. As we wrote the load model and capacitor model for two classical SC-MLI in Section II, the model of the load is obtained from (2)–(5), and the model of the capacitors can be

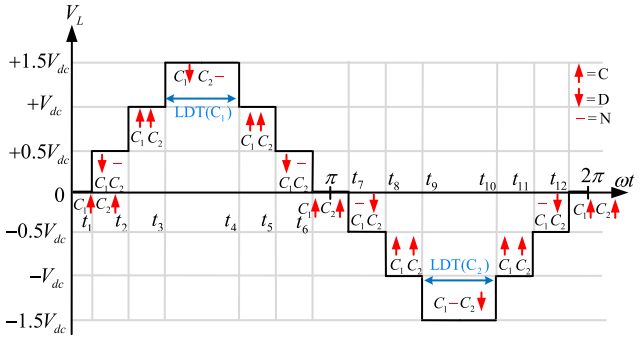


FIGURE 7. Longest discharging time for the capacitors of the proposed seven-level switched-capacitor multilevel inverter.

obtained from (6)–(11). In the proposed topology, the capacitors' currents vary according to the applied switching states and the output current direction of the inverter. According to Table 5, the predicted capacitor current is related to the measured output current of the inverter (i_L) and the DC source current (i_{dc}) as follows:

$$i_{C1}(k+1) = K_{1C_1} i_{dc}(k) + K_{2C_1}(F_{S_2} - F_{S_1}) i_L(k) \tag{24}$$

$$i_{C2}(k+1) = F_{S_7} i_{dc}(k) + K_{1C_2}(F_{S_2} - F_{S_1}) i_L(k) \tag{25}$$

where K_{1C_1}, K_{2C_1}, and K_{1C_2} are:

$$K_{1C_1} = F_{S_3} \wedge F_{S_7} \vee F_{S_8} \tag{26}$$

$$K_{2C_1} = \overline{(F_{S_3} \wedge F_{S_5})} \wedge F_{S_1} \vee F_{S_2} \wedge F_{S_3} \wedge F_{S_5} \tag{27}$$

$$K_{1C_2} = \overline{(F_{S_6} \wedge F_{S_7})} \wedge F_{S_2} \vee F_{S_1} \wedge F_{S_7} \wedge F_{S_6} \tag{28}$$

Here, "$\wedge$" is the AND sing, "$\vee$" is the OR sign, and "$\neg$" is the NOT sign as used in Boolean logic.

The last step of the proposed guideline is to define the cost function. Load current control and capacitor voltage control are two control objectives that are included in the cost function. Therefore, the predicted and reference load currents and capacitor voltages of the inverter are included in the cost function as follows:

$$\begin{aligned} G(k) = {} & (i_L^*(k) - i_L(k+2))^2 \\ & + \lambda[(V_{C_1}^*(k) - V_{C_1}(k+2))^2 \\ & + (V_{C_2}^*(k) - V_{C_2}(k+2))^2] \end{aligned} \tag{29}$$

The weighting factor of λ and the reference values of the capacitor voltages are computed by (15) and (16), respectively.

D. CAPACITOR RIPPLE ANALYSIS

In the proposed topology, both used capacitors are charged to generate voltage levels ($\pm 0.5, \pm 1.5V_{dc}$). Therefore, the voltages of these two capacitors shouldn't drop to less than an allowable value. Hence, to calculate the capacitance of the capacitors, it is necessary to measure their stored energy (that pumps to the output). Fig. 7 shows the capacitor charging and discharging in all operating modes. As can be seen from this figure, the longest discharging time (LDT) for both capacitors is the same, which happens for the maximum output levels ($\pm 1.5V_{dc}$) in time intervals ($t_4 - t_3$) and ($t_{10} - t_9$).

Therefore, the amount of charge discharged during LDTs for (C_1, C_2) are obtained as follows [20], [21], [22]:

$$\triangle Q_{C1} = \int_{t_3}^{t_4} I_L.sin(\omega t).d(t) \tag{30}$$

$$\triangle Q_{C2} = \int_{t_9}^{t_{10}} I_L.sin(\omega t).d(t) \tag{31}$$

where I_L is the magnitude of the load current, and $\omega = 2\pi f_o$. Since the switching frequency of MPC is variable, the time intervals t_3, t_4 and t_9, t_{10} are variable but similar average frequency calculations for MPC, these time intervals can be obtained by calculating their average values ($\overline{t_i}$) from the following equation:

$$\overline{t_i} = \frac{t_{i_1} + t_{i_2} + \cdots + t_{i_k}}{k} \quad \text{for} \quad i = 3, 4, 9, 10 \tag{32}$$

Here, k is the number of cycles. It is obvious that the highest discharging value and, thus, the greatest voltage ripple of capacitors occur in a purely resistance load. However, because MPC works with a resistance inductive load, we assume the inductance value of the load is so small that it is ignored. Hence, $\triangle Q_{C_1,C_2}$ are computed as follows:

$$\triangle Q_{C1} = \frac{1.5V_{dc}}{\omega R_L}(\overline{t_4} - \overline{t_3}) \tag{33}$$

$$\triangle Q_{C2} = \frac{1.5V_{dc}}{\omega R_L}(\overline{t_{10}} - \overline{t_9}) \tag{34}$$

Hence, the ripple voltage of capacitors ($\triangle V_{ripple,C_1}$, $\triangle V_{ripple,C_2}$) are obtained as:

$$\triangle V_{ripple,C_1} = \frac{1.5V_{dc}}{\omega R_L C_1}(\overline{t_4} - \overline{t_3}) \tag{35}$$

$$\triangle V_{ripple,C_2} = \frac{1.5V_{dc}}{\omega R_L C_2}(\overline{t_{10}} - \overline{t_9}) \tag{36}$$

V. COMPARISON OUTCOMES

To demonstrate the performance of the proposed seven-level SC-MLI, a study is performed on the proposed topology and state-of-art switched-capacitor MLI topologies [16], [17], [18], [19], [20], [21], [22], [23], [24], [25], [26], [27], [35], [36], [37]. The parameters used to compare the proposed topology with the other existing SC-MLIs are given in Table 8. The parameters of the comparative study are the number of components, on-state IGBTs, the per-unit value of TSV, boosting gain, generalized configuration, leakage current, charge balancing, control or modulation technique, and efficiency. In addition, the proposed topologies' costs are compared by defining a cost function (CF). The greatest costs of multilevel inverters are related to the number of components and the TSV

TABLE 8. The Number of Required Components for the Proposed Seven-Level Topology and the Previously Described Five-Level and Seven-Level SC-MLI Topologies

Topologies	N_{Level}	N_{IGBT}	N_{Driver}	N_{Diode}	N_{DC}	N_{Cap}	N_{Ind}	N_{On}	$TSV_{p.u}$	CF/N_{Level} α=0.5	CF/N_{Level} α=1.5	Gain	Generalized	Leakage Current	Charge Balancing	Control	Efficiency
2018 [16]	5	6	6	8	1	2	1	3	8	5.2	6.8	2	No	Not Zero	Inherent	NLC(OL)	94.3%@320W
2018 [17]	5	7	7	10	1	4	1	7	10	6.2	8.2	2	No	Not Zero	Inherent	PWM(OL)	NA%@500W
2019 [18]	7	10	8	10	1	4	1	6	8	5.14	6.3	1.5	No	Not Zero	Inherent	PWM(OL)	96.5%@270W
2019 [19]	7	10	8	10	1	4	1	5	11	5.36	6.9	1.5	No	Not Zero	Inherent	PWM(OL)	98.2%@150W
2019 [20]	7	9	8	9	1	3	1	5	8	7.71	5.9	1.5	No	Not Zero	Inherent	PWM(OL)	95.8%@300W
2019 [21]	7	8	8	8	1	3	1	4	4	4.14	4.7	1	No	Not Zero	Inherent	PWM(OL)	97.3%@800W
2019 [22]	7	8	8	10	1	2	1	4	16	5.14	7.4	3	No	Not Zero	Inherent	NLC(OL)	95%@360W
2021 [23]	7	10	8	10	1	2	1	6	8	4.71	5.6	1.5	No	Not Zero	Inherent	PWM(OL)	93%@500W
2020 [24]	7	10	9	10	1	3	1	8	8.5	5.18	6.4	1.5	No	Not Zero	Inherent	PWM(OL)	98.5%@200W
2020 [25]	7	10	8	10	1	3	1	4	8	5	6.1	1.5	No	Not Zero	Inherent	PWM(OL)	NA%@150W
2020 [26]	7	10	10	14	1	2	1	4	12	6	7.7	3	No	Not Zero	Inherent	PWM(OL)	95.8%@600W
2021 [27]	7	10	8	10	1	2	1	4	8	4.86	6	1.5	Yes	Not Zero	Inherent	PWM(OL)	95.5%@200W
2021 [35]	7	10	6	10	1	4	1	3	6	3.8	4.7	3	No	Zero	Inherent	PWM(OL)	98%@800W
2019 [36]	5	10	10	10	1	4	1	5	5	7.3	8.3	0.5	Yes	Not Zero	Needed	PWM (CL)	NA%@50W
2020 [37]	5	9	9	9	1	3	1	4	6	6.6	7.8	2	Yes	Zero	Inherent	PWM (OL)	96.7%@1000W
2021 [38]	5	8	8	8	1	3	2	4	5.28	6.14	5.5	2	Yes	Zero	Inherent	PWM(CL)	98.3%@600W
	7	11	11	11	2	4	2	5	5.28	6.14	6	3	Yes	Zero	Inherent	PWM(CL)	98.2%@600W
Proposed	**7**	**8**	**8**	**6**	**1**	**2**	**1**	**4**	**7**	**3.92**	**4.92**	**1.5**	Yes	Not Zero	Inherent	MPC(CL)	94.6%@1000W

NLC: Nearest Level Control; PWM: Pulse Width Modulation; MPC: Model Predictive; OL: Open-Loop; CL: Close-Loop Control.

value; the CF can thus be defined as follows:

$$CF = N_{DC} \times (N_{Cap} + N_{IGBT} + N_{Driver} + N_{Diode} + \alpha TSV_{p.u}) \tag{37}$$

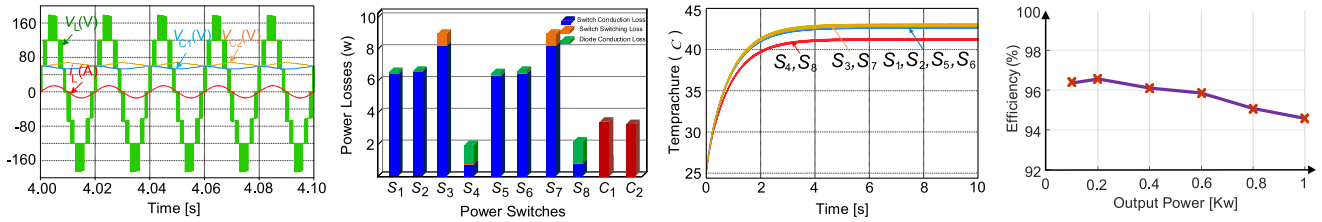
where α is the TSV weighting factor. According to Table 6, [16] and [17] produce five levels with six and seven switches, respectively, so they have a high-cost factor. The high number of IGBTs required to produce seven levels is attributed to [18] and [19], as well as the presented MLIs [23], [24], [25], [26], [27]. Meanwhile, the lowest number of required IGBTs is for the proposed topology and [21], [22] to generate seven-level. Also, [37] uses eight switches to generate five levels. As a result, the proposed topology requires fewer switches than the other MLIs. In addition, the proposed SC-MLI produces less voltage stress than the other SC-MLIs, except for [21], which has a low TSV. Furthermore, the proposed SC-MLI requires fewer diodes than other SC-MLIs. This reduction is due to the use of two IGBTs without the need for anti-parallel diodes in the proposed topology. The number of capacitors for the proposed topology is also less than most of the presented SC-MLIs. Although [22] uses the same number of switches and capacitors as the proposed topology, the voltage stress of the switches is very high, which results in the cost factor of the inverter. Also, it cannot be extended as a generalized topology to reach a high number of levels. The presented topologies [35], [36], [37] are grid-connected inverters that have been presented for photovoltaic systems. We also compared the proposed topology with these topologies. As you can see, the proposed topology still generates seven levels and requires a low number of switches and capacitors. It also doesn't need any extra inductance in its circuit. As can be observed in Table 8, almost all topologies use low frequency PWM (NLC) or high frequency PWM techniques, which are open-loop (OL), except for grid-connected inverters [35], [36], [37] that are close-loop (CL), in contrast to the proposed topology that uses MPC, which naturally is a simple close-loop control without using any PI controller of modulation signal. As depicted in Table 8, the proposed seven-level SC-MLI requires fewer semiconductors and capacitors than other similar SC-MLIs to generate a seven levels with the lowest TSV and low CF; this makes it more efficient, affordable, and practical.

TABLE 9. Used Parameters for Junction Temperature Evaluation of IGBT and Its Parallel Diode (IGBT IKFW60N60DH3E)

i	1	2	3	4	5	6
			IGBT			
R_i[K/W]	$3e^{-3}$	0.104852	0.13662	0.1914	0.26906	0.3091
τ_i[s]	$1.6e^{-5}$	$2.6e^{-4}$	$2.2e^{-3}$	0.018514	0.201746	0.902516
C_i[J/K]	$5.3e^{-3}$	$2.5e^{-3}$	0.0161	0.0967	0.07498	2.9198
			Diode			
R_i[K/W]	0.341	0.56903	0.28633	0.34265	0.36597	0.023397
τ_i[s]	$2.6e^{-4}$	$1.6e^{-3}$	0.013093	0.158585	0.778817	15.94388
C_i[J/K]	$7.33e^{-4}$	$28.11e^{-4}$	0.0457	0.4628	2.128	681.445

VI. THERMAL LOSSES AND EFFICIENCY

To calculate the power losses, the suggested seven-level structure is thermally modeled in PLECS software. For this investigation, the IGBT IKFW60N60DH3E is used. The value of (Ron) is chosen based on the switch and diode datasheet, which is used for power loss analysis of the proposed topology. The current-voltage curve of the switch is defined in the software. In addition, the junction temperature evaluation of all power switches is also being investigated. The junction temperature of all the IGBTs is evaluated using their characteristics and the thermal models mentioned in Table 9. The inverter's input is connected through a DC link with a value of 120[V]. The inverter's output is linked to a 10[Ω] and 5[mH] resistance inductive load to deliver power 1[kW]. The



(a) (b) (c) (d)

FIGURE 8. (a) load voltage and current and capacitor voltages; (b) power loss of all switches in the proposed inverter; (c) switch temperature; (d) efficiency.

suggested FCS-MPC is used to control the proposed topology. The starting temperature is 25[°C] for this study.

Fig. 8(a) shows the output waveform of the proposed topology and capacitor voltages. This figure confirms that seven voltage levels with a peak of 180[V] are generated by the proposed topology and that the capacitors are charged at 60[V]. The power losses of each IGBT and its parallel diodes are shown in Fig. 8(b). In addition, the capacitor voltage ripple losses are displayed in Fig. 8(b). Because the switches S_3 and S_7 are used to charge the capacitors, they have a larger power loss than the other devices, as illustrated in Fig. 8(b). Fig. 8(c) shows the junction temperature of each switch, and as can be observed, two switches, S_3 and S_7, have greater temperatures than the others due to larger power losses. The proposed inverter has a total loss of 54[W] at an output power of 1[kW], with an efficiency of 94.6%, as shown in Fig. 8(d).

In this investigation, the capacitor ripple loss ($P_{Ripple,C}$), it is also known as the capacitor loss, and is calculated as follows:

$$P_{Ripple,C} = \frac{f_o}{2} \times C \times \triangle V_C^2 \tag{38}$$

Here f_o indicates the output frequency.

VII. EXPERIMENTAL VALIDATION AND DISCUSSION

The experimental results for the proposed seven-level inverter are presented to validate the theoretical study. The prototype of the proposed topology is built using eight IGBTs as switches and two electrolyte capacitors. The input of the proposed topology is a dc-link voltage that is supplied by a laboratory dc power supply (which is set to 120[V]), and the output of the topology interface consists of a resistance-inductive load (R = 50[Ω], L = 10[mH]).

The proposed model predictive control algorithm is programmed on a Digital Signal Processing (DSP), and a Field-Programmable Gate Array (FPGA) is used to apply dead time 2[μs] to prevent short-circuiting. The gating signals are transferred to the IGBTs through an optic wire. The load voltage, load current, and the capacitor's voltages are measured by a separate sensor board. Table 10 provides a list of the components used in the experiment.

Table 11 illustrates the switching frequency of each switch in proposed inverter for sample time 100[μs]. The frequency of each switch in the proposed topology is different due to the nature of MPC, which has a variable frequency.

TABLE 10. Experimental Parameters

Symbol	Parameters	Values
V_{dc}	DC-link voltage	120[V]
$S_1 - S_8$	IGBT	600[V], 40[A]
C_1, C_2	Capacitors	2200[μF]
f_L	Load frequency	50[Hz]
R-L	Load	50[Ω], 10[mH]
T_D	Dead time	2[μs]
T_s	Sample time	100[μs]

TABLE 11. Switching Frequency of Power Switches in the Proposed Seven-Level SC-MLI for T=100[μs]

Switches	S_1	S_2	S_3	S_4	S_5	S_6	S_7	S_8
$f_{switching}$ [Hz]	250	250	2200	600	260	260	2200	600

A. STEADY-STATE PERFORMANCE

In order for the inverter to control the load current in the proposed FCS-MPC strategy, a sinusoidal waveform with a peak value i_L^* of 3[A] is chosen as the reference load current. Fig. 9 illustrates the steady-state experimental results of the proposed seven-level inverter. Fig. 9(a) shows the load voltage, load current, and capacitor voltages. Fig. 9(b) shows a zoomed view of Fig. 9(a) for 0.05[s]; as can be seen, the proposed inverter generates seven voltage levels with a peak of 180[V] and voltages of 0, ± 60[V], ±120[V], and ±180. In addition, the weighting factor proposed in (14) efficiently balances the capacitors at half the value of the dc-link voltage V_{dc}/2=60[V]. Fig. 9(c) displays the capacitor voltages, load, and reference current waveform. The load current tracks the reference load current with high accuracy and balances the capacitor voltages at half of the dc-link voltage with a low voltage ripple range of 1[V], which is the advantage of the proposed FCS-MPC.

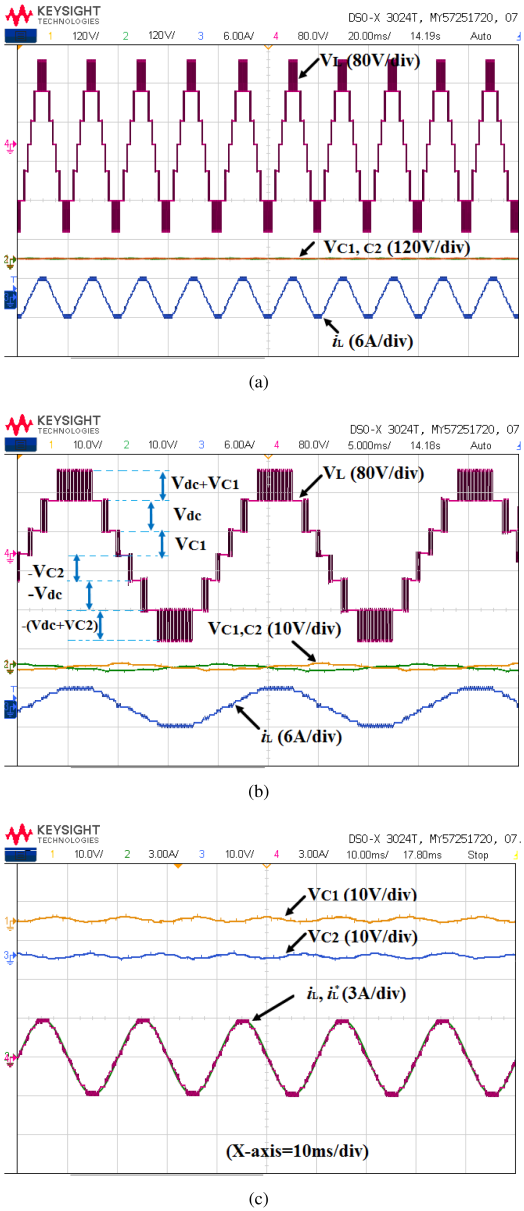


FIGURE 9. Experimental results of the steady state of the load waveform and capacitor voltages for the reference load current of i_{ref}=3[A]: (a) seven levels load voltage V_L and load current and capacitor voltages V_{C1}, V_{C2} for 0.2[s]; (b) a zoomed view of (a) for 0.05[s]; (c) capacitor voltage waveform, load current i_L and reference current i_{ref} for 0.1[s].

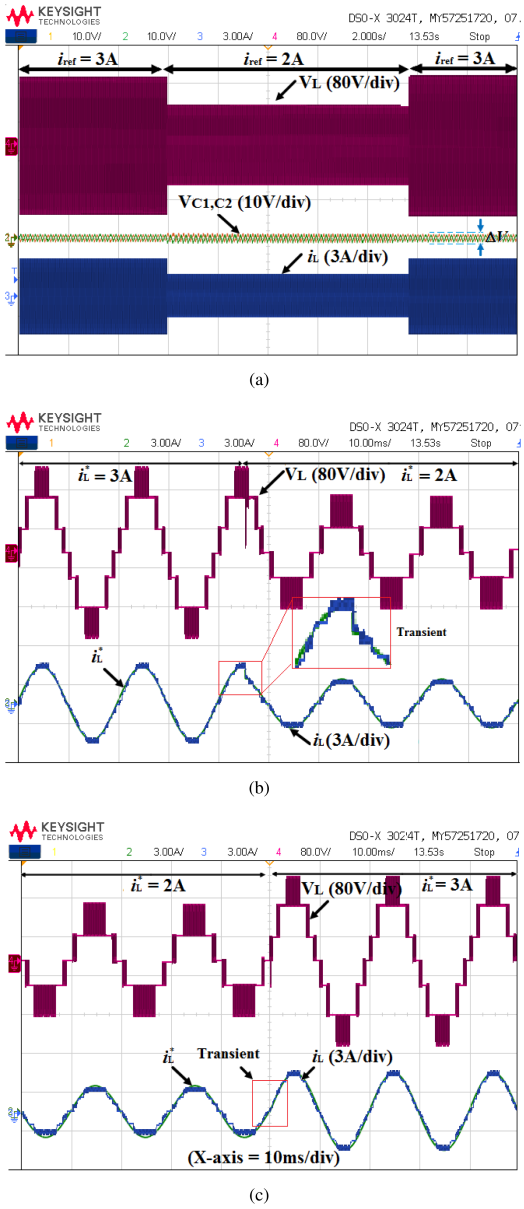


FIGURE 10. Dynamic response of step change load reference current: (a) load waveform and capacitor voltages for 20[s]; (b) zoomed (a) for 0.1[s] when reference current is reduced from 3[A] to 2[A]; (c) zoomed (a) for 0.1[s] when reference current is increased from 2[A] to 3[A].

B. TRANSIENT AND DYNAMIC PERFORMANCE

The transient and dynamic response of the proposed topology is tested with load reference current changes, which is a typical test for the evaluation of multilevel inverters. The system is evaluated by making changes in the amplitude, phase angle, and frequency parameters of the reference load current. Fig. 10 displays the load voltage, load current, and reference load current along with capacitor voltages used for adjusting the amplitude of the load reference current.

The first test is for the load current amplitude changes. As shown in Fig. 10(a), the test starts with i_L^*=3[A], and this value is then decreased to 2[A] before returning to 3[A]. Close-up views of the step changes are displayed in Fig. 10(b) and (c). Fig. 10(b) shows the inverter's response to the step change in the current from 3[A] to 2[A] (66% decrease). This figure shows that by decreasing the amplitude of the reference current signal, the number of voltage levels of the proposed topology is decreased from seven to five, which means the peak of the load voltage is reduced from 180[V] to 120[V]. The proposed control strategy implemented in the proposed topology demonstrates a good dynamic response to this sudden change, as the load current tracks the reference signal such that it does not cause a spike in the load current and causes only a small shape change in the load voltage and current waveform.

Fig. 10(c) exhibits the inverter's response to the increase in the reference current from 2[A] to 3[A]. This figure shows that by raising the amplitude of the reference current signal, the number of voltage levels increases from five to seven, raising the peak voltage from 120[V] to 180[V]. The figure also shows that the proposed MPC has a good dynamic response to this amplitude increase as the transient time required to track the reference current signal is minimal. Additionally, it shows that the load current tracks the reference current signal quickly with a short transition time that does not cause a spike in the load current.

The test of the proposed topology with the proposed FCS-MPC then continues for the amplitude changes, phase shift, and frequency step change. Fig. 11 shows the experimental results of load current and load reference for these step changes. Fig. 11(a) shows the experimental results of load current and load reference current for the amplitude step increasing from 0 to 3[A]. As shown in this figure, the load current tracks the reference current signal properly without any change in the shape or amplitude of the load current.

Fig. 11(b) documents the dynamic and transient response of the proposed topology for a phase shift in the load reference current from 0 to 180°. In this case, the load current can track the reference load current, and no spike is observed during the transient process. It reveals that the proposed topology has a good dynamic performance with the proposed FCS-MPC technique.

The experimental results of the load reference signal and load current for a step frequency change from 50[Hz] to 100[Hz] are shown in Fig. 11(c). For this test, like in previous tests, the proposed FCS-MPC control strategy implemented on the proposed topology has good dynamic and transient responses due to good tracking of the load reference current with no spike or change observed in the load current.

C. COMPARISON FCS-MPC AND CLASSICAL PWM TECHNIQUES FOR SC-MLIS

In this subsection, the FCS-MPC is compared with the classical PWM methods for the control of SC-MLIs in order to show the advantage of FCS-MPC for this family of inverters. As we showed in Section II and this section, FCS-MPC has the ability to control multiple objectives, such as current control, balancing the voltage of the capacitors, and switching frequency control, by including them in the cost function. In addition, it reduces the capacitor's voltage ripples and THD magnitudes. In contrast, a classical PWM control technique for SC-MLIs uses two or more PI controllers for current control and balancing the voltage of the capacitors, which makes the control hard and complex [38], [39]. In addition, industrial applications need several operational amplifiers (OpAmp) to tune the control objectives, which increases the final cost of massive production.

In conclusion, by advancing the speed of the microprocessor model, predictive control can be applied in the future to industrial productions to overcome the computational burden, which is the main disadvantage of MPC.

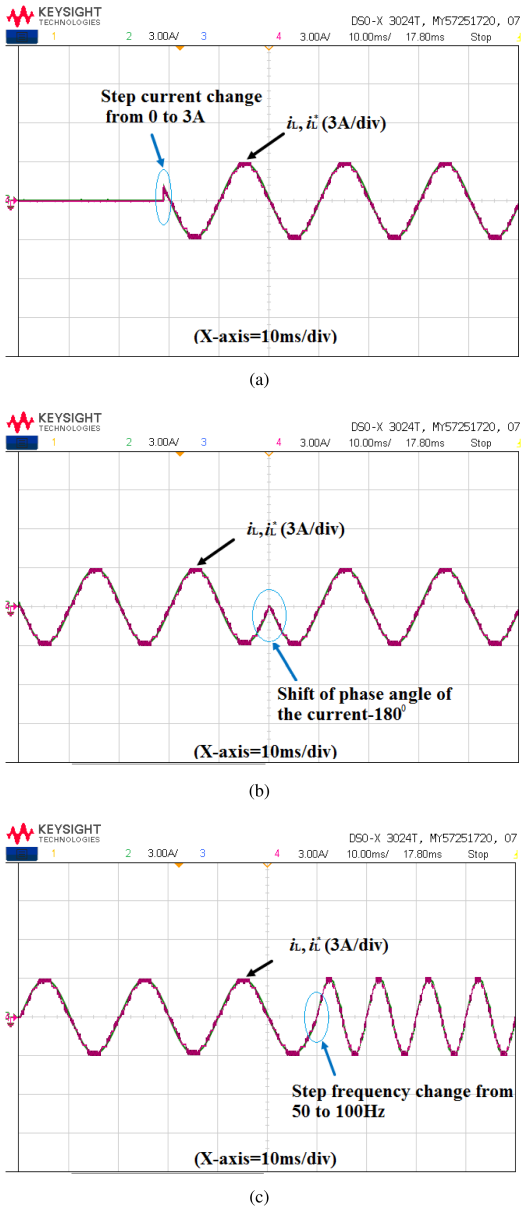


FIGURE 11. Transient and dynamic responses of the load current control: (a) for a step increase in the reference current from 0 to 3[A]; (b) for a phase shift of the load reference current from 0 to 180°; (c) for a step increase in the frequency of the load reference current from 50[Hz] to 100[Hz].

VIII. CONCLUSION

Single-phase multilevel inverters are attractive topologies for improving quality in low power applications, such as photovoltaic systems. However, control and modulation with classical strategies are not easy to implement. On the other hand, finite set model predictive control has been positioned as a good alternative for complex topologies, in which the direct control and application of the states of the converter help to correctly and easily manage different kinds of converters. In this article, a generalized guideline for the implementation of the FCS-MPC strategy to control single-phase SC-MLIs was presented. Through simulation results, the FCS-MPC was

tested and evaluated for two classical SC-MLI topologies. Then, to facilitate the application of FCS-MPC in all types of SC-MLIs, the generalized FCS-MPC guideline was presented. Furthermore, a seven-level SC-MLI topology was presented; it has several advantages over previously reported SC-MLIs, such as lowering the TSV and reducing the number of power semiconductors and capacitors. FCS-MPC was easily implemented in this novel topology by following the proposed guidelines. The experimental results show that the proposed FCS-MPC technique can provide a high-quality output waveform while maintaining a balanced capacitor voltage with a low voltage ripple.

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