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A New Soft-Switched High Step-Up Trans-Inverse DC/DC Converter Based on Built-In Transformer

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ABSTRACT This article proposes a new Zero-Voltage Switching (ZVS) high step-up DC/DC converter based on a built-in transformer for renewable energy applications. The proposed topology utilizes a Three-Winding Built-In Transformer (TWBT) to increase the voltage gain, but unlike most coupled-inductor-based DC-DC converters, high output voltages can be obtained under a lower magnetic turns ratio. In this circuit, with the help of a regenerative active clamp circuit, the energy of the leakage inductor from the TWBT is absorbed and transferred to the output, therefore, the ZVS conditions at turn-on time are achieved for switches. The voltage stresses across the switches of the proposed topology are limited, and the diodes reverse-recovery issue are eliminated. Due to the low input current ripple, the suggested topology can be used for renewable energy sources. Furthermore, because of the low number of components along with the soft-switching operation, the proposed circuit can offer enough high efficiency. The operational principle, steady-state analysis, and characteristics of the proposed converter are provided. Finally, a 200 W prototype with 25 V input and 400 V output voltage is built to validate the analytical results.

INDEX TERMS Coupled-inductor, high step-UP DC-DC converter, soft-swithing performance, trans-inverse.

LIST OF SYMBOLS AND ABBREVIATIONS

D	Duty cycle of the switches.
f_s	Switching frequency.
LRR	Low Reverse Recovery.
CI	Coupled-Inductor.
ZVS	Zero Voltage Switching.
ZCS	Zero Current Switching.
VM	Voltage Multiplier.
SI	Switched Inductor.
SC	Switched Capacitor.
RES	Renewable Energy Sources.
CCM	Continuous Conduction Mode.
TWBT	Three-Winding Built-In Transformer.
AVG	Averaged Value.
n_{21}	N_2/N_1.
n_{31}	N_3/N_1.

I. INTRODUCTION

In recent years, for Renewable Energy Sources (RES) applications, there has been special attention to increasing efficiency and obtaining higher power density of high-voltage gain DC-DC converters [1]. These converters act as an interfacing circuit to boost the low input DC voltage(typically 20-40 V) to the demanded regulated high output DC voltage (380-400 V_{DC}) for providing acceptable ac utility voltage. High voltage gain DC-DC converters are also required for various applications like robotics, UPS, automobile HID lamps, data center, satellite, appliances, medical devices, motor drive, and server power supplies [1], [2].

High-voltage gain ratio and continuous input current are the primary critical requirements for RES applications [1], [3]. For low-power applications, the non-isolated type of high step-up converters with the common ground between input

and output with a low number of components and low cost are more desirable [4], [5].

In conventional current-fed step-up converters, such as boost and flyback, because of low conversion ratio, high switch voltage stress, and serious reverse recovery problems, improving the key indicators of such converters are necessary. So that, high voltage gains are obtained at acceptable efficiency without requiring ultra-high duty cycles. So far, many transformer-less DC-DC converters with the help of boosting techniques like voltage multipliers, switched capacitors, switched inductors, and cascading connections have been proposed to enhance the voltage gain [1]. However, the ultra-high voltage gains of these modified structures are often achieved by using more power stages and more components, with increased cost, complexity, and conduction losses [6].

To further improve the key indicators of the high step-up DC-DC converters such as voltage gain ratio, components count, and efficiency, many topologies based on the transformer (isolated or built-in) and Couple-Inductor (CI) have been developed [7], [8]. In these circuits, the magnetic devices along with other voltage-boosting methods are employed under different configurations of step-up topologies [9]. Here, the turns ratio of the transformer or CI helps to further increase the voltage gain ratio with fewer components. However, a considerable voltage spike on the main power switches under high turns ratio caused by the leakage inductance of the magnetic device is a serious issue with the use of CI or transformer, which can be limited using clamp circuits (active or passive) [5], [10]. Also, in high-voltage gain DC-DC converters, hard-switching performance and diode reverse recovery often have a negative effect on the conversion efficiency. To solve this problem, the operation of the circuit under soft-switching using Zero Voltage Switching (ZVS) or Zero Current Switching (ZCS) is highly recommended to improve the converter performance and power density [8], [11].

In the last two decades, many non-isolated high step-up DC-DC structures using CI (two or three winding) combined with other boosting methods (VM, SC, or SI) with proper performance have been presented. In [11], [12], [13], two-winding CI along with VMs are utilized to raise the voltage gain ratio. Despite an ultra-high voltage conversion ratio along with soft-switching performance, these converters suffer from a high input current ripple, which is accounted as the main disadvantage of the proposed converter. To solve the aforementioned problems, new types of high-voltage gain converters with continuous input current have been introduced [14], [15], [16], [17]. In these converters, the single power switch operates under turn-ON ZCS transition with low voltage stress. Besides, the leakage inductor energy of the CI is absorbed with help of a regenerative passive clamp circuit. However, in these converters, a wide range of voltage conversion ratios cannot be provided. Also, a new type of ultra high-gain DC-DC converter with low input current ripple using a three-winding coupled-inductor is suggested in [18]. Nevertheless, using many semiconductor components is the main disadvantage of this converter.

In [19], [20], [21], high step-up DC-DC converters with active clamp circuits have been presented to provide ZVS performance for the power switch. The active clamp circuit not only absorbs the leakage energy of the magnetic devices but also passes the leakage current from the anti-parallel diode (body diode) of the main power switch before the gate signal comes. However, due to the series connection of the CI and input DC source, high input current ripple is created in these circuits, which is the main demerit of the converters. Furthermore, two new types of high-gain converter with ZVS condition and low input current ripple are proposed in [22] and [23]. However, this converter cannot provide high voltage gain ratios.

A new design of high voltage gain DC-DC converters has been proposed with high voltage gain in the form of trans-inverse characteristic versus turns ratio of the CI [24]. In this topology, unlike other conventional CI-based converters, the voltage gain is increased by reducing the magnetic turns ratio, which leads to more efficiency improvement. Although the converter draws a continuous current from the input DC source, hard-switching performance and considerable reverse recovery problems are the disadvantages of this circuit. In [25], [26], [27], some single-switch CI-based structures of trans-inverse or partial trans-inverse of DC-DC converters with low input current ripple and ZCS performance have been presented to provide high output voltage for RESs. In these converters, a regenerative passive clamp circuit helps to recycle the leakage inductor energy. In addition, the leakage inductor eliminates the diodes reverse recovery problem of the converter diodes. A new modified Y-source step-up DC-DC converter with ZVS characteristics is also proposed [28]. In this topology, higher voltage gains are achieved by decreasing of turns ratios of the secondary and the tertiary sides of the CI.

Another effective way to improve the efficiency of the high-step-up converters is utilizing a built-in transformer (BIT). Due to the zero average value of the currents passed through windings of the BIT, the magnetic flux is balanced which increases the core saturation capability. Consequently, comparing the CI-based topology, it is feasible to build the BIT with a lower volume core. Also, the RMS values of the currents that pass through the winding of a built-in transformer are reduced than the CI, which alleviates its conduction losses [11]. In [29] and [30], two new step-up DC-DC converters using BIT and low input current ripple are introduced. These topologies operate under ZVS conditions with LRR. Moreover, in [31] and [32] two new type of BIT-based DC-DC converter are presented. However, these converters suffer from low voltage gain ratio and complex design procedure.

Based on the above discussions, a new high step-up DC/DC converter using a Three-Winding built-in transformer with continuous input current is presented. The main benefits of this proposed structure are categorized as follows:

1) The capability to provide an ultra-High voltage gain under a lower turns ratio (Trans–Inverse property);
2) Utilizing a TWBT with zero average current value;
3) Low component count (10 components);

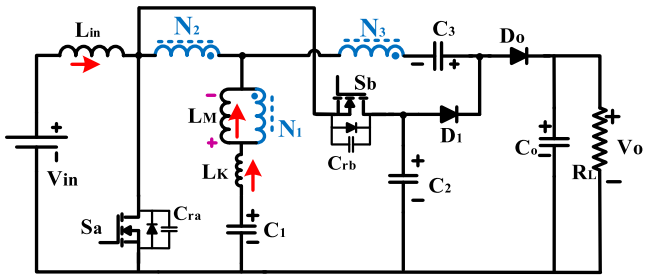

FIGURE 1. Equivalent circuit of the proposed converter.

4) Turn-ON ZVS performance for both switches;
5) Low input current ripple;
6) Low voltage stress of the switches;
7) Very Low Reverse Recovery (LRR) problem;

This article is organized as follows. The topology description and mathematical derivation of the suggested topology are provided and its soft-switching operation is analyzed in Sections II and III. In Section IV, the main key indicators of the introduced converter are compared with some counterparts. Converter design considerations are given in Section V. Then, experimental results from a laboratory prototype are shown in Section VI to verify the theoretical analysis. Finally, a brief conclusion are provided in Section VII.

II. THE PROPOSED CONVERTER STRUCTURE AND PERIODIC STEADY-STATE OPERATION

Schematic diagram of the proposed converter along with circuit variables is shown in Fig. 1. This converter is based on SEPIC and composed of a TWBT, an input inductor (L_{in}), two active switches including the main power switch (S_a), and an auxiliary switch (S_b), two diodes (D_1, and D_o), and four capacitors (C_1, C_2, C_3, and C_o). TWBT comprises an ideal transformer with turns of the primary, secondary, and tertiary windings N_1, N_2, and N_3, a magnetizing inductance L_m and a leakage inductance L_k, which is merged to the primary side of the built-in transformer. Combining the tertiary side of the built-in transformer along with C_3 and D_1 in the form of a VM increases the voltage gain ratio of the converter by setting the turns ratio. According to Fig. 1, the voltage stress across the power switch S_a is limited by a regenerative active clamp circuit, consisting of C_2 and S_b. In this state, the recovered energy of the leakage inductance L_k, which is stored in C_2, is transferred to the output with the help of a VM circuit. In this circuit, the leakage inductances of the TWBI help to eliminate the reverse recovery issue for the diodes D_1 and D_o. To simplify the circuit steady-state analysis, the following assumptions are considered during one switching period.

1) All switching components are regarded as ideal.
2) All capacitors are large enough. Thus, their voltage is constant without any ripple.
3) The TWBT is modeled as an ideal transformer with a magnetizing inductor (L_M) and a merged leakage inductor (L_k) referred to the primary side.

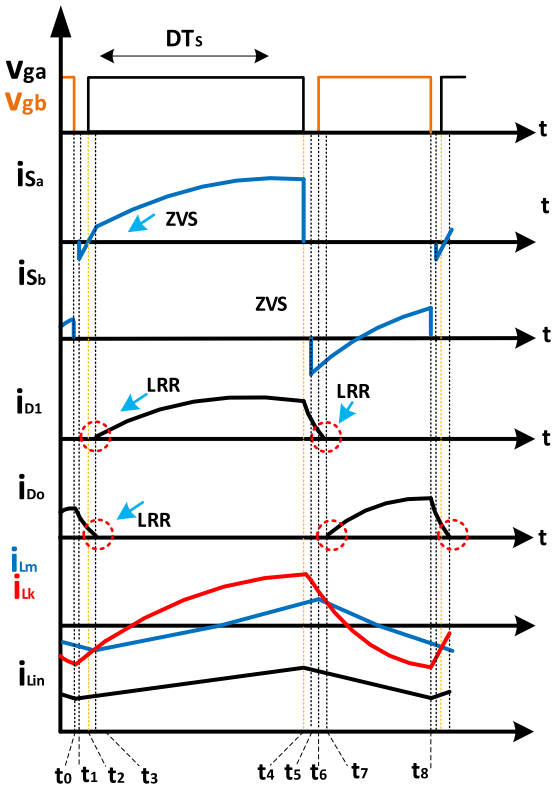

FIGURE 2. Typical key waveforms of the proposed converter under CCM operation.

Fig. 2 shows the theoretical key waveforms of the presented converter under CCM for one switching cycle, which are divided into six intervals. The equivalent circuits corresponding to each mode are depicted in Fig. 3. The detailed operation principle is presented as follows.

Mode 1 [$t_0 - t_1$]: From Fig. 2(a), before $t = t_0$, the current of the leakage inductance of the TWBT (i_{Lk}) is negative. At $t = t_0$, the switch S_b turns off; while S_a has not yet received the power-on command. In this state, the leakage inductance of the TWBT begins to resonate with the switch output capacitances C_{rSa} and C_{rSb}. Therefore, C_{rSb} is charged while C_{rSa} is discharged by the difference between i_{Lin} and i_{N2}.

Mode 2 [$t_1 - t_2$]: The difference current between the input inductor and the secondary side of the TWBT (i_{Lin} and i_{N2}) flows through the antiparallel diode (body diode) of switch S_a (Fig. 3(b)). To achieve the soft-switching ZVS, the power switch S_a should be turned on while its antiparallel diode conducts. In this condition, the turn-on loss of S_a is greatly reduced. In this mode, the input DC voltage is applied to the input inductor L_{in} and TWBT, thus i_{Lin} and i_{Lk} start to increase linearly.

Mode 3 [$t_2 - t_3$]: At the beginning of the third time interval, the power switch S_a starts to conduct under turn-ON ZVS condition. As it is shown in Fig. 3(c), the output diode D_o is conducting, while D_1 is reverse-biased in this time duration.

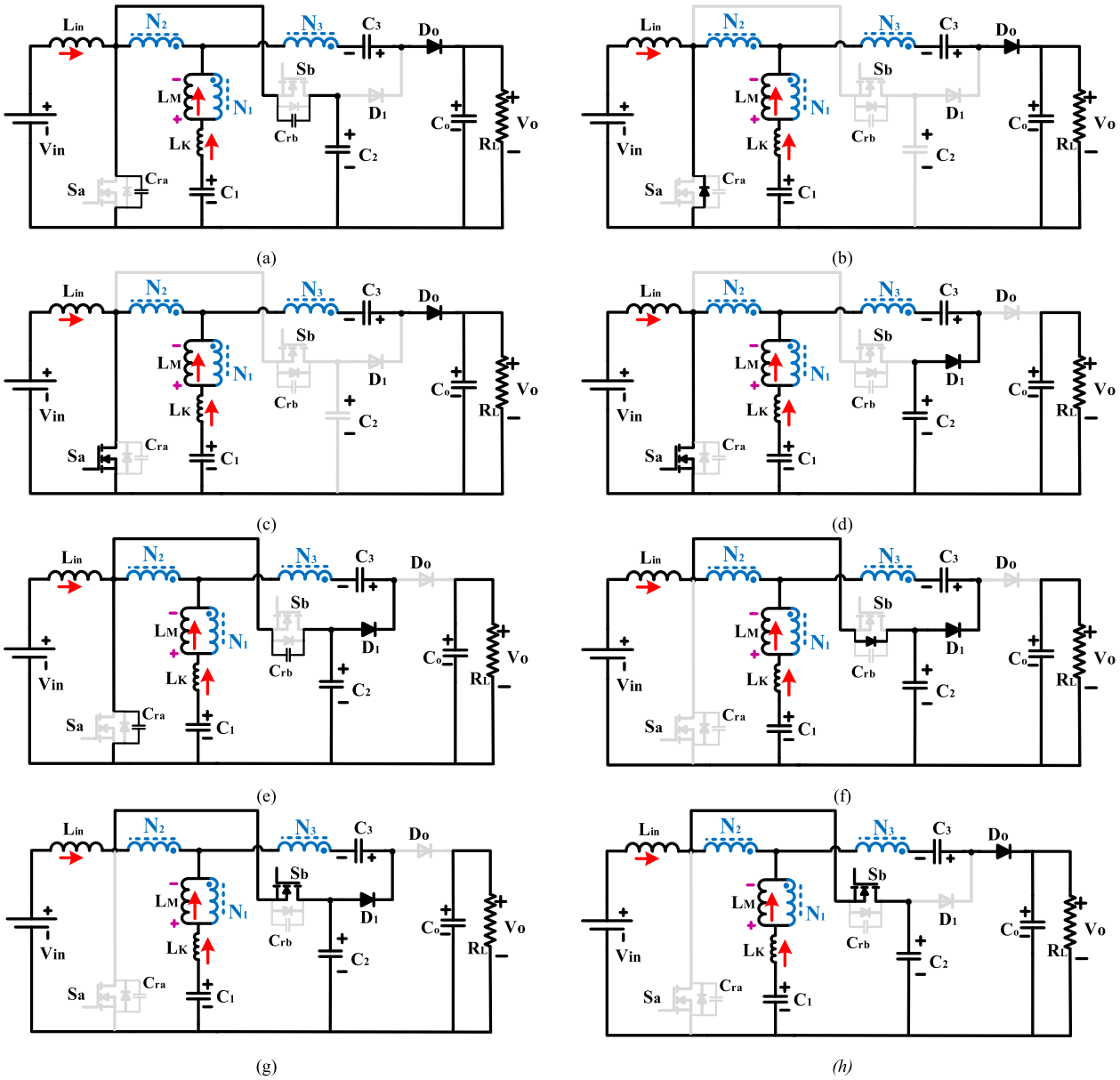

FIGURE 3. Operation modes of the proposed converter. (a) Mode-1(t_0-t_1), (b) mode-2 (t_1-t_2), (c) mode-3 (t_2-t_3), (d) mode-4 (t_3-t_4), (e) mode-5 (t_4-t_5), (f) mode-6 (t_5-t_6), (g) mode-7 (t_6-t_7), and (h) mode-8 (t_7-t_8).

The leakage inductance of the TWBT decreases the *di/dt* in the main switch S_a during this state. In this mode, the input inductor (L_{in}) receives energy from the input DC voltage. Thus, its current starts to increase at a positive slope. The series connection between the leakage inductance of the tertiary side of the TWBT and the output diode leads to i_{Do} reaches to zero with a gentle slope without a reverse recovery problem at the end of this transient mode ($t = t_3$).

Mode 4 [$t_3 - t_4$]: In the state, the power switch S_a is still on, and the diode D_1 starts to turn on at ZCS condition. As shown in Fig. 3(d), the input inductor L_{in} is magnetized by the input power supply V_{in}; therefore its current (i_{Lin}) increases linearly. Moreover, due to the positive voltage applied across the magnetizing inductor (L_M) from the capacitor C_1, its current (i_{LM}) starts to increase under a positive slope. Moreover, the capacitor C_3 is charged by the tertiary side of the TWBI and the capacitor C_2. In this mode, the following equations can be given:

$$v_{Lin} = V_{in} \tag{1}$$

$$v_{LM} = K\frac{v_{C1}}{1 - n_{21}} \tag{2}$$

$$v_{C3} = v_{C2} - v_{C1} + (1 + n_{31})v_{LM} \tag{3}$$

$$i_{sa} = i_{in} + i_{N2} \tag{4}$$

$$i_{D1} = \frac{i_{Lk}(1 - n_{21})}{n_{21} + n_{21}} \tag{5}$$

TABLE 1. Summary of Soft-Switching Performance of Switching Elements of the Proposed Converter

Device	S_a	S_b	D_1	Do
Turn-on Time	ZVS	ZVS	Low Reverse Recovery	Low Reverse Recovery
Turn-off Time	-	-	ZCS	ZCS

Here, K denotes the coupling coefficient of the TWBT, which is defined as:

$$K = \frac{L_M}{L_M + L_K} \tag{6}$$

Mode 5 [$t_4 - t_5$]: S_a is turned off at $t = t_4$; while S_b has not yet received the power-on command. In this time interval, Diode D_1 is still on (Fig. 3(e)). The leakage inductance of the built-in transformer begins to resonate with the switch output capacitances C_{rSa} and C_{rSb}. Therefore, C_{rSb} is discharged by I_{Lin} as well as i_{N2} while C_{rSa} is charged. At the end of this interval, output capacitance C_{rSa} is charged to V_{C2}.

Mode 6 [$t_5 - t_6$]: At t_5, the antiparallel diode of the auxiliary switch S_b is forced to conduct with the difference current between i_{Lin} and i_{N2} (Fig. 3(f)). In this mode, the energy stored in the leakage inductance of the TWBT is absorbed by the clamp capacitor C_2. To achieve ZVS, the auxiliary switch S_b should be turned on when its antiparallel diode conducts. In this interval, the negative voltage is placed across L_m, thus its current start to reduce. In this state, the voltage stress across the main switch S_a is clamped.

Mode 7 [$t_6 - t_7$]: At t_6, the turn-on signal of the clamp switch S_b comes, and this switch begins to conduct under ZVS conditions. In this transition interval, the diode D_1 is also conducting. In this mode, the capacitor C_1 is charged by the leakage inductance current of the built-in transformer. Because of the series connection between the tertiary side of the TWBT and D_1, the current of this diode (i_{D1}) reaches zero with a low slope under the LRR conditions at the end of this mode.

Mode 8 [$t_7 - t_8$]: In the mode, the auxiliary switch S_b is still on, and the diode D_o starts to turn on at ZVS condition, as it is shown in Fig. 3(h). During this interval, the output capacitor C_o receives energy from the capacitor C_3 and the magnetizing inductor of the TWBT. Also, the capacitor C_1 receives energy from the primary side of the TWBT. Due to the negative voltage applied to the magnetizing inductor, its current starts to decrease at a negative slope. In this mode, the following equations can be given:

$$v_{Lin} = V_{in} - v_{C2} \tag{7}$$

$$v_{LM} = K\frac{v_{C1} - v_{C2}}{1 - n_{21}} \tag{8}$$

$$v_o = v_{C2} + v_{C3} - (n_{21} + n_{31})v_{LM} \tag{9}$$

$$i_{sb} = i_{in} + i_{N2} \tag{10}$$

A summary of soft-switching performance of the switching elements of the proposed topology is illustrated in Table 1.

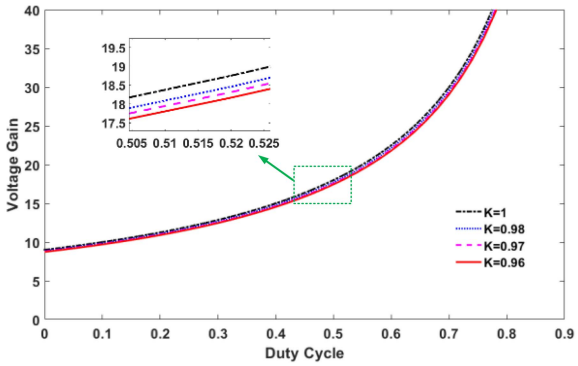

FIGURE 4. Voltage gain versus duty-ratio and K ($n_{21} = 0.7$ and $n_{31} = 1.4$).

III. STEADY-STATE ANALYSIS OF THE PROPOSED TOPOLOGY

For the sake of simple analysis, only operations Modes 4 and 8 are considered, since the time duration of these modes is larger than other intervals significantly.

A. VOLTAGE GAIN

The average value of the voltage of the capacitors C_1 and C_2 can be calculated by employing the voltage-second balance principle for the input and magnetizing inductors over one switching period as follows:

$$V_{C1} = V_{in} \tag{11}$$

$$V_{C2} = \frac{V_{in}}{1 - D} \tag{12}$$

Here, D is the duty cycle of the switch S_a. Using (2), (11), and (12), the voltage of the capacitor C_3 is obtained as:

$$V_{C3} = \frac{K(n_{31} + n_{21})(1 - D) + 1 - n_{21}}{(1 - n_{21})(1 - D)}.V_{in} \tag{13}$$

Finally, by using the relations (7)–(9), and (11)–(13), the overall voltage gain of the suggested converter is calculated as:

$$M = \frac{V_o}{V_{in}} = \frac{K(n_{31} + n_{21}) + 2 - 2n_{21}}{(1 - n_{21})(1 - D)} \tag{14}$$

Fig. 4 shows the voltage gain of the suggested converter under various duty cycle and some coupling coefficient ($n_{21} = 0.7$ and $n_{31} = 1.4$). It is clear that the existence of the leakage inductance has no significant effect on the conversion ratio, so it can be neglected. Consequently, the ideal voltage gain of the proposed converter with $K = 1$ is obtained as:

$$M = \frac{V_o}{V_{in}} = \frac{2 + n_{31} - n_{21}}{(1 - n_{21})(1 - D)} \tag{15}$$

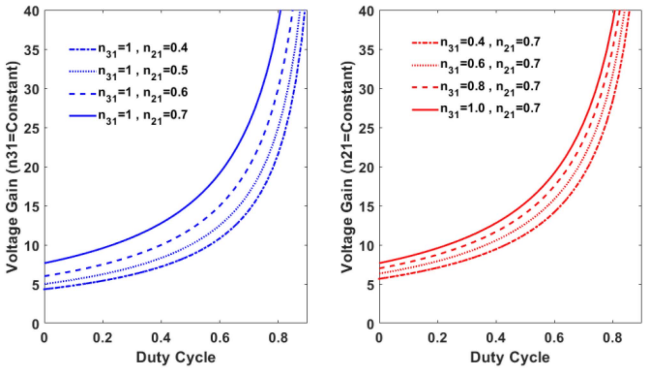

FIGURE 5. Relationship between the voltage gain and duty cycle of the proposed converter for different values of n_{21} and n_{31}.

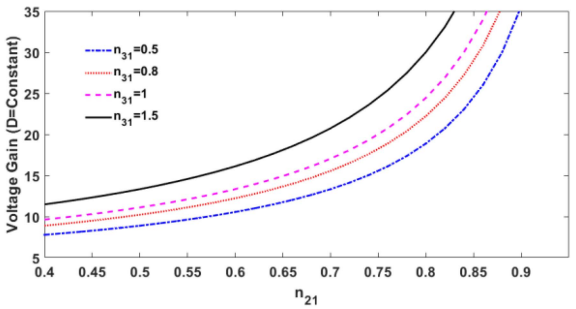

FIGURE 6. Voltage gain of the converter versus n_{21} for some values of n_{31} ($D = 0.55$).

Fig. 5 illustrates the voltage gain of the proposed converter versus the duty cycle for some given turn ratios of the TWBT (n_{21} and n_{31}). It reveals that high voltage gains can be obtained by increasing parameters D, n_{21}, and n_{31}. Regarding this figure, it is clear that increasing n_{21} towards unity ($n_{21} \rightarrow 1$) leads to a considerable increase in the voltage gain of the proposed converter. In other words, the output voltage of the converter is more sensitive to n_{21} than n_{31}. Thus, in this converter, higher voltage gain can be achieved under fewer turns ratios of the TWBT, which helps to reduce the conduction power losses.

Moreover, Fig. 6 shows the voltage gain of the proposed topology as a function of the turns ratio n_{21} for some values of n_{31} at a constant duty cycle $D = 0.55$. From this figure, by increasing the turns ratio n_{21} toward unity ($n_{21} \rightarrow 1$) an ultra-high voltage gain can be achieved. In other words, unlike the most coupled-inductor-based DC-DC converters, the voltage gains of the proposed converter are increased under small turns ratios which can be considered as a unique merit of this topology.

B. VOLTAGE AND CURRENT STRESS ACROSS THE POWER DEVICES

According to Fig. 3 and using (15), the magnitudes of drain-source voltage stress (V_{ds}) on the switches S_a and S_b can be obtained as follows:

$$V_{ds(Sa)} = V_{ds(Sb)} = \frac{V_{in}}{1-D} = \frac{(1-n_{21})}{2+n_{31}-n_{21}} V_o \tag{16}$$

Also, the maximum repetitive peak reverse voltage on the converter diodes D_1 and D_o can be deduced as:

$$V_{D1} = V_{Do} = \frac{1+n_{31}}{2+n_{31}-n_{21}} V_o \tag{17}$$

Considering (15), the input average current of the presented converter is given as:

$$< i_{in} >= M I_o \tag{18}$$

Here I_o denotes the output load current. In this circuit, with the help of the current average law for the converter capacitors, the average current values of the magnetic and leakage inductors of the TWBT are obtained as:

$$< i_{LM} >=< i_{LK1} >= 0 \tag{19}$$

Since the average current value of the magnetic inductor of the built-in transformer in the proposed converter is zero, the ac flux is balanced in the core which increases the saturation margin. The peak current of the diodes D_1 and D_o can be estimated as follows:

$$i_{D1_{peak}} = \frac{2I_o}{\mathrm{D}} \tag{20}$$

$$i_{Do\_peak} \approx \frac{2I_o}{1-D} \tag{21}$$

Besides, the peak value of the currents passing through the switches S_a and S_b can be given using (20) and (21) as:

$$i_{Sa(Off)} \approx \left(M + \frac{2(1+n_{31})}{(1-n_{21})\,\mathrm{D}} \right) I_o \tag{22}$$

$$I_{Sa(RMS)} = I_o \left(M + \frac{2(1+n_{31})}{(1-n_{21})\,\mathrm{D}} \right) \sqrt{\frac{D}{3}} \tag{23}$$

$$i_{Sb(Off)} \approx \left(\frac{2(1+n_{31})}{(1-n_{21})\,(1-\mathrm{D})} - M \right) I_o \tag{24}$$

$$I_{Sb(RMS)} = I_o \left(\frac{2(1+n_{31})}{(1-n_{21})\,(1-\mathrm{D})} - M \right) \sqrt{\frac{D_3}{3}} \tag{25}$$

$$i_{N1(RMS)} = 2I_o \frac{(n_{21}+n_{31})}{(1-n_{21})} \sqrt{\frac{1}{3D\,(1-D)}} \tag{26}$$

$$i_{N2(RMS)} = 2I_o \frac{(1+n_{31})}{(1-n_{21})} \sqrt{\frac{1}{3D\,(1-D)}} \tag{27}$$

$$i_{N3(RMS)} = 2I_o \sqrt{\frac{1}{3D\,(1-D)}} \tag{28}$$

$$i_{C1(RMS)} = 2I_o \frac{(n_{21}+n_{31})}{(1-n_{21})} \sqrt{\frac{1}{3D\,(1-D)}} \tag{29}$$

$$i_{C2(RMS)} = I_o \sqrt{\frac{4}{3D\,(1-D)} + i_{Sa(Off)}^2 \frac{D_2}{2} + i_{Sb(Off)}^2 \frac{D_3}{2}} \tag{30}$$

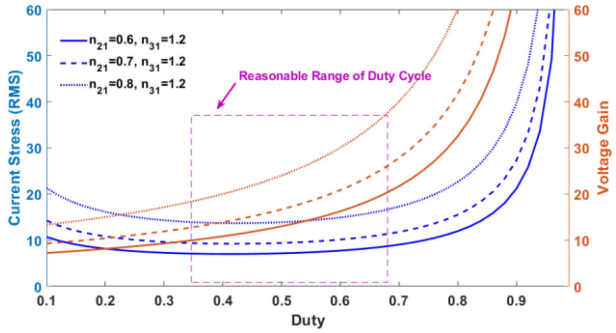

FIGURE 7. RMS current value of S_a along with voltage gain ratio of the proposed converter versus the duty cycle.

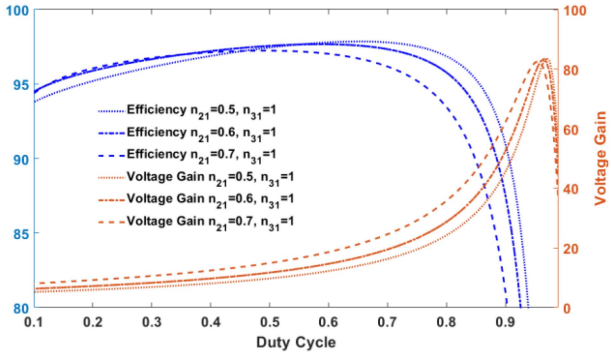

FIGURE 8. Voltage gain (non-ideal) and theoretical efficiency of the proposed converter versus duty cycle under several turns ratios of n_{21}.

$$i_{C3(RMS)} = 2I_o\sqrt{\frac{1}{3D\,(1-D)}} \tag{31}$$

$$i_{Co(RMS)} = 2I_o\sqrt{\frac{1}{3D\,(1-D)} + \frac{D-1}{2}} \tag{32}$$

Here, D_2 is the conduction time duration of the body diode of the S_b. Moreover, D_3 is the conduction time duration of the switch S_b. The time durations D_3 and D_4 are obtained as:

$$D_3 = \frac{2I_o + (1-D)\,i_{Sa(Off)}}{i_{Sa(Off)} + i_{Sb(Off)}} \tag{33}$$

$$D_2 = 1 - D - D_3 \tag{34}$$

Fig. 7 shows the RMS current value of the main power switch S_a along with the voltage gains as a function of the duty cycle at some turns ratios n_{21} and n_{31}. Considering that the power switch in high-gain converters bears the most current stress, therefore its analysis is a suitable method to determine the reasonable range of the duty cycle. From this figure, The best range to choose the duty cycle is in the middle range (0.35<D<0.7). Because in this range, high voltage gains are obtained under minimum current stress level.

C. POWER LOSS ANALYSIS

In this part, an analysis of the theoretical power dissipations for the components used in the suggested converter is provided.

Switch Loss: Every switch presents switching losses at on and off states along with conduction loss during their on-state. As the presented topology operates under ZVS performance for both switches S_a and S_b, only switch off-transitions involve losses. Therefore, the switches' power losses in the proposed circuit are given as:

$$P^{loss}_{S(Sa\&Sb)} = \frac{1}{2T_s}.V_{DS}\left(i_S^{t=off}.t_{off}\right) + R_{DS(on)}.I^2_{S(RMS)} \tag{35}$$

Here, t_{off} represents the switch fall time.

Diode Loss: The power losses of diodes include conduction resistive dissipations, forward voltage drop, and reverse recovery losses. In the proposed circuit, all diodes are turned- off without reverse recovery problem. Consequently, the diodes power loss of the converter is calculated as:

$$P^{loss}_{D_{1,o}} = V_F.I_{D(Mean)} + r_{D(on)}.I^2_{D(RMS)} \tag{36}$$

Here, V_F and $r_{D(on)}$ are the forward voltage drop and the diode on-state resistance, respectively.

Capacitor Loss: due to the equivalent series resistance (r_{ESR}), the capacitors of the converter are expressed the conduction losses as:

$$P^{loss}_{Cap.(12,3,\,o)} = r_{ESR}.I^2_{C(RMS)} \tag{37}$$

Magnetic device Loss: The magnetic power losses of the input inductor (L_{in}) and built-in transformer (TWBT) can be estimated as:

$$P^{loss}_{Lin} = r_{L_{in}}.I^2_{L_{in}(RMS)} + P_{Core(Lin\ )} \tag{38}$$

$$P^{loss}_{TWBT} = r_{w1}.I^2_{N1(RMS)} + r_{w2}.I^2_{N2(RMS)} + r_{w3}.I^2_{N3(RMS)} + P_{Core(\ TWBT)} \tag{39}$$

Where r_{Lin} and $r_{w1\text{-}3}$ denote the series winding resistances of the input inductor and TWBT, respectively.

The core power losses of the magnetic components of the proposed converter, including the input inductor and TWBT, are calculated by the help of Steinmetz's equation as follows:

$$P_{Core} = \rho_c.V_c.K_c.f^{\alpha}.\Delta B^{\beta} \tag{40}$$

Here, α, β, and K_c are constant and are dependent on the core material. Also, V_c is volume of core, ρ_c is mass density of core material. Moreover, the flux density in (40) can be calculated as:

$$B_{ac} = \Delta B = \frac{V_{Lin}.D}{2N.A_c.f} \tag{41}$$

Using the efficiency of the converter, the non-ideal voltage gain ratio can be given as:

$$M_{Non-Ideal} = \eta.M_{Ideal} \tag{42}$$

The theoretical efficiency curve as a function of duty cycle under several values of turns ratios n_{21} is provided in Fig. 8. The main parameters of the presented topology are $V_{in} = 25$ V, $R_L = 800\ \Omega$, $n_{21} = 0.7$, $n_{31} = 1.1$, and $f_s = 50$ kHz. In addition, the parasitic components of the circuit are $r_{DS} = 7.6\ m\Omega$,

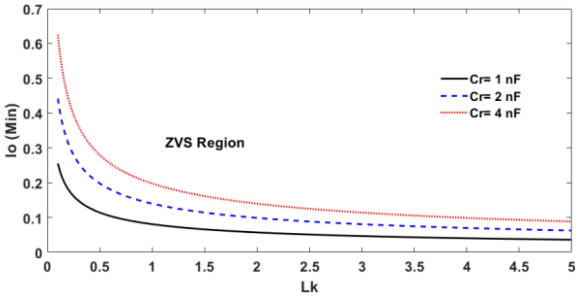

FIGURE 9. ZVS region of the main power switch S_a of the proposed converter in different output parasitic capacitors.

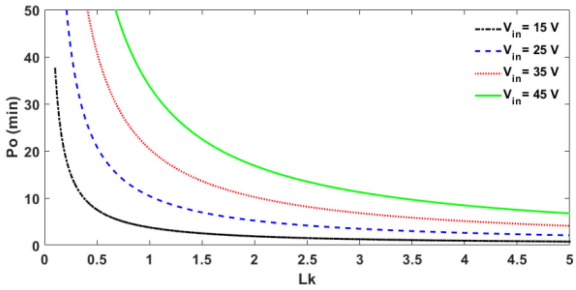

FIGURE 10. ZVS region of the main power switch S_a of the proposed converter in different input and output voltages.

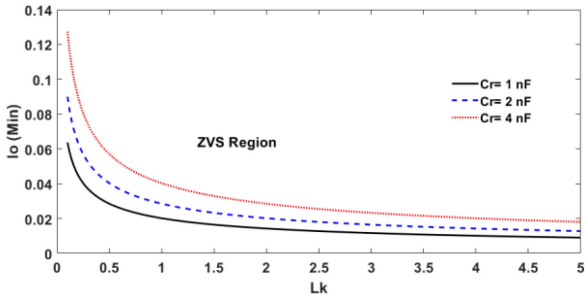

FIGURE 11. ZVS region of the auxiliary switch S_b of the proposed converter at $n_{21} = 0.7$, $n_{31} = 1.1$ and $V_{in} = 25V$.

$t_{off} = 4$ ns, $r_{C1} = 5$ mΩ, $r_{C2} = 7$ mΩ, $r_{C3} = 7$ mΩ, $r_{Co} = 160$ mΩ, $V_{FD1} = 0.7$ V, $V_{FD\text{-}Body\ (Sb)} = 0.8$, $V_{FDo} = 0.7$ V, $r_{D1} = 3$ mΩ, $r_{Do} = 8$ mΩ, $r_{Lin} = 25$ mΩ, $r_{N1} = 15$ mΩ, $r_{N2} = 10$ mΩ, $r_{N3} = 22$ mΩ). As can be seen, increasing the turns ratios of the TWBT leads to an increase in voltage gain and a decrease in the converter efficiency. However, the proposed converter with a high voltage gain and soft-switching performance, is able to provide high power-handling capacities.

D. SOFT-SWITCHING CONDITION

The efficiency of the suggested circuit is improved with ZVS performance for main and auxiliary switches (S_a and S_b). During operating modes 1 and 2 of the proposed converter, the ZVS turn-ON of S_a is achieved due to the fact that its anti-parallel diode is ON before the gate pulse comes. To satisfy the ZVS turn-ON of S_a, the available inductive energy should be high enough so that $i_{in} + i_{N2}$ will still remain negative after C_{ra} is fully discharged during the resonant time of the mode-1; thus:

$$\frac{1}{2}n_{21}^2 L_k I_{N2}^2 \geq \frac{1}{2}C_r V_{Cra}^2 \tag{43}$$

By placing the values of i_{N2} in mode 1, and the voltage of the switches, the following equation is obtained.

$$L_k > \frac{(2 + n_{31} - n_{21})^2 C_r V_{in}^2}{4n_{21}^2 (1 + n_{31})^2 (I_{in})^2 (1 - D)^2} \tag{44}$$

Here, $C_r = C_{ra} + C_{rb}$. From (44), the minimum value of the output load to achieve the ZVS condition can be given as:

$$I_{o(min)} > \frac{(2 + n_{31} - n_{21})\, V_{in}}{2M n_{21}\, (1 + n_{31})\, (1 - D)} \sqrt{\frac{C_r}{L_k}} \tag{45}$$

Fig. 9 shows the ZVS region of the main power switch S_a of the proposed converter as a function of the output current and the leakage inductance, in different output parasitic capacitors of the switches at $n_{21} = 0.7$, $n_{31} = 1.1$, and $V_{in} = 25$V. Regarding this figure, by increasing the leakage inductance of the TWBI, the ZVS Region can be extended. Nevertheless, large values of the leakage inductance decrease the voltage gain of the circuit. Moreover, the minimum value of the output power under different values of the input DC voltage source to achieve the soft-switching ZVS for the main power switch S_a is illustrated in Fig. 10.

Moreover, During operating mode-5, the leakage inductance of the built-in transformer begins to resonate with the switch output capacitances C_{rSa} and C_{rSb}. To satisfy the ZVS turn-ON of S_b, the following condition should be provided:

$$\frac{1}{2}n_{21}^2 L_k I_{N2}^2 \geq \frac{1}{2}C_r V_{Crb}^2 \tag{46}$$

From (46):

$$L_k > \frac{(2 + n_{31} - n_{21})^2 (D)^2 C_r V_{in}^2}{4n_{21}^2 (1 + n_{31})^2 (I_{in})^2} \tag{47}$$

Regarding (47), the minimum value of the output load current to achieve the ZVS condition for auxiliary switch S_b can be given as:

$$I_{o(min)} > \frac{(2 + n_{31} - n_{21})\, DV_{in}}{2M n_{21}\, (1 + n_{31})} \sqrt{\frac{C_r}{L_k}} \tag{48}$$

The ZVS region of the auxiliary switch S_b of the presented topology at $n_{21} = 0.7$, $n_{31} = 1.1$ and $V_{in} = 25$V is decpicted in Fig. 11.

IV. CIRCUIT PERFORMANCE COMPARISON AND EVALUATION

Table 2 summarizes an analytical comparison of the main circuit features of the proposed converter with its previously published non-isolated counterparts with low components.

Fig. 12 shows the line charts of the voltage gain comparison of the converters mentioned in Table 2 versus the

TABLE 2. Performance Comparison of the Proposed Converter With Other Related Converters

Converter Topology	No. of Components S/D/C/CI+L/T	Voltage Gain	L.I.C.R	Voltage Stress on Main Switch	Voltage Stress on Diodes	Soft-Switching (Main Switch)	$F_{req}/P_{out}/V_{in}/V_{out}$/Eff. kHz / W / V / V / %
[14]	1/3/4/1^{2w} +1/10	$\frac{n+2}{(1-D)}$	Yes	$\frac{V_o}{n+2}$	$\frac{(1+n)V_o}{n+2}$	ZCS	*30kHz/225W/27V/300V /93.2%*
[15]	1/3/4/1^{2w} +1/10	$\frac{n+1}{(1-D)}$	Yes	$\frac{V_o}{n+1}$	$\frac{nV_o}{n+1}$	ZCS	*24kHz/100W/15V/150V /91.5%*
[19]	2/2/5/1^{2W} +0/10	$\frac{2n+1}{(1-D)}$	No	$\frac{V_o}{2n+1}$	$\frac{nV_o}{2n+1}$	ZVS	*60kHz/250W/40V/380V /94.2%*
[20]	2/3/5/1^{2W} +1/12	$\frac{1+n(2-D)}{(1-D)}$	No	$\frac{V_o}{1+n(2-D)}$	$\frac{(1+n)V_o}{1+n(2-D)}$	ZVS	*100kHz/200W/20V/400V /96.5%*
[21]	2/4/4/1^{3W} +0/11	$\frac{n+2}{(1-D)}$	No	$\frac{V_o}{n+2}$	$\frac{(1+n)V_o}{n+2}$	ZVS	*100kHz/250W/30V/500V /96.4%*
[22]	1/3/4/1^{2w} +1/10	$\frac{n+2}{(1-D)}$	Yes	$\frac{V_o}{n+2}$	$\frac{(1+n)V_o}{n+2}$	ZCS+QR	*100kHz/500W/30V/380V /94.0%*
[23]	2/2/4/1^{2W} +1/10	$\frac{n+1}{(1-D)}$	Yes	$\frac{V_o}{n+1}$	$\frac{nV_o}{n+1}$	ZVS	*85kHz/135W/24V/250V /91.6%*
[24]	1/4/5/1^{2W} +1/12	$\frac{2(n-1)+D}{n(1-D)-1}$	Yes	$\frac{(n-1)V_o}{2(n-1)+D}$	$\frac{nV_o}{2(n-1)+D}$	-	*48kHz/400W/40V/400V /92.5%*
[25]	1/3/4/1^{3W} +1/10	$\frac{2+n_{21}-n_{31}(1+D)}{(1-n_{31})(1-D)}$	Yes	$\frac{(1-n_{31})V_o}{2+n_{21}-n_{31}(1-D)}$	$\frac{(1+n_{21}+n_{31}(1-D))V_o}{2+n_{21}-n_{31}(1-D)}$	ZCS+QR	*44kHz/225W/29V/300V /94.1%*
[26]	1/3/4/1^{3W} +1/10	$\frac{n_{31}+n_{21}(1+D)-\mathrm{D}}{(n_{21}-1)(1-D)}$	Yes	$\frac{(n_{21}-1)V_o}{n_{31}+n_{21}(1+D)-\mathrm{D}}$	$\frac{(1+n_{31})V_o}{n_{31}+n_{21}(1+D)-\mathrm{D}}$	-	*50kHz/200W/25V/200V /96.5%*
[27]	1/3/4/1^{3W} +1/10	$\frac{2n_{21}+n_{31}-1}{(n_{21}-1)(1-D)}$	Yes	$\frac{(1-n_{21})V_o}{2n_{21}+n_{31}-1}$	$\frac{(n_{31}+n_{21})V_o}{2n_{21}+n_{31}-1}$	ZVS	*50kHz/200W/30V/300V /95.4%*
[28]	1/3/4/1^{3W} +1/10	$\frac{n_{21}(1+D)-n_{31}+D}{(n_{21}-n_{31})(1-D)}$	Yes	$\frac{(n_{21}-n_{31})V_o}{n_{21}(1+D)-n_{31}+D}$	$\frac{(1+n_{21})(n_{21}-n_{31})V_o}{n_{21}(1+D)-n_{31}+D}$	ZVS	*500kHz/160W/48V/400V /94.4%*
[29]	2/2/4/1^{3W} +1/10	$\frac{2n-1}{(n-1)(1-D)}$	Yes	$\frac{(n-1)V_o}{2n-1}$	$\frac{nV_o}{2n-1}$	ZVS	*50 kHz/250W,40V/400V /96.5%*
[30]	2/2/4/1^{3W} +1/10	$\frac{2+n_{21}+n_{31}(1-D)}{(1-D)}$	Yes	$\frac{V_o}{2+n_{21}+n_{31}(1-D)}$	$\frac{(n_{21}+n_{31})V_o}{2+n_{21}+n_{31}(1-D)}$	ZVS	*100kHz/350W/45V/400V /96.5%*
Proposed Converter	2/2/4/1^{3W} +1/10	$\frac{2+n_{31}-n_{21}}{(1-n_{21})(1-D)}$	Yes	$\frac{(1-n_{21})V_o}{2+n_{31}-n_{21}}$	$\frac{1+n_{31}}{2+n_{31}-n_{21}}V_o$	ZVS	*50kHz/200W/25V/400V /95.2 %*

S=Switch, **D**=Diode, **C**=Capacitor, **CI** =Coupled-Inductor, **L**=inductor, **T**=Total Device Count, **L.I.C.R**= Low Input Current Ripple, **Eff**=Efficiency

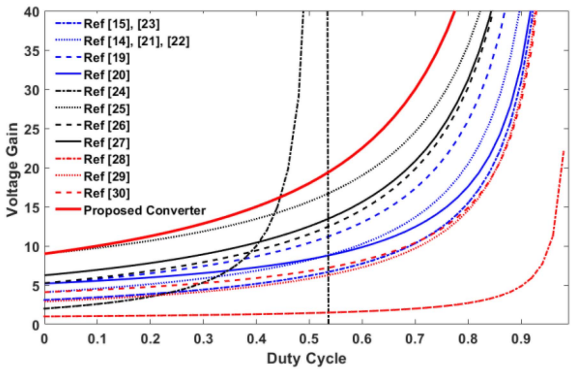

FIGURE 12. Voltage gain comparison of converters given in Table II.

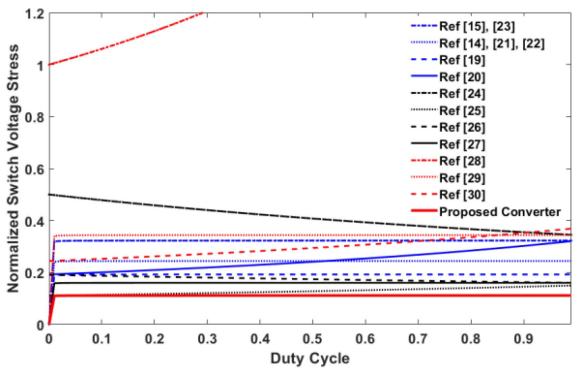

FIGURE 13. Comparison of normalized voltage stress across the power switch of the converters given in Table 2.

duty cycle under the same conditions $n_{21} = 0.7$, $n_{31} = 1.4$ (for three-winding CI-based converters), $n = n_{21}+n_{31} = 2.1$ (for two-winding CI-based converters). It can be seen that among these converters, the presented converter has a superior voltage gain ratio compared to other converters. It is worth mentioning that the converter in [24] is also able to provide high voltage gains at the range of $0.43 < D < 0.5$. Nevertheless, the steep slope of voltage gain changes in this topology leads to its more complicated control.

Further, the normalized voltage stresses across the main power switch of the converters in Table 2 are drawn in Fig. 13. Among the converters, the proposed topology has less switch voltage stress for all ranges of the duty cycle. Similarly, Fig. 14 depicts the normalized voltage across the output diode of the converters. From this plot, the output diode voltage stress is lower than the output voltage. The other converters that provide less voltage stress across the output diode, are inferior in their other features. The electrical characteristics of the converters are also presented in Table 2. Of course,

TABLE 3. Power Density Comparison of the Converters in Table 2 at P_o = 200W

Converter	[14]	[15]	[19]	[20]	[21]	[22]	[23]	[24]	[25]	[26]	[27]	[28]	[29]	[30]	Proposed Converter
Power Density (w/cm^3)	1.58	1.58	1.57	1.21	1.65	1.58	1.47	1.66	2.24	2.24	1.95	1.52	2.24	1.58	2.24

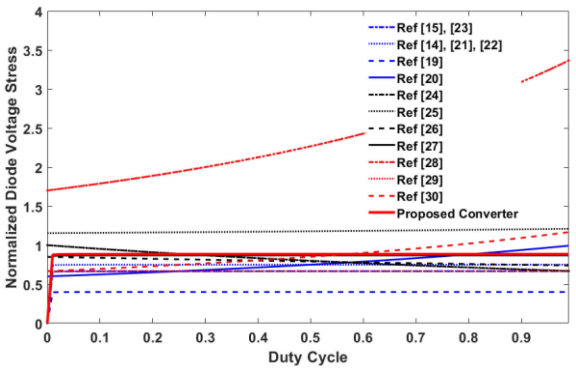

FIGURE 14. Comparison of normalized total voltage stress of the diodes of the converters given in Table 2.

it is worth mentioning that different topologies have been tested in different conditions. In addition, the power density of the converters by considering the size of the capacitors and magnetic components are are provided and shown in Table 3 at V_{in} = 25 V, V_{out} = 400 V, P_o = 200 W, D = 0.55, ΔI_{in} = 2A, and f_s = 50 kHz. From this table, it can be stated that the proposed converter has a suitable and acceptable power density.

According to the above discussions, the suggested converter with low components count and soft-switching performance meets good performance for the renewable energy cases applications.

V. CONVERTER DESIGN CONSIDERATIONS

From Fig. 7, the best range to choose the duty cycle is in the middle range (0.35<D<0.7). Because in this range, high voltage gains can be obtained at the minimum current stress levels across the main power switch S_a. After determining the appropriate range of the duty cycle, it is necessary to select the proper values of the turns ratios n_{21} and n_{31}. As mentioned before, n_{21} has a more significant effect on increasing the voltage gain of the converter. However, according to Figs. 5 and 6, although the increase of n_{21} leads to an increase in the voltage gain, it also leads to an exponential increase in the current stress. Consequently, choosing values very close to the unit is not recommended. It seems that choosing $n_{21} < 0.8$ can be reasonable.

By considering an acceptable current ripple, the minimum value of the input inductor can be derived as:

$$L_{in} = \frac{V_{in}.D}{\Delta I_{in}.f_s} > \frac{R_L.D}{\delta\%M^2.f_s} \tag{49}$$

where ΔI_{in} represents the permitted input current ripple. The minimum value of magnetizing inductance (L_m) of the TWBT

TABLE 4. Introduction of Symbols A_p

Symbol	Meaning
K_u	Window utilization factor
K_t	Constant coefficient (=48200)
K_i	Current waveform factor
γ	Ratio of iron loss to copper loss
B_{max}	Maximum flux density
L	Inductance value
$\hat{I}$	Peak current value
ΔT	temperature rise

can be designed by:

$$L_M > \frac{V_{Lm}.D}{\Delta I_{LM}.f_s} = \frac{V_{in}.D}{\Delta I_{LM}.(1-n_{21}).f_s} \tag{50}$$

The core sizes of magnetic devices are typically determined by the product of window winding area cross-sectional area (A_P) factor [33]. This parameter is calculated as:

$$A_p = \left[\frac{K_i.L.\hat{I}^2.\sqrt{1+\gamma}}{B_{max}.K_t.\sqrt{K_u\Delta T}}\right]^{\frac{8}{7}} \tag{51}$$

Where, the meaning of symbols used in (51) are listed in Table 4. Then, the number of turns for input and magnetizing inductor can be determined as:

$$N = \sqrt{\frac{L}{A_L}} \tag{52}$$

Where, A_L is inductance per turn that can be find in selected magnetic core datasheet.

According to the converter output power, capacitor voltage, the maximum tolerant voltage ripple (ΔV_{Co}), and converter switching frequency f_s, the minimum value of the output capacitor C_o can be obtained as:

$$C_o > \frac{D.I_o}{\Delta V_{co}.f_s} \tag{53}$$

In addition, the proper values of the capacitors C_1, C_2, and C_3 are calculated as follows:

$$C_1 = \frac{i_{N1}D}{\Delta V_{c1}.f_s} > \frac{(n_{21}+n_{31}).V_{out}}{\Delta V_{C1}.(1-n_{21}).R_L.f_s} \tag{54}$$

$$C_2 = \frac{i_{D1}.D}{\Delta V_{c2}.f_s} > \frac{V_{out}}{\Delta V_{c2}.R_L.f_s} \tag{55}$$

$$C_3 = \frac{i_{D1}.D}{\Delta V_{c3}.f_s} > \frac{V_{out}}{\Delta V_{c3}.R_L.f_s} \tag{56}$$

where $\Delta V_{C1,2,\&3}$ denote the allowable voltage ripple. Also, during the operating mode 4, a resonant tank is created between the leakage inductor of the TWBT and the capacitor C_1. In order to avoid high frequency resonant oscillation between

TABLE 5. Parameters of Prototype Setup

Parameter	Values
Output Power (P_{out})	200 W
Input Voltage (V_{in})	25 V
Output Voltage (V_{out})	400 V
Switching Frequency ($f_{s1\&s2}$)	50 kHz
Capacitor C_1	2*8.2 µF / 250 V
Capacitor C_2	10 µF / 100 V
Capacitor C_3	10 µF / 250 V
Capacitor C_o	220 µF / 450 V
Switches S_a and S_b	IPP076N15N5/R_{DS}=7.6mΩ
Input Inductors L_{in}	160 µH / T184-52
Magnetizing Inductor of the BT (L_m)	200 µH
Turns Ratios of the TWBT (n_{21}:n_{31})	(0.7:1.1) / EE42/21/20
Leakage Inductance L_K	1.65 µH
Diodes D_1 and D_o	MUR440 ($V_{F\,(Max)}$=1.05 V)

L_k and C_1, it is necessary the half of the resonant period be more than the duration time of mode-4.

$$\pi\sqrt{L_k C_1} > DT_s \tag{57}$$

VI. EXPERIMENTAL RESULTS

The theoretical analysis of the presented topology has been validated with a 200 W, 25 V input, and 400 V output sample prototype in the laboratory. The main components of the prototype are listed in Table 5. In this prototype, two photocouplers TLP350 are used for driving the state of the MOSFETs. Because of the low voltage rate on the converter switches S_a and S_b, two MOSFETs IPP076N15N5 with very low $R_{DS(on)}$ are utilized. To decrease the conduction power loss in the circuit, MKT capacitors are used for C_1-C_3. The experimental waveforms of the voltage and current of the components were obtained using a high-frequency current probe PA-667 and a differential voltage probe GDP-025. Current probe PA-667 has division coefficients of 500 m and 50 m and differential voltage probe GDP-025 has division coefficients of x20, x50 and x200.

Fig. 15(a) represents the gate signals of the MOSFETs S_a and S_b. In Figs. 15(b) and 16, the experimental results of the voltage and current of the converter switches at full load are provided. In these figures, the soft-switching performance (ZVS turn-on) of the MOSFETs S_a and S_b with zoomed ZVS region are shown. With the help of an active clamp, the switches' voltage stress are limited to about 50 V under V_o = 400 V. This low voltage rate across the switches lets to use of MOSFETs with lower $R_{ds(ON)}$. The LRR conditions at the turn- off instant of the diodes D_1 and D_o of the converter are realized in Figs. 17 and 18(a). Continuous input current waveforms along with the leakage inductance current and the output voltage of the proposed converter at full load condition in steady-state, are given in Fig. 18(b). Because of the soft-switching performance and LRR conditions for all diodes of the converter, the output DC voltage is constant without voltage spikes and noises at the switching instants, which is the other benefits of the suggested topology. For different output power levels, the efficiency of the proposed converter is measured and illustrated in Fig. 19. Measured maximum

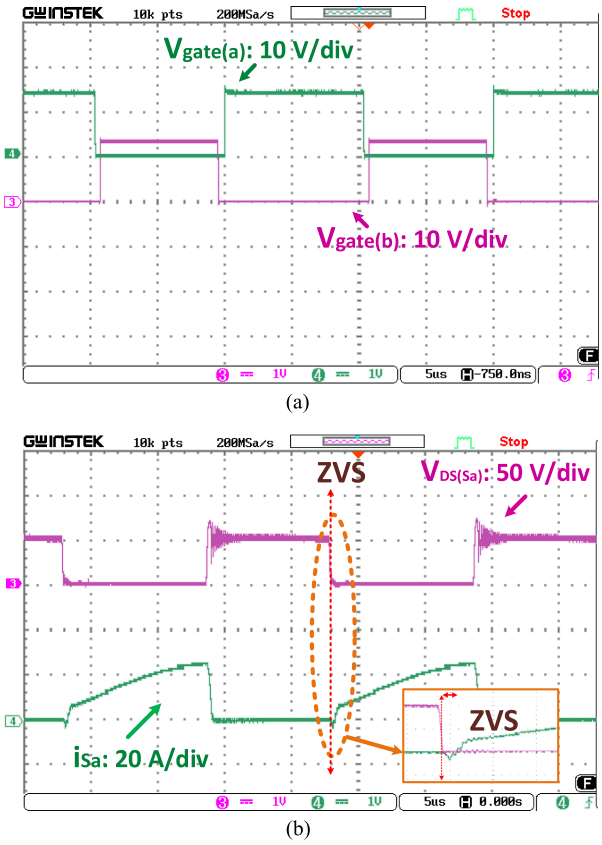

FIGURE 15. Experimental results of the converter at full load. (a) gate signals, and (b) MOSFET S_a.

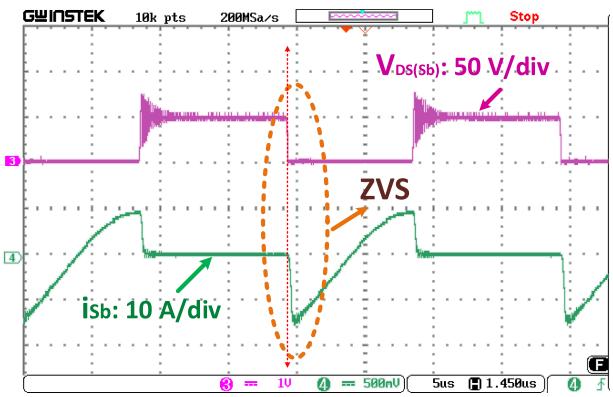

FIGURE 16. Experimental results of the *MOSFET S_b*.

efficiency of the converter is about 95.8% at P_o = 120 W for V_{in} = 25 V and V_o = 400 V. From this figure, increasing the output power leads to decreasing the converter efficiency with a light slope. Also, Fig. 20 shows a pie diagram of power loss breakdown at full load conditions.

The experimental results of the dynamic response under a 50% disturbance in the output load by considering a simple closed-loop controller (PI) (from R_{L1} = 800 Ω to R_{L2} = 1200 Ω in periodic form) are shown in Fig. 21. A photograph

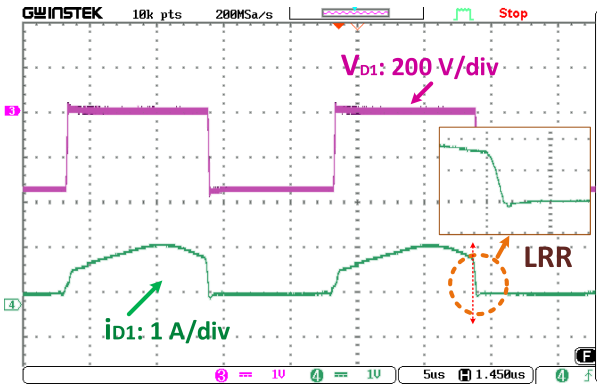

FIGURE 17. Experimental results of the *Diode* D_1.

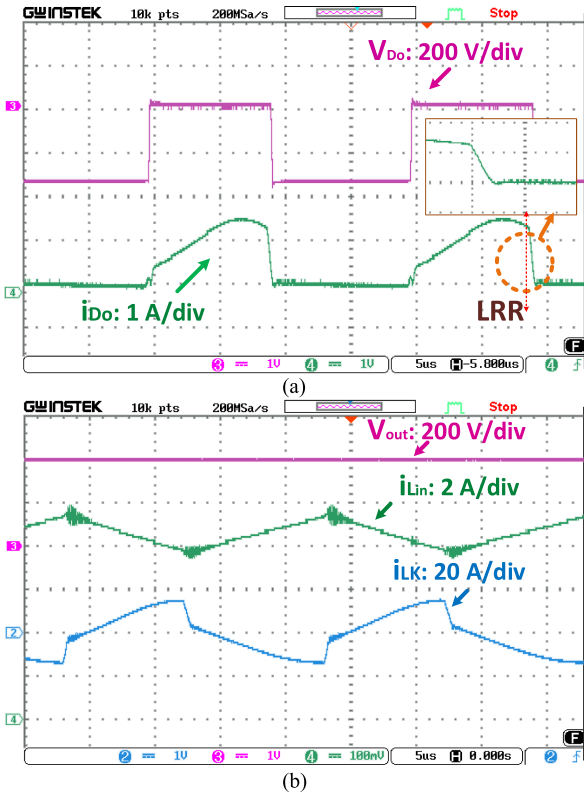

FIGURE 18. Experimental results of the converter at full load. (a) Diode D_o, and (b) V_o, i_{Lin} and i_{Lk}.

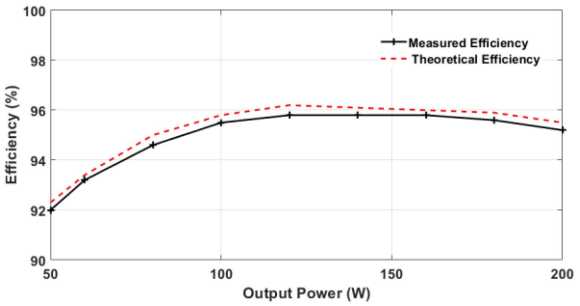

FIGURE 19. Theoretical and Measured efficiency versus output power of the proposed converter.

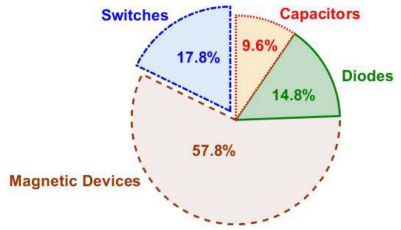

FIGURE 20. Break-down of power dissipitions at full load condition (V_{in} = 25 V, V_o = 400 V, and P_{out} = 200 W).

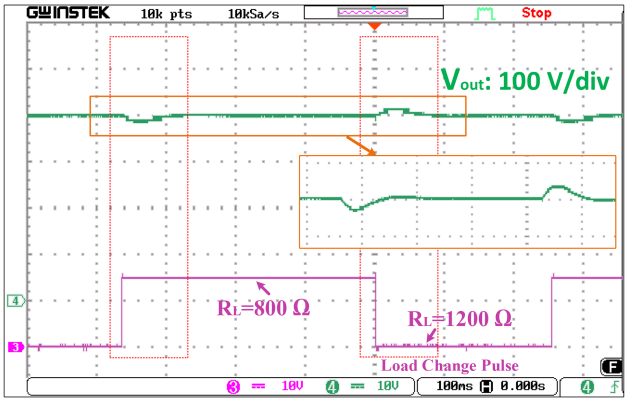

FIGURE 21. Experimental results of the dynamic response with a closed-loop controller (PI) for a 50% disturbance in the output load.

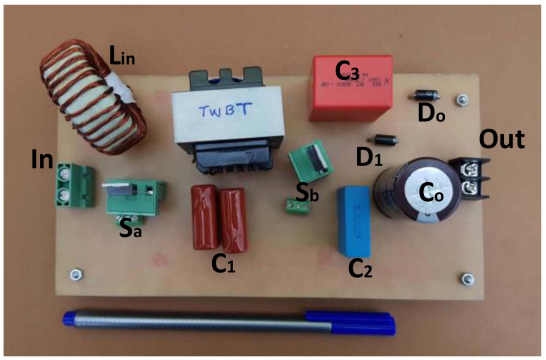

FIGURE 22. Photographs of the proposed converter prototype.

of the experimental prototype of the presented converter is shown in Fig. 22.

VII. CONCLUSION

In this article, a new ZVS high voltage gain DC-DC converter with a low number of components has been proposed for renewable energy source applications. By implementing a three-winding built-in transformer with a voltage multiplier circuit, a flexible voltage gain with trans-inverse property is achieved. In such a case, high voltage gain can be obtained under a lower turns ratio of the transformer. The maximum voltage stress on the power MOSFET is considerably restricted by utilizing an active clamp circuit, which is also guaranteed the soft-switching (ZVS tuns-on) performance for the switches. High voltage gain, low components count, the

soft-switching (ZVS) performance, continuous input current with low ripple, enough high efficiency, low voltage stress, and low reverse recovery are the main advantages of the proposed converter. The feasibility of the proposed converter design has been proved through a 25 V–400 V and 200 W laboratory prototype.

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