IEEE Open Journal of
Power Electronics

Received 4 March 2023; revised 30 March 2023; accepted 9 April 2023. Date of publication 12 April 2023;
date of current version 3 May 2023. The review of this article was arranged by Associate Editor Zhixiang Zou.

Digital Object Identifier 10.1109/OJPEL.2023.3266658

Power Flow Control for Decoupled Load Performance of Current-Fed Triple Active Bridge Converter

ZACHARY T. SMITH [1] (Student Member, IEEE), RICHARD B. BEDDINGFIELD [2] (Member, IEEE), AND BRANDON M. GRAINGER [1] (Senior Member, IEEE)

[1]Department of Electrical and Computer Engineering, University of Pittsburgh, Pittsburgh, PA 15260 USA
[2]FREEDM Systems Center, North Carolina State University, Raleigh, NC 27606 USA

CORRESPONDING AUTHOR: Zachary Smith (e-mail: zas59@pitt.edu)

ABSTRACT This article presents a phase-shift control method for a converter containing a multi-winding transformer. The control strategy is developed from a power flow analysis of the converter and uses the derived power flow equations to supply constant power at a load port while the second load port experiences large load changes. This control method prevents the constant load port from experiencing transient behavior caused by magnetic coupling with the other load port. The approach is demonstrated with an experiment using a controller within a control hardware-in-the-loop set-up and then a full experimental setup within a lower power test bed. By using control to mitigate the effects of mutual flux within a multi-winding transformer, the load ports of the converter are effectively decoupled. The analytical procedure described in this article can also be applied to other converter topologies containing multi-winding transformers to achieve similar decoupled load performance, as demonstrated in the triple active bridge converter test bed.

INDEX TERMS Centralized control, DC-DC power converters, load flow control, solid-state transformer.

I. INTRODUCTION

The widespread adoption of dc systems for low-voltage applications at the distribution level has spurred further research into even higher power dc networks, including increased system voltages into the medium voltage (MV) range. However, as the capacity of dc networks is increased, certain concerns arise. Namely, DERs themselves typically increase the control burden of the network [1], [2], [3]. In addition, the intermittent nature of renewable energy resources usually requires the system designer to include energy storage devices to reduce transient power fluctuation within the network [4]. On top of it all, traditional AC circuit breakers cannot be used currently within MVDC networks, making fault protection of these networks difficult.

A key component within dc networks that can address many of these issues is the converters that interface with the network. Modern solid-state switches and stacked topologies have recently enabled the possibility of operating at the kilovolt level for connection to the utility grid [5], [6], [7]. Power electronics can be used to increase flexibility of the dc network and also to respond to DERs [8], [9], [10], [11].

In addition, multi-port converters provide a method to tie in energy storage into the network using centralized control [12], [13], [14], [15]. At present, there are also at least six different categories of fault current limiting power converters available to protect the network from fault events [16].

A centralized converter with multiple ports can be used within a dc network to incorporate DERs, storage, and other networks into a grid with minimal conversion steps [13], [17], [18], [19]. Also, by adding inductance to a converter, fault tolerant operation can be achieved [20]. If these features are combined, the result is a current-fed, multi-port converter that can interconnect multiple MVDC buses within a dc network [21]. See Fig. 1 for an example dc network that makes use of such multi-port converters to create a ring network.

The current-fed triple active bridge (CFTAB) converter design is the basis for the research performed in this article [21]. With emerging state-of-the-art magnetics enabling the

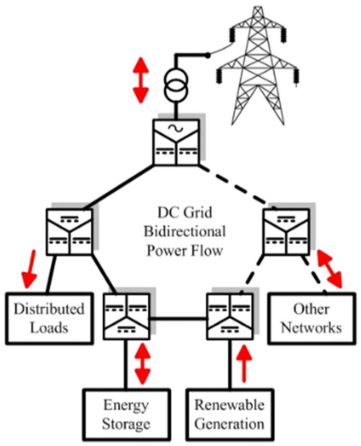

FIGURE 1. Example dc distribution ring bus network using bidirectional multi-port converters.

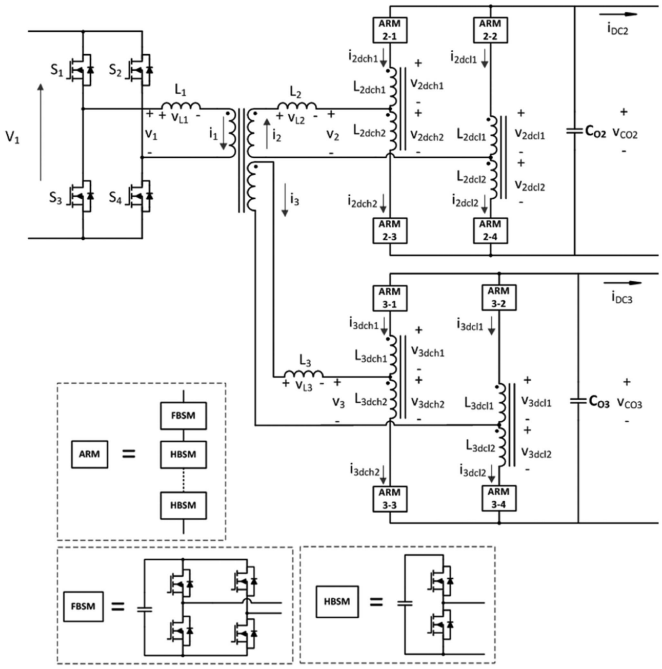

FIGURE 2. Current-fed triple active bridge topology for the example application of a LV-MV-MV converter. The MV arms consist of stacked submodules. Each MV port also contains two pairs of mutual inductors.

design of transformers and inductors for solid-state transformers (SSTs), the previously theoretical coupled inductor design becomes within hardware. Before taking that next step into hardware, further study into the converter performance to design a stable controller is required.

The contribution of this article is twofold. First, this article provides a comprehensive power flow analysis for all operating modes of the CFTAB converter. This article provides a step-by step description of the analysis, which makes the method easily repeatable not only for this topology, but for other converter topologies containing multi-winding transformers. The second contribution of this article is to harness the results of the power flow analysis to propose a control strategy based on the resulting power flow equations. Such a controller for the CFTAB converter has not been proposed before in the literature. The critical feature of the proposed control is that transient power flow conditions at one of the load ports do not affect the power flow performance at the second load port. This is because the coupled flux effects within the multi-winding transformer are predicted from the power flow analysis and compensation is incorporated within the controller. This control compensation is useful when significant load changes can create voltage disturbances at the other two dc ports, particularly in the case of weak grid systems like an islanded microgrid [22]. In electric vehicle applications as well, it is an important controller design metric to shield the battery port from transient disturbances [23]. Traditionally, a decoupling matrix is used to prevent transient disturbances. However, this method requires linearization around an operating point to derive the decoupling gain matrices. The proposed control strategy will be able to achieve decoupled performance without the need to re-calculate the control laws as the operating point changes.

The article layout is as follows: in Section II, the circuit schematic and phase shift control strategy are introduced. Then in Section III, the power flow analysis is performed to provide power output equations of each port for the entire operating range of the converter. Next, in Section IV, the control strategy is developed from the results of the power flow analysis. Section V demonstrates stable operation and provides the results of a control hardware-in-the-loop experiment employing the proposed control strategy. Section VI contains experimental results of using the controller with a prototype triple active bridge converter. Finally, Section VII concludes with the results of the work effort.

II. CIRCUIT SCHEMATIC

Traditionally, a dual active bridge (DAB) converter is comprised of a high frequency transformer with both the primary and secondary windings each having a full H-bridge interface to the primary and secondary dc buses [2], [24], [25], [26]. This traditional DAB topology can be controlled by adjusting the phase angle delay of the secondary side square wave with respect to the primary. Triple active bridge (TAB) converters are similar, with the addition of a tertiary H-bridge port and a 3-winding high frequency transformer [12], [27].

The CFTAB converter developed in this article takes the typical design of a TAB converter and adds mutual inductor pairs to the medium voltage windings of the three-winding transformer [21]. The topology of the converter is shown in Fig. 2. The secondary and tertiary ports are both connected to their respective MV dc buses and could represent a redundant connection to a critical load, or to two separate dc buses all with independent load and generation profiles. To operate at MV levels, the secondary and tertiary sides will require switching submodules to be placed in arm configurations as shown in the figure. The arm configurations of the MV ports

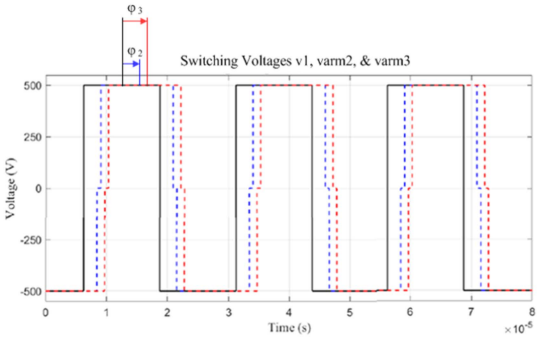

FIGURE 3. Switching voltage waveforms for each port: v_1 (black), v_{arm2} (blue), and v_{arm3} (red). For this study, the port voltages will all be assumed to be 500 V. The phase angles ϕ_2 and ϕ_3 are the control variables and use the primary waveform v_1 as the reference.

resemble the stacked submodule style within a modular multilevel converter (MMC). A simplification is made in this article by approximating each stacked arm submodule as a single ideal voltage source.

The winding leakage inductance of the primary, secondary, and tertiary windings are L_1, L_2, and L_3, respectively. The MV ports have mutual inductor pairs, and the naming convention is based on the pattern L_{xDCyz}, where x is the port number, y is either 'h' for high-voltage side (positive polarity of xfmr) or 'l' for low-voltage side (negative polarity of xfmr), and z is either 1 or 2 which identifies which inductor within the mutual inductor pair.

The converter power flow is determined by the voltages v_1, v_2, and v_3 and currents i_1, i_2, and i_3 which correspond to the primary, secondary, and tertiary transformer windings, respectively. The power flow at any port x can be computed as:

$$p_x = v_x i_x \tag{1}$$

Since MMF is shared within an ideal transformer, the overall power flow of the converter can be defined as:

$$p_1 = p_2 + p_3 \tag{2}$$

Phase shift control is used to regulate the power flow of this converter. As is typical based converters, the average current through the transformer is assumed to be zero under stable operation. The proposed control is phase shift-based and uses average power output as the control reference. Shown in Fig. 3 are the square voltage waveforms that are applied at each port of the converter. Note that while the voltage v_1 is directly applied to the primary windings of the transformer, the arm voltage waveforms v_{arm2} and v_{arm3} are not directly applied to the secondary and tertiary MV transformer windings due to the mutual inductors. The voltages across the secondary and tertiary windings of the transformer (v_2 and v_3) can nevertheless be computed from the three controlled switched voltage waveforms (v_1, v_{arm2}, and v_{arm3}) The primary voltage waveform v_1 is used as the reference, and the two controllable parameters are the phase shifts of the secondary (ϕ_2) and tertiary (ϕ_3). In addition to controlling phase shift, it is possible to additionally regulate the duty cycles of each square wave. However, the duty cycles at the ports with mutual inductors are bound by the relationship in (3), [28].

$$V_{busDC} = 2DV_{arm} \tag{3}$$

Where $D = 0.5$ is an ideal square wave. If this condition is not met, the mutual inductor pairs will experience a dc voltage bias, and the current will become unstable. Therefore, the duty cycles at the secondary and tertiary ports in this application are not freely available to be used as control variables.

III. AVERAGE POWER FLOW ANALYSIS

The average power flow was computed by using a switched circuit model for all eight possible states. There are potentially more states, but in this application a duty cycle of D = 0.5 was maintained on the secondary and tertiary ports for stability purposes. To reduce possible states, the duty cycle of the primary was maintained at 0.5 as well.

A single switching cycle of this converter is expected to be within the kilohertz range. This makes it intuitive to assume that the dc bus voltages and submodule voltages will remain constant within a switching cycle. Under this assumption, the currents become linear, and a state space representation of the circuit can be constructed.

A. DECOUPLING MUTUAL INDUCTOR CHARACTERISTIC EQUATIONS

One key challenge in the circuit analysis is mathematically decoupling the currents within the mutual inductor pairs. The standard equation for the voltage applied across an inductor with mutual coupling is:

$$v_\alpha = L_\alpha \frac{di_\alpha}{dt} - M\frac{di_\beta}{dt} \tag{4}$$

Where α denotes the first inductor within the coupled pair and β denotes the second inductor. This equation is unfortunately not linear but it is possible to perform a circuit analysis to substitute for one of the inductor current derivatives.

Reflecting on the topology in Fig. 2, there are two mutual inductor pairs on each of the two MV ports. This equates to a total of eight inductors that have non-linear state equations. Performing the substitution to a linear form will require 21 equations. The equations can be derived from the circuit diagram in Fig. 2 and will be shown now.

Mutual inductor equations from Kirchhoff's voltage loop within one MV port:

$$v_{2dch2} - v_{2dch1} = v_{2dcl1} - v_{2dcl2} \tag{5}$$

$$v_{3dch2} - v_{3dch1} = v_{3dcl1} - v_{3dcl2} \tag{6}$$

Kirchhoff's voltage loops within each MV port:

$$\begin{aligned} &v_{Co2} - v_{Carm2-1} - v_{2dch1} - v_{2dch2} - v_{Carm2-3} \\ &\quad = v_{Co2} - v_{Carm2-2} - v_{2dcl1} - v_{2dcl2} - v_{Carm2-4} \end{aligned} \tag{7}$$

$$\begin{aligned} &v_{Co3} - v_{Carm3-1} - v_{3dch1} - v_{3dch2} - v_{Carm3-3} \\ &\quad = v_{Co3} - v_{Carm3-2} - v_{3dcl1} - v_{3dcl2} - v_{Carm3-4} \end{aligned} \tag{8}$$

$$v_{Co2} = v_{Carm2-2} + v_{2dcl1} - v_2 + v_{2dch2} + v_{Carm2-3} \quad (9)$$

$$v_{Co3} = v_{Carm3-2} + v_{3dcl1} - v_3 + v_{3dch2} + v_{Carm3-3} \quad (10)$$

$$v_{Co2} = v_{Carm2-1} + v_{2dch1} + v_2 + v_{2dcl2} + v_{Carm2-4} \quad (11)$$

$$v_{Co3} = v_{Carm3-1} + v_{3dch1} + v_3 + v_{3dcl2} + v_{Carm3-4} \quad (12)$$

Kirchoff's current law at ports 2 and 3:

$$\frac{v_{L2}}{L_2} = -\frac{di_{2dch1}}{dt} + \frac{di_{2dch2}}{dt} \quad (13)$$

$$\frac{v_{L3}}{L_3} = -\frac{di_{3dch1}}{dt} + \frac{di_{3dch2}}{dt} \quad (14)$$

Faraday's law for mutual inductors in ports 2 and 3:

$$v_{2dch1} = L_{dc}\frac{di_{2dch1}}{dt} + M\frac{di_{2dch2}}{dt} \quad (15)$$

$$v_{2dch2} = L_{dc}\frac{di_{2dch2}}{dt} + M\frac{di_{2dch1}}{dt} \quad (16)$$

$$v_{2dcl1} = L_{dc}\frac{di_{2dcl1}}{dt} + M\frac{di_{2dcl2}}{dt} \quad (17)$$

$$v_{2dcl2} = L_{dc}\frac{di_{2dcl2}}{dt} + M\frac{di_{2dcl1}}{dt} \quad (18)$$

$$v_{3dch1} = L_{dc}\frac{di_{3dch1}}{dt} + M\frac{di_{3dch2}}{dt} \quad (19)$$

$$v_{3dch2} = L_{dc}\frac{di_{3dch2}}{dt} + M\frac{di_{3dch1}}{dt} \quad (20)$$

$$v_{3dcl1} = L_{dc}\frac{di_{3dcl1}}{dt} + M\frac{di_{3dcl2}}{dt} \quad (21)$$

$$v_{3dcl2} = L_{dc}\frac{di_{3dcl2}}{dt} + M\frac{di_{3dcl1}}{dt} \quad (22)$$

Note that the second current slope term is added instead of subtracted as in (4). This is simply due to the current direction defined in the other direction in the circuit schematic in Fig. 2.

Three-winding transformer turns ratio and current balance equations:

$$\frac{v_1 - v_{L1}}{n_1} = \frac{v_2 + v_{L2}}{n_2} \quad (23)$$

$$\frac{v_1 - v_{L1}}{n_1} = \frac{v_3 + v_{L3}}{n_3} \quad (24)$$

$$n_1 i_{L1} = n_2 i_{L2} + n_3 i_{L3} \quad (25)$$

The final step in preparation to solve the equations is to establish which variables are states within the system and which are controllable inputs. After decoupling the mutual inductor currents, the system can then easily be rewritten into state space form. The state space equation is of the form $\dot{\boldsymbol{x}} = \boldsymbol{Ax} + \boldsymbol{Bu}$ where the arrays $\boldsymbol{x}$ and $\boldsymbol{u}$ are:

$$\boldsymbol{x} = [i_{L1}\ i_{L2}\ i_{L3}\ v_{Co2}\ v_{Co3}\ v_{Carm2-11}\ v_{Carm2-12}\ \cdots$$
$$\cdots\ v_{Carm2-21}\ v_{Carm2-22}\ i_{2dch1}\ i_{2dcl1}\ i_{2dch2}\ i_{2dcl2}\cdots$$
$$v_{Carm3-11}\ v_{Carm3-12}\ v_{Carm3-21}\ v_{Carm3-22}\cdots$$
$$i_{3dch1}\ i_{3dcl1}\ i_{3dch2}\ i_{3dcl2}]^T \quad (26)$$

$$\boldsymbol{u} = [V_1\ I_{DC2}\ I_{DC3}]^T \quad (27)$$

Solving for each state variable is done through MATLAB's symbolic solver toolkit. This solver was used to solve the system of 21 equations to mathematically decouple the mutual inductor currents from their respective pair. The result of the analysis provided a linear equation for the current derivatives for each mutual inductor, which allowed the system to be put into state space form.

B. COMPUTING INITIAL CURRENT

Before computing the average power flow, the average current through the transformer inductors must equal zero. Typically, this means that at steady-state, the current values at the start of a switching cycle are non-zero. To determine the correct initial current values, begin with zero initial current within all inductors, and then compute the final current values after the third switched state (halfway through the switching cycle). The initial current is equal to: $i(0) = -\frac{1}{2}i(\frac{T_s}{2})$.

As the system is in state-space form, the linear derivatives of currents are known. The change in current during a state is equal to the following equation where φ is the fraction of the total switching cycle that the state is active:

$$\Delta i = \frac{di}{dt}\varphi T_s \quad (28)$$

All switching signals have a 50% duty cycle, the converter will be exactly halfway through a switching cycle after three states.

Once the steady-state initial current values are known, the current waveform for an entire cycle can be computed by applying (28) for each of the six states. Since there are six states, there will be six intervals to compute the change in current. The current value at the end of each state can be computed with (29):

$$i_{Lx}\left(t_{fn}\right) = \Delta i_{Lx} + i_{Lx}\left(t_{in}\right) \quad (29)$$

Where x represents the port number, t_{fn} is the final time at the end of state n, and $i_{Lx}(0)$ is the initial current at the beginning of state n.

Computing Average Power Flow

The voltage during a state is assumed to remain constant. The current changes in a linear trajectory. Therefore, the average power flow at a port during a single state is equal to

$$P_{xn} = v_x\frac{\left(i_x\left(0\right) + i_x\left(t_{fn}\right)\right)}{2} \quad (30)$$

Where x represents the port number and t_{fn} is the final time at the end of state n. Recall that the current i_x is equivalent to the current flowing through the transformer winding at that port i_{Lx}. The MV voltages can be computed from (9) and (10), and the primary port voltage is already known. Since the transformer leakage inductor currents are states, the initial and final current at each state can easily be computed using the state space matrices using the method described in (28). The average power flow through the converter during an entire

TABLE 1. Operating Modes of the CF3P-DAB Converter

Mode	Operating Range
1	$0 < \phi_2 < \phi_3$
2	$0 < \phi_3 < \phi_2$
3	$\phi_3 < \phi_2 < 0$
4	$\phi_2 < \phi_3 < 0$
5	$\phi_2 < 0 < \phi_3$ $\phi_3 - \phi_2 < 0.5$
6	$\phi_2 < 0 < \phi_3$ $\phi_3 - \phi_2 > 0.5$
7	$\phi_3 < 0 < \phi_2$ $\phi_2 - \phi_3 < 0.5$
8	$\phi_3 < 0 < \phi_2$ $\phi_2 - \phi_3 > 0.5$

switching cycle can be computed by:

$$P_{xavg} = \sum_{n=1}^{6} P_{xn}\varphi_{xn} \tag{31}$$

Where P_{xn} is the average power at port x during state n, and φ_{xn} is the fraction of the total switching cycle that state n occurs. The phase shift φ can be converted to radians by multiplying by 2π.

C. AVERAGE POWER FLOW ACROSS ALL MODES

The average power flow was computed for the entire operating range of the converter ($-0.5 < \varphi_2 \leq 0.5$ and $-0.5 < \varphi_3 \leq 0.5$). A key feature to note is that the power flow equations are unique to the sequence of the switches. There are eight possible switching sequences, and each sequence will be called a 'mode' of the converter. See Table 1 for the list of possible operating modes of the converter. The resulting power flow equations for the first five modes are as follows:

MODE 1 : $0 < \phi_2 < \phi_3$

$$P_1 \approx L_1^{-1}L_\alpha^{-1}\left\{T_s n_1 V_1\left[L_2 L_{3\alpha} n_2 V_{Carm2-0}\left(-2\,\phi_2^2+\phi_2\right)+L_{2\alpha}L_3 n_3 V_{Carm3-0}\left(-2\phi_3^2+\phi_3\right)\right]\right\} \tag{32}$$

$$P_2 \approx L_\alpha^{-1}\left\{T_s n_2 V_{Carm2-0}\left[-2\left(L_{3\alpha}n_1V_1 - L_3 n_3 V_{Carm3-0}\right)\phi_2^2 + \left(L_{3\alpha}n_1V_1 + L_3 n_3 V_{Carm3-0}\right)\phi_2 + L_3 n_3 V_{Carm3-0}\left(2\phi_3^2-\phi_3\right) - 4L_3 n_3 V_{Carm3-0}\phi_2\phi_3\right]\right\} \tag{33}$$

$$P_3 \approx L_\alpha^{-1}\left\{T_s n_3 V_{Carm3-0}\left[L_2 n_2 V_{Carm2-0}\left(-2\phi_2^2-\phi_2\right) + \left(L_{2\alpha}n_1V_1 + L_2 n_2 v_{Carm2-0}\right)\left(-2\phi_3^2+\phi_3\right) + 4L_2 n_2 V_{Carm2-0}\phi_2\phi_3\right]\right\} \tag{34}$$

Where,

$$L_\alpha = (L_{dc}-M)^2 n_1^2 + L_2L_3\left(n_1^2+n_2^2+n_3^2\right) + (L_{dc}-M)\left(L_2n_1^2 + L_2n_2^2 + L_3n_1^2 + L_3n_3^2\right) \tag{35}$$

MODE 2 : $0 < \phi_3 < \phi_2$

$$P_1 \approx L_1^{-1}L_\alpha^{-1}\left\{T_s n_1 V_1\left[L_2 L_{3\alpha} n_2 V_{Carm2-0}\left(-2\,\phi_2^2+\phi_2\right)+L_{2\alpha}L_3 n_3 V_{Carm3-0}\left(-2\phi_3^2+\phi_3\right)\right]\right\} \tag{36}$$

$$P_2 \approx L_\alpha^{-1}\left\{T_s n_2 V_{Carm2-0}\left[\left(L_{3\alpha}n_1V_1 + L_3 n_3 V_{Carm3-0}\right)\left(-2\phi_2^2+\phi_2\right) - L_3 n_3 V_{Carm3-0}\left(2\phi_3^2+\phi_3\right) + 4L_3 n_3 V_{Carm3-0}\phi_2\phi_3\right]\right\} \tag{37}$$

$$P_3 \approx L_\alpha^{-1}\left\{T_s n_3 V_{Carm3-0}\left[L_2 n_2 V_{Carm2-0}\left(2\phi_2^2-\phi_2\right) - 2\left(L_{2\alpha}n_1V_1 - L_2 n_2 v_{Carm2-0}\right)\phi_3^2 + \left(L_{2\alpha}n_1V_1 + L_2 n_2 v_{Carm2-0}\right)\phi_3 - 4L_2 n_2 V_{Carm2-0}\phi_2\phi_3\right]\right\} \tag{38}$$

MODE 3 : $\phi_3 < \phi_2 < 0$

$$P_1 \approx L_1^{-1}L_\alpha^{-1}\left\{T_s n_1 V_1\left[L_2 L_{3\alpha} n_2 V_{Carm2-0}\left(2\,\phi_2^2+\phi_2\right)+L_{2\alpha}L_3 n_3 V_{Carm3-0}\left(2\phi_3^2+\phi_3\right)\right]\right\} \tag{39}$$

$$P_2 \approx L_\alpha^{-1}\left\{T_s n_2 V_{Carm2-0}\left[2\left(L_{3\alpha}n_1V_1 - L_3 n_3 V_{Carm3-0}\right)\phi_2^2 + \left(L_{3\alpha}n_1V_1 + L_3 n_3 V_{Carm3-0}\right)\phi_2 + L_3 n_3 V_{Carm3-0}\left(-2\phi_3^2-\phi_3\right) + 4L_3 n_3 V_{Carm3-0}\phi_2\phi_3\right]\right\} \tag{40}$$

$$P_3 \approx L_\alpha^{-1}\left\{T_s n_3 V_{Carm3-0}\left[L_2 n_2 V_{Carm2-0}\left(2\phi_2^2-\phi_2\right) + \left(L_{2\alpha}n_1V_1 + L_2 n_2 v_{Carm2-0}\right)\left(2\phi_3^2+\phi_3\right) - 4L_2 n_2 V_{Carm2-0}\phi_2\phi_3\right]\right\} \tag{41}$$

MODE 4 : $\phi_2 < \phi_3 < 0$

$$P_1 \approx L_1^{-1}L_\alpha^{-1}\left\{T_s n_1 V_1\left[L_2 L_{3\alpha} n_2 V_{Carm2-0}\left(2\,\phi_2^2+\phi_2\right)+L_{2\alpha}L_3 n_3 V_{Carm3-0}\left(2\phi_3^2+\phi_3\right)\right]\right\} \tag{42}$$

$$P_2 \approx L_\alpha^{-1}\left\{T_s n_2 V_{Carm2-0}\left[\left(L_{3\alpha}n_1V_1 + L_3 n_3 V_{Carm3-0}\right)\left(2\phi_2^2+\phi_2\right) + L_3 n_3 V_{Carm3-0}\left(2\phi_3^2-\phi_3\right) - 4L_3 n_3 V_{Carm3-0}\phi_2\phi_3\right]\right\} \tag{43}$$

$$P_3 \approx L_\alpha^{-1}\left\{T_s n_3 V_{Carm3-0}\left[L_2 n_2 V_{Carm2-0}\left(-2\phi_2^2-\phi_2\right) + 2\left(L_{2\alpha}n_1V_1 - L_2 n_2 v_{Carm2-0}\right)\phi_3^2 + \left(L_{2\alpha}n_1V_1 + L_2 n_2 v_{Carm2-0}\right)\phi_3 + 4L_2 n_2 V_{Carm2-0}\phi_2\phi_3\right]\right\} \tag{44}$$

MODE 5 : $\phi_2 < 0 < \phi_3$; $\phi_3 - \phi_2 < 0.5$

$$P_1 \approx L_1^{-1}L_\alpha^{-1}\left\{T_s n_1 V_1\left[L_2 L_{3\alpha} n_2 V_{Carm2-0}\left(2\,\phi_2^2+\phi_2\right)+L_{2\alpha}L_3 n_3 V_{Carm3-0}\left(-2\phi_3^2+\phi_3\right)\right]\right\} \tag{45}$$

$$P_2 \approx L_\alpha^{-1}\left\{T_s n_2 V_{Carm2-0}\left[\left(L_{3\alpha}n_1V_1 + L_3 n_3 V_{Carm3-0}\right)\left(2\phi_2^2+\phi_2\right) + L_3 n_3 V_{Carm3-0}\left(2\phi_3^2-\phi_3\right) - 4L_3 n_3 V_{Carm3-0}\phi_2\phi_3\right]\right\} \tag{46}$$

$$P_3 \approx L_\alpha^{-1}\left\{T_s n_3 V_{Carm3-0}\left[L_2 n_2 V_{Carm2-0}\left(-2\phi_2^2-\phi_2\right)\right.$$

TABLE 2. CFTAB Converter Circuit Parameters

Variable	Parameter	Value
n_1	Primary Turns Ratio	1
n_2	Secondary Turns Ratio	1
n_3	Tertiary Turns Ratio	1
L_1	Primary Winding Inductance	800µH
L_2	Secondary Winding Inductance	800µH
L_3	Tertiary Winding Inductance	800µH
L_{dc}	Coupled Inductor Inductance	4.0mH
M	Mutual Inductance	3.2mH
f_s	Switching Frequency	1.0kHz
D_1	Primary Duty Cycle	0.5
D_2	Secondary Duty Cycle	0.5
D_3	Tertiary Duty Cycle	0.5
V_1	Primary DC Voltage	500V
V_{2DC}	Secondary DC Voltage	500V
V_{3DC}	Tertiary DC Voltage	500V
V_{arm2}	Secondary Arm Voltage	500V
V_{arm3}	Tertiary Arm Voltage	500V
T_s	Switching Period	1.0ms

$$+ (L_{2\alpha} n_1 V_1 + L_2 n_2 v_{Carm2-0}) \left(-2\phi_3^2 + \phi_3\right) + 4 L_2 n_2 V_{Carm2-0} \phi_2 \phi_3 \Big]\Big\} \quad (47)$$

Table 2 provides the circuit design parameters for the CFTAB converter, as mentioned. These parameters are based on the design parameters of a previous analysis and are similar to analyses on other multi-port structures [13], [21]. One key feature to note is that the switching frequency of the design has been slowed down from 40kHz to 1kHz to account for performance restrictions within the TI controller and real-time digital simulator (discussed in Section V). To achieve similar output power of the converter, the inductance values are increased by a factor of 40 from the reference design. Note that this limitation of the experimental setup is not in itself a limitation of the speed of the proposed control or converter.

The circuit component values in Table 2 were substituted into (32)–(47) and the resulting power output waveforms at each port are plotted in Fig. 5 for the full switching range for $-0.5 \leq \phi_2 \leq 0.5$ and $-0.5 \leq \phi_3 \leq 0.5$. The eight different modes are colored separately in the graphs to clearly show each mode. A key feature to note is that the power output at a port x trends from negative to positive for the range $-0.25 \leq \phi_x \leq 0.25$, regardless of the phase shift at the other port. This linear behavior is used in typical control strategies to independently control each port by increasing its phase shift to increase power flow to that port, and vice versa. A key result of any change in phase shift, however, is a clear change in power output at both ports. For example, if an increase at port 2 power flow is desired and ϕ_2 is increased accordingly, the power output at port 3 will certainly change as a result. The following section of this article will describe a method of adjusting the power output at one port without affecting the power output at the other port. As a reminder, the power output at port 1 is simply equal to the sum of the power flow to ports 2 and 3 as described in (2). Therefore, the power output at port 1 is also controlled by manipulating ϕ_2 and ϕ_3.

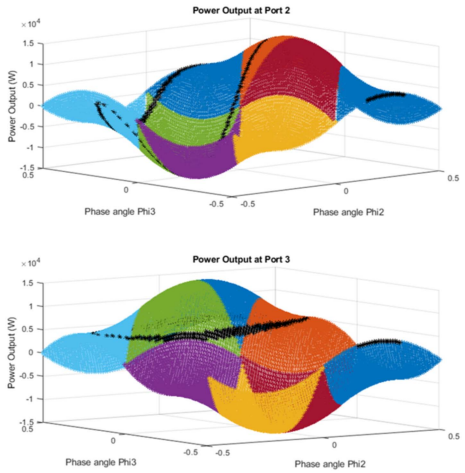

FIGURE 4. Power output at port 2 across the entire operating range ($-0.5 \leq \phi_2 \leq 0.5$ and $-0.5 \leq \phi_3 \leq 0.5$) (top) and power output at port 3 across the entire operating range (bottom).

Ports 2 and 3 power output with 5 kW power reference at port 3. Valid operating points that output 5 kW at port 3 are highlighted in dark black. Note that at port 2, the power output can equal zero near the origin with power output increasing or decreasing according to the phase angle ϕ_2.

IV. AVERAGE POWER FLOW CASE STUDY–CONSTANT 5 KW POWER OUTPUT AT PORT 3

Deriving the power flow equations makes it possible to compute the valid operating points of (ϕ_2, ϕ_3) that will deliver a constant power output at one of the ports. Then, a trajectory of these operating points can be discovered to allow the other port to adjust power flow while maintaining constant power at the original port. To demonstrate this concept, a case study will be explored using the parameters in Table 2 for a constant 5 kW load at port 3.

In Fig. 4, the highlighted operating points (dark black) are in a flat plane at 5 kW for port 3 output power while the trajectory of port 2 output power can range from approximately −10 kW to 10 kW. It can also be noted that the control strategy can be simplified further by restricting the operating points to $-0.25 \leq \phi_2 \leq 0.25$ and $-0.25 \leq \phi_3 \leq 0.25$ to force proportional control. This means the power output at port 2 increases as the phase angle ϕ_2 is increased (and vice versa), which makes standard feedback control well-suited to regulating the power output at Port 2 by regulating ϕ_2. The phase shift ϕ_3 can then be computed from ϕ_2 to achieve a constant 5 kW power output at port 3.

V. CONTROL HARDWARE-IN-THE-LOOP EXPERIMENTAL RESULTS

For the case study, port 3 was treated as a constant power load of 5 kW. The decoupled control strategy that will be described

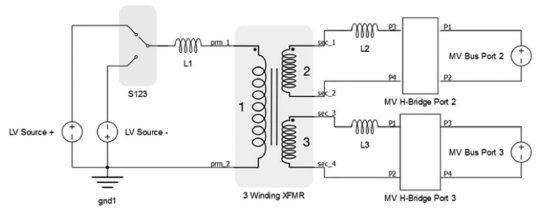

FIGURE 5. Typhoon HIL model of a 3-bus network (LV-MV-MV) with 3-port interfacing converter.

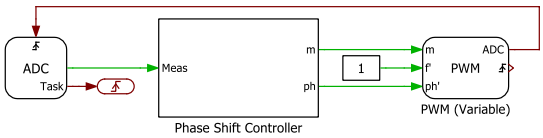

FIGURE 6. PLECS phase-shift controller using TI C2000 target blocks. The ADC block is the analog power flow measurements coming from the Typhoon HIL simulation. The digital out blocks are switching signals sent back to the simulation.

below allows the power at port 2 to swing between 0W and upwards of 7 kW. To confirm that the proposed control strategy was viable, a Typhoon HIL 402 real time digital simulator was used to emulate the converter and grid behavior in real time. The converter control was installed onto a TI 28379 controller. A Typhoon DSP180 interface was used to connect the controller input and output signals to the Typhoon HIL 402. This control hardware-in-the-loop (CHIL) experiment successfully demonstrated steady-state stability of the simulated converter when using the external controller.

A. TYPHOON HIL SCHEMATIC AND SCADA PANEL

The circuit topology in Fig. 2 was designed within Typhoon HIL's schematic editor. The Typhoon model is shown in Fig. 5. The component values are selected per the converter parameters in Table 2.

The MV H-Bridge ports contain the switches and mutual inductor pairs according to Fig. 2. The switches are set within the Typhoon HIL simulation software to be controlled by an external digital signal produced by the TI 28379 controller. In the SCADA system the values of P_2 and P_3 are set as analog output reference signals to the controller.

B. TEXAS INSTRUMENTS CONTROLLER

The controller is programmed by flashing PLECS control blocks onto the controller using the coder compiler software package for rapid controller prototyping. The PLECS control blocks are shown in Figs. 6 through 8.

Fig. 6 is the overall control system that receives analog inputs from the Typhoon HIL simulation and uses those signals to generate the phase shift control strategy. The result of the control is 6 digital output signals (2 square wave forms per port) that are sent to the switches at each port. Looking into the phase shift controller block gives Fig. 7.

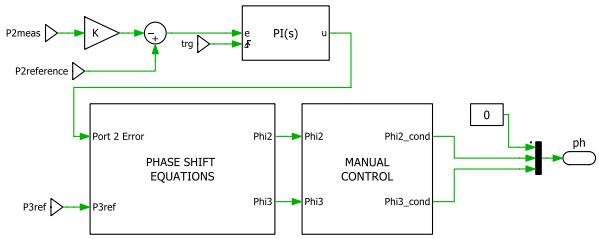

FIGURE 7. Control logic for phase-shift control. Measured power flow at each port is compared to the desired reference. The error signals are used as an input to the phase shift equations. The output modulation signals are then used to generate the gate switching signals.

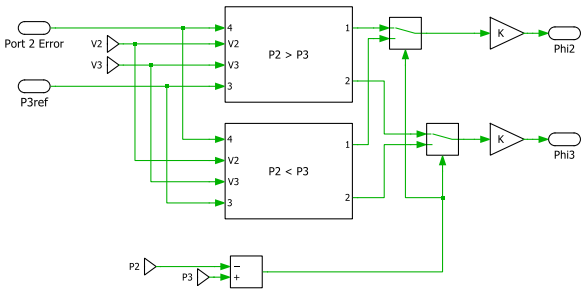

FIGURE 8. Control blocks for tracking the voltage reference at port 2 and the power reference at port 3. There are two separate control laws depending on if P2 > P3 or P2 < P3, and the proper phase shift values are selected by comparing the measured values of P2 and P3.

Fig. 7 compares the reference values set by the user in Typhoon HIL SCADA to the average power output of the Typhoon HIL simulation. The error signals are then passed into a phase shift equations subsystem, which generates modulation values for the secondary and tertiary ports. The modulation signals are passed into standard phase shift PWM blocks, which uses a triangular carrier wave and waveform crossing detection to generate the switching signals for the primary, secondary, and tertiary ports of the converter. Fig. 8 shows the details of the phase shift equations block. ϕ_3 is generated from the value of ϕ_2 while in mode 2. A similar derivation and control law is applied for mode 1.

The controller receives a power reference signal for each port, as well as the measured power signal output from the Typhoon HIL simulation. The controller takes the difference of P_3 from the reference value to determine which equation to use. In this case study, if $P_3 < 5kW$, then the control will attempt to output a higher power (7 kW) until 5 kW is reached. Likewise, if $P_3 > 5kW$, the control will output a lower power (3 kW) until 5 kW is reached. Note that this control was limited to only unidirectional power flow. However, the control can be extended to the full range of operation using the computed power flow equations in (32)–(47). Also, this control strategy can be adapted to instead control the bus voltage or to control the output current at a port instead of the average power.

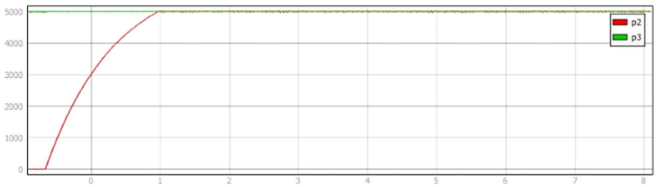

FIGURE 9. Simulated CFTAB power output waveforms at ports 2 and 3 as the load for port 2 changes from 0 kW to 5 kW. Note that port 3 power (P3) remains unaffected by the load change at port 2.

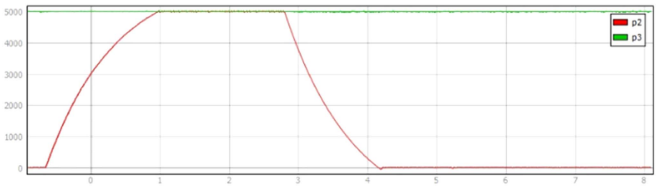

FIGURE 10. Quick turn-on then turn-off of the load at port 2.

C. REAL-TIME DIGITAL SIMULATOR EXPERIMENTAL RESULTS

The results of the C-HIL experiment are shown in Figs. 9 and 10. The primary source feeds a continuous 5 kW to the constant power load at port 3. Initally, port 2 is disabled. When a 5 kW demand is activated at port 2, the power output at port 3 remains unaffected. Fig. 10 is provided to 1) verify stable steady-state operation, 2) verify transient load conditions at port 2 do not affect the power flow at port 3 and 3) stable steady-state operation.

VI. TRIPLE ACTIVE BRIDGE CONVERTER TEST BED EXPERIMENTAL RESULTS

A. CONTROL CARD SETUP

The PLECS controller described in Section V was downloaded to a Texas Instruments F28335 control card using a USB probe interface and the PLECS TI C2000 blockset. The F28335 controller was interfaced with the converter via a TMS320F28335 evaluation board. Digital outputs and analog inputs were buffered using op amps to introduce high impedance between the control card and the converter. This prevents common mode noise generated by the converter from affecting the F28335 control card. The USB probe interface allowed continuous communication between the F28335 control card and the PC through the PLECS coder external mode.

B. TEST BED PARAMETERS AND EXPERIMENTAL SETUP

The proposed controller's performance was validated by using a triple active bridge converter test bed. The converter components are rated for 1kV and 50 kW using 1200V CREE SiC MOSFET half bridges as the switching devices. However, due to infrastructure limitations of the power supply and loads of the test bed, a 150V, 1 kW test was implemented for validation of the control. The effects of this de-rated test will be discussed in section C. The TAB converter parameters are given

TABLE 3. TAB Converter Circuit Parameters

Variable	Parameter	Value
V_{1DC}	Primary DC Voltage	150V
V_{2DC}	Secondary DC Voltage	75V
V_{3DC}	Tertiary DC Voltage	50V
n_1	Primary Turns Ratio	12
n_2	Secondary Turns Ratio	9
n_3	Tertiary Turns Ratio	15
L_1	Primary Winding Inductance	44µH
L_2	Secondary Winding Inductance	44µH
L_3	Tertiary Winding Inductance	72µH
f_s	Switching Frequency	10kHz
D_1, D_2, D_3	Switching Duty Cycles	0.5
R_{Load2}	Secondary Load	13.7Ω
R_{Load3}	Tertiary Load	8.0Ω

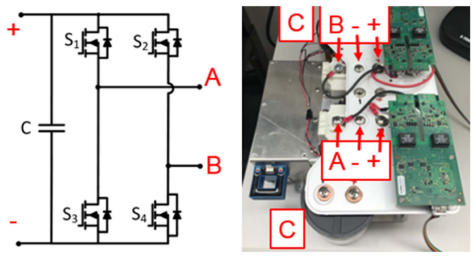

FIGURE 11. Single H-bridge schematic (left) and physical layout with SiC modules and mounted gate driver boards (right).

in Table 3, and further information about the TAB converter test bed can be found in [29].

One key difference between the TAB converter within the existing test bed and the current-fed TAB converter discussed in earlier sections is the absence of the mutual inductor pairs at the current-fed ports. As a result, the proposed controller was re-derived using the techniques mentioned in Sections III and IV—this time for a voltage-fed TAB converter topology. The successful implementation of the proposed controller highlights the controller's flexibility for use within voltage-fed 3-port converter topologies in addition to the original current-fed design.

The test bed setup is shown in Figs. 11 and 12. Fig. 11 is a picture of an individual H-bridge module. The bus capacitors are connected to the SiC half bridges through a bus plane. The gate drivers are mounted directly above the MOSFETs. The entire assembly is mounted to a heat sink. Each H-bridge module is mounted to the chassis and is labeled by port number in the figure. Port 1 is the input port and ports 2 and 3 are the load ports. The 3 winding transformer is mounted at the top, and external series inductors are connected to give the inductance values in Table 3. A block diagram showing the connection between the control and the hardware test bed is found in Fig. 13.

C. EXPERIMENTAL RESULTS AND DISCUSSION

After evaluating the ac waveforms of the converter, the steady-state stability of the dc bus voltages were confirmed. Also, the

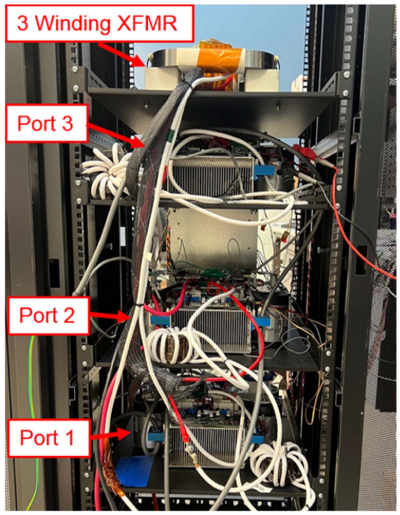

FIGURE 12. Triple active bridge converter test bed.

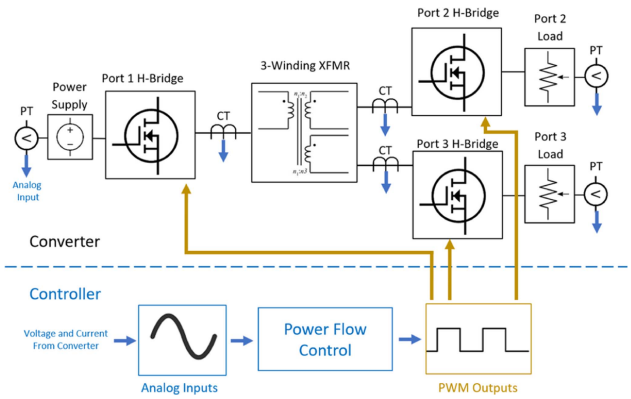

FIGURE 13. Block diagram of control and hardware testbed.

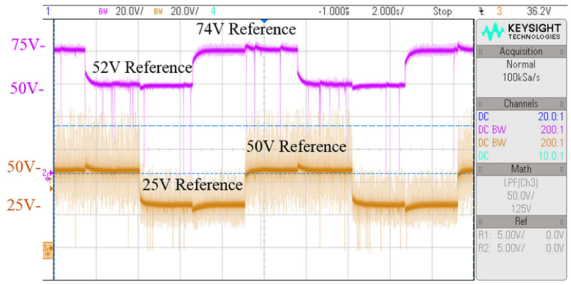

FIGURE 14. Voltage reference changes for port 2 DC bus voltage (purple) and port 3 DC bus voltage (orange) with PI controller on both ports 2 and 3 (reference case). Port 2 shows the transition between a 200 W reference and 400 W reference while port 3 shows the transition between a 25 V reference and 50 V reference.

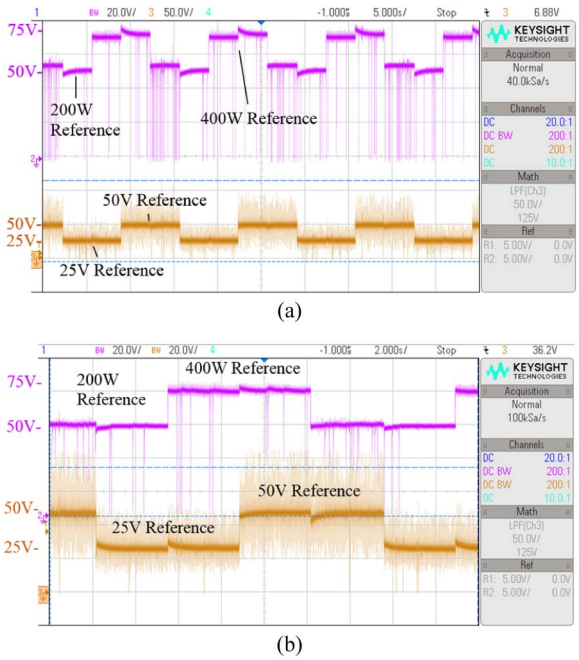

FIGURE 15. Port 2 power flow control before tuning (a) and after tuning (b). Port 2 DC bus voltage (purple) and port 3 DC bus voltage (orange) with proposed power flow controller on port 2 and PI controller on port 3. Port 2 shows the transition between a 200 W reference and 400 W reference (with a resistive load) while port 3 shows the transition between a 25 V reference and 50 V reference.

transient behavior of the dc bus voltages were studied. The converter was operated with a traditional PI controller as a reference, and then operated again with the proposed power flow controller.

Fig. 14 shows the results of PI dc bus voltage regulation at ports 2 and 3. The PI control was tuned to have a critically damped response with no overshoot. The figure shows port 2 tracking a 52V reference (200W) with a reference transition to 74V (400W) and port 3 tracking a 25V reference with a reference transition to 50V. The settling times during a voltage reference change can be seen in Fig. 14. The settling time for port 2 is approximately 125 ms during a voltage reference change at port 2 and approximately 500 ms during a voltage reference step change at port 3. Likewise, the setting time for port 3 is approximately 125 ms during a voltage reference change at port 3 and approximately 500 ms during a voltage reference change at port 2.

Fig. 15 shows the results of the power flow controller at port 2 with a PI controller at port 3. Fig. 15 shows port 2 tracking a 200W reference with a reference transition to 400W and port 3 tracking a 25V reference with a reference transition to 50V. The voltage references were continually changed in this experiment since part of the motivation for developing the power flow control strategy was to operate during varying bus voltages. One thing to note is the transient voltage drops in the dc bus voltage waveforms. This is a disturbance caused by the converter operation and not due to the control. In future work, ringing at the load ports for the test bed will need to be suppressed to prevent this transient discharging of the dc bus capacitors.

Fig. 15 demonstrates stable operation of the power flow controller at port 2. Port 2 was selected instead of port 3 for

the power flow controller because, due to its lower inductance, port 2 was more susceptible to experiencing coupled transients due to a load change at port 3. One key requirement for correctly tracking the power reference at port 2 is to have exact parameter information for the inductance values of the transformer. If not, the output power at port 2 will not accurately track the power reference. Fig. 15(a) shows the performance of the controller using the inductance values from Table 3, before tuning. Note how the steady-state bus voltage at port 2 changes with the bus voltage at port 3. Fig. 15(b) shows the performance of the controller after manually tuning the inductance values within the control until the power reference was properly tracked at port 2, regardless of the bus voltage at port 3. Finally, after tuning the control, an outer PI control loop was added to increase/decrease the input into the controller if the measured power output deviated from the reference. The settling times for port 2 in Fig. 15 are approximately 20 ms during a voltage reference change at port 2 and approximately 500 ms during a voltage reference change at port 3. Likewise, the settling times for port 3 in Fig. 15 are approximately 20 ms during a voltage reference change at port 3 and approximatly 500 ms during a voltage reference change at port 2. This applies to both Fig. 15(a) and (b). Referring back to the purely PI control in Fig. 14, this is an improvement of the $\sim$125 ms settling time at a port when a port undergoes a voltage reference change.

While the real-time experiment in Section V was able to both demonstrate stable operation of the controller as well as compensation to eliminate voltage disturbances, a key gap in this test bed experiment for Section VI is the inability to implement a large enough load change to create a voltage disturbance. This scenario requires a power supply and loads rated for the 50 kW converter. However, despite not being able to generate a significant voltage sag during a load change, the stability of the power flow controller can still be confirmed when comparing Figs. 14 and 15. The proposed power flow controller in Fig. 15 achieves similar steady-state performance to the PI controller in Fig. 14.

VII. CONCLUSION

This experiment successfully employed a control strategy for a current-fed triple active bridge converter that prevents disturbances at a load port from disturbing the power flow at the second load port. By computing the relationships between the phase angles ϕ_2 and ϕ_3 and the port power outputs P_2 and P_3, the power output at port 2 was able to be freely controlled by ϕ_2 while ϕ_3 was used to maintain a constant power output at port 3. The procedure was presented in such a way that the process for deriving the control relationships can be replicated for the CFTAB converter topology, enabling a pathway for further advanced magnetics within the multi-port converter. The controller was validated at the MV scale using real-time digital simulation and at a low voltage and power scale with a triple active bridge converter test bed.

REFERENCES

[1] R. A. Walling, R. Saint, R. C. Dugan, J. Burke, and L. A. Kojovic, "Summary of distributed resources impact on power delivery systems," *IEEE Trans. Power Del.*, vol. 23, no. 3, pp. 1636–1644, Jul. 2008.

[2] Q. Ye, R. Mo, and H. Li, "Stability analysis and improvement of a dual active bridge (DAB) converter enabled DC microgrid based on a reduced-order low frequency model," in *Proc. IEEE Energy Convers. Congr. Expo.*, 2016, pp. 1–7.

[3] X. Zhang, X. Ruan, and C. K. Tse, "Impedance-based local stability criterion for DC distributed power systems," *IEEE Trans. Circuits Syst. I: Regular Papers*, vol. 62, no. 3, pp. 916–925, Mar. 2015.

[4] F. Chen, R. Burgos, and D. Boroyevich, "A bidirectional high-efficiency transformerless converter with common-mode decoupling for the interconnection of AC and DC grids," *IEEE Trans. Power Electron.*, vol. 34, no. 2, pp. 1317–1333, Feb. 2019.

[5] A. Alfares, E. Afshari, M. Amirabadi, and B. Lehman, "A modular SCR-based DC-DC converter for medium-voltage direct-current (MVDC) grid applications," in *Proc. IEEE Energy Convers. Congr. Expo.*, 2017, pp. 5170–5177.

[6] K. Vechalapu, S. Bhattacharya, E. Van Brunt, S.-H. Ryu, D. Grider, and J. W. Palmour, "Comparative evaluation of 15-kV SiC MOSFET and 15-kV SiC IGBT for medium-voltage converter under the same DV/DT conditions," *IEEE J. Emerg. Sel. Topics Power Electron.*, vol. 5, no. 1, pp. 469–489, Mar. 2017.

[7] D. Krug, S. Bernet, and S. Dieckerhoff, "Comparison of state-of-the-art voltage source converter topologies for medium voltage applications," in *Proc. 38th IAS Annu. Meeting Conf. Rec. Ind. Appl. Conf.*, 2003, vol. 1, pp. 168–175.

[8] R. W. De Doncker, "Power electronic technologies for flexible DC distribution grids," in *Proc. Int. Power Electron. Conf. Energy Convers. Congr. Expo. Asia*, 2014, pp. 736–743.

[9] N. C. Foureaux, B. J. C. Filho, and J. A. S. Brito, "Cascaded multilevel SST medium voltage converter for solar applications," in *Proc. 9th Int. Conf. Power Electron. Energy Convers. Congr. Expo. Asia*, 2015, pp. 801–808.

[10] C. Dincan, P. Kjaer, Y. Chen, S. Munk-Nielsen, and C. L. Bak, "A high-power, medium-voltage, series-resonant converter for DC wind turbines," *IEEE Trans. Power Electron.*, vol. 33, no. 9, pp. 7455–7465, Sep. 2018.

[11] F. Mura and R. W. De Doncker, "Design aspects of a medium-voltage direct current (MVDC) grid for a university campus," in *Proc. 8th Int. Conf. Power Electron. Energy Convers. Congr. Expo. Asia*, 2011, pp. 2359–2366.

[12] M. Michon, J. L. Duarte, M. Hendrix, and M. G. Simoes, "A three-port bi-directional converter for hybrid fuel cell systems," in *Proc. IEEE 35th Annu. Power Electron. Specialists Conf.*, 2004, vol. 6, pp. 4736–4742.

[13] C. Zhao, S. D. Round, and J. W. Kolar, "An isolated three-port bidirectional DC–DC converter with decoupled power flow management," *IEEE Trans. Power Electron.*, vol. 23, no. 5, pp. 2443–2453, Sep. 2008.

[14] H. Tao, J. L. Duarte, and M. A. M. Hendrix, "High-power three-port three-phase bidirectional DC-DC converter," in *Proc. IEEE Ind. Appl. Annu. Meeting*, 2007, pp. 2022–2029.

[15] R. W. De Doncker, D. M. Divan, and M. H. Kheraluwala, "A three-phase soft-switched high power density DC/DC converter for high power applications," in *Proc. Conf. Rec. IEEE Ind. Appl. Soc. Annu. Meeting*, 1988, vol. 1, pp. 796–805.

[16] P. Cairoli, R. Rodrigues, and H. Zheng, "Fault current limiting power converters for protection of DC microgrids," in *Proc. IEEE SoutheastCon*, 2017, pp. 1–7.

[17] S. Falcones, R. Ayyanar, and X. Mao, "A DC–DC multiport-converter-based solid-state transformer integrating distributed generation and storage," *IEEE Trans. Power Electron.*, vol. 28, no. 5, pp. 2192–2203, May 2013.

[18] P. Marcin, Z. Krzysztof, Z. Zbigniew, and G. Maciej, "3-terminal high power medium voltage grid coupling converter," in *Proc. 9th Int. Conf. Compat. Power Electron.*, 2015, pp. 340–345.

[19] H. Tao, A. Kotsopoulos, J. L. Duarte, and M. A. M. Hendrix, "Transformer-coupled multiport ZVS bidirectional DC–DC converter with wide input range," *IEEE Trans. Power Electron.*, vol. 23, no. 2, pp. 771–781, Mar. 2008.

[20] Y. Shi and H. Li, "A novel modular dual-active-bridge (MDAB) DC-DC converter with DC fault ride-through capability for battery energy storage systems," in *Proc. IEEE Energy Convers. Congr. Expo.*, 2016, pp. 1–6.
[21] Z. T. Smith and B. M. Grainger, "Analytical treatment of the power transfer relationships for a coupled, current-fed, multi-port dual active bridge converter," in *Proc. IEEE Elect. Ship Technol. Symp.*, 2019, pp. 562–568.
[22] A. C. Nair and B. G. Fernandes, "A novel multi-port solid state transformer enabled isolated hybrid microgrid architecture," in *Proc. IECON 43rd Annu. Conf. IEEE Ind. Electron. Soc.*, 2017, pp. 651–656.
[23] S. Kurm and V. Agarwal, "Novel dual active bridge based multi port converter for interfacing hybrid energy storage systems in electric vehicles," in *Proc. IEEE Transp. Electrific. Conf.*, 2019, pp. 1–5.
[24] P. Xuewei and A. K. Rathore, "Comparison of bi-directional voltage-fed and current-fed dual active bridge isolated DC/DC converters low voltage high current applications," in *Proc. IEEE 23rd Int. Symp. Ind. Electron.*, 2014, pp. 2566–2571.
[25] B. Zhao, Q. Song, W. Liu, and Y. Sun, "Overview of dual-active-bridge isolated bidirectional DC–DC converter for high-frequency-link power-conversion system," *IEEE Trans. Power Electron.*, vol. 29, no. 8, pp. 4091–4106, Aug. 2014.
[26] R. J. G. Montoya, A. Mallela, and J. C. Balda, "An evaluation of selected solid-state transformer topologies for electric distribution systems," in *Proc. IEEE Appl. Power Electron. Conf. Expo.*, 2015, pp. 1022–1029.
[27] H. Tao, A. Kotsopoulos, J. Duarte, and M. Hendrix, "Family of multiport bidirectional DC-DC converters," *IEE Proc. Elect. Power Appl.*, vol. 153, no. 3, pp. 451–458, 2006, doi: 10.1049/ip-epa:20050362.
[28] Y. Shi and H. Li, "Isolated modular multilevel DC–DC converter with DC fault current control capability based on current-fed dual active bridge for MVDC application," *IEEE Trans. Power Electron.*, vol. 33, no. 3, pp. 2145–2161, Mar. 2018.
[29] P. R. Ohodnicki, "Final technical report DE-EE00031004 combined PV/battery grid integration with high frequency magnetics enabled power electronics," NETL, pp. 1–50, 2019. Accessed: May 16, 2022. [Online]. Available: https://netl.doe.gov/projects/files/CombinedPVBatteryGridIntegrationwithHighFrequencyMagneticsEnabledPowerElectronics_031620.pdf