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HERIC-Clamped and PN-NPC Inverters With Five-Level Output Voltage and Reduced Grid-Interfaced Filter Size

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ABSTRACT Transformerless grid-connected inverters with highly efficient and reliable inverter concept (HERIC) and positive-negative neutral point-clamped (PN-NPC) circuit configurations exhibit excellent performance in terms of overall efficiency, common-mode voltage, and alleviated leakage current concern. These inverters are designed to generate only a three-level (3L) output voltage waveform, thereby reducing the power density of a conversion system. On the other hand, it is well-known that increasing the inverter output voltage levels entails the reduction of the output filter size. In this regard, this article aims to develop a five-level (5L) inverter output voltage for the improved versions of HERIC-clamped and original PN-NPC inverters. This is achieved with either phase-shifted or level-shifted pulse width modulation technique leading to further quality improvement of ac voltage and current waveforms through increasing the number of output voltage levels. Therefore, a much smaller output filter size can be utilized, while the overall efficiency of the entire system is enhanced. Two laboratory-built SiC-based prototypes for both the proposed HERIC-clamped (1.8 kW) and PN-NPC-5L (2 kW) inverters have been fabricated to show the feasibility and effectiveness of the proposed solution via experiments.

INDEX TERMS HERIC-clamped inverter, multilevel inverters, PN-NPC inverter, pulse width modulation (PWM).

I. INTRODUCTION

Power electronic inverters with high-efficiency/high-power density performance have attracted increasing attention during the latest decade in many industrial and domestic applications such as grid-connected photovoltaic (PV) systems, motor drives, and electric vehicles [1], [2]. Reduced voltage stress across the semiconductor devices, improved modulation, and reduced/mitigated value of the high-frequency common-mode voltage (HF-CMV) and leakage current are the most important factors for these types of converters to possess high overall efficiency [2]. Removing/detaching the galvanic transformer and increasing the number of inverter output voltage levels can also help to achieve a high-power density design by reducing the weight and size of the output filters in grid-connected inverters [3].

Considering the above, transformerless grid-tied PV systems are counted as an efficient, compact, and popular solution during the latest years, and in turn, many commercialized versions of newly developed inverters have been widely released [4], [5]. To target a relatively constant HF-CMV profile, and to reduce the switching losses as well as output filter size of the converters, three-level (3L) inverters with a unipolar pulse-width modulation (PWM) and several new circuitry designs have been proposed. The well-known 3L-H5 inverter from SMA Corporation [6], the so-called 3L-highly efficient and reliable inverter concept (HERIC)

inverter from Sunways Company [7], and the H-bridge inverter with zero-voltage state rectifier (HB-ZVR) from Aalborg university [8] are all based on either dc- or ac-decoupling approach, which results in a floating CMV profile during the free-wheeling mode. Despite having a relatively constant CMV, the goal of leakage current mitigation imposed by the updated versions of some strict grid codes, e.g., German code VDE-AR-N 4105, IEC 60755, VDE 0100-410, and VDE 0100-721, is not fully attended yet in these topologies since during the freewheeling period, the parasitic capacitance of the switches still demands a charging current [9], [10]. Therefore, additional measures in designing an appropriate electromagnetic-interference (EMI)/common-mode filter should be taken into account to further mitigate the leakage current concern [11]. Alternatively, the optimized H5 (oH5) inverter introduced in [12], H5-D inverter proposed in [13], and different families of the H6 inverters reported in [14], [15], [16], are all based on generating a 3L output voltage waveform but with a relatively constant HF-CMV, unipolar PWM, and a reasonable leakage current. However, due to the effects of junction capacitors of the switches during the freewheeling period, the concern of leakage current reduction still persists [17].

In this context, the HERIC-passive/active clamped inverters in [17] and the positive-negative neutral point-clamped (PN-NPC) inverter in [18] are designed based on the mid-point-clamping technique. Although the output voltage of these inverters is measured based on the leg's voltages, the charging current of the junction parasitic capacitance in the OFF-state condition of the switches is considerably reduced, while the HF-CMV is clamped to the half value of the dc-link voltage. This reduces the complexity of designing the output EMI filter leading to a reduced resultant leakage current. Unlike the 3L-T-type or NPC/active NPC (ANPC) inverters, which suffer from half dc-link voltage utilization, both the PN-NPC and HERIC-clamped inverters can generate a 3L output voltage waveform with a full dc-link voltage utilization at the ac-side. 3L-transformerless inverters such as Karschny [19], dual-buck [20] and switched-capacitor (SC) common-ground (CG)-based configurations [21], [22] are other well-known topologies with relatively constant CMV and fully mitigated leakage current concern. However, due to the need for additional inductors and capacitors with an SC technique, their efficient performance with high-power density is still a questionable challenge compared to the aforementioned structures.

Motivated by the concept of multilevel inverters, the output filter size of the above-mentioned transformerless inverters is reduced remarkably, leading to improving the power density/overall efficiency with a quality ac voltage waveform [24]. A conceptual illustration for such improvement is depicted in Fig. 1, where, at the same condition of the input dc voltage, effective switching frequency, and filter inductor size, the conduction losses associated with the grid-interfaced filter are reduced by the enhancement of the inverter output voltage levels [25]. Herein, the type of PWM scheme, i.e.,

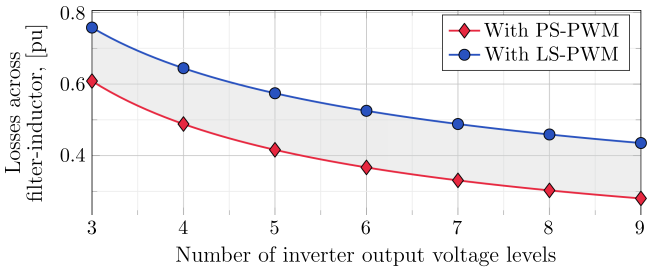

FIGURE 1. Effects of multilevel output voltage with different types of modulation on loss reduction of the grid-interfaced filter.

level-shifted (LS) or phase-shifted (PS) applied to the multilevel converters can also affect the apparent switching frequency of the inverter output voltage/current waveforms [25]. Hence, the modulation effect is reflected in the ripple content of the inverter output current and can thereby affect the grid-interfaced filter losses. Thanks to this concept, the five-level (5L)-inverters proposed in [26], [27] have used 12 power switches to attain all the possible output voltage levels with a constant HF-CMV. A combination of T-type and half-bridge leg introduces another 5L inverter in [28] in which its HF-CMV is not constant but varied within half and one-quarter of the main dc-link voltage. Alternatively, the so-called H8-5L inverter presented in [29] attained the same achievement with eight power switches but with the cost of the SC-integrated technique, which may cause additional power losses due to charging currents passing through the switches. Similarly, through NPC, ANPC, T-type or CG-based inverters, enhancement of the inverter output voltage levels is also possible with a reduced leakage current profile; however, additional active and passive elements are needed, which reduces the power density.

Taking into account the excellent performance of the conventional 3L-HERIC passive/active-clamped [17] and PN-NPC transformerless [18] inverters from the efficiency, constant HF-CMV, and reduced leakage current, an amorphous version of them to generate a 5L output voltage waveform is proposed in this article, while this is an extended version of the previously-published paper in [23]. This increment of output voltage levels is achieved with either LS-or PS-PWM-based schemes, while the switching and conduction losses of the inverter stage and output filter are reduced compared to the existing 3L-version of these converters. Therefore, the output ac voltage spectrum of these new versions of inverters possesses lower total harmonic distortion (THD) with a double apparent output switching frequency, while the size of the output filter is reduced, leading to an improved efficiency and power density of the overall system.

The rest of this article is organized as follows: the working principles of the proposed HERIC active/passive-clamped and PN-NPC inverters with a 5L output voltage waveform are discussed in Section II. HF-CMV analysis and the solution to mitigate the leakage current value in the proposed converters

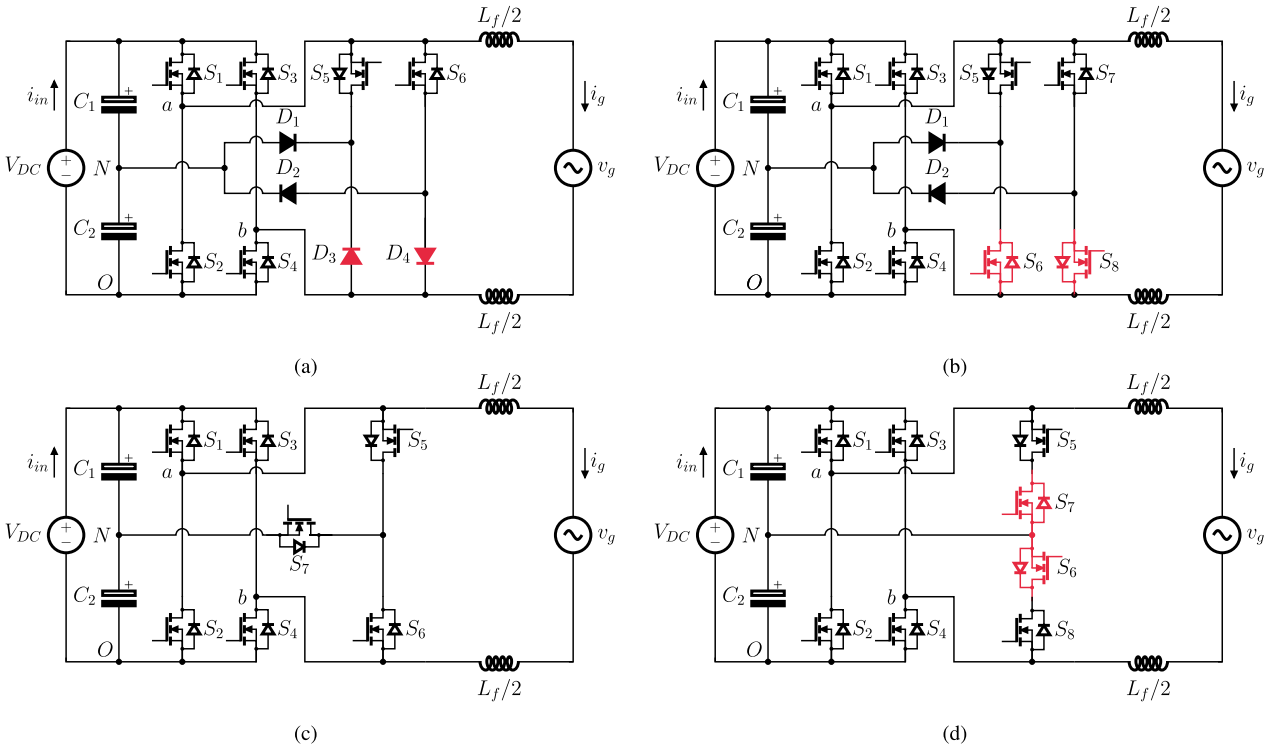

FIGURE 2. HERIC-clamped inverters. (a) The conventional 3L topology based on a passive-clamped approach [Fig. 22(a) in [17]], (b) the proposed HERIC passive-clamped 5L inverter [Fig. 1(b) in [23]], (c) the conventional 3L topology based on active-clamped approach [Fig. 22(c) in [17]], and (d) the proposed HERIC active-clamped 5L inverter.

are studied in Section III. Design guidelines for the incorporated passive elements besides a comparative study in terms of efficiency and loss are presented in Section IV. Afterwards, experimental results obtained from two different laboratory-built prototypes, i.e., the proposed HERIC passive-clamped and PN-NPC-5L inverters, are given in Section V to verify the effectiveness and feasibility of this proposal. Finally, conclusions are drawn in Section VI.

II. THE PROPOSED 5L HERIC-CLAMPED AND 5L PN-NPC INVERTERS WITH MODULATION STRATEGY

To be able to generate the distinct 5L output voltage waveform, some modifications to existing HERIC active- and passive-clamped topologies should be performed to fully control the current flow during different switching stages. On the other hand, the conventional PN-NPC topology can synthesize a 5L output voltage waveform without any circuit modifications.

A. THE PROPOSED 5L HERIC-CLAMPED INVERTERS

The most popular HERIC passive-clamped transformerless inverter capable of generating a 3L output voltage waveform using either unipolar-PWM or unipolar double-frequency PWM schemes is depicted in Fig. 2(a) [Fig. 22(a) in [17]]. This topology is based on an ac-decoupling approach, where two passive diodes are used to connect the mid-point of the dc-link capacitors to the drain of the switch S_5 and the source of the switch S_6. In contrast to the conventional HERIC converter, this clamping approach is useful to maintain a constant CMV, which is equal to half of the dc-link voltage, $V_{DC}/2$, when the ac-side switches, i.e., S_5 and S_6, are ON during the generation of the zero-level at the output voltage. To produce a 5L output voltage waveform from the existing HERIC passive-clamped 3L inverter, two discrete power diodes, D_3 and D_4, connected in series with S_5 and S_6, respectively, need to be replaced by two active power switches S_6 and S_8, as shown in Fig. 2(b). Therefore, two four-quadrant switches can be used on the ac-side while they still have been clamped to the mid-point of the dc-link capacitors through the diodes D_1, and D_2.

Details of all the switching states to generate a 5L output voltage through the proposed improved version of HERIC passive-clamped inverter are stated in Table 1, where, v_{out} is the inverter output voltage between the converter terminals a and b. As can be seen in this table, there is an additional middle level of the output voltage, i.e., $V_{DC}/2$, in both half cycles, which can be generated through two different redundant switching states (RSSs). The availability of these RSSs is helpful in adopting a PS-PWM scheme to provide the required gate switching pulses. Therefore, the apparent switching frequency of the inverter is twice the carrier frequency, leading to further improving the THD with a reduced output filter size. The maximum value of the proposed inverter output voltage is equal to the main dc-link voltage, V_{DC}, while the HF-CMV

TABLE 1. Switching states of the proposed improved 5L HERIC passive-clamped inverter

State	v_{out}	S_1	S_2	S_3	S_4	S_5	S_6	S_7	S_8
A	$+V_{DC}/2$	1	0	0	0	0	0	0	1
B	$+V_{DC}/2$	0	0	0	1	1	0	0	0
C	$-V_{DC}/2$	0	0	1	0	0	0	1	0
D	$-V_{DC}/2$	0	1	0	0	0	1	0	0
E	$+V_{DC}$	1	0	0	1	0	0	0	0
F	$-V_{DC}$	0	1	1	0	0	0	0	0
G	0	0	0	0	0	1	1	1	1

TABLE 2. Switching states of the proposed 5L HERIC active-clamped inverter

State	v_{out}	S_1	S_2	S_3	S_4	S_5	S_6	S_7	S_8
A	$+V_{DC}/2$	1	0	0	0	0	1	0	1
B	$+V_{DC}/2$	0	0	0	1	1	0	1	0
C	$-V_{DC}/2$	0	0	1	0	1	0	1	0
D	$-V_{DC}/2$	0	1	0	0	0	1	0	1
E	$+V_{DC}$	1	0	0	1	0	0	0	0
F	$-V_{DC}$	0	1	1	0	0	0	0	0
G	0	0	0	0	0	1	1	1	1

of the converter is varied between $V_{DC}/4$ and $3V_{DC}/4$. Although this HF-CMV is not constant as its 3L counterpart [see, Fig. 2(a)], due to the high-frequency nature of the output voltage, it can be easily filtered out through designing a proper EMI filter [11]. Details of the leakage current reduction are discussed in Section III.

An additional remark drawn from Table 1 is related to the number of ON-state switches at each switching state. Herein, only two power switches are ON at the same time to realize different output voltage levels, albeit for generating zero output voltage level, four switches should be turned on. This can significantly reduce the conduction losses associated with the switches and can improve the overall efficiency of the converter thereby. It is worth mentioning that the maximum voltage stress (MVS) across all the switches involved in the proposed improved version of the HERIC passive-clamped 5L inverter is similar to the original 3L one, i.e., both are equal to the main dc-link voltage; however, the switching frequency of the switches is significantly reduced since a larger number of output voltage levels are generated by this newly-developed topology.

Alternatively, Fig. 2(c) shows the circuit configuration of the existing HERIC active-clamped 3L inverter [Fig. 22(c) in [17]]. As can be seen, instead of the diodes, a power switch S_7 is used to clamp the mid-point of the dc-link capacitors to the switching node of S_5 and S_6. Similar to the passive-clamped version, the HF-CMV is constant during all the switching states but with the added capability of handling reactive power. To derive a 5L variant of this topology, an improved HERIC active-clamped inverter is proposed as shown in Fig. 2(d). As can be realized, only one more power switch has been added to the existing topology, while the ac-decoupling approach is made by the ON-state condition of two four-quadrant switches at the ac-side. The inverter output voltage is measured with respect to output terminals a and b, and the switching states of this topology have been tabulated in Table 2. Similar to the improved HERIC passive-clamped 5L inverter, there are two RSSs for both the middle positive and negative output voltage levels, i.e., states A and B for the positive half-cycle and states C and D for the negative half-cycle. This opens the door to using a PS-PWM scheme. Herein, the number of ON-state switches at each switching instant is still two, and the maximum inverter output voltage

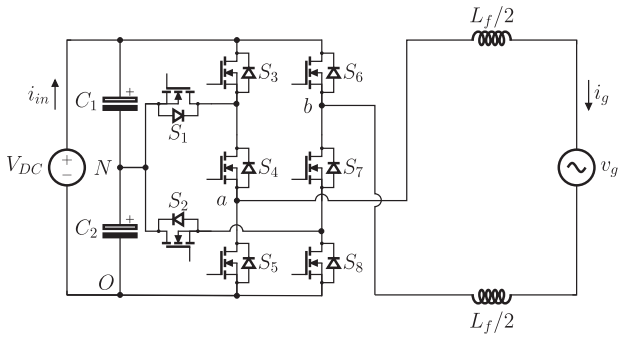

FIGURE 3. Schematics of the PN-NPC inverter topology proposed in [18].

is equal to V_{DC}. It is worth noting that except the switch S_7, all the switches in the existing HERIC active-clamped 3L inverter [see Fig. 2(c)] must block MVS equal to the main dc-link voltage, while this value for the switch S_7 is half. Conversely, only the switches in the front-end H-bridge side of the proposed HERIC active-clamped 5L inverter [see Fig. 2(d)] must tolerate V_{DC} as the MVS, while this value for the remaining switches is $V_{DC}/2$. This improvement is an extra achievement rather than a lower value of the effective switching frequency for all the switches of this 5L variant of the proposed topology. Similar to the proposed HERIC passive-clamped 5L inverter, the HF-CMV fluctuation of this HERIC active-clamped based 5L inverter varies between $V_{DC}/4$ and $3V_{DC}/4$. Moreover, given its high-frequency nature, it can be easily filtered out through designing a compact EMI filter.

B. OPERATION PRINCIPLES OF THE PN-NPC 5L INVERTER

The overall structure of the existing PN-NPC inverter is depicted in Fig. 3 [18], where it is connected to the grid, v_{ac} through split filter inductors, $L_f/2$. This famous structure is able to generate a 3L output voltage waveform, while due to its mid-point-clamped topological feature, its HF-CMV is clamped to $V_{DC}/2$ over each switching state. Without changing the overall structure, a 5L voltage waveform can be generated using a modulation-based technique. Table 3 shows all the switching states, which create a 5L output voltage waveform without changing the existing PN-NPC 3L structure. Similar to the previous cases as for the HERIC active/passive-clamped 5L inverters, there are two RSSs per middle output voltage levels, $\pm V_{DC}/2$, in both half cycles. In

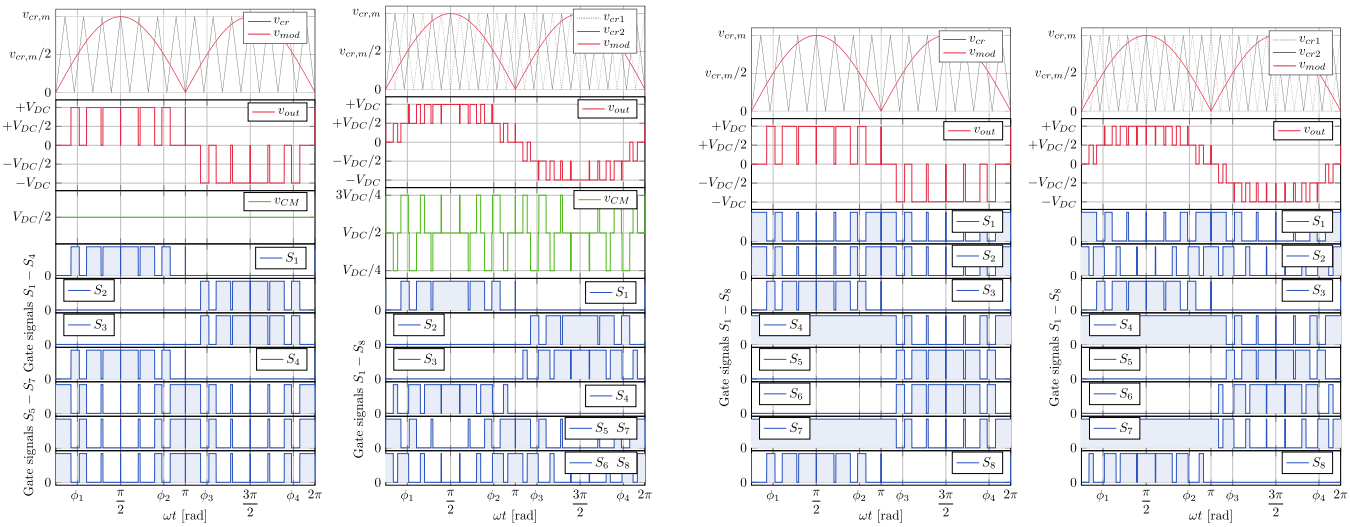

FIGURE 4. Applied PWMs to the HERIC-clamped and PN-NPC topologies through one fundamental voltage cycle for the (a) conventional HERIC-active clamped 3L-inverter with SPWM, (b) proposed HERIC-active clamped 5L-inverter with PS-PWM, (c) PN-NPC 3L-inverter with SPWM, and (d) PN-NPC 5L-inverter with PS-PWM.

TABLE 3. Switching states of the proposed 5L PN-NPC inverter

State	v_{out}	S_1	S_2	S_3	S_4	S_5	S_6	S_7	S_8
A	$+V_{DC}/2$	0	1	1	1	0	0	1	0
B	$+V_{DC}/2$	1	0	0	1	0	0	1	1
C	$-V_{DC}/2$	1	0	0	1	0	1	0	0
D	$-V_{DC}/2$	0	1	0	0	1	0	1	0
E	$+V_{DC}$	0	0	1	1	0	0	1	1
F	$-V_{DC}$	0	0	0	0	1	1	0	0
G	0	1	1	0	1	0	0	1	0

this case, the MVS across all the switches remains the same; however, due to the possibility of applying a PS-PWM, the switching frequency of the involved switches in the 5L-based structure of the PN-NPC inverter is reduced to half, leading to a further reduction in the overall switching losses of the converter. As can be realized through Table 3, to generate each level of the output voltage, four out of eight switches must be ON at the same switching instant. Here, the HF-CMV profile of the 5L-PN-NPC inverter is varied between $V_{DC}/4$ and $3V_{DC}/4$. Due to its high-frequency nature, a reduced leakage current profile can be achieved through designing a reduced-size EMI filter [11]. The operating principles of the PN-NPC converter based on the switching states from Table 3 can be observed in Fig. 5.

C. MODULATION STRATEGY

Taking into account the above, due to the availability of two RSSs per the middle positive/negative output voltage levels, all the aforementioned 5L inverters can be modulated using PS-PWM with two carriers with a 180° relative phase-shift. The logic-based structure of the modulator is depicted in Fig. 6(a), while the resultant 5L output voltage waveform of the discussed topologies with the PS-PWM strategy is shown in Fig. 6(b). Here, v_{mod} is the absolute value of the modulation signal generated by any typical controller, and v_{cr1}, and v_{cr2} are the two high-frequency carrier waveforms. Concerning Fig. 6(b), the operation region of this modulator is as follows:

- Positive half-cycle: from 0 to $+V_{DC}/2$ (Area I *AGBG*).
- Positive half-cycle: from $+V_{DC}/2$ to $+V_{DC}$ (Area II *EAEB*).
- Negative half-cycle: from 0 to $-V_{DC}/2$ (Area III *CGDG*).
- Negative half-cycle: from $-V_{DC}/2$ to $-V_{DC}$ (Area IV *FCFD*).

To keep the voltages of the dc-link capacitors balanced, it is critical to generate the output voltage levels of $\pm V_{DC}/2$ using the RSSs namely written as *A* and *B* in the positive half-cycle and *C* and *D* in the negative half cycle. It is worth highlighting that with a complementary switching fashion among the above-mentioned RSSs per each switching area, the LS-PWM technique also can be applied. However, the apparent output frequency will be equal to the carrier frequency. Figs. 4(a)–(d) show the differences in the applied modulation between the 3L and 5L versions of the HERIC active-clamped and PN-NPC topologies in terms of the inverter output voltage, gate switching pulses and the HF-CMV. Here, the 3L topologies were modulated using the original sinusoidal PWM (SPWM) with one carrier. As can be seen from these results, not only a 5L output voltage waveform is achieved through the proposed HERIC active-clamped and PN-NPC inverters, but also the effective switching frequency of the switches has been reduced to half due to the applied PS-PWM technique. What can further be seen is the reduced number of turning-ON and OFF states of the switches over a full fundamental grid cycle

in the 5L derivation of the discussed topologies. These two remarks can help both the 5L HERIC active/passive-clamped and PN-NPC inverters to operate at a higher apparent switching frequency with less overall switching losses and higher overall efficiency.

III. HF-CMV ANALYSIS AND LEAKAGE CURRENT REDUCTION

As discussed above, the RSSs generating $\pm V_{DC}/2$ output voltage levels in the proposed HERIC active/passive-clamped and PN-NPC 5L inverters lead to the HF-CMV fluctuations between $V_{DC}/4$ and $3V_{DC}/4$ as demonstrated in Fig. 4(b). Provided that the inverters are modulated with a PS-PWM technique, the HF-CMV frequency is equal to the carrier frequency f_{sw}. As a consequence, the common-mode attenuation can be performed by the employment of relatively small common-mode filters.

To reduce the effect of differential-mode voltage on the total leakage current generation, split inductors are connected at the converter's terminals, which results in circulating a common-mode current, i_{CM}, through the ground and dc-side parasitic capacitance. Herein, an additional common-mode filter as shown in Fig. 7 is normally integrated into a conversion system. In this case, the determination of the leakage current path impedance leads to choosing the carrier/switching frequency for operating outside the resonance region. To determine the leakage current, the common-mode simplified model of the inverter shown in Fig. 8(a) can help to derive the following [30]:

$$i_{CM} = \frac{v_{Cpar} + v_{OM} + v_{Rng}}{Z_{eq}} \tag{1}$$

where, Z_{eq} is the equivalent impedance of the common-mode path, determined by the neutral-to-ground resistance R_{ng}, equivalent inductance L_f that is formed by the output filter, and parasitic capacitance C_{par}. On the other hand, v_{Cpar}, v_{OM}, and v_{Rng} stand for the voltage drops across the parasitic capacitance, conversion system circuit, and ground neutral-to-ground resistance, respectively. In turn, these voltage drops form the total CMV v_{CM}. In this regard, the corresponding common-mode current i_{CM} can be expressed in the form of a transfer function as:

$$i_{CM}(s) = \frac{v_{CM}(s)}{\frac{1}{4}L_f s + \frac{1}{C_{par}s} + R_{ng}} \tag{2}$$

where s is the Laplace operator. The effect of Z_{eq} on the leakage current value varies depending on the effective switching frequency. Commonly, the value of C_{par} varies from 50 nF to 150 nF [30]. The value of common-mode amplification is maximum near the resonant frequency area. Given the LC-circuit resonance, the maximum value of the leakage current in the resonant frequency depends on the resistance between the neutral-point and ground, R_{ng}. Additionally, the presented simplified common-mode current path model loses its validity with the increasing switching frequency, since the effect of other parasitic components will be amplified. The frequency response analysis of the common-mode current path impedance illustrated in Fig. 8(b) leads to selecting a suitable switching frequency to operate far enough from the resonant region and, thus, mitigating the impact of switching frequency on the leakage current.

IV. DESIGN GUIDELINES OF THE PASSIVE ELEMENTS AND OVERALL EFFICIENCY ANALYSIS

A. DESIGN GUIDELINES

The input current of the proposed HERIC active/passive-clamped and the PN-NPC 5L-inverters in the single-phase grid-connected design possesses a double-line frequency ripple, 2ω. The role of the dc-link capacitors C_1 and C_2 is to store the ripple component of the input dc source [31]. Hence, the required capacitance can be expressed as [24], [26]:

$$C_1 = C_2 = \frac{V_m I_m}{\omega V_{DC} \Delta V_{DC}} \tag{3}$$

where, ω and ΔV_{DC} are the angular term at the grid fundamental frequency and the voltage ripple across the capacitors, respectively. Additionally, V_m, and I_m denote the peak value of the grid voltage and the injected grid current, respectively.

On the other hand, the current across the output filter inductor is a function of the applied volt-seconds across L_f. Therefore, with respect to [25], the current ripples of the inductor can be drastically reduced with the relation of $\propto 1/(n-1)^2$, where n is the number of inverter output voltage levels. Conversely, the employed PS-PWM allows the converter to double the apparent output switching frequency, $f_{so} = 2f_{sw}$ as earlier discussed. Using a piece-wise approximation of the inductor volt-second balance, the following equation is obtained:

$$\Delta i_g^{p-p} = \frac{V_{DC}}{(n-1)^2 f_{sw} L_f} = \frac{V_{DC}}{16 f_{sw} L_f} \tag{4}$$

where Δi_g^{p-p} is the peak-to-peak injected grid current ripple passing through the split filter inductors, and L_f is the total inductance of them. Given the lower current ripples across the filter-inductor, which can be translated to lower injected grid current THD, the overall filter size of the proposed 5L inverters can be reduced in comparison to their original 3L inverters versions. This reduction in the filter size leads to reduced magnetic and resistive loss as well, which will further improve the overall efficiency of the entire system.

B. EFFICIENCY ANALYSIS

To evaluate the efficiency improvement of the proposed HERIC active/passive-clamped and the PN-NPC 5L inverters, an overall efficiency analysis is conducted to reflect the differences between the original 3L and the proposed 5L inverter topologies. Herein, to attain less than one per cent THD content in the inject grid current, while using the discussed L-type filter, the 5L inverter topologies require $L_f/2 = 1$ mH inductors at 40 kHz switching frequency, whereas, the 3L topologies need at least $L_f/2 = 2.5$ mH filter inductors at

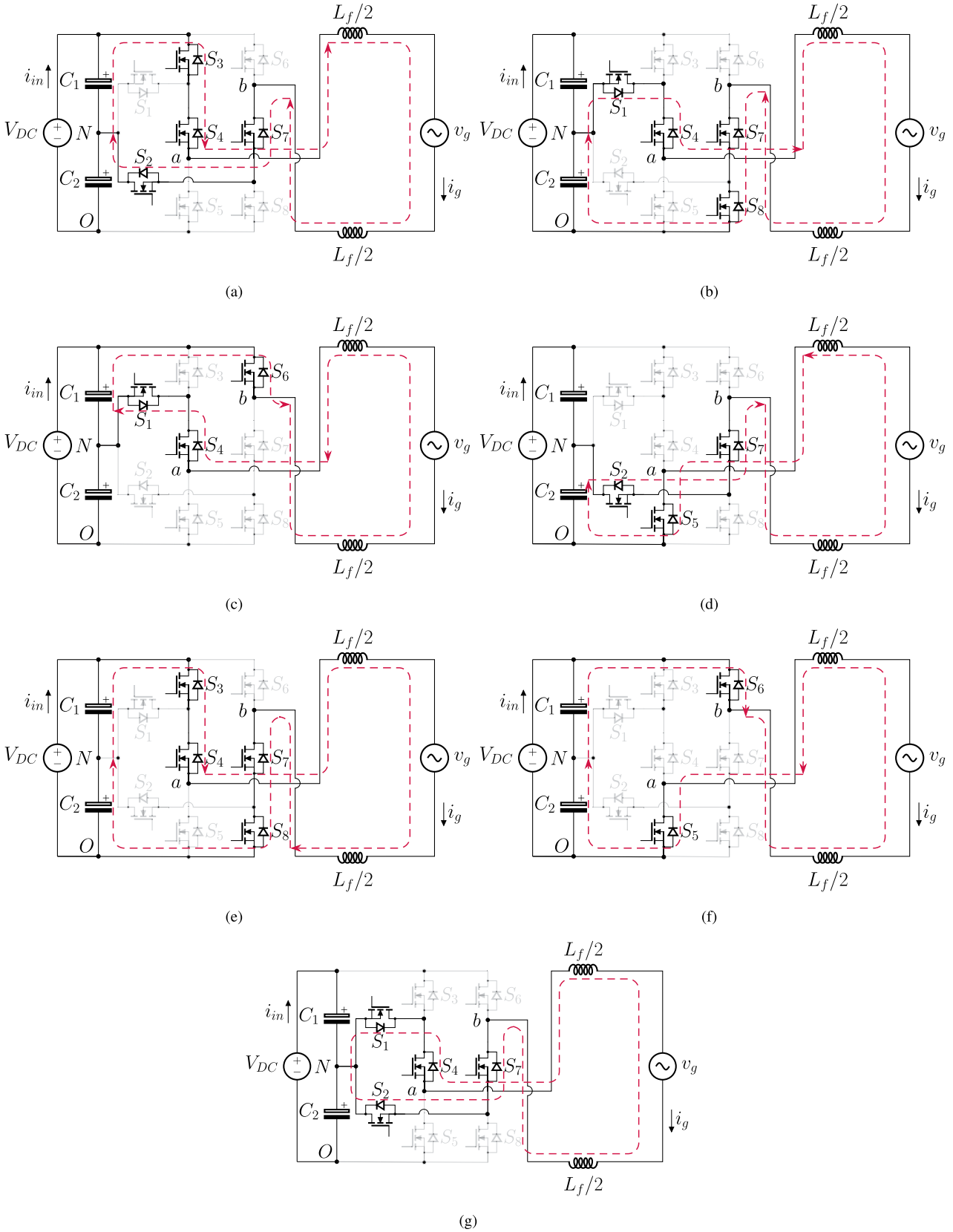

FIGURE 5. Operating states of the 5L PN-NPC converter with the current flowing paths and corresponding inverter output voltage. (a) A: $+V_{DC}/2$, (b) B: $+V_{DC}/2$, (c) C: $-V_{DC}/2$, (d) D: $-V_{DC}/2$, (e) E: $+V_{DC}$, (f) F: $-V_{DC}$, and (g) G: 0.

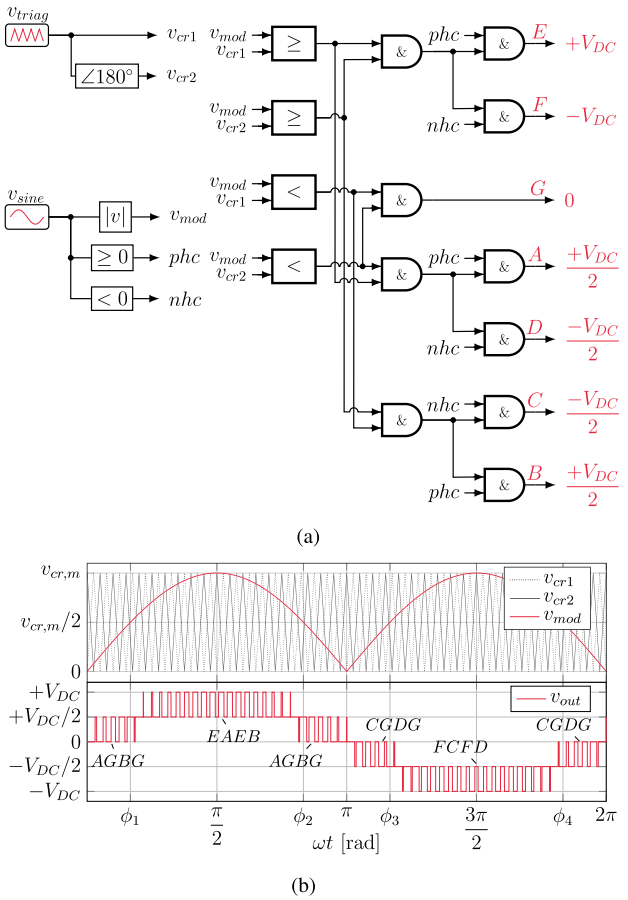

FIGURE 6. The modulation strategy to generate 5L output voltage. (a) Switching logic of the modulation technique with 180° PS carriers v_{cr1} and v_{cr2} and (b) PS-PWM with generated 5L PWM and operating areas.

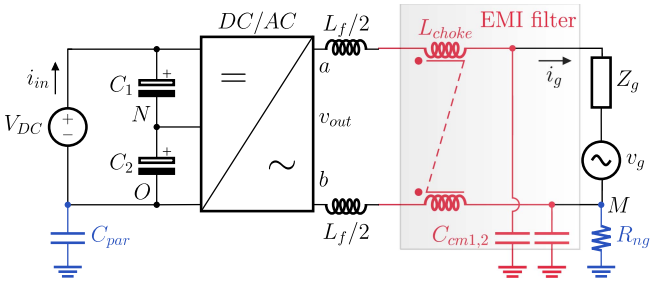

FIGURE 7. The simplified structure of the grid-connected transformerless inverter with the split-inductors L-filter and CM-filter.

the same apparent frequency. For both scenarios, efficiency curves are obtained using PLECS software and are presented in Fig. 9. Herein, all the semiconductor devices have been assumed to be a SiC power MOSFET UJ4C075018K4S. The reason for selecting this type of power MOSFET is its very low $R_{DS,ON}$, which leads to lower conduction losses, besides a very low value of the reverse recovery charge, Q_{rr}, C_{oss}, and turn ON/OFF energy, $E_{ON/OFF}$ featuring reduced overall switching losses. The overall efficiency comparison is

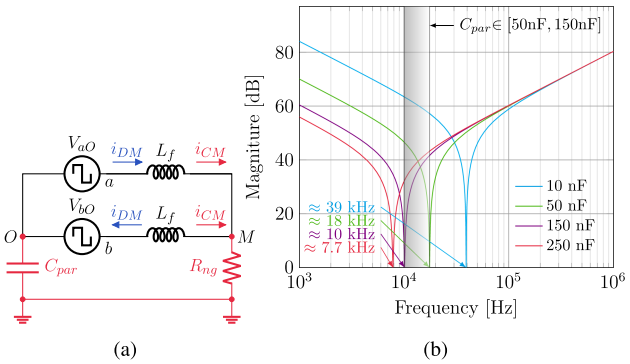

FIGURE 8. (a) Simplified model of differential- and common-mode currents path through the inverter circuit and (b) resulting frequency response diagram with various values of C_{par}. The results are obtained with $L_f = 6.6$ mH and $R_{ng} = 1\ \Omega$.

performed taking into account the losses in semiconductors and output filters. As for the semiconductor, both the turn ON/OFF switching and conduction losses have been considered using the data provided in the datasheet of the above-mentioned power MOSFET. Alternatively, losses in the inductors are divided into electrical and magnetic losses. Due to the unavailability of the core and winding data from the manufacturers, magnetic losses have been neglected. Conversely, electrical losses are determined by the equivalent series resistances of the inductors. Details of the efficiency analysis and loss distribution results at the considered rated power of 2 kW are illustrated in Fig. 10. As can be deduced from Figs. 9 and 10, a clear improvement of the overall efficiency is achieved using the 5L variants of the proposed HERIC active/passive-clamped and PN-NPC inverters. This efficiency enhancement leads to better scalability of these practical types of transformerless grid-connected inverters in real applications, while requiring lower volume/cost of the overall cooling system, which can indirectly target higher overall power density. Based on the simulation results, 5L versions of HERIC and PN-NPC converters do not show large discrepancies since the parameters and thermal models of semiconductors are similar to each converter. Additionally, in the mentioned 5L topologies, power semiconductors and passive elements experience similar current and voltage stresses, which results in the same switching and conduction losses.

V. EXPERIMENTAL RESULTS

In order to verify the correctness and circuit feasibility of the proposed HERIC-clamped and PN-NPC inverters in generating all the distinctive 5L output voltage, extensive laboratory-based experimental results are presented in this section. As for this, two SiC-based prototypes have been fabricated to address the circuit performance of the proposed HERIC passive-clamped and PN-NPC 5L inverters [Figs. 2(b) and 3]. The main circuit parameters used in the experiments have been enlisted in Table 4. The results for the proposed HERIC passive-clamped 5L inverter are presented under the

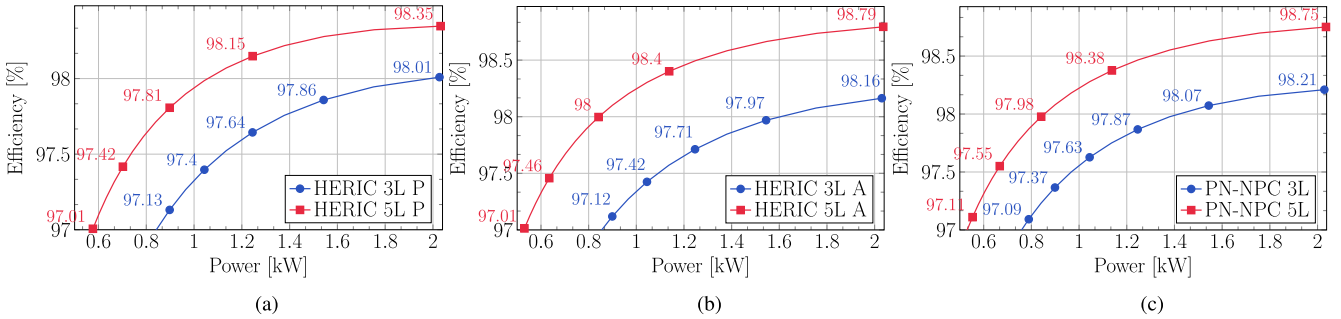

FIGURE 9. Calculated efficiency curves of the 3L and 5L converters under discussion with a fixed THD in the injected grid current and the same switching frequency, active components, DC-link capacitors, modulation strategy as for (a) HERIC passive-clamped 3L and 5L inverters, (b) HERIC active-clamped 3L and 5L inverters, and (c) the PN-NPC 3L and 5L inverters.

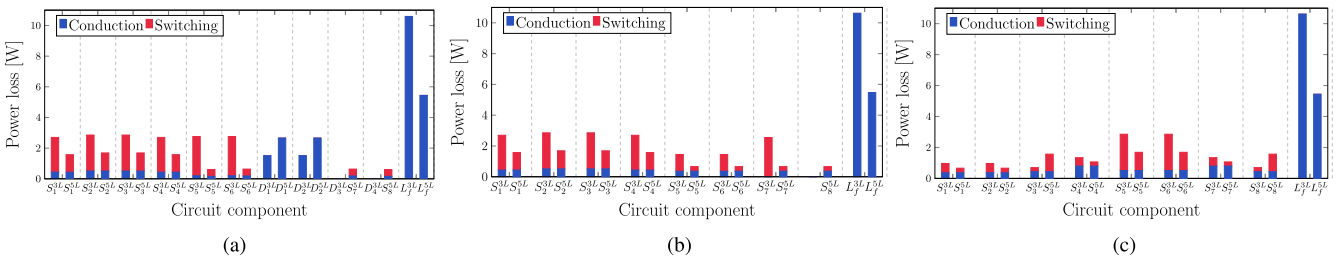

FIGURE 10. Loss breakdown details among the components at the rated 2 kW power as for the (a) HERIC passive-clamped 3L and 5L, (b) HERIC active-clamped 3L and 5L, and (c) PN-NPC 3L and 5L inverters.

TABLE 4. Experimental prototype components and equipment

Description	Value/Type
Power Rating (P_R)	2 kW
Carrier Frequency (f_{sw})	40 kHz
DC-link Voltage (V_{DC})	360 and 400 V
DC-link Capacitors ($C_{1,2}$)	0.47 mF
Filter Inductor ($L_f/2$)	3.3 mH, 100 mΩ
Filter Capacitor (C_f)	2.2 μF (only HERIC)
Power MOSFETs	UJ4C075018K4S
Power Diodes	C6D08065A (only HERIC)
Gate Drivers	UCC21520DW
DSP	TMS320F28379D

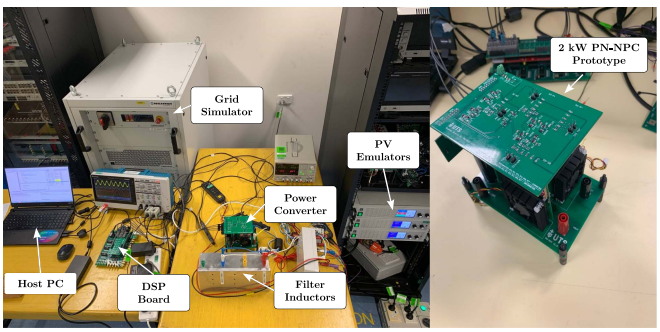

FIGURE 11. 2 kW prototype of the proposed system with the measurement and grid-connection setup.

open-loop condition with a simple *RL* load. For the proposed PN-NPC 5L-inverter, both the open- and closed-loop grid-connected results are shown. In all the experiments, a PV emulator, model EA-PSI-9750-12, is used to electrically feed the converters, while a four-quadrant grid simulator (REGATRON TC30.528.43-ACS) is employed to perform the closed-loop grid-connected tests. Fig. 11 shows the details of the prototype and the measurement setup. The gate switching pulses of the switches have also been provided using the described PS-PWM technique and are generated by a TMS320F28379D digital signal processor (DSP).

Having taken the above-mentioned notions into account, Fig. 12 shows the details of the experimental results for the proposed HERIC passive-clamped 5L inverter. In the first test, the converter is operating under a 1.8 kW loading condition, while the maximum modulation index of the PS-PWM technique is set at 0.95. Herein, an *LC*-filter is used in the output as the interface between the converter and the load, while the input dc voltage is set at 400 V. Fig. 12(a) shows the results of the 5L inverter output voltage, the filtered-voltage across the load, the input current, and the load current. The same set of the results when a step-change in the load is applied (from 0.6 kW to 1.8 kW) is shown in Fig. 12(b). The dynamic results to show the proper operation of the converter under a step change in the maximum value of the modulation index (from 0.6 to 0.95) are shown in Fig. 12(c). As can be

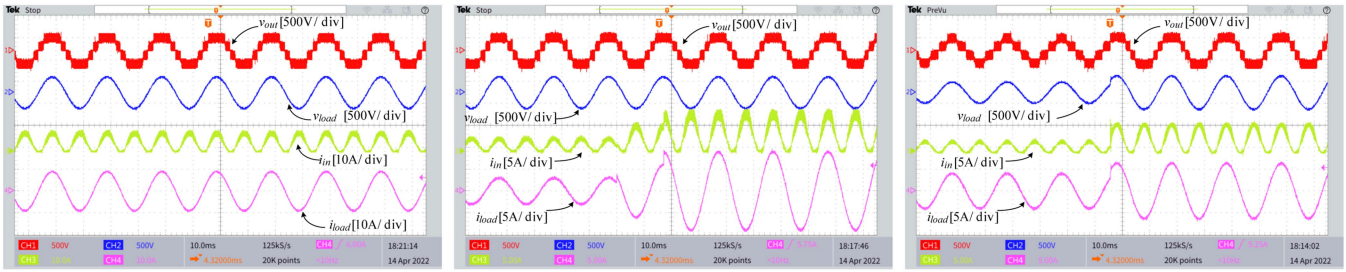

FIGURE 12. Experimental results of the proposed HERIC passive-clamped 5L inverter at open-loop condition showing from top to bottom: the 5L output voltage, the load-side output voltage after the filter, the input current, and the load current (a) at the rated power of 1.8 kW (b) under the load step-change from 0.6 kW to 1.8 kW, (c) under the step-change in the maximum value of the modulation index from 0.6 to 0.95 with constant load.

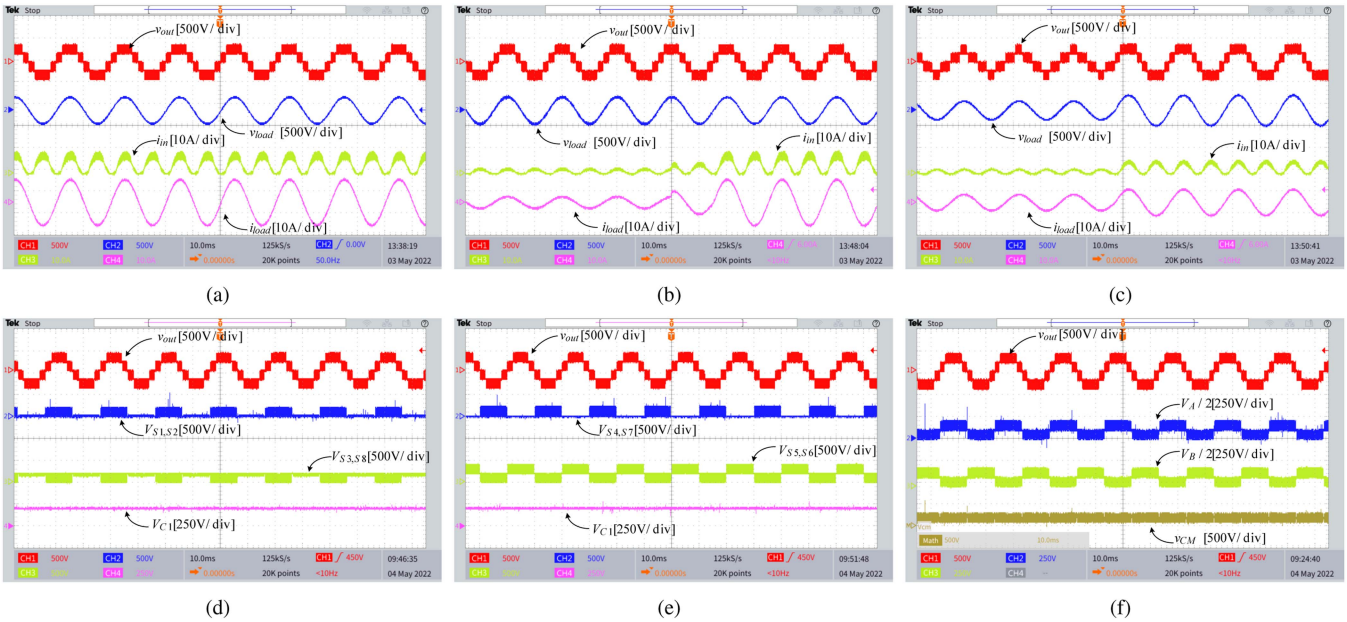

FIGURE 13. Experimental results of the PN-NPC 5L inverter at open-loop conditions showing the 5L output voltage, the filtered-voltage across the load, the input current, and the load current from top to bottom, respectively. (a) At the rated power of 1.8 kW, (b) under the load step-change from 0.5 kW to 1.8 kW, (c) under the m_a step-change in the maximum value of the modulation index from 0.6 to 0.95, (d) Voltage stress across the switches S_1, S_3 with voltage across capacitor C_1. (e) Voltage stress across the switches S_4, S_5 with the voltage across capacitor C_1, and (f) 5L inverter output voltage with the presence of the resultant HF-CMV.

confirmed from these results, all the 5L output voltage with a quality ac-current waveforms and spike-free input current are generated through the experiment. The efficiency analysis of HERIC passive-clamped was performed with the Yokogawa WT1806 power analyzer and reached 96.7% at 1.8 kW power. It comprises losses in the converter circuitry and the passive components. Both simulated and measured efficiency curves for HERIC passive-clamped converter can be observed in Fig. 15.

The detailed open-loop experimental results of the proposed PN-NPC 5L inverter are shown in Fig. 13. The type of semiconductor devices, the switching frequency and the value of the input voltage are the same as given in Table 4. Fig. 13(a)–(c) show the same set of waveforms, i.e., the 5L inverter output voltage, the voltage after the filter across the load, the input current and the load current under the 1.8 kW rated power, the step-change in the load from 0.5 to 1.8 kW, and the step-change in the maximum value of the modulation index from 0.6 to 0.95, respectively. As can be seen, the results perfectly show the effectiveness of the proposed solution in delivering a 5L output voltage with a measured efficiency of around 97.05% at the rated power of 2 kW, as shown in Fig. 15. Taking 400 V as the input dc voltage into account, the MVS across the switches and the dc-link capacitors have also been shown in Fig. 13(d) and (e), while the voltages of the converter terminals a and b with respect to the mid-point N and the resultant HF-CMV with the presence of 5L inverter output voltage are presented in Fig. 13(f).

As for the grid-connected tests of the proposed PN-NPC 5L inverter, a closed-loop system with a simple

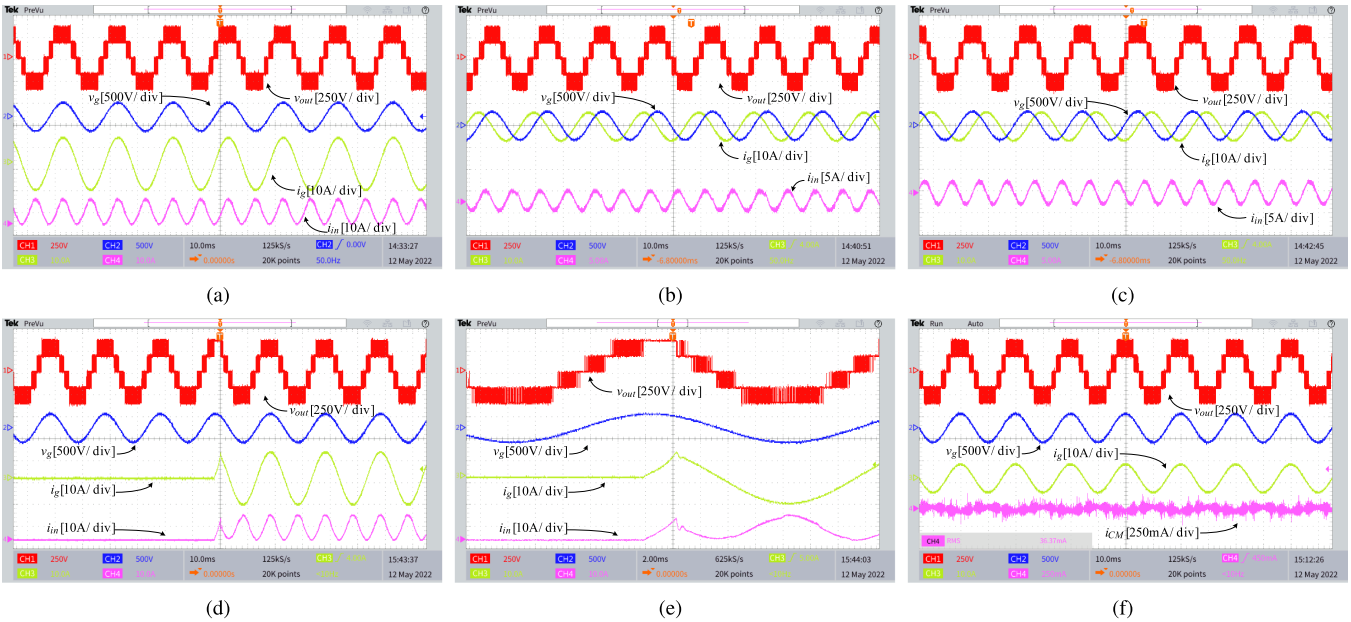

FIGURE 14. Grid-connected experimental results of PN-NPC 5L inverter, from top to bottom: 5L inverter output voltage, grid voltage, injected grid current, and the input current. (a) At 2 kW rated power, (b) with the purely leading PF, (c) with the purely lagging PF. (d) under a step-change in power injection from zero to the rated 2 kW, (e) a zoomed shot under a step-change in power injection from zero to the rated 2 kW, and (f) the results at 1 kW injected power and in the presence of the resultant leakage current.

proportional-resonant (PR) controller and grid-voltage observer (GVO) technique has been considered. The PR controller parameters are obtained based on the selected switching frequency/sampling time, and *L*-type split filters [32]. The role of GVO is to capture the phase and amplitude of the grid to generate a proper reference current for the PR controller [33]. To cancel out the effect of HF-CMV, and to reduce the leakage current value, an EMI filter based on the discussion given in Section III has also been designed. The peak voltage of the grid is considered 320 V at 50 Hz fundamental frequency. Hence, with a full scale of the maximum modulation index, a DC voltage of 360 V is enough in this case. Details of these grid-connected tests at the steady-state 2 kW rated power are shown in Fig. 14(a), while the reactive power support results of the converter with purely leading and lagging power factor (PF) are given in Fig. 14(b) and (b), respectively. The dynamic results of the proposed PN-NPC 5L inverter when a step change in the injected active power from zero to 2 kW is applied are shown in Fig. 14(d) and (e). One can see the correct closed-loop operation of the converter and the double-line frequency in the input current profile of the proposed PN-NPC 5L inverter. Finally, the resultant leakage current, the 5L inverter output voltage, the grid voltage, and the injected grid current when the converter is injecting 1 kW to the grid are presented in Fig. 14(f). As can be confirmed, although the converter induces an HF-CMV, varying between $V_{DC}/4$, and $3V_{DC}/4$, the root-mean-square (rms) value of the leakage current is still within an acceptable range, i.e., 36 mA. This is mainly achieved because of employing a reduced-size EMI filter at the output.

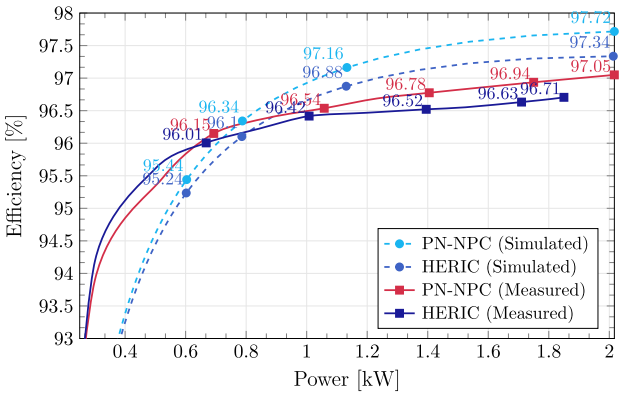

FIGURE 15. Efficiency curves of the 5L PN-NPC and HERIC passive-clamped converters under grid-connected conditions and unity power factor, using the same parameters listed in Table 4 for simulation.

VI. CONCLUSION

In this article, amorphous 5L versions of HERIC-clamped and PN-NPC converters have been proposed. Given the benefits of the 5L output voltage and multiplicative effect of PS-PWM, these converters can significantly improve the power density, and efficiency, and reduce THD level, while retaining a similar number of circuit components as their 3L counterparts. Conventional HERIC-clamped and PN-NPC inverters are counted as important circuit designs for transformerless grid-connected systems because of their highly efficient performance, constant HF-CMV and low value of the leakage current. However, they can only generate 3 distinctive output voltage levels, which requires a larger output filter to be

connected to the grid with an acceptable THD profile, when compared to the proposed 5L converter. Although through the proposed solution, the concern of variable HF-CMV remains in place, a reduced-size EMI filter was adopted in the output to get an acceptable value of the leakage current. Design guidelines with laboratory-built experimental results under both open- and closed-loop grid-tied environments have been presented, which have verified the circuit feasibility and correctness of the proposal.

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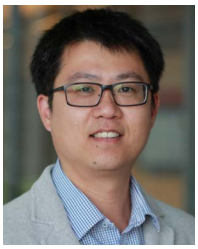

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