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Hybrid Modular Multilevel Converters for High-AC/Low-DC Medium-Voltage Applications

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ABSTRACT With ever-increasing power-density requirements, technologies such as energy storage systems and electric-vehicles can benefit greatly from interfacing medium-voltage (MV)-AC grid like 13.8kV or 30kV using high-AC/low-DC voltage converter. Using modular high-AC/low-DC voltage converter can help increase power-density and efficiency, while reducing total conversion steps and providing flexibility. Full-bridge modular multilevel converters (FB-MMC) and solid-state transformers are existing solutions for such operations, but suffer from limitations of high semiconductor requirements, large submodule capacitors and/or many high-frequency transformers. Three new hybrid-MMC (HMMC) topologies are proposed in this paper as alternative solutions for such high-AC/low-DC voltage operations. Each of the three developed HMMCs utilizes a unique combination of low-frequency high-voltage switches and fast-switching low-voltage switch based submodules to generate multilevel-AC voltage. HMMCs are compared extensively to state-of-the-art FB-MMC and are shown to have semiconductor savings of over 27%, 38% lower submodule capacitor size, and 53% lower losses for 13.8-kV-AC/6-kV-DC operation. Due to these benefits like higher efficiency, significantly smaller submodule capacitance requirements, and fewer semiconductors, HMMCs can be an excellent option for high-AC/low-DC applications. Practical considerations like snubber and DC split-capacitor requirement are also elaborated for developing and commercializing HMMCs. Comparison results are verified using a 17.5 kW three-phase MV laboratory prototype.

INDEX TERMS Hybrid modular multilevel converters, modular multilevel converters, medium voltage converter, electric vehicle chargers, energy storage systems, solid state transformer.

I. INTRODUCTION

With ever-increasing environmental concerns and growing efforts to reduce greenhouse emissions [1], a few technologies are receiving unprecedented research interest. Energy storage systems (ESS) and electric vehicles (EV) are two of these key technologies poised to shape the future. ESS can support the grid with voltage and frequency regulation, demand support, and renewable smoothing, making the grid more resilient [2], [3]. Yet, with increasing penetration of renewables into the grid, the capability required per ESS is rising significantly. EVs have also seen enormous growth due to their promise of lower pollution and lower lifetime cost [4]. Yet EVs accounted for less than 1% of the worldwide fleet in 2019 [5]. Historically, the major challenges to EV adoption are high initial price, range anxiety, and lack of fast EV charging infrastructure [6]. The latter two can be mitigated by more compact and powerful EV chargers.

Both ESS and EV chargers are increasingly demanding higher power with some recently proposed EVs capable of megawatt level charging. For such high-power applications, using very high current is challenging due to the large copper usage and high losses. The ratio of peak power and average

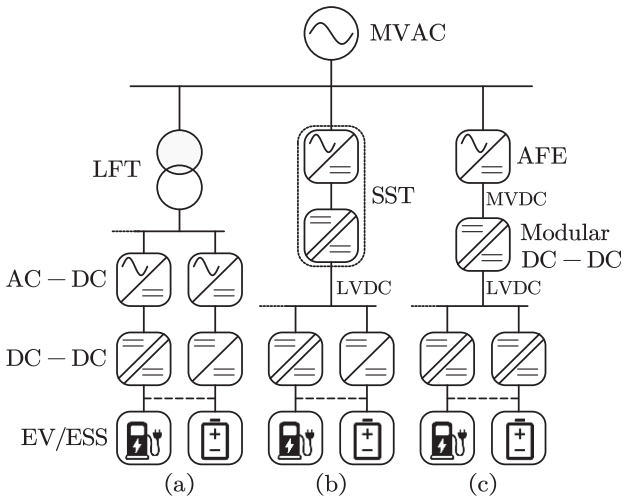

FIGURE 1. Different EV charging infrastructures (a) LFT + AC-DC + DC-DC (b) SST + DC-DC (c) AFE + Modular DC-DC + DC-DC.

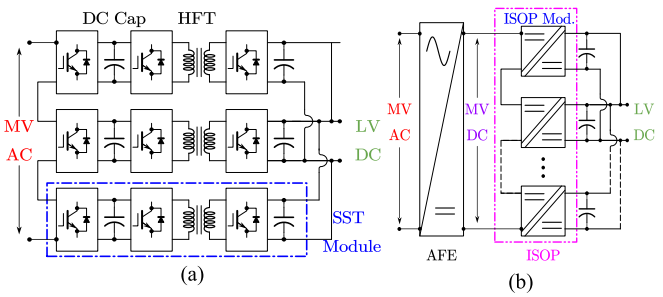

FIGURE 2. Advanced MV-AC to LV-DC converters (a) solid state transformer highlighting module, high-frequency transformer (HFT), and module capacitors (DC Cap) (b) proposed solution with active front end (AFE) and input series output parallel (ISOP) converter.

power for these applications is also high, which further results in oversized equipment. Considering these constraints, increasing voltage has emerged as a viable alternative for such high power applications, with medium voltage (MV) converters now being explored for such use. Both ESS and EV chargers can have similar voltage conversion interfacing with the MV-AC grid, e.g., 13.8 kV and 30 kV classes, to provide low voltage (LV)-DC on the EV charging pole (CP) or battery. In many cases, ESS is employed with EV chargers to help with peak shaving [4], with such integration already realized by EVgo [7], Volkswagen, and Tesla [8]. Several EV charging infrastructures have been proposed for off-board EV charging [9], [10], [11] but can be divided into three major categories shown in Fig. 1.

The conventional EV charging infrastructure is shown in Fig. 1(a). It uses a line-frequency transformer (LFT) to convert MV-AC to LV-AC. The LV-AC is then fed to a rectifier. In some configurations, a central rectifier is used, and the configuration is referred to as a common dc-link [12]. If instead, distributed rectifiers are used, as shown in Fig. 1(a), the configuration is referred to as a common ac-link [12]. The rectifier output is fed to an array of LV DC-DC converters, as shown in Fig. 1(a). This DC-DC conversion can use a variety of topologies like three-level buck utilized by Porsche, interleaved buck used by ABB, or phase-shifted full bridge employed by Tesla [11]. The EV CP or battery can be connected to one or multiple paralleled DC-DC Converters, as dotted in Fig. 1(a). Each EV CP has a power rating from tens of kilowatts to a few megawatts. For this configuration, the LFT is very bulky and voluminous, making it difficult to reduce the charging station's volume and weight [4], [9], [10]. With rising demand for charging stations in urban areas, this is a critical challenge for future mass electrification. Additionally, the pulsating power profile needed for EV/ESS applications needs faster power delivery and low feeder impedance. LFTs struggle to provide such low impedances.

Solid state transformers (SSTs) have also been explored for application within EV charging stations, as shown in Fig. 1(b) [13], [14]. SST is used for direct MV-AC to LV-DC conversion, followed by LV DC-DC converter [15], [16], [17]. SST-based solutions can have a 65% lower footprint than LFT-based solutions [13], with about 40% lower installation costs [18]. SSTs can also control the power flow actively, resulting in better controllability. Yet, the SST solution faces a wide range of practical challenges. Each high-frequency transformer (HFT) within the SST module, as shown in Fig. 2(a), needs to be insulation rated at MV-AC voltage [19]. This, in turn, results in a limited power rating due to thicker insulation with higher thermal resistance [20]. In addition to the HFT, the SST module itself requires considerable volume due to insulation considerations, as both MV and LV components are packed within the same SST module [21]. The insulation necessity towards the cabinet also increases the volume of the SST module [22]. Consequently, the insulation requirements for MV operation are a major challenge for SST power density. One alternative to avoid this complication is to use different insulation ratings for each SST module, but this results in a loss of modularity. The DC capacitor, 'DC Cap' sizing within SST can also be a critical concern due to the second harmonic ripple [23]. Moreover, upgrading old SST modules for higher MV-AC voltage in the future is not easy as insulation requirements may change with MV-AC, limiting scalability.

Considering the insulation, modularity, and scalability challenges of SSTs, a recent approach to decouple MV-AC to LV-DC conversions into two separate stages, as shown in Fig. 1(c), is explored [24]. The first stage is an active front end (AFE) converter for MV AC to DC conversion. The second stage is a modular MV-DC to LV-DC converter like the input-series output-parallel (ISOP) converter [24], as shown in Fig. 2(b). The isolation design of the high-frequency transformer in such ISOP can be decoupled from the MV-AC grid, leading to reduced requirements, such as basic insulation level (BIL). Only DC power flowing through the ISOP also reduces the total losses in both devices and transformers.

For this configuration, if the voltage at the second stage modular converter's MV-DC input is significantly higher than

its LV-DC output, a high DC-DC step-down is required at the second stage. The high DC-DC step necessitates a large number of ISOP modules, making them expensive and bulky. It is thus preferred to have a low DC-DC step-down ratio in the second stage. Consequently, the MV input of the second-stage converter needs to be closer to its LV output. This opens the opportunity to use a high-AC/low-DC rectifier as the first stage AFE converter to get a low MV-DC as the second stage's input. This approach has the benefit that the second stage can be independently designed and optimized, irrespective of the first stage, and without concerns about MVAC voltage level. The burden of scalability in the present and future is now moved to only the first stage AFE converter. The use of AFE as the first stage also allows the use of EV charging stations for providing support to the grid and is utilized in practice by ENICRON [11]. The first stage AFE converter with high-AC/low-DC conversion is the focus of this paper.

MMCs with full-bridge submodules (FB-MMCs) are proposed as the ideal solution for this first-stage AFE [24] due to their ability to operate at MV, their modularity, scalability, fault handing capabilities, and ability to operate for low-DC/high-AC voltage operation [25], [26], [27]. Yet, FB-MMCs have not gained prominence within the industry because of the large number of switching devices required, high losses, and bulky capacitors. A few FB-MMC alternatives are proposed recently in literature [28], [29], [30], [31], [32], [33]. MMC with a mix of half-bridge submodule (HB-SM) and full-bride submodule (FB-SM) in each arm combine the lower loss advantage of HB-SM with fault-blocking capabilities of FB-SMs. However, for high-AC/low-DC operation, as AC voltage is increased, only FB-SMs are inserted to generate negative arm voltage. This difference in operation leads to different duty ratios for FB-SMs and HB-SMs within the same arm. With increase in ratio of AC and DC voltage, this difference in the duty ratio is further enlarged, leading to severe capacitor voltage imbalance issues which can be challenging for control [28], [29].

The alternate arm converter (AAC) [30] is also an excellent converter combining the benefits of a two-level converter with modularity and scalability of MMC. AAC uses an FB-SMs in series with high/medium voltage switches in each arm to reduce device voltage and lower SM capacitance rating, while also introducing fault-blocking capabilities. However, AAC is limited in the operating modulation ratio and a discrepancy from its modulation 'sweet-spot' results in severe SM capacitor voltage balancing challenges. The extended overlap AAC (EO-AAC) [32] was proposed recently as an improvement over AAC. EO-AAC extends operating range of AACs to other modulation ratios, but the arm current in EO-AAC has discontinuity or sharp undesired changes for most power factors and modulation ratios. The sharp changes in arm current can be challenging to control [32].

Modular embedded multilevel converters (MEMCs) [34] and Hybrid MMCs (HMMCs) [35], [36], [37] have emerged recently as another possible option. HMMCs available in the literature are usually similar to HB-SM-based MMCs (HB-MMCs) in their utilization of HB-SM as the building block. But unlike HB-MMCs, HMMCs also use additional high/medium-voltage switching stacks, referred to as 'medium voltage switching stack (MVSS).' The MVSS usually comprise either one single MV switching device or multiple semiconductor devices connected in series. MVSSs are switched at line frequency. While the use of MVSS in HMMCs provides an opportunity to reduce the number of devices, losses, and SM capacitor size compared to HB-MMCs, HMMCs currently available in the literature are unable to increase modulation index to more than one, limiting their use for high-AC/low-DC applications. Here modulation ratio, M, is defined as $M{=}V_{AC}/(0.5V_{DC})$ where V_{AC} is the peak AC phase-neutral voltage and V_{DC} is DC bus voltage. The ability to not generate negative SM voltage also limits the fault-handling capabilities within HB-MMCs and HB-based HMMCs.

Understanding the limitations of FB-MMCs, this paper extends the HMMC concept to develop three new HMMC topologies as viable alternatives to FB-MMC for high-AC/low-DC applications. These topologies are referred to as $HMMC_1$, $HMMC_2$, and $HMMC_3$ and are shown in Fig. 3. Like the FB-MMCs, the proposed HMMCs provide advantages like fault-ride-through, bidirectional power flow and staircase multilevel AC voltage. Yet, the three proposed HMMC topologies use much fewer switching devices compared to conventional FB-MMCs and have the potential for much lower costs, losses, volume, and SM capacitance requirements. Each of the three HMMC topologies have unique advantages and limitations, making them suitable for different applications.

It was established in [35] that for high-DC/low-AC applications ($M < 1$), $HMMC_1$, shown in Fig. 3(a) but with HB-SMs, has a 30% lower device count, 50% lower capacitance requirement and 32% lower losses compared to HB-MMCs. This paper focuses instead on applications with $M > 1$, i.e., high-AC/low-DC cases, and highlights the changes required in topologies and operation accordingly. The topologies are extensively compared for high-AC/low-DC operating cases, and it is established in this paper that $HMMC_2$, shown in Fig. 3(b), can operate at higher than one modulation index with about 50% fewer devices than FB-MMCs, while also having potentially lower SM capacitance requirements and lower losses. This huge advantage can be attributed to $HMMC_2$'s capability to operate for high-AC/low-DC applications using just HB-SMs.

This paper also investigates and establishes that $HMMC_3$, shown in Fig. 3(c), is the best-suited topology for most high-AC/low-DC applications with significantly lower semiconductor requirements, much smaller SM capacitor size, and excellent loss savings compared to FB-MMCs and other HMMCs. $HMMC_3$'s unique capability of zero voltage turn-on and turn-off is also extensively explored, which permits the use of series stacking of devices for MVSS without the concerns of unequal voltage sharing among series devices [38] and lower losses. The limited di/dt and dv/dt in $HMMC_3$

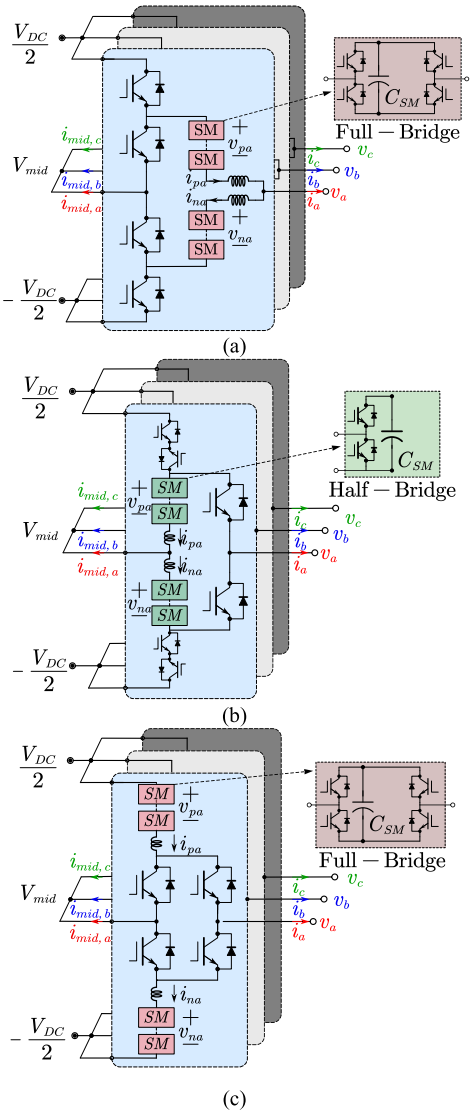

FIGURE 3. New hybrid modular multilevel converter (HMMC) topologies (a) $HMMC_1$, (b) $HMMC_2$, and (c) $HMMC_3$.

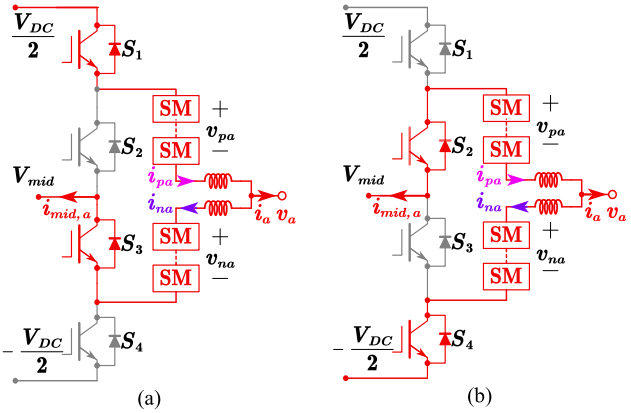

FIGURE 4. $HMMC_1$ operation (a) *P* Mode ($v_a \geq 0$), (b) *N* Mode ($v_a < 0$).

also makes use of silicon-controlled rectifier (SCR) as MVSS possible with intelligent control of commutation process. This would result in considerably lower losses and costs. All three proposed HMMCs are thoroughly analyzed, not only for their advantages compared to FB-MMCs, but also for their limitations and practical implementation challenges.

The rest of the paper is organized into six sections. Section II expands on and develops the three HMMC topologies and their operation. Discussion on each topology's semiconductor requirements and arm voltage/current patterns are also included in this section. Section III compares the three HMMCs to traditional FB-MMC on several critical matrices like devices used, efficiency, and SM capacitance requirements. Section IV discusses the practical challenges and considerations for HMMC utilization compared to conventional MMCs. Section V includes both single-phase and three-phase experimental results for selected topologies. Section VI compares the proposed implementation with SSTs, followed by the conclusions.

II. PROPOSED HYBRID MODULAR MULTILEVEL CONVERTERS

The three HMMC topologies are presented in Fig. 3. The key topological difference between them is the different locations of chain-link developed by series connection of SMs. As can be observed from Fig. 3, $HMMC_1$ and $HMMC_3$ utilize FB-SMs, whereas $HMMC_2$ uses HB-SMs. All HMMCs utilize MVSSs. Each MVSS is operated at line frequency and can be developed using high/medium-voltage low-frequency switching devices. The SMs, on the contrary, utilize low/medium voltage switches, just like conventional MMCs. Each of the three HMMC topologies is discussed in detail in the following subsections. It is important to highlight that all topologies have the capability of bidirectional power flow, but for ease of understanding, inverter mode operation is elaborated upon in this section.

A. HYBRID MODULAR MULTILEVEL CONVERTER–ONE ($HMMC_1$)

$HMMC_1$, as shown in Fig. 3(a), uses four MVSSs per phase represented as S_1-S_4 in Fig. 4. The MVSSs are utilized to maintain $0.5V_{DC}$ voltage across the two arms in the same phase. The MVSS switching operation is dependent on phase AC voltage, with each phase leg operating in the MVSS switching configuration dependent on its AC voltage polarity. Considering the two polarity possibilities, the operation of each phase can be divided into two modes: *P* and *N*. *P* mode operation is observed when the phase voltage is greater than or equal to zero, with *N* mode being used for phase voltage less than zero. Fig. 4 highlights these two possible operating modes for one phase, phase *A*.

MVSSs S_1-S_2 and S_3-S_4 operate in a complementary manner for these two modes. The configuration shown in Fig. 4(a), with switches S_1 and S_3 on, is utilized when phase-*A* AC

voltage, v_a, is equal to or more than zero. Alternatively, the configuration shown in Fig. 4(b) is utilized when v_a is less than zero. Over the line cycle, the converter traverses between these two states once, resulting in the MVSSs switching at line frequency.

The number of SMs required per arm depends on the maximum voltage each arm is required to produce without overmodulating. In conventional FB-MMC, each arm, at its maximum, must provide half of the DC voltage in addition to the AC voltage. Consequently, for traditional FB-MMC, each arm observes a maximum arm voltage of $0.5V_{DC}+V_{AC}$, assuming V_{AC} is the absolute value of peak phase voltage. For $HMMC_1$, because of the utilization of the MVSSs to decrease the total voltage observed across the two arms, each arm is required to only generate a maximum voltage of either V_{AC} or $0.5V_{DC}$, whichever is larger, as long as the mid-point voltage, V_{mid}, is maintained at zero. For this section, it would be assumed that the V_{mid} is maintained always at zero. Assuming the capacitor voltage is maintained around V_{SM}, and the phase voltage and current of v_a and i_a as shown in (1), the number of required SMs in $HMMC_1$ and FB-MMC, $N_{SM,HMMC1}$, and $N_{SM,MMC}$, respectively, can be calculated as (2). For high-AC/low-DC voltage operation, V_{AC} is higher than $0.5V_{DC}$ and would be utilized in (2) for $HMMC_1$. Here ω is the angular frequency of AC voltage, and equal voltage sharing is assumed between capacitors of the same arm. The upper arm voltage reference, $v_{pa}{}^*$, and lower arm voltage reference, $v_{na}{}^*$ of $HMMC_1$ are shown in (3) and (4), respectively.

$$\begin{aligned} v_a &= V_{AC}.sin\left(\omega t\right) \\ i_a &= i_{AC}.sin\left(\omega t+\phi\right) \end{aligned} \tag{1}$$

$$\begin{aligned} N_{SM,HMMC1} &= \max\left[0.5V_{DC}, V_{AC}\right]/V_{SM} \\ N_{SM,MMC} &= \left(0.5V_{DC}+V_{AC}\right)/V_{SM} \end{aligned} \tag{2}$$

$$\begin{aligned} v_{pa}^* &= 0.5V_{DC}-v_a \qquad 0<\omega t\le\pi \\ v_{pa}^* &= V_{mid}-v_a \qquad \pi<\omega t\le 2\pi \end{aligned} \tag{3}$$

$$\begin{aligned} v_{na}^* &= v_a - V_{mid} \qquad 0<\omega t\le\pi \\ v_{na}^* &= 0.5V_{DC}+v_a \qquad \pi<\omega t\le 2\pi \end{aligned} \tag{4}$$

Unlike the conventional FB-MMCs, $HMMC_1$ may require a DC-side split capacitor. But the split capacitor can be eliminated if the current through the mid-point is maintained at zero and the DC current is maintained constant [36]. To ensure these conditions, a trapezoidal current allocation scheme is discussed in [35] and is utilized here. This arm current control scheme ensures that arm currents are regulated to maintain the sum of all phases' mid-point currents as zero. The upper arm current reference, $i_{pa}{}^*$ based on DC side current, i_{DC}, and phase-A AC current, i_a can be shown in (5). The other arm and phase currents can be derived in similar manner. The AC voltage, AC current, arm voltage for phase A, arm current pattern for phase A, and MVSS blocking voltage for phase A for $HMMC_1$ with a non-unity power factor assuming ideal converter operation are presented in Fig. 5.

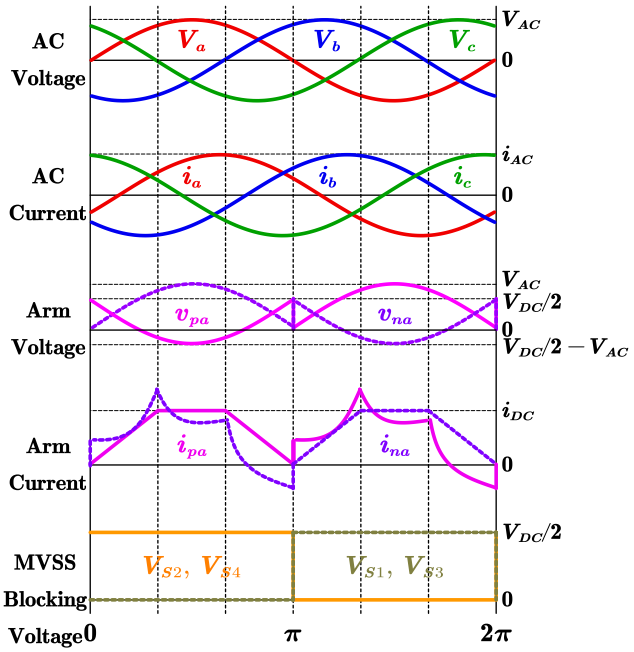

FIGURE 5. Operating waveforms for $HMMC_1$.

$$\begin{aligned} i_{pa}^* &= 3i_{DC}\omega t/\pi \qquad 0<\omega t\le\pi/3 \\ i_{pa}^* &= i_{DC} \qquad \pi/3<\omega t\le 2\pi/3 \\ i_{pa}^* &= 3i_{DC}\left(\pi-\omega t\right)/\pi \qquad 2\pi/3<\omega t\le\pi \\ i_{pa}^* &= 3i_{DC}\left(\omega t-\pi\right)/\pi+i_a \qquad \pi<\omega t\le 4\pi/3 \\ i_{pa}^* &= i_{DC}+i_a \qquad 4\pi/3<\omega t\le 5\pi/3 \\ i_{pa}^* &= 3i_{DC}\left(2\pi-\omega t\right)/\pi+i_a \qquad 5\pi/3<\omega t\le 2\pi \end{aligned} \tag{5}$$

As observed, the two MVSSs: S_2 and S_4 block $0.5V_{DC}$ for half line cycle, whereas the other two MVSS: S_1 and S_3 block $0.5V_{DC}$ in another half cycle. As can be observed from Fig. 5, with trapezoidal current allocation, one phase supports either end of the DC bus current. For phase A, upper arm current, i_{pa} supports part of the DC bus current for $v_a>0$. During that period, the lower arm has current i_{na}, which is the difference between i_{pa} and i_a. Roles are reversed for supporting negative DC rail during $v_a<0$. For the three-phase system, the three legs combine to maintain DC bus currents as constant. The trapezoidal allocation also enables the mid-point current to be maintained at zero. For $V_{AC}>0.5V_{DC}$, a negative voltage is required from the arm, requiring the use of FB-SM.

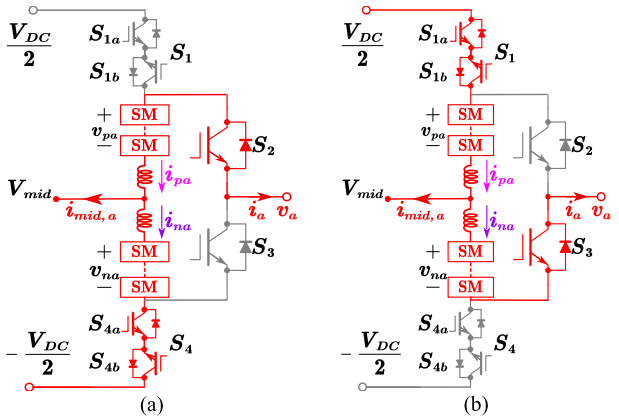

FIGURE 6. HMMC$_2$ operation (a) *P* Mode ($v_a \geq 0$), (b) *N* Mode ($v_a < 0$).

B. HYBRID MODULAR MULTILEVEL CONVERTER–TWO (HMMC$_2$)

HMMC$_2$, as shown in Fig. 3(b), uses four MVSSs per phase. Two of these MVSSs, S_1, and S_4, need bidirectional capability when used for low-DC/high-AC operation, where $V_{AC} > 0.5V_{DC}$. These are necessary to avoid unintentional current flow through the freewheeling diode. For cases with $V_{AC} \leq 0.5V_{DC}$, the bidirectional blocking switch is unnecessary; only switches S_{1a} and S_{4a} can be utilized. HMMC$_2$ also operates with two different operating modes: *P* and *N*, depending on the polarity of AC voltage. Fig. 6 presents there two modes for phase *A*. As can be observed, switches S_1-S_4 and S_3-S_2 operate in a complementary manner across these two modes. The configuration of Fig. 6(a), where switches S_2 and S_4 are turned on, is utilized when the AC voltage for phase *A*, v_a, is more than or equal to zero. Fig. 6(b) operation is alternatively utilized when v_a is less than zero.

As observed in Fig. 6, the upper and lower arms of HMMC$_2$ phase leg can be interpreted to be operated independently of each other, completing two different functions. One arm generates AC voltage and current supporting the AC side, while the other arm supports the DC side voltage and current. This is different from MMC or HMMC$_1$, where arm voltage and currents are dependent on both AC and DC simultaneously. The reference arm voltage for the upper arm, v_{pa}^*, and lower arm v_{na}^* for phase *A* in terms of its phase voltage and current, as shown in (1), can be calculated in (6) and (7).

$$v_{pa}^* = v_a - V_{mid} \qquad 0 < \omega t \leq \pi$$
$$v_{pa}^* = 0.5V_{DC} - V_{mid} \qquad \pi < \omega t \leq 2\pi \tag{6}$$
$$v_{na}^* = 0.5V_{DC} + V_{mid} \qquad 0 < \omega t \leq \pi$$
$$v_{na}^* = V_{mid} - v_a \qquad \pi < \omega t \leq 2\pi \tag{7}$$

As observed from (6) and (7), if the V_{mid} is maintained at zero, each arm is required to generate a peak voltage of either V_{AC} or $0.5V_{DC}$, whichever is higher. Assuming V_{mid} is maintained at zero, the number of required SMs, $N_{SM,HMMC2}$ can be calculated as in (8).

$$N_{SM,HMMC2} = \max\left[0.5V_{DC}, V_{AC}\right]/V_{SM} \tag{8}$$

For high-AC/low-DC voltage operation, V_{AC} is higher than $0.5V_{DC}$ and would be utilized in (8). Further, as observed from (6) and (7), each arm is only expected to generate positive arm voltage if V_{mid} is maintained at zero. This provides a unique ability for HMMC$_2$ since it can use only HB-SM that generates zero or positive SM output voltage, even for high-AC/low-DC applications. Traditional MMCs, in such cases, require FB-SMs that use more switches. Like HMMC$_1$, HMMC$_2$ also utilizes the trapezoidal arm current to eliminate/reduce the DC split-capacitor requirement. The upper arm current reference allocation, i_{pa}^* for phase A is shown in (9). The lower arm can be easily derived similarly. The phase *A* midpoint current can be deduced from Fig. 3(b). For this arm current allocation, the sum of all three phase midpoint currents can be calculated as zero for all instances. The AC voltage, AC current, arm voltages, and arm current patterns for phase *A* for HMMC$_2$ with non-unity power factor assuming ideal converter operation are presented in Fig. 7. It can be observed that for HMMC$_2$, each arm's voltage is dependent on either of AC or DC voltage. For MVSSs, as observed from Fig. 6(a) during *P* state, S_3 blocks the AC voltage while its other end is referenced to -0.5V_{DC}. The total blocking voltage across S_3 can then be calculated to be V_a+0.5V_{DC}. Similar blocking voltage requirements can be established for S_2 during *N* state. The two other MVSSs, S_1, and S_4, on the contrary have lower blocking voltage requirements, equating to 0.5V_{DC}-V_a. This can be easily inferred from Fig. 6, as they are connected between the other DC rail

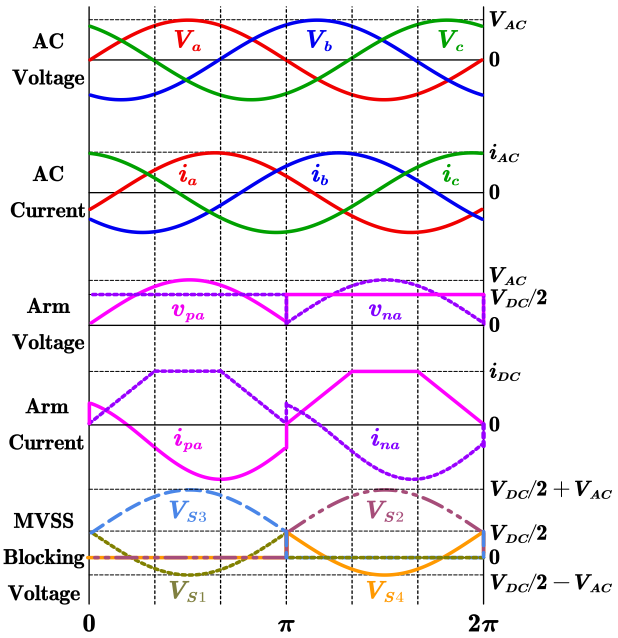

FIGURE 7. Operating waveforms for HMMC$_2$.

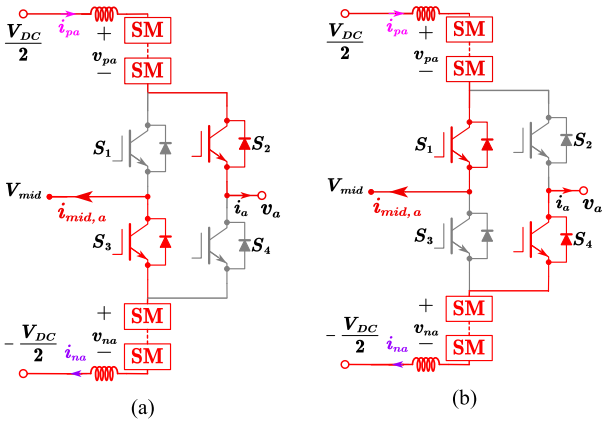

FIGURE 8. HMMC$_3$ operation (a) *P* Mode ($v_a \geq 0$), (b) *N* Mode ($v_a < 0$).

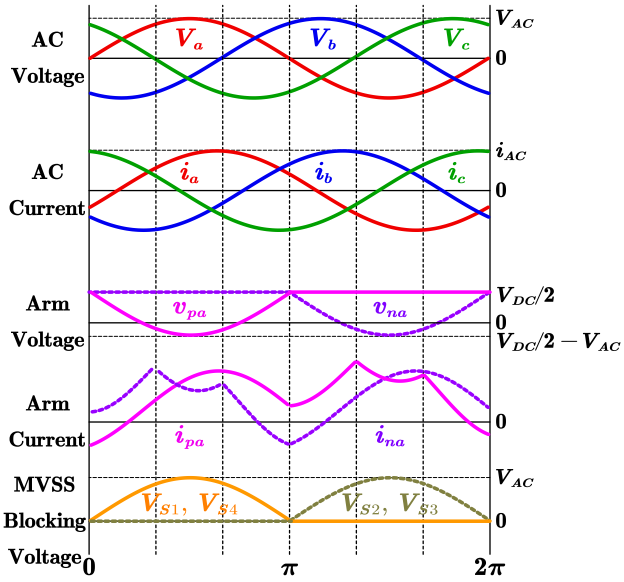

FIGURE 9. Operating waveforms for HMMC$_3$.

and AC voltage. Based on this, if blocking voltage requirements for MVSSs S_1 and S_4 are negative, i.e., $V_a \geq 0.5V_{DC}$, these MVSSs require the bidirectional blocking capability. All MVSS blocking voltage waveforms are also shown in Fig. 7.

$$\begin{aligned} i^*_{pa} &= -i_a && 0 < \omega t \leq \pi \\ i^*_{pa} &= 3i_{DC}\,(\omega t - \pi)\,/\pi && \pi < \omega t \leq 4\pi/3 \\ i^*_{pa} &= i_{DC} && 4\pi/3 < \omega t \leq 5\pi/3 \\ i^*_{pa} &= 3i_{DC}\,(2\pi - \omega t)\,/\pi && 5\pi/3 < \omega t \leq 2\pi \end{aligned} \tag{9}$$

C. HYBRID MODULAR MULTILEVEL CONVERTER–THREE (HMMC$_3$)

HMMC$_3$ is presented in Fig. 3(c) and uses FB-SMs in the arms in addition to four MVSS. HMMC$_3$ also operates across two different modes: *P* and *N*, depending on the polarity of the AC voltage. Fig. 8 presents there two operating modes for phase A. Switches S_1-S_2 and S_3-S_4 operate in a complementary manner across these two modes. The configuration is shown in Fig. 8(a), where switches S_2 and S_3 are on when the AC voltage, v_a, is more than zero. The switching configuration shown in Fig. 8(b), with switches S_1 and S_4 turned on, is used when v_a is less than zero. As observed from Fig. 8, one arm of HMMC$_3$ generates the AC voltage while also utilizing the DC voltage. This arm also generates AC current. The other arm supports DC side voltage and current. Mathematically, upper and lower arm voltage references, $v_{pa}{}^*$ and $v_{na}{}^*$, respectively, for phase *A* can be given as in (10) and (11).

$$\begin{aligned} v^*_{pa} &= 0.5V_{DC} - v_a && 0 < \omega t \leq \pi \\ v^*_{pa} &= 0.5V_{DC} - V_{mid} && \pi < \omega t \leq 2\pi \end{aligned} \tag{10}$$

$$\begin{aligned} v^*_{na} &= 0.5V_{DC} + V_{mid} && 0 < \omega t \leq \pi \\ v^*_{na} &= 0.5V_{DC} - v_a && \pi < \omega t \leq 2\pi \end{aligned} \tag{11}$$

Incorporating the DC voltage to generate AC side voltage can provide the advantage of using the same FB-SM to generate both positive and negative SM output voltage within one line cycle. This may help reduce the number of FB-SMs required compared to MMCs. The number of SMs required per arm in HMMC$_3$, $N_{SM,HMMC3}$ can be given as shown in (12).

$$N_{SM,HMMC3} = \max\left[0.5V_{DC},\ |V_{AC} - 0.5V_{DC}|\ \right]/V_{SM} \tag{12}$$

Here $|V_{AC}$-$0.5V_{DC}|$ defines the absolute value of the difference between the two. Like the other two HMMCs, HMMC$_3$ also utilizes a trapezoidal current allocation scheme to eliminate the DC split capacitor. The arm current allocation pattern can be developed as shown in (13), with upper current references for phase *A* shown as $i_{pa}*$. The negative arm current can be easily derived similarly. The sum of all three-phase midpoint currents can be maintained at zero using this developed scheme. The midpoint currents for one phase, phase *A*, can be deduced from Fig. 8.

$$\begin{aligned} i^*_{pa} &= i_a && 0 < \omega t \leq \pi \\ i^*_{pa} &= 3i_{DC}\,(\omega t - \pi)\,/\pi + i_a && \pi < \omega t \leq 4\pi/3 \\ i^*_{pa} &= i_{DC} + i_a && 4\pi/3 < \omega t \leq 5\pi/3 \\ i^*_{pa} &= 3i_{DC}\,(2\pi - \omega t)\,/\pi + i_a && 5\pi/3 < \omega t \leq 2\pi \end{aligned} \tag{13}$$

The AC voltage, AC current, phase *A* arm voltage, phase *A* arm current, and MVSS blocking voltage for phase *A* for a non-unity power factor operation under ideal converter operation are presented in Fig. 9. As observed, unlike the other two HMMCs where the arm voltages have a big change when crossing over between the *P* and *N* operating modes, HMMC$_3$ has a smooth transition, resulting in lower *dv/dt*. Also, since

TABLE 1. Parameters for Topology Comparison

Parameter	Symbol	Value
AC Voltage (L-L)	$V_{L\text{-}L,\ RMS}$	13.8 kV
DC Voltage	V_{DC}	12 kV (Case 1), 9 kV (Case 2), and 6 kV (Case 3)
AC phase angle	ϕ	0-2π
AC frequency	f_{AC}	60 Hz
Rated Power	P	1.8 MVA
SM device switching frequency	f_{sw}	1200 Hz
SM Capacitor ripple	δ	10%

the arm current is a function of the DC current and AC phase current opposing each other, the arm current can be much smaller compared to other HMMCs in cases where both DC and AC currents have similar magnitudes. This would result in smaller arm energy requirements for some cases, as highlighted in the next section.

The MVSS voltage in $HMMC_3$ has a unique inherent advantage of zero-voltage turn-on and zero-voltage turn-off, irrespective of the modulation index and power factor, as demonstrated in 'MVSS Blocking voltage' in Fig. 9. This unique topological advantage not only significantly reduces switching losses but also permits easy series stacking of switching devices for MVSS usage without any additional voltage balancing scheme. This is a very important advantage compared to other converters because, for MV applications, the voltage-sharing of series switches may pose a challenge if the voltage across series devices changes very fast, requiring special controls [38], but a soft turn-on and turn-off would mitigate this concern.

III. TOPOLOGY EVALUATION

The three developed HMMC topologies and FB-MMC are compared to evaluate the advantages and optimal application scenarios of each topology. Additionally, a fair comparison would require comparing topologies across a wide range of practical operating conditions. Considering high-AC/low-DC EV charging station as one example, the AC voltage is fixed to MVAC of 13.8 kV RMS line-line [13]. The DC voltage is varied across three different values of 12 kV, 9 kV, and 6 kV, as shown in Table 1. Topologies are compared for three key system characteristics and performance metrics: number of semiconductors required, SM capacitance requirements, and semiconductor losses. The results are discussed in the next few subsections.

A. NUMBER OF SEMICONDUCTORS REQUIRED

The total number of required semiconductors is critical to the size, cost and efficiency of converters. In addition to making converters more efficient, a lower number of switching devices results in a reduction in the total number of required gate drivers, auxiliary power supplies, controllers, and heat sinks, among other components. Consequently, the reduction in switching devices can contribute towards a more power-dense and cost-effective converter. Ignoring redundant SMs

TABLE 2. Number of Switching Devices Required for a Three-Phase Converter

Topology	Device Location	Device Eff. Rating	Peak MVSS Voltage	Peak Arm Voltage	13.8kVAC /12kVDC (Case 1)	13.8kVAC /9kVDC (Case 2)	13.8kVAC /6kVDC (Case 3)
FB-MMC	SM: FB	1.1 kV	N/A	V_{AC}+ $0.5V_{DC}$	384	360	312
	Total Switching Devices				**384**	**360**	**312**
$HMMC_1$	SM: FB	1.1 kV	N/A	V_{AC}	264	264	264
	S_1, S_2, S_3, and S_4	4 kV	$0.5V_{DC}$	N/A	24	24	12
	Total Switching Devices				**288**	**288**	**276**
$HMMC_2$	SM: HB	1.1 kV	N/A	V_{AC}	132	132	132
	S_2 and S_3	4 kV	V_{AC} + $0.5V_{DC}$	N/A	30	24	24
	S_{1A} and S_{4A}	4 kV	$0.5V_{DC}$	N/A	12	12	12
	S_{1B} and S_{4B}	4 kV	V_{AC}- $0.5V_{DC}$	N/A	12	12	18
	Total Switching Devices				**186**	**180**	**186**
$HMMC_3$	SM: FB	1.1 kV	N/A	V_{AC} - $0.5V_{DC}$	144	168	192
	S_1, S_2, S_3, and S_4	4 kV	V_{AC}	N/A	36	36	36
	Total Switching Devices				**180**	**204**	**228**

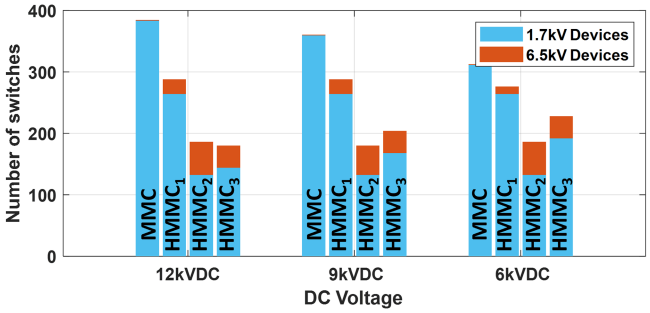

FIGURE 10. Comparison of the number of switching devices utilized.

and the negligible voltage drops at arm inductors, the number of required SMs per arm can be calculated based on the maximum voltage each arm is required to generate. For this comparison, the SM capacitor voltage is assumed to be 1.1 kV. This enables the utilization of mature 1.7 kV switching devices within SMs. The MVSS module operates at line frequency and can use larger voltage-rated 6.5 kV switching devices, operating at 60%-70% utilization. This equates to the effective (Eff.) device voltage of around 4 kV. For voltages higher than 4 kV, MVSSs need devices to be connected in series. Based on the required SMs per arm calculated in (2), (7), and (11), the required number of devices can be calculated as shown in Table 2 and Fig. 10. Here, V_{AC} is the peak line-ground voltage, V_{DC} is the DC side voltage, and the midpoint voltage is assumed to be zero. The overall system is a three-phase system.

As can be observed from Table 2, $HMMC_2$ has excellent switching device savings of around 40% to 52% compared to FB-MMC across all three DC voltages under consideration because it uses HB-SM as the core building block. As can be observed from Table 2, FB-MMC uses 27% to 53%

TABLE 3. Total and Normalized Blocking Voltage Comparison

Topology	MVSS Blocking Voltage	Peak Arm Voltage	Total Blocking Volt.	Normalized Blocking volt.
FB-MMC	N/A	V_{AC}+ $0.5V_{DC}$	$24V_{AC}$+$12V_{DC}$	12(M+1)
HMMC$_1$	$0.5V_{DC}$	V_{AC}	$24V_{AC}$+$6V_{DC}$	12(M+0.5)
HMMC$_2$	V_{AC}+$0.5V_{DC}$ (S_2 & S_3) $0.5V_{DC}$ (S_{1A} & S_{4A}) V_{AC}-$0.5V_{DC}$ (S_{1B} & S_{4B})	V_{AC}	$24V_{AC}$+$3V_{DC}$	12(M+0.25)
HMMC$_3$	V_{AC}	MAX [$0.5V_{DC}$, V_{AC} -$0.5V_{DC}$]	MAX [$12V_{AC}$+$12V_{DC}$, $36V_{AC}$-$12V_{DC}$]	MAX [12(1+0.5M), 12(1.5M-1)]

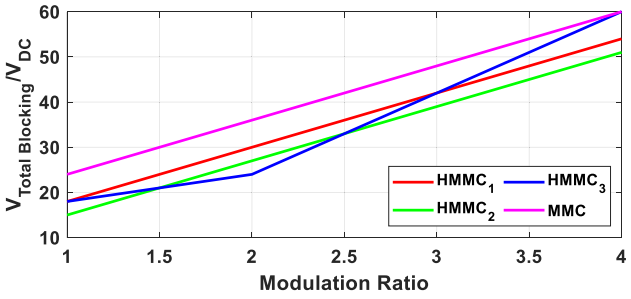

FIGURE 11. Normalized blocking voltage requirements.

more devices than HMMC$_3$ for the same voltage conversion. HMMC$_1$ also uses far more SMs than HMMC$_3$ resulting in a higher device count. Both these observations can be attributed to the similar distribution of blocking voltage required in positive and negative arm voltage in HMMC$_3$. HMMC$_1$ has the advantage of lower MVSS voltage blocking requirements compared to the other two HMMC topologies. As observed from Table 2, HMMC$_2$ requires different ratings of the MVSS depending on their position, unlike the other topologies, which may impact the modular nature of HMMC.

Unlike FB-MMC, HMMC$_1$, and HMMC$_2$ where the required number of devices may reduce as DC voltage reduces due to less blocking voltage requirement, number of devices in HMMC$_3$ might increase. This is because the reduction in DC voltage limits HMMC$_3$'s similar distribution of peak arm voltage requirement in upper and lower arms. Consequently, HMMC$_3$ follows the trend of increasing the device requirement per arm as DC voltage decreases. An optimization can be deduced here, where the HMMC$_3$ SM number can be optimized with it having the fewest SM number when the peak line AC voltage is equal to DC voltage. The device comparison remains similar for the inverter or rectifier mode operation of the converter. Also, while the number of devices and SM number varies, the power quality remains the same across all topologies, ensuring a similar filter design for all compared topologies.

Semiconductor switches are one of the most expensive components in any converter and a critical design consideration. Since HMMCs use two different types of switches in different quantities, a single metric to compare different topologies without considering two different categories for device number is very useful. Device blocking voltage requirement for a converter is chosen as that single unified metric. Table 3 aims to provide a generalized blocking voltage comparison for the four converters. The generalization is achieved by calculating the total blocking voltage ($V_{TotalBlocking}$) requirement as the sum of the peak blocking voltage requirement of each device within the converter. The total blocking voltage is normalized with respect to the DC voltage V_{DC}, resulting in the normalized blocking voltage (NBV). NBV can act as a general comparison parameter to evaluate the switching device blocking voltage requirement among topologies with changing modulation index. The NBV is also plotted in Fig. 11. As can be observed, HMMC$_3$ has an optimal operation area between modulation ratios of 1.6 to 2.5, where the NBV is minimal for it. HMMC$_2$, on account of its HB-SM utilization, also has a lower NBV almost across the whole range. As observed, all three HMMCs are better than FB-MMC in terms of NBV for the discussed operating range for high-AC/low-DC conversion.

B. SM CAPACITANCE REQUIREMENT

The SM capacitor is one of the most voluminous parts of MMC, occupying up to 50% of the overall size and up to 80% of the converter weight [39]. There is hence a strong impetus to reduce SM capacitor size, making the converter more power-dense. Assuming the SM capacitor reference voltage is V_{SM}, the capacitor ripple coefficient, δ is defined as (14).

$$\delta = {}^{\Delta V_{SM}}/_{2V_{SM}} \tag{14}$$

Here ΔV_{SM} is the peak-to-peak voltage ripple at SM capacitor voltage. Assuming that the ripple is the same across all SMs in the same arm, the required chain link capacitor energy storage, E_{CL} is related to maximum energy deviation, ΔE, δ and number of SM, N_{SM} for total power, S, in per unit value as [40]:

$$E_{CL} = 6N_{SM}\frac{C_{SM}V_{SM}^2}{2S} = 3\frac{\Delta E_{CL}}{2\delta S} \tag{15}$$

Here arm energy can be derived as a function of arm voltage and current in (16).

$$E = \int_0^{\omega t} V_{pm}.i_{pm}dt \tag{16}$$

Based on (14) and (15) for all the four topologies under consideration, plots of the arm energy requirements assuming δ=0.1 can be derived in Fig. 12.

Considering the different arm current and voltage references across the four topologies, the arm energy requirements are different. Moreover, this arm energy pattern also varies for different power factors ($\cos(\phi)$) and modulation ratios. Fig. 12(a), (b), and (c) highlight the curves for Case 1, Case 2, and Case 3 presented in Table 1. The energy requirement values are in per unit, E_{unit}, and are generalized for any power rating. For MMC, the conventional control with DC circulating current is used. Due to symmetry among phases as well as the upper and lower arm, only the arm energy of the upper arm in one phase is compared.

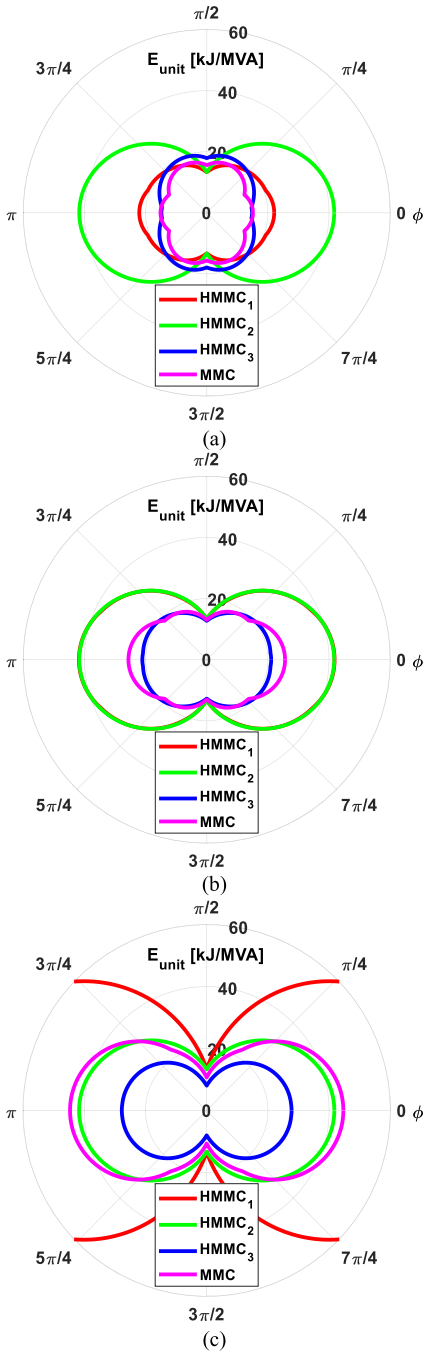

FIGURE 12. Variation of arm energy requirement for 13.8kVAC for 1.8MVA converter at (a) 12 kV DC (b) 9 kV DC (c) 6 kV DC.

It can be observed from Fig. 12 that as the DC voltage reduces, the SM capacitance requirement rises for all topologies except $HMMC_2$. $HMMC_2$ is immune to arm energy requirement changes with any change in DC voltage because both the DC and AC sides of $HMMC_2$ operate independently of one another, and a change in DC voltage does not impact as long as the power remains constant. For $HMMC_1$, the impact of change in DC voltage for E_{unit} requirement is most pronounced. For unity power factor (*P.F.*)=1, the E_{unit} increases 274% from 22.04 kJ/MVA to 82.4 kJ/MVA as DC voltage changes from 12kV to 6kV. As DC voltage decreases from 12kV to 6kV, the modulation ratio increases from 1.86 to 3.73, resulting in more circulating energy without traveling to the AC side. This circulating energy increases the required capacitance for MMCs. The arm energy requirement for $HMMC_3$ also increases with lowering DC voltage. For *P.F.*=1, the E_{unit} increases 87% from 14.82 kJ/MVA to 27.7 kJ/MVA as DC voltage changes from 12 kV to 6 kV. As observed, the change required per unit energy per arm with a reduction in DC voltage in $HMMC_3$ is less pronounced than in $HMMC_1$.

It can be inferred from Fig. 12 that $HMMC_3$ has the lowest E_{unit} and, consequently, capacitance requirement of any topology among the four options, especially at lower DC voltages like 9 kV and 6 kV. As can be observed from Fig. 12, the MMC has comparable capacitance requirements as $HMMC_3$ for a DC voltage of 9 kV. At *P.F.*=1, $HMMC_1$ has a E_{unit} requirement of 21.06 kJ/MVA, which is 17% smaller than the 25.59 kJ/MVA required for MMC. But at even lower DC voltages, the required capacitance is multiple times that of $HMMC_3$. At 6kV, the E_{unit} requirement for MMC is 61% more than $HMMC_3$ for *P.F.*=1. This can be attributed to the fact that at higher modulation ratios than 1.4, the arm voltage of $HMMC_3$ traverses through both positive and negative voltages over one line cycle. The arm currents, on the contrary, remain positive for such modulation ratios of more than 1.4. This results in the direct cancellation of accumulated arm energy, culminating in a lower total arm energy requirement. It is also important to highlight here that the capacitance requirement is similar for the same magnitude of positive and negative power factors, verifying that the capacitance requirement is similar for both the rectifier and inverter mode of operation for similar parameters.

The curves showing variations in E_{unit} values as a function of changing modulation index ($M=2V_{AC}/V_{DC}$) for *P.F.*=1 and *P.F.*=0 are shown in Fig. 13(a) and (b), respectively. As can be observed, for *P.F.*=1, $HMMC_3$ and $HMMC_1$ have minimum arm energy requirements around M=1.26. FB-MMCs also have an optical operating M at 1.41, as observed from Fig. 13. This can be attributed to minimal energy exchange at this modulation ratio, as discussed in [41], [42]. As M increases beyond 3.8, $HMMC_3$ tends towards $HMMC_2$, whereas E_{unit} for both MMC and $HMMC_1$ increases drastically, resulting in a much large arm capacitance requirement. Consequently, the proposed $HMMC_3$ solution is better from an arm energy perspective for any modulation index higher than 1.8. For the *P.F.*=0 case, the arm energy requirements for $HMMC_1$ and $HMMC_2$ are similar and constant. $HMMC_3$ can be observed to have a lower arm energy requirement for such cases beyond M=2.4.

C. SEMICONDUCTOR LOSSES

Efficiency is a key consideration in topology selection, especially for MV high/medium power converters. This subsection compares the efficiency of FB-MMC with the three HMMCs. The semiconductor losses are the primary source of losses

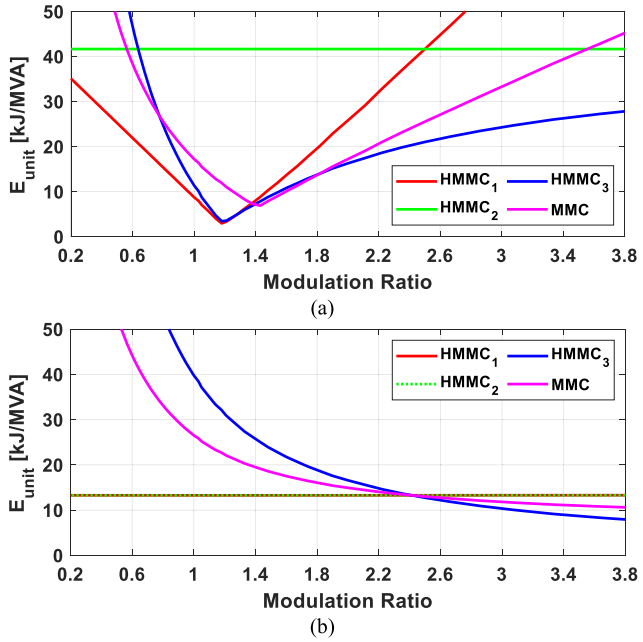

FIGURE 13. Variation of per unit arm energy (a) *P.F.*=1 (b) *P.F.*=0.

TABLE 4. Switching Modules Used for Loss Comparison

Location	Module	Manufacturer	Type	Rated blocking voltage
MVSS	CM600HG-130H	MITSBUSHI	IGBT	6.5 kV
SM	CM300DY-34T	MITSUBISHI	IGBT	1.7 kV

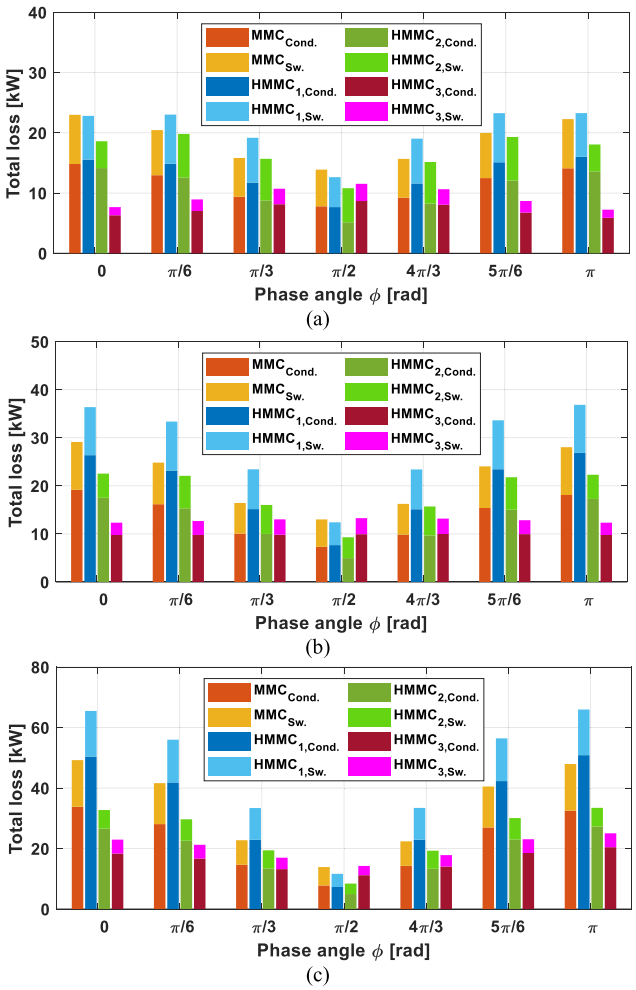

FIGURE 14. Loss distribution for 13.8 kV AC for 1.8 MVA converter at (a) 12 kV DC (b) 9 kV DC (c) 6 kV DC.

in power electronic converters and can be divided into conduction and switching losses. For loss calculation, converter models are developed within commercial software, PLECS, considering switch and diode on-state resistance and switching energy information from datasheets. For this comparison, commercial switching modules are used. The two modules with relevant characteristics are presented in Table 4. The results for comparison are presented in Fig. 14. All three cases highlighted in Table 1 are considered, with the total power for all cases chosen to be 1.8 MVA.

Results for the 12 kV DC bus are presented in Fig. 14(a). As can be observed, $HMMC_3$ has lower conduction and switching losses except P.F.=0 among all considered options. This can be primarily attributed to the lower total device requirements for $HMMC_3$ and the zero-voltage turn-on and turn-off. Also, it is critical to observe that as the power factor changes from resistive ($P.F.=\pm1$) towards inductive load ($P.F.=0$), all topologies except $HMMC_3$ have lower losses. This is because arm current in these topologies is directly proportional to either only DC current or AC current or the sum of both. $HMMC_3$, on the contrary, has an arm current pattern such that DC and AC currents oppose each other. So as the DC current continues to reduce from resistive to inductive load due to less real power being delivered, the overall current becomes dominated by AC. For $HMMC_3$, this results in more arm current and, consequently, higher losses. Considering that the losses for the negative and positive power factors are very similar for the same power factor magnitude, it can be confirmed that the inverter and rectifier operations have similar loss patterns. The slight variation between the two can be accounted for by the different current paths through either the diode or switch.

For 9 kV DC voltage and the same 13.8 kV AC, it can be observed from Fig. 14(b) that $HMMC_3$ has the lowest losses among all topologies, except at the $P.F.=0$ case. This is due to lower number of switching devices used in $HMMC_3$ as well as lower arm currents at $P.F.\neq0$. Also, unlike the 12 kV DC operation case, where the losses increase by loading change from resistive to inductive, the losses in $HMMC_3$ remain almost consistent for the 9 kV DC operation. This can be attributed to two opposing factors: an increase in AC current compared to DC, resulting in lower total current, and a significant change in arm current pattern as observed from (13) and Fig. 9, resulting in higher switching losses. $HMMC_2$ has 6.2% lower losses at zero power factor than $HMMC_3$ on account of lower SM switching devices resulting in significantly lower conduction losses. At $P.F.=1$, $HMMC_1$ has 194%, and MMC has 136%

TABLE 5. Summary of Comparison Study

Case 1 (13.8kVAC/12kVDC)				
Topology	**FB-MMC**	**HMMC$_1$**	**HMMC$_2$**	**HMMC$_3$**
Device Number	384(L) (1 p.u.)	264(L)+24(H) =288 (0.75 p.u.)	132(L)+54(H) =186 (0.48 p.u.)	144(L)+36(H) =180 (0.47 p.u.)
E_{unit} (kJ/MVA at PF=1)	15.11 (1 p.u.)	22.04 (1.46 p.u.)	41.66 (2.78 p.u.)	14.82 (0.98 p.u.)
Device Losses (kW at PF=1, Power=1.8MVA)	22.99 (1 p.u.)	22.81 (0.99 p.u.)	18.60 (0.81 p.u.)	7.66 (0.33 p.u.)
Case 2 (13.8kVAC/9kVDC)				
Topology	**FB-MMC**	**HMMC$_1$**	**HMMC$_2$**	**HMMC$_3$**
Device Number	360(L) (1 p.u.)	264(L)+24(H) =288 (0.80 p.u.)	132(L)+48(H) =180 (0.5 p.u.)	168(L)+36(H) =204 (0.57 p.u.)
E_{unit} (kJ/MVA at PF=1)	25.598 (1 p.u.)	41.67 (1.63 p.u.)	41.66 (1.63 p.u.)	21.06 (0.83 p.u.)
Device Losses (kW at PF=1, Power=1.8MVA)	29.125 (1 p.u.)	36.36 (1.25 p.u.)	22.54 (0.77 p.u.)	12.33 (0.43 p.u.)
Case 3 (13.8kVAC/6kVDC)				
Topology	**FB-MMC**	**HMMC$_1$**	**HMMC$_2$**	**HMMC$_3$**
Device Number	312(L) (1 p.u.)	264(L)+12(H) =276 (0.88 p.u.)	132(L)+54(H) =186 (0.60 p.u.)	192(L)+36(H) =228 (0.73 p.u.)
E_{unit} (kJ/MVA at PF=1)	44.62 (1 p.u.)	82.40 (1.85 p.u.)	41.66 (0.93 p.u.)	27.7 (0.62 p.u.)
Device Losses (kW at PF=1, Power=1.8MVA)	49.23 (1 p.u.)	65.49 (1.33 p.u.)	32.72 (0.66 p.u.)	22.95 (0.47 p.u.)

higher losses than HMMC$_3$. These higher losses are due to the high DC current going through both arms simultaneously. Compared to MMC, HMMC$_1$ has more losses because the peak DC current is much higher on account of trapezoidal current allocation.

At a 6 kV DC bus shown in Fig. 14(c), the DC side current becomes exceedingly dominant in loss distribution. As the power factor changes towards zero, the DC current tends to zero. This results in a different loss distribution pattern and sharp changes in loss distribution with a change in power factor. HMMC$_3$ is still the optimal topology near non-zero power factors due to lower SM count, followed very closely by HMMC$_2$, which becomes the most efficient topology at inductive loading. MMC and HMMC$_1$ have much higher losses compared to the other two topologies at non-zero power factor due to the much higher DC going through both arms.

D. SUMMARY OF COMPARISON STUDY

The results of the comparison study are summarized in Table 5 in terms of per unit (p.u.) comparison with FB-MMC. The terms in green are an improvement over FB-MMC, whereas those in red are worse. The low voltage and high voltage switching devices are also delineated with symbols, (H) and (L), respectively. As can be observed, HMMC$_3$ has a better performance compared to other HMMCs and FB-MMC across the whole range of chosen high-AC/low-DC operating points. The optimal operating point can be chosen based on the priority in terms of capacitor sizing, devices, or losses for the particular application under consideration.

IV. PRACTICAL CONSIDERATIONS

While the analysis presented in earlier sections establishes that HMMCs can be an improvement over FB-MMC in some crucial aspects, HMMCs also introduce some complexities not observed in conventional MMCs. This section analyzes two of these complexities introduced by HMMCs: MVSSs' impact on HMMC performance and the DC split capacitor and snubber necessity in HMMCs. These differences are highlighted comprehensively, providing guidelines for the practical operation and commercialization of HMMCs.

A. MVSS DEAD-TIME CONSIDERATIONS

The MVSS deadtime requirement for each HMMC can be evaluated by analyzing HMMC operation under the worst-case switching arrangement. The worst-case switching arrangement for MVSS in HMMCs is when all the MVSS in the same phase turn on at the same time. For HMMC$_1$, as observed from Fig 3(a), if all MVSSs: S_1-S_4 are on at the same time, the DC side would be shorted, causing DC shoot-through fault. It is critical to avoid this, and consequently, there is a necessity to use dead time in HMMC$_1$. Similarly, as observed from Fig. 3(b), for HMMC$_2$, if all four MVSSs: S_1-S_4, are accidentally on at the same time, the DC side can be shorted. This is undesired, and hence HMMC$_2$ also requires a dead time for MVSS. On the contrary, as can be inferred from Fig. 3(c), such deadtime restrictions are not necessary for HMMC$_3$. Even when all four switches, S_1-S_4, are on at the same time for HMMC$_3$, no DC shoot-through is expected. Moreover, around the AC voltage's zero crossover point, each arm's voltage is around $0.5V_{DC}$. Considering MVSSs are on, both arms can combine to handle the DC voltage, V_{DC}. This further eliminates any possibility of a high shoot-through current. Consequently, the deadtime requirements can be waived for HMMC$_3$, thus preventing it from complications like load current interruption and increased total harmonic distortion (THD) due to dead time.

B. DC SPLIT CAPACITOR AND SNUBBER NECESSITY

The DC Split capacitor can be a key cost consideration for MV applications. Some previous works have recommended the use of DC split capacitors in HMMCs [29] to support commutation, while others have explored its exclusion [30]. This subsection clearly delineates the necessity of such DC split capacitors. If the sum of midpoint currents from each phase of three-phase HMMC can be maintained at zero throughout the converter operation, there is no necessity for a DC split capacitor. The midpoint current for HMMC$_1$, HMMC$_2$, and HMMC$_3$ was discussed in the last section. Calculating the sum of the midpoint current across the three-phase based on the arm current patterns provided in this paper, it can be shown that the midpoint current across the HMMCs is zero at each point, irrespective of power factor or modulation index, and

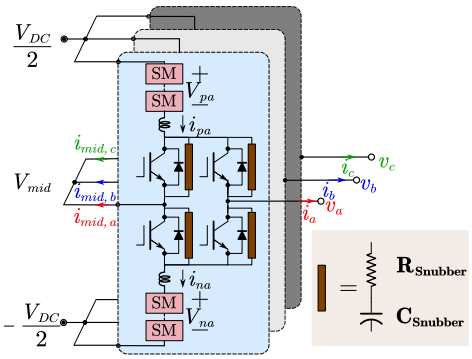

FIGURE 15. HMMC$_3$ with RC snubber.

TABLE 6. Parameters for Experimental Setup

Location	Module/Controller	Manufacturer	Type	Rated blocking voltage
MVSS	CM600HG-90H	MITSBUSHI	IGBT	4.5 kV
SM	G3R20MT17K	Genesic	SiC MOSFET	1.7 kV
Controller	TMS320F28379D	TI	DSP	N/A
Controller	Cyclone V	Altera	FPGA	N/A

hence DC split capacitor is not necessary for the converter operation.

The split capacitor can also be useful to provide a path in cases where gate signals are lost, resulting in MVSSs being open for a period of time. In such cases, in the absence of a DC split capacitor, an additional current path must be provided to dissipate the energy stored in MVSS if it is interrupted mid-operation. A simple RC or RCD snubber, as shown in Fig. 15 for HMMC$_3$, can be utilized in such scenarios.

Adding a snubber is a very common practice for devices used in MV converters. The losses introduced by snubber are insignificant because of the low switching frequency of the MVSS. For the single-phase operation of HMMCs, on the contrary, split capacitors are a necessity since the midpoint current cannot be maintained at zero.

V. EXPERIMENTAL VERIFICATION

Medium voltage HMMC and FB-MMC prototypes are developed to verify the HMMC operation and compare it with FB-MMC. One of the developed SMs is shown in Fig. 16(a). It comprises of the main power board, including a 1.7 kV SiC switching device listed in Table 6 and its driver, a local control board, an auxiliary power supply (APS) secondary, and a modular capacitor bank, among others. The control signals are provided through optical fiber, and the SM can also measure and broadcast faults as well as SM capacitor voltage.

The converter arrangement for one phase, two SMs per arm HMMC$_3$ setup is shown in Fig. 16(b). As observed, the setup comprises of SMs, MVSSs, arm inductors, APS primary, and sensors as listed in Tables 6 and 7. Each phase uses a single APS primary that can supply 11 loads. The APS secondary, like the one in Fig. 16(a) is used in all converter

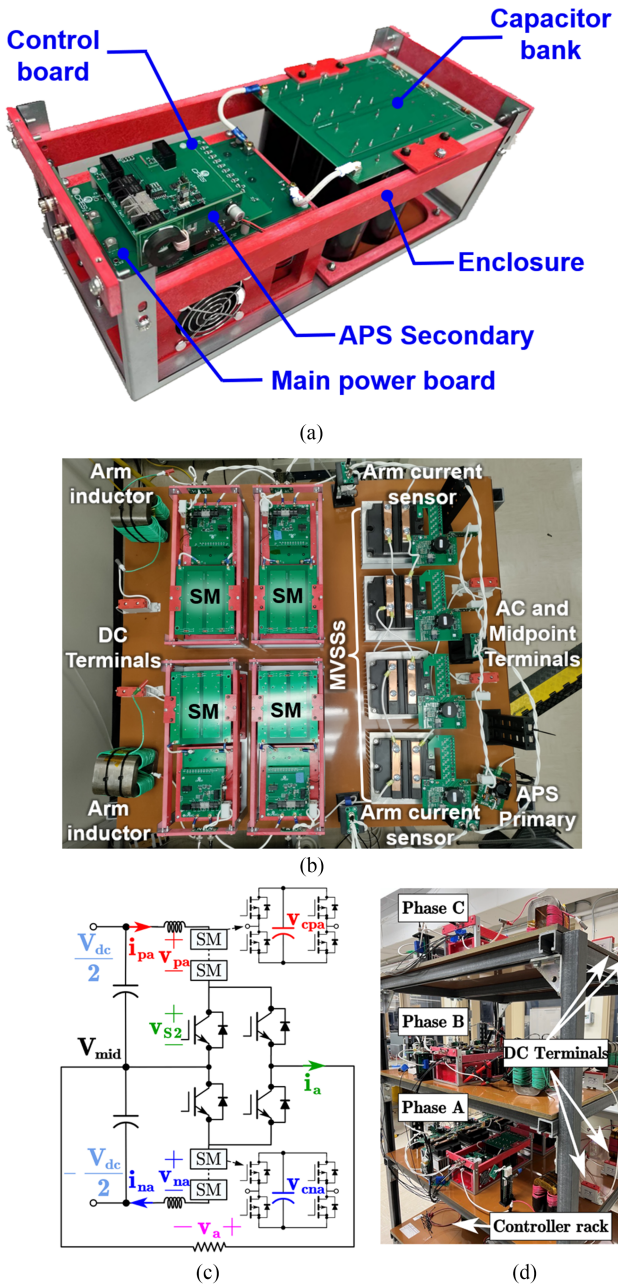

FIGURE 16. Experimental prototype (a) developed 1.1kV submodule using 1.7kV device (b) one-phase HMMC$_3$ setup with two SMs per arm (c) circuit configuration for one-phase tests (d) three phase HMMC$_3$ setup and converter rack with one SM per arm.

TABLE 7. Parameters for Experiments

		1-Phase	3-Phase
Submodules per arm	N	2	1
Submodule voltage	V_{SM}	400-800 V	550 V
DC voltage	V_{DC}	800V	800 V
AC voltage L-G pk-pk	$V_{AC,pk\text{-}pk}$	2160V	1600 V
AC frequency	f_{AC}	60 Hz	
Impedance	Z	120Ω	55Ω per phase
Module capacitance	C	0.667 mF	1 mF
Module switching frequency	f_{sw}	20 kHz	
Arm inductance	L_{arm}	2 mH	

components, including SMs, sensors, and MVSSs. The APS is a current transformer based, similar to the one discussed in [43], and has an insulation rating of over 10 kV. The single-phase equivalent test circuit with measured parameters is presented in Fig. 16(c). The three-phase converter rack with one SM per arm is also shown in Fig. 16(d). As observed, it has four shelves, with three shelves for the three phases and the last (bottom) shelf for the controller setup. All communication with the converter is completed using optical fibers. The important semiconductor devices and controllers used are listed in Table 6. A combination of DSP and FPGA is used to regulate the converter. Considering the lower number of SM available within the laboratory prototype, a SiC device switching at 20 kHz is used within SM. For practical considerations, the SiC device is not necessary because the number of modules will offset the switching frequency requirements. The key parameters for testing single-phase and three-phase converters are listed in Table 7.

A. SINGLE-PHASE VERIFICATION

As was concluded based on Sections III and IV, $HMMC_3$ is the most promising HMMC for high-AC/low-DC operating conditions. Consequently, $HMMC_3$ will be compared to FB-MMC in this section to evaluate its performance. It must be highlighted that peak arm voltage requirements for $HMMC_3$ and FB-MMC are greatly different, yet to maintain consistency of the output voltage levels, two submodules per arm are used for both converters.

The test results for the single-phase converter operation of $HMMC_3$ using two submodules per arm are shown in Fig. 17. As can be observed, the AC voltage peak is more than half the DC voltage verifying the low-DC/high-AC operation capability of the converter. The peak arm voltage for $HMMC_3$ is V_{AC}-0.5V_{DC}=680V. This permits the utilization of a low SM capacitor voltage reference of 400V per SM if two SM are used. As observed from Fig. 17, the arm current and arm voltage follow the ideal waveforms provided in Fig. 9, and the load current can be observed to be sinusoidal.

The MVSS blocking voltage can be observed to have a sinusoidal waveform for half a line cycle and follow a symmetrical pattern across all four MVSSs in the arm, as highlighted in Fig. 9. It can also be verified from Fig. 17 that MVSS blocking voltage has zero voltage turn-on and zero voltage turn-off, supporting lower switching losses as observed in Section III. This unique ability for zero voltage turn-on and turn-off will also assist in equal voltage sharing among the MVSS switches if several switches are connected in series for MVSS. The SM ripple for one capacitor in the upper and lower arm is also shown in Fig. 17 as v_{cpa} and v_{cna}, respectively. As observed, the capacitor voltage follows the set reference of 400V and has a peak-to-peak ripple of 49V.

The FB-MMC DC/AC operation at the same ratings as given in Table 7 for one-phase operation is presented in Fig. 18. It can be calculated that the arm voltage requirements for FB-MMC are much higher than $HMMC_3$ for the same

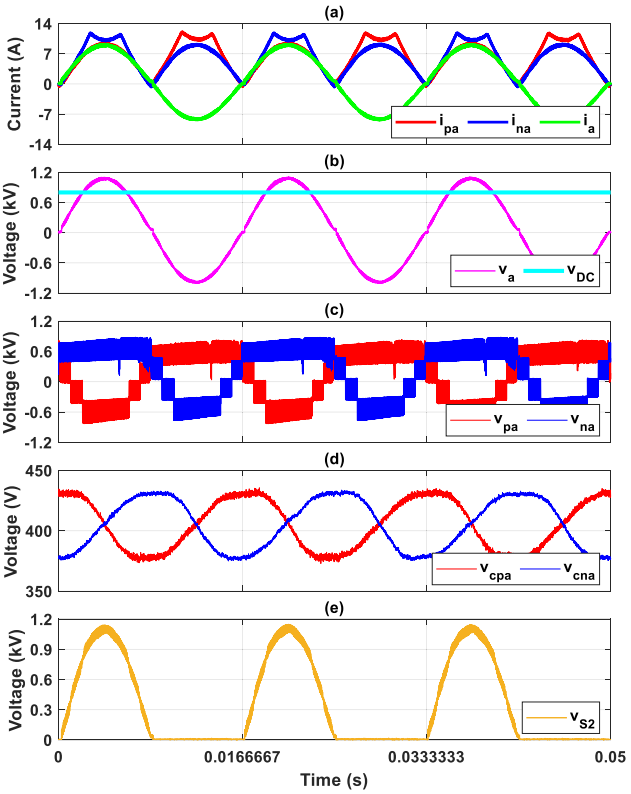

FIGURE 17. $HMMC_3$ operation (a) arm and load currents (b) input/output voltage (c) arm voltages (d) SM capacitor voltages (e) MVSS blocking voltage.

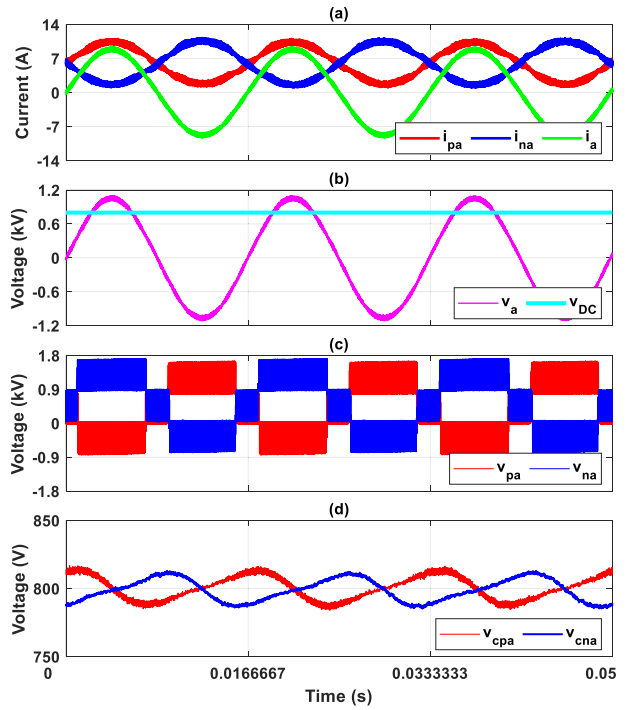

FIGURE 18. FB-MMC operation (a) arm and load currents (b) input/output voltage (c) arm voltages (d) SM capacitor voltages.

TABLE 8. Experimental Comparison Summary: Single Phase

	$HMMC_3$	MMC
Theoretical peak arm energy variation	21.85 J	27.9 J
Submodule capacitance	0.67 mF	0.67 mF
Number of SM per arm	2	2
SM reference voltage	400 V	800V
Theoretical SM ripple	41.4 V	26.4 V
Experimental SM ripple	49 V	29 V

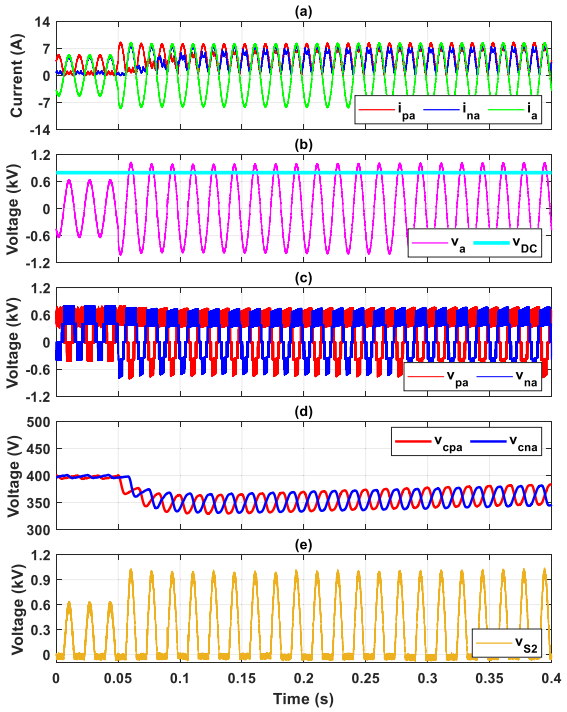

FIGURE 19. $HMMC_3$ transient operation with modulation ratio change at t=0.05s (a) arm and load currents (b) input/output voltage (c) arm voltages (d) SM capacitor voltages (e) MVSS blocking voltage.

operating conditions, with each arm expected to handle a peak of $V_{AC}+0.5V_{DC}$=1480V. This forces the requirement of much higher SM voltage at 800V, twice compared as $HMMC_3$. The capacitor voltage can be observed to follow the 800V reference with a peak-to-peak ripple of 29V. The arm voltage and arm current follow the set reference as well.

The experimental results obtained from both $HMMC_3$ and MMC can now be compared in Table 8.

The total arm energy requirement can be calculated as shown in Section III. As observed, the total arm energy requirements for MMC are about 20% more than for $HMMC_3$, which means keeping everything else consistent, the capacitor size of $HMMC_3$ would be 20% smaller than MMC for the given ratings in Table 4. But, since the SM reference voltage is different, the expected capacitor voltage ripple is slightly higher for $HMMC_3$ than MMC. The experimental and theoretical ripples can be observed to be matching well with a small difference due to non-idealities.

The transient performance of $HMMC_3$ is also verified experimentally, and results are presented in Fig. 19. For this verification, the modulation ratio of $HMMC_3$ is changed

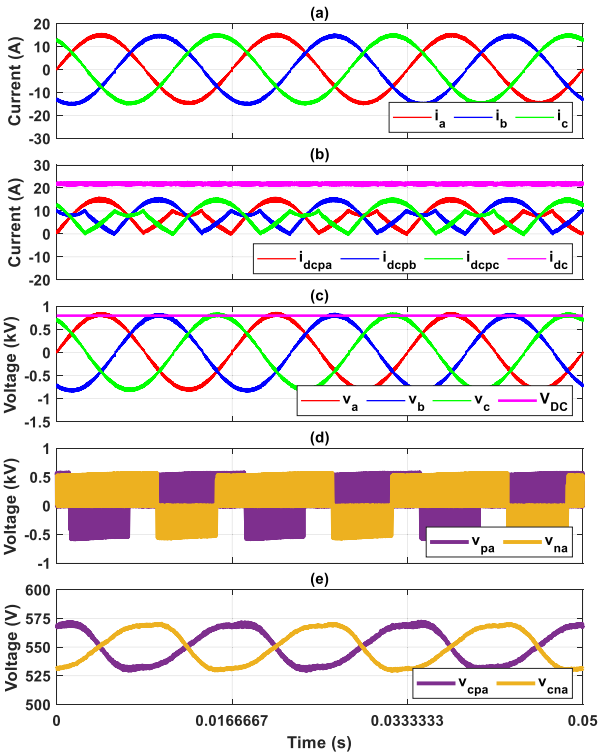

FIGURE 20. $HMMC_3$ Three-phase operation (a) load currents (b) DC side currents (c) input/output voltage (d) arm voltages: Phase A (e) SM capacitor voltages: Phase A.

mid-operation from 1.25 to 2.5 at t=0.05s. The DC voltage is fixed at 800V, and the SM reference voltage is 400V. As can be observed from Fig. 19, the arm current has a non-ideal behavior after modulation change but reaches a steady state within three-line cycles. Meanwhile, the capacitor voltage can also be observed to drop slightly for a short time after the introduced transient change, but the capacitor voltage balancing control can effectively bring the capacitor voltage back around the reference. The capacitor voltage ripple can be observed to increase as the modulation changes due to more arm energy flowing at higher power. The arm voltage can also be observed to have a higher number of levels after the change in the modulation index on account of higher arm voltage requirements after the change.

B. THREE-PHASE VERIFICATION

The three-phase converter operation of $HMMC_3$ for ratings provided in Table 7 is presented in Fig. 20. The results are captured without DC-split capacitors verifying that the converter can operate without the DC Split capacitors. As can be observed, the three-phase currents are well-balanced. The current harmonics are slightly higher in the three-phase case than single phase case due to the use of one submodule in the former instead of two in the latter. The DC current from the source is also shown as i_{dc}, with each arm's current from the DC source shown as $i_{dcpx,\ x=a,b,c}$ in Fig. 20(b). The AC and DC voltages are also shown in Fig. 20(c). As can be observed, the converter operates in high-AC/low-AC operation mode.

TABLE 9. Comparison on Number of Devices

	Conversion stage	Conversion ratio	Number of switches	Number of HFTs
SST	Converter	13.8 kV AC / 1 kV DC	396(L)	33
Proposed Solution (12 kV DC)	First: $HMMC_3$	13.8 kV AC / 12 kV DC	144(L)+36(H) =180	0
	Second: ISOP	12 kV DC / 1 kV DC	88(L)	11
	Total	13.8 kV AC / 1 kV DC	268 (33% fewer)	11 (66% fewer)
Proposed Solution (9 kV DC)	First: $HMMC_3$	13.8 kV AC / 9 kV DC	168(L)+36(H) =204	0
	Second: ISOP	9 kV DC / 1 kV DC	72(L)	9
	Total	13.8 kV AC / 1 kV DC	276 (30% fewer)	9 (73% fewer)
Proposed Solution (6 kV DC)	First: $HMMC_3$	13.8 kV AC / 6 kV DC	192(L)+36(H) =228	0
	Second: ISOP	6 kV DC / 1 kV DC	48(L)	6
	Total	13.8 kV AC / 1 kV DC	276 (30% fewer)	6 (81% fewer)

The submodule voltages for phase A, v_{cpa}, and v_{cna} are also presented in Fig. 20(e), demonstrating that arm voltage is both positive and negative, as expected for higher modulation ratios. The submodule voltages for phase A are shown and can be seen to be balanced well around the set reference of 550V.

VI. COMPARISON WITH SOLID STATE TRANSFORMER

It is demonstrated in this paper that the proposed $HMMC_3$ topology can be proven to be better than FB-MMC for the AFE stage in the EV charging infrastructure on account of several key considerations. Yet, the comparison with SST can further provide key insights on the improvements of the proposed topologies compared to the state-of-the-art. While many different SSTs exist in the literature, a cascaded H-Bridge SST with dual active bridge SST modules is used for comparison. For the AFE and ISOP based solution, MV AC/DC converter is $HMMC_3$, followed by a DAB-based ISOP converter. The two main considerations for comparison are cost and volume.

Cost in power-electronic converters is primarily dependent on the number of active semiconductors utilized, which in turn directly influences the gate driver, auxiliary, and controllers needed. Consequently, the number of semiconductors utilized in SST is compared with $HMMC_3$ on the three conversion ratios listed in Table 9, with 6 kV, 9 kV, and 12 kV acting as intermediary stages for AFE-based solutions. The results are highlighted in Table 9. To maintain consistency, the SST Module and FB-SM in $HMMC_3$ are both using switches rated at 1.7 kV, with effective utilization of 1.1 kV. MVSS are rated at 6.5 kV with effective utilization of 4 kV. The 1.7kV switch and 6.5kV MVSS are represented by (L) and (H), respectively. The ISOP stage is completely independent of the AFE design and can use the device of any blocking voltage rating. For this analysis, to maintain consistency and standardization, 1.7kV devices are also considered for ISOP, resulting in the ISOP module rated voltage at 1.1kV.

As can be observed, the total number of devices required for conversion from MVAC to LVDC is lower in $HMMC_3$ compared to SST, providing device savings of over 30%. While some switches in SST might be rated lower and maybe more cost-effective, a large number of $HMMC_3$ devices are also low-cost slow-switching IGBTs. The volume of the proposed converter structure would be lower than SST, at least for 9 kV DC and 6 kV DC cases, due to lower insulation requirements. Moreover, the lower HFT requirements for the proposed solution also can help reduce the overall volume and weight. A more detailed study is necessary to fully compare the various SST options with combination of proposed MVAC/MVDC and various possible MVDC/LVDC solutions. Such a study is beyond the scope of this work, but future research would explore this extensively.

VII. CONCLUSION

A new family of three hybrid MMC converters for high-AC/low-DC applications is proposed and analyzed for MV applications. All three topologies utilize a unique combination of submodules and MVSS. Compared to conventional FB-MMC, one of the three proposed topologies, $HMMC_3$ has about 27% lower semiconductor device requirements, 38% smaller SM capacitor size, and has 53% lower losses than conventional FB-MMC when operating at 13.8kVAC/6kVDC operation. $HMMC_3$ also has soft turn-on and turn-off capabilities, contributing to lower losses and possibly much better voltage sharing among series devices within MVSS. The practical challenges like MVSS deadtime requirement and DC split-capacitor necessity are also explored, and it has been demonstrated that $HMMC_3$ doesn't require MVSS deadtime or DC split capacitor. The converter performance is evaluated using extensive single and three-phase MV experimental analysis, demonstrating significant savings on the number and costs of SMs, desirable soft turn-on and turn-off capabilities for MVSSs, and satisfactory transient performance. Additionally, the $HMMC_3$-based concept is compared to SST-based solutions, demonstrating considerable improvements for high-AC/low-DC voltage operations. The proposed converter can be a possible potential alternative within EV charging stations, ESS integration, HV/MV distribution and transmission networks.

REFERENCES

[1] The Paris Agreement-UNFCCC. 2016. Accessed: Jun. 13, 2022. [Online]. Available: https://unfccc.int/sites/default/files/resource/parisagreement_publication.pdf

[2] "Megapack: Massive Energy Storage." Accessed: Mar. 28, 2023. [Online]. Available: https://www.tesla.com/en_eu/megapack

[3] "TMEIC: Energy Storage." Accessed: Mar. 28, 2023. [Online]. Available: https://www.tmeic.com/products/energy-storage-0#

[4] A. Ahmad, Z. Qin, T. Wijekoon, and P. Bauer, "An overview on medium voltage grid integration of ultra-fast charging stations: Current status and future trends," *IEEE Open J. Ind. Electron. Soc.*, vol. 3, pp. 420–447, 2022.

[5] Global EV Outlook 2020, 2020. [Online]. Available: https://www.iea.org/reports/global-ev-outlook-2020

[6] K. Lebeau, J. van Mierlo, P. Lebeau, O. Mairesse, and C. Macharis, "Consumer attitudes towards battery electric vehicles: A large-scale survey," *Int. J. Electric Hybrid Veh.*, vol. 5, no. 1, pp. 28–41, Apr. 2013.

[7] M. Blenner and B. Rosen, "EVGO balances EV fast charging with 14 battery storage systems across 11 EVGO fast charging stations," Jun. 2009. [Online]. Available: https://www.evgo.com/about/news/evgobalances-ev-fast-charging-with-14-battery-storage-systems-across-11-evgo-fast-charging-stations/

[8] F. Lambert, "Tesla opens new V3 supercharger with solar and battery-looks like EV charging station of the future. Electrek," Jun. 2009. [Online]. Available: https://electrek.co/2019/07/18/tesla-v3-supercharger-station-las-vegas-solar-power-battery/

[9] S. Rivera et al., "Charging infrastructure and grid integration for electromobility," in *Proc. IEEE*, 2022, early access, Nov. 07, 2022, doi: 10.1109/JPROC.2022.3216362.

[10] S. Srdic and S. Lukic, "Toward extreme fast charging: Challenges and opportunities in directly connecting to medium-voltage line," *IEEE Electrific. Mag.*, vol. 7, no. 1, pp. 22–31, Mar. 2019.

[11] S. Rivera, S. Kouro, S. Vazquez, S. M. Goetz, R. Lizana, and E. Romero-Cadaval, "Electric vehicle charging infrastructure: From grid to battery," *IEEE Ind. Electron. Mag.*, vol. 15, no. 2, pp. 37–51, Jun. 2021.

[12] M. R. Khalid, I. A. Khan, S. Hameed, M. S. J. Asghar, and J.-S. Ro, "A comprehensive review on structural topologies, power levels, energy storage systems, and standards for electric vehicle charging stations and their impacts on grid," *IEEE Access*, vol. 9, pp. 128069–128094, 2021.

[13] C. Zhu, High-Efficiency, Medium-Voltage Input, Solid-State, Transformer Based 400-kW/1000-V/400-A Extreme Fast Charger for Electric Vehicles [PowerPoint slides], 2021. [Online]. Available: https://www.energy.gov/eere/vehicles/articles/high-efficiency-medium-voltage-input-solid-state-transformer-based-400-0

[14] A. Lahooti Eshkevari, A. Mosallanejad, and M. Sepasian, "In-depth study of the application of solid-state transformer in design of high-power electric vehicle charging stations," *IET Elect. Syst. Transp.*, vol. 10, pp. 310–319, 2020.

[15] J. Liu, S. Yue, W. Yao, W. Li, and Z. Lu, "DC voltage ripple optimization of a single-stage solid-state transformer based on the modular multilevel matrix converter," *IEEE Trans. Power Electron.*, vol. 35, no. 12, pp. 12801–12815, Dec. 2020.

[16] D. Dong, M. Agamy, J. Z. Bebic, Q. Chen, and G. Mandrusiak, "A modular SiC high-frequency solid-state transformer for medium-voltage applications: Design, implementation, and testing," *IEEE J. Emerg. Sel. Topics Power Electron.*, vol. 7, no. 2, pp. 768–778, Jun. 2019.

[17] J. E. Huber and J. W. Kolar, "Applicability of solid-state transformers in today's and future distribution grids," *IEEE Trans. Smart Grid*, vol. 10, no. 1, pp. 317–326, Jan. 2019.

[18] D. Bowermaster, M. Alexander, and M. Duvall, "The need for charging: Evaluating utility infrastructures for electric vehicles while providing customer support," *IEEE Electrific. Mag.*, vol. 5, no. 1, pp. 59–67, Mar. 2017.

[19] Z. Li, Y.-H. Hsieh, Q. Li, F. C. Lee, and C. Zhao, "Insulation design on high-frequency transformer for solid-state transformer," in *Proc. IEEE Energy Convers. Congr. Expo.*, 2021, pp. 1149–1155.

[20] Q. Chen, R. Raju, D. Dong, and M. Agamy, "High frequency transformer insulation in medium voltage SiC enabled air-cooled solid-state transformers," in *Proc. IEEE Energy Convers. Congr. Expo.*, 2018, pp. 2436–2443.

[21] J. W. Kolar and J. E. Huber, "Fundamentals and application-oriented evaluation of solid-state transformer concepts," in *Proc. Tut. Southern Power Electron . Conf.*, Dec. 2016, pp. 9–69.

[22] M. Steiner and H. Reinold, "Medium frequency topology in railway applications," in *Proc. Eur. Conf. Power Electron. Appl.*, 2007, pp. 1–10.

[23] Z. Li, C. Zhao, Y.-H. Hsieh, and Q. Li, "Partial fluctuating power control of resonant converter for solid-state transformer," in *Proc. IEEE Appl. Power Electron. Conf. Expo.*, 2022, pp. 770–776.

[24] L. Camurca, T. Pereira, F. Hoffmann, and M. Liserre, "Analysis, limitations, and opportunities of modular multilevel converter-based architectures in fast charging stations infrastructures," *IEEE Trans. Power Electron.*, vol. 37, no. 9, pp. 10747–10760, Sep. 2022.

[25] S. S. Thakur, M. Odavic, A. Allu, Z. Q. Zhu, and K. Atallah, "Analytical modelling and optimization of output voltage harmonic spectra of full-bridge modular multilevel converters in boost mode," *IEEE Trans. Power Electron.*, vol. 37, no. 3, pp. 3403–3420, Mar. 2022.

[26] J. Yu, "DC fault current analysis and control for modular multilevel converters," M.S. thesis, Virginia Tech., Blacksburg, VA, USA, 2016.

[27] J. Stewart, J. Motwani, J. Yu, I. Cvetkovic, and R. Burgos, "Improved power density of a 6 kV 1 mW power electronics building block through insulation coordination," in *Proc. 23rd IEEE Workshop Control Model. Power Electron.*, 2022, pp. 1–7.

[28] Y. Dong, J. Tang, H. Yang, W. Li, and X. He, "Capacitor voltage balance control of hybrid modular multilevel converters with second-order circulating current injection," *IEEE J. Emerg. Sel. Topics Power Electron.*, vol. 7, no. 1, pp. 157–167, Mar. 2019.

[29] J. Zhang, Y. Zhang, F. Deng, and Z. Din, "Overmodulation operation of hybrid modular multilevel converter with reduced energy storage requirement," *IEEE J. Emerg. Sel. Topics Power Electron.*, vol. 10, no. 3, pp. 2946–2958, Jun. 2022.

[30] M. M. C. Merlin et al., "The alternate arm converter: A new hybrid multilevel converter with DC-fault blocking capability," *IEEE Trans. Power Del.*, vol. 29, no. 1, pp. 310–317, Feb. 2014.

[31] H. R. Wickramasinghe, G. Konstantinou, S. Ceballos, and J. Pou, "Alternate arm converter energy balancing under parameter variation," *IEEE Trans. Power Electron.*, vol. 34, no. 4, pp. 2996–3000, Apr. 2019.

[32] M. M. C. Merlin et al., "The extended overlap alternate arm converter: A voltage-source converter with DC fault ride-through capability and a compact design," *IEEE Trans. Power Electron.*, vol. 33, no. 5, pp. 3898–3910, May 2018.

[33] E. M. Farr, R. Feldman, J. C. Clare, and O. F. Jasim, "The alternate arm converter 'extended-overlap' mode: AC faults," *IEEE Trans. Power Electron.*, vol. 36, no. 5, pp. 5371–5388, May 2021.

[34] D. Zhang, D. Dong, R. Datta, A. Rockhill, Q. Lei, and L. Garces, "Modular embedded multilevel converter for MV/HVDC applications," *IEEE Trans. Ind. Appl.*, vol. 54, no. 6, pp. 6320–6331, Nov./Dec. 2018.

[35] J. Liu, D. Dong, and D. Zhang, "A hybrid modular multilevel converter family with higher power density and efficiency," *IEEE Trans. Power Electron.*, vol. 36, no. 8, pp. 9001–9014, Aug. 2021.

[36] J. Yang, Z. He, J. Ke, and M. Xie, "A new hybrid multilevel DC–AC converter with reduced energy storage requirement and power losses for HVDC applications," *IEEE Trans. Power Electron.*, vol. 34, no. 3, pp. 2082–2096, Mar. 2019.

[37] J. Liu, D. Zhang, and D. Dong, "Modeling and control method for a three-level hybrid modular multilevel converter," *IEEE Trans. Power Electron.*, vol. 37, no. 3, pp. 2870–2884, Mar. 2022.

[38] X. Lin, L. Ravi, R. Burgos, and D. Dong, "Hybrid voltage balancing approach for series-connected SiC MOSFETs for DC–AC medium-voltage power conversion applications," *IEEE Trans. Power Electron.*, vol. 37, no. 7, pp. 8104–8117, Jul. 2022.

[39] Y. Tang, M. Chen, and L. Ran, "A compact MMC submodule structure with reduced capacitor size using the stacked switched capacitor architecture," *IEEE Trans. Power Electron.*, vol. 31, no. 10, pp. 6920–6936, Oct. 2016.

[40] J. Liu and D. Dong, "A flying capacitor hybrid modular multilevel converter with reduced number of submodules and power losses," *IEEE Trans. Ind. Electron.*, vol. 70, no. 4, pp. 3293–3302, Apr. 2023.

[41] Y. Gupta, "Modeling and control of modular multilevel converter," M.S. thesis, Virginia Tech, Blacksburg, VA, USA, 2022.

[42] K. Ilves, S. Norrga, and H. Nee, "On energy variations in modular multilevel converters with full-bridge submodules for Ac-Dc and Ac-Ac applications," in *Proc. 15th Eur. Conf. Power Electron. Appl.*, 2013, pp. 1–10.

[43] N. Yan, D. Dong, and R. Burgos, "A multichannel high-frequency current link based isolated auxiliary power supply for medium-voltage applications," *IEEE Trans. Power Electron.*, vol. 37, no. 1, pp. 674–686, Jan. 2022.

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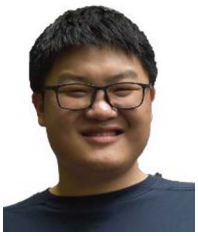

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