IEEE Open Journal of
Power Electronics

Received 29 January 2023; revised 22 February 2023; accepted 26 February 2023. Date of publication 1 March 2023;
date of current version 28 March 2023. The review of this article was arranged by Associate Editor Rafael Pea-Alzola.

Digital Object Identifier 10.1109/OJPEL.2023.3250762

An Integrated 50 V Boost Controller With Digitally-Assisted MPPT for Submodule PV Applications

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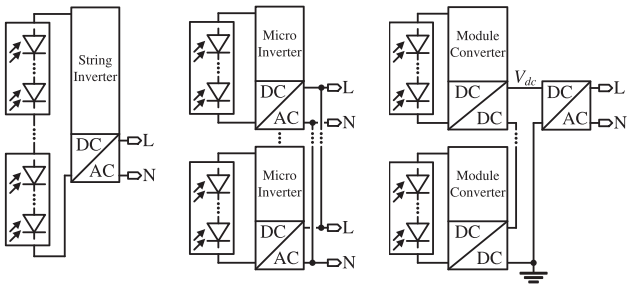
ABSTRACT This work introduces an integrated maximum power point tracking boost controller for photovoltaic submodule applications. The IC offers a wide input voltage range from 7 V to 24 V, whereas the output voltage is actively limited to 50 V. The presented design utilizes discrete, low-ohmic MOSFETs for the output stage and thus supports input power levels up to 144 W. The converter operates with peak-current-mode control at 300 kHz switching frequency in continuous conduction mode. During light load operation, the control transitions to direct input voltage sensing pulse-frequency-modulation (PFM) with input and output voltage dependent peak inductor current. Moreover, the low-side resistive current sense is explained in detail together with an inductor current replication circuit for precise high-side turn-off. The maximum power point tracker (MPPT) is based on an adjustable resistive sense element and a delta modulator and achieves 99.9% tracking efficiency, omitting any need for a high resolution analog-to-digital converter (ADC). In addition, the series connection of multiple DC/DC converters is examined. The peak system efficiency measures 98.4%. The application-specific integrated circuit (ASIC) is manufactured in an 0.18 µm HV-BCD process and occupies 6.25 mm^2 of silicon area.

INDEX TERMS Boost controller, Boost converter, DC/DC converter, light load efficiency, mode switching, MPPT, PFM, photovoltaic system, PV, solar.

I. INTRODUCTION

Renewable energy generation is an ever-increasing industry with strong growth over the past decades. Notably, the wind and photovoltaic (PV) sectors have undergone continuous expansion in the last decade and are seen as key drivers for future renewable energy generation [1]. In particular, the decreasing cost per kWh and the possibility for local electricity generation are major advantages of PV. The growing market of electrical vehicles and battery storage systems enforces this successful trend further [2], making it an appealing choice for private homeowners. Moreover, PV technology offers small and large scale solutions which can be configured flexibly. Technological progress will enable higher cell efficiencies by using Passivated Emitter and Rear Cell (PERC) architectures. In addition, thin film cells, such as copper indium gallium selenide (CIGS), offer new looks, shapes and form factors, enabling flexible structures with attractive cost and power per area [3].

Fig. 1 shows multiple solar system configurations. The most common architecture is depicted in Fig. 1(a), in which PV-modules are connected in series to a central string inverter. The summed overall voltage is thereby boosted automatically, which reduces the voltage drop across the wiring cables to a comparable small fraction and hence, reduces the associated losses. However, the disadvantage of using a common string current for all modules grows clear by considering partial shading. Single module or even submodular shading deteriorates the overall system performance significantly [4]. State-of-the-art inverters, such as the Sunny Boy inverters from SMA [5], are capable of proper maximum power point (MPP)-tracking and can securely avoid local MPP operation by searching for the global MPP periodically. Additionally,



(a) Conventional (b) Microinverter (c) Module DC/DC

FIGURE 1. Different PV system configurations: conventional single string inverter, microinverter per module and module DC/DC converter with central inverter.

multiple bypass diodes are added to standard PV-panels, which can short low irradiated modules. Nevertheless, partial shading leads to additional avoidable losses, due to non-optimal module level MPP-tracking. Moreover, nonuniform panel aging can be considered similarly to partial shading.

PV-panel degradation and lifetime effects are still subject of current research. Different root-causes lead to temporary and permanent cell degradation [6], [7]. Nonuniform and nonlinear deterioration can lead to large panel mismatch with major impact on system efficiency [8]. The modeling of these effects poses additional challenges [9]. Especially thin film panels are subject of reliability issues [10].

To counteract the disadvantage of single central inverter operation, microinverters had been introduced to the market cf. Fig. 1(b). They benefit from module level MPP-tracking and a comparably small solution size. Each module is operated in its individual MPP and therefore always contributes to the overall power generation. Moreover, panel mismatch over lifetime is fully compensated. In addition, new products offer live monitoring data for each panel [11]. Therefore, microinverters may regain market share, especially in small scale applications, like balcony PV. However, they are more expensive for large rooftop applications, compared to traditional string inverters.

Differential power processing (DPP) is another technique, also classified as module converters shown in Fig. 1(c). DC/DC converters are used to maximize the energy output of PV systems by processing the power difference between modules/submodules. Therefore, they operate in light load operation most of the time [12]. However, under partial shaded conditions, DPP-converters must be able to handle the full missing power to be as efficient as the aforementioned architectures. Additionally, communication channels between adjacent converters are necessary for MPP-tracking.

This work proposes an integrated MPP-tracking boost controller for submodule PV applications [13]. The PV system topology is shown in Fig. 1(c). All converter outputs are connected in series to a single inverter. The presented solution is ideally suited to be used in submodule applications. Therefore, a standard PV-panel is divided into three sub-strings, consisting of 20–24 cells. Each sub-string is fitted with one DC/DC converter, which increases the system granularity further and thereby enables submodular MPP-tracking with significantly better performance under partial shaded conditions. In addition, the solution size, complexity and cost can be reduced compared to microinverter systems.

Maxim Integrated designed a buck converter with MPP-tracking for submodule PV integration [14]. A buck converter has the advantage of a larger input to output voltage ratio, which determines the shading tolerance of the system. On the other hand, the output current is always larger, in contrast to a boost converter. Therefore, the inevitable wiring losses are increased. STMicroelectronics introduced a four-phase boost converter IC [15] with an input power compensation factor of four. The boost controller of this work limits V_{out} to 50 V and can thus balance different P_{in} ratios up to five. The integrated overvoltage protection ensures safe operation by overriding the MPPT and forcing the sub-string out of MPP. Moreover, the presented single inductor approach reduces complexity, is smaller than the multi-phase design of STMicroelectronics and uses less external components. This reduces PCB area and cost. Furthermore, this work proposes an MPPT which is based on an adjustable sense element combined with a mixed-signal implementation of a delta modulator with a feedback digital-to-analog converter (DAC). Therefore, in contrast to the majority of other MPPT implementations, no high resolution ADC is required to maintain excellent tracking efficiency across all input power levels. The use of discrete power switches provides greater flexibility in the power stage design to match the peak power of the actual PV panel. Therefore, the presented boost controller can be used for a very wide range of applications with various power ratings and different form factors, ranging from standard high power single-crystal silicon panels to flexible CIGS thin film technology.

The key advantages of the proposed MPP-tracking boost controller for submodular PV applications can be summarized as follows:

1) Superior shading management, due to finer granularity of submodular MPP-tracking.
2) Optimizing system efficiency through aggressive switching frequency reduction in discontinuous conduction mode (DCM). This is realized by targeting much higher V_{in}-ripple with input and output voltage dependent inductor peak current.
3) Peak-current-mode control with a low-side current sense resistor architecture that uses a high-side inductor current replica circuit for precise zero current FET turn-off in DCM.
4) MPPT and boost controller integration in one ASIC, reducing system complexity, size and power consumption, while maximizing tracking speed.
5) Digitally-assisted analog MPPT, operating with a fixed sense-voltage, which enables highest tracking efficiency across the full load range. This avoids decreasing tracking accuracy caused by limited ADC resolution.

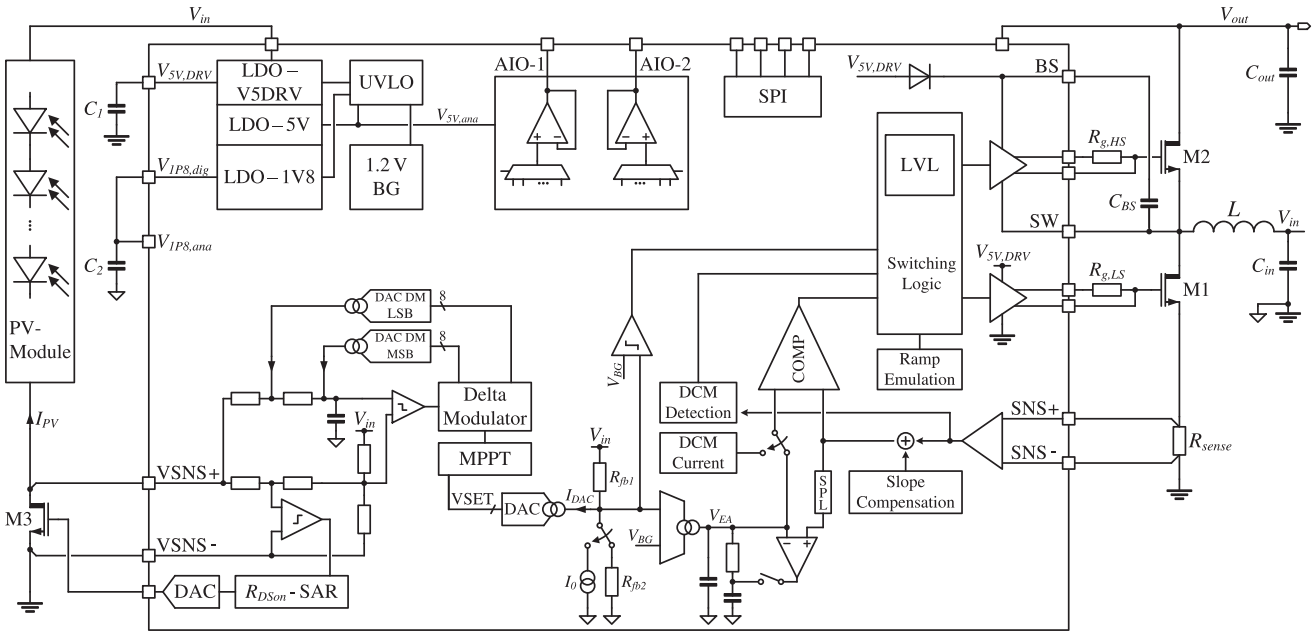


FIGURE 2. Block diagram of the MPPT Boost-Controller with external components. The ASIC integrates a MPPT and a peak-current-mode boost controller. The IC also includes a power management circuit with a bandgap voltage reference [16]. The SPI interface is used for prototyping.

II. SYSTEM ARCHITECTURE

Fig. 2 shows the block diagram of the MPP-tracking boost controller with external components for a single PV-panel sub-string. The system architecture is based on an all NMOS boost output stage with external power transistors. The developed boost controller with integrated low-side (LS) and high-side (HS) driver circuits regulates the input voltage of the PV source. The output behaves like a current source and is loaded with a fixed voltage rail. In Subsection II-B, a closer look is taken at the series connection of multiple boost converters and the corresponding performance under partially shaded conditions. The input voltage range measures 7 V to 24 V, whereas output voltages up to 50 V are supported. Therefore, very different panel/string configurations can be used, as well as different PV-panel technologies. The controller operates with peak-current-mode control and a constant switching frequency of 300 kHz in continuous conduction mode (CCM). A 8.2 μH inductor is used, which offers a good trade-off between inductor current ripple, magnetic losses and resistive winding losses. The ASIC has a built-in power management circuit for internal supply voltage generation, which is supervised by an undervoltage-lockout circuit, described in [17].

A. MAXIMUM POWER POINT TRACKING

The maximum power point tracker is based on a perturb-and-observe principle. However, the MPPT does not rely on a high resolution ADC for measuring current and voltage, but uses an adjustable resistance as a sense element together with a delta modulator feedback loop. The overall principle is based on [18] and has been adapted to a digitally-assisted analog circuit, feasible for full integration as described in [19]. The principal block diagram is depicted in the lower left corner of Fig. 2. The MPPT controls a current DAC which manipulates the feedback voltage of the boost converter control loop to regulate the PV-panel into its MPP, at which the following condition is fulfilled:

$$\frac{\partial I_{PV}}{\partial V_{PV}} = -\frac{I_{PV}}{V_{PV}}. \tag{1}$$

The right part of the equation is equal to a conductance, whereby the reciprocal value is proportional to the $R_{DS,\mathrm{on}}$ of the MPP-tracking MOSFET M3. The drain voltage V_{SNS+} is regulated by a DAC and a successive approximation register (SAR) algorithm to a fixed fraction of V_{in}. By that, a current perturbation leads to a voltage change at V_{SNS+}, which is sensed and tracked by the delta modulator. At the MPP, both weighted magnitudes – V_{in} change and I_{PV} variation – are equal. Depending on the sign of the relation in (1), the current DAC value is altered. Thereby, the perturbation is simply done by varying the PV-panel voltage with the same DAC.

$$V_{\mathrm{in}} = 6\,\mathrm{V} + I_{DAC} \cdot R_{fb1} \tag{2}$$

The fixed voltage term in (2) results from the resistive divider R_{fb1} and R_{fb2} and the bandgap voltage V_{BG}.

$$6\,\mathrm{V} = \left(\frac{R_{fb1}}{R_{fb2}} + 1\right) \cdot V_{BG} \tag{3}$$

The overall system stability is guaranteed by separating the outer boost voltage loop and the MPPT loop by one order of magnitude: Thus, a mixed-signal implementation of the $R_{DS,\mathrm{on}}$-loop is the key to a successful integration of large time constants.

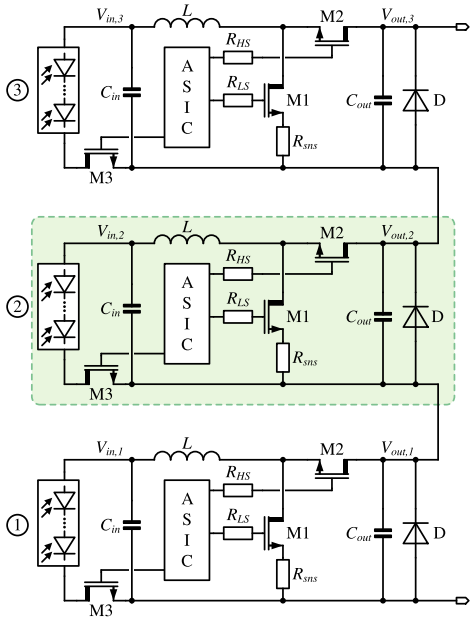


FIGURE 3. Concept schematic of three MPPB-converters connected in series, representing one PV-panel, where each converter is supplied by one sub-string.

The biggest advantage of the chosen MPPT implementation is the constant V_{ds}-voltage sensing approach. It widens the dynamic measurement range, allowing for low input power levels, occurring at small panel currents. This is in contrast to conventional ADC implementations, in which the limited ADC resolution is dictating the MPP-tracking accuracy for low insolation, leading to poor tracking performance. Moreover, sense losses at high solar insolation are minimized and measure only 0.4%, independent of the current and input voltage level. In addition to that, the digitally-assisted feedback loop of the delta modulator is based on two overlapping 8 b DACs. This eases the design significantly compared to conventional high resolution ADCs with strict linearity requirements for precise absolute PV voltage and current measurements.

B. SERIES CONNECTION OF MULTIPLE BOOST CONVERTERS

The system efficiency of partially shaded PV-arrays can be enlarged by reducing the overall size of in series connected modules – in other words, the number of serial connected cells has to be reduced. This work presents a PV-system which uses three boost converters for a 370 W module. This features a good trade-off between number of converters, input voltage and power range. The DC/DC converter is designed with discrete power transistors to maximize the efficiency with low $R_{DS,\text{on}}$ switches. The specific transistors have to be selected according to the rated string power.

Fig. 3 depicts the series connection of three MPP-tracking boost converters (MPPB), representing the electronics added to one PV-panel. For different insolation and, therefore, unevenly distributed input power levels, the output voltages of the converters deviate proportionally, as the output current is common for all converters, due to their series connection. Hence, the shading tolerance is dictated by the maximum output to input voltage ratio. If the input power drops under the minimum relative threshold – in comparison to the largest panel P_{in} – the affected controller stops switching. Because of the HS body diode, the panel still delivers power to the system, but with larger losses. If the sub-string is further shaded, the added discrete Diode D conducts and disconnects the PV string from the system. The output capacitance C_{out} stabilizes the boosted string voltage and filters the V_{out}-ripple.

III. CONTROL LOOP DESIGN

The boost controller regulates the input voltage, and therefore the sub-string voltage, to the desired set point. The target input voltage, is determined by the MPPT. As defined by the perturb-and-observe principle, the MPPT sets a new target voltage, observes the power change, and determines whether to decrease or increase V_{in} in the next step. Because of the control loop nesting, the inner input voltage regulating boost loop needs to be faster than the outer MPP loop.

For low input power levels, the capacitive switching losses in the external power stage exceed the resistive losses significantly. Therefore, a pulse-frequency modulation scheme has been implemented, which reduces the switching frequency depending on inductor current, input, and output voltage conditions. Due to the increased switching period, a different compensation of the outer voltage loop would be necessary, which would lead to an unrealistic large compensation capacitance to achieve a sufficient low transition frequency. To overcome this challenge, the inductor peak current is determined by a fixed relation instead of using the error amplifier (EA) output. A direct input voltage sensing method is used to detect and schedule the next switching cycle. Thereby, the EA is no longer part of the feedback loop during DCM operation.

A. CURRENT SENSE IMPLEMENTATION

The current sense core circuit is depicted on the right-hand side of Fig. 4. An external 10 mΩ LS sense resistor reduces the conduction losses due to the duty-cycled operation. The measured shunt voltage is level-shifted by $V_{GS,M0}$ and applied across the integrated resistor R_1. Thus, the following relationship between the LS current – which is equal to the inductor current – and I_x can be obtained:

$$I_x = I_{LS} \cdot \frac{R_{\text{sense}}}{R_1}. \tag{4}$$

I_2 subtracts an additional offset current from the output and consequently extends the measurement range to negative currents. The output current is split into two identical tail currents – the first ($I_{CS,1}$) is used as the actual current sense output, whereas the second branch is used for DCM detection. The high input power rating, including PV currents up to 12 A, and the additional slope compensation ramp voltage limit the possible current sense gain to 1.1 in CCM, due to the limited

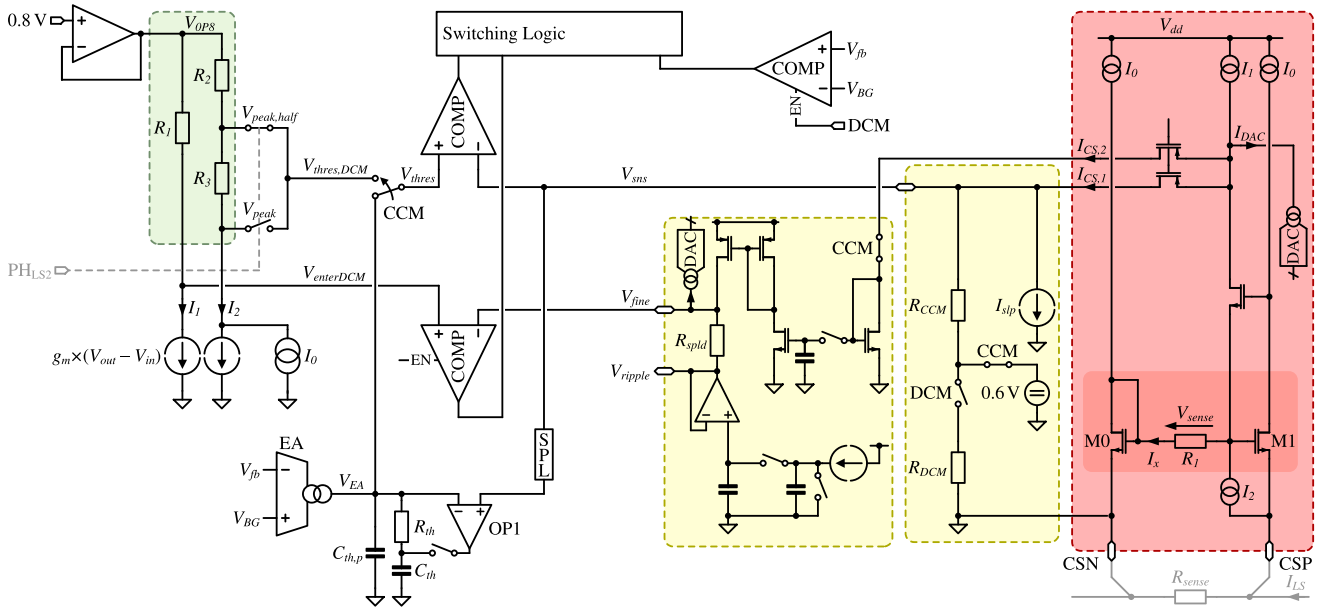


FIGURE 4. Block-level schematic of the converter control loop principle.

dynamic range. Hence, in DCM, where no slope compensation is required and only currents smaller than 6.5 A are measured, the gain is increased to 7.4. The gain adjustment is realized by reducing the internal sense resistor R_1 and by adding R_{DCM} to the load resistance. Good matching is guaranteed by using the same unit resistor for R_1 and for the load. Thus, temperature effects are canceled. Nevertheless, a 5 bit current DAC is used for calibration to compensate process variations of the sense resistor. In addition, a V-to-I converter, based on the same resistor type, is used for local bias current generation. Therefore, the necessary calibration range is smaller and temperature changes do not alter V_{sns}. The second output current $I_{CS,2}$ is used to determine the transition point between CCM and DCM. For this purpose, the peak inductor current is sampled, amplified and compared to the reference voltage $V_{enter,DCM}$. Additionally, half of the inductor current ripple (V_{ripple}) is added to the sampled peak current. This is inevitable to account for the wide ranging ripple current magnitudes, dependent on V_{in} and V_{out}, to achieve a precise hysteresis for each operating point.

$$70\% \cdot 0.5 \cdot I_{peak,DCM} > \overline{I_{L,CCM}} \tag{5}$$

$$\overline{I_{L,CCM}} = I_{peak,CCM} - \frac{I_{ripple}}{2} \tag{6}$$

$\overline{I_{L,CCM}}$ is the average inductor current in CCM, whereby $I_{peak,CCM}$ stands for the peak inductor current in CCM operation.

Fig. 5 shows the block level schematic of the inductor current ripple generation circuit principle. The capacitance C_1 can be trimmed for calibration.

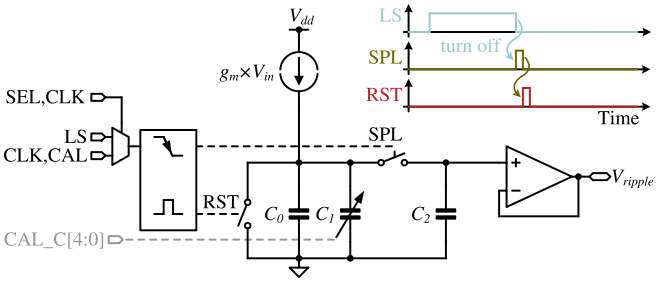


FIGURE 5. Circuit diagram of the inductor ripple current replication.

B. REFERENCE GENERATION AND OPERATION MODE CHANGE

(5) shows the relation between peak inductor current and the smallest possible average input current for which the controller still operates in CCM. When the EA reduces the peak inductor current further and $V_{enter,DCM}$ exceeds V_{fine}, the converter transitions into DCM operation. On circuit level, the reference voltage is generated with a g_m-stage and a suitable resistor, pictured in the left part of Fig. 4. The reference potential for the peak inductor current V_{thres} is synthesized by the same principle. Therefore, matched relations are realized, which ensures a stable hysteresis across PVT-variations. This results in the following equation for the peak inductor current in DCM.

$$1.55\,\text{A} + 0.114\,\frac{\text{A}}{\text{V}} \cdot (V_{\text{out}} - V_{\text{in}}) \tag{7}$$

Due to the LS current sense principle, there is no inductor current information available during the HS-phase. While in CCM, with peak-current-mode control, this information is not necessary, the zero-crossing of I_L becomes an important

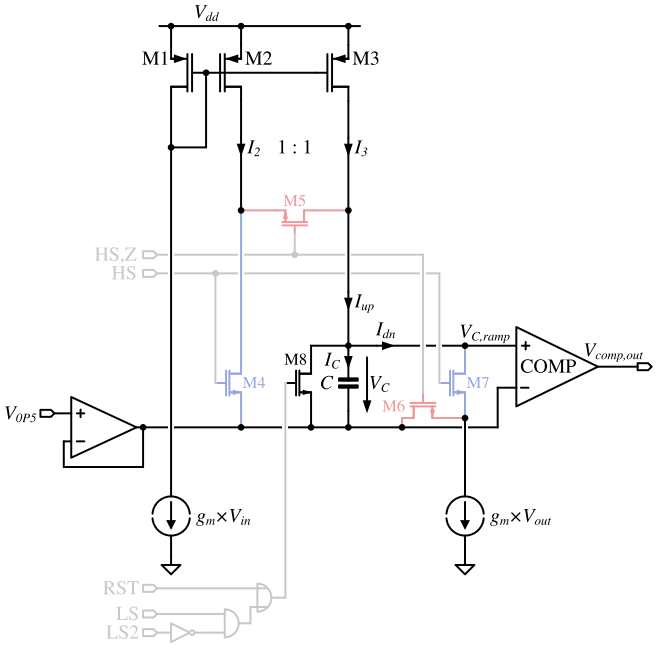


FIGURE 6. Principle schematic of the inductor current replication circuitry, which uses V_{in} and V_{out} dependent current sources together with a capacitor to emulate the integrating inductor behavior.

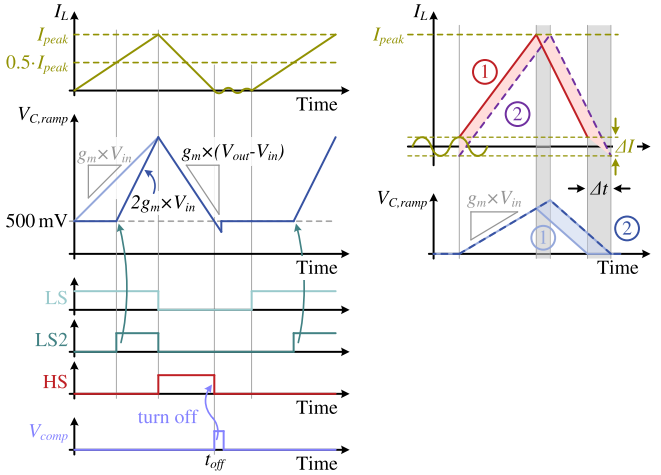


FIGURE 7. Idealized waveforms of the I_L replica circuit.

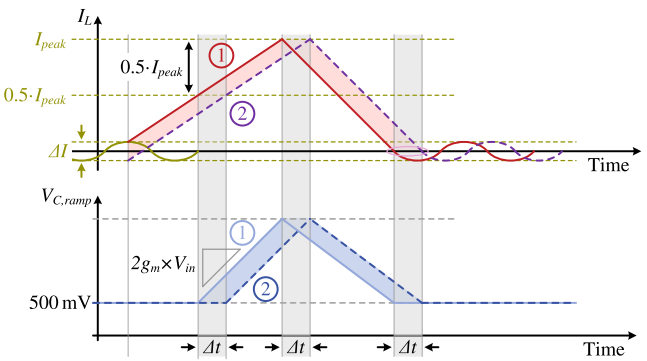


FIGURE 8. Precise HS turn-off, omitting residual I_L offset current.

measure in DCM with synchronous rectification. If the HS transistor is turned off too late, a negative inductor current builds up, which deteriorates the efficiency. Likewise, an early HS turn-off engages the body diode to conduct the inductor current with increased conduction losses. Direct $V_{DS,HS}$ sensing is very challenging to implement, due to only 4.3 mΩ on-resistance of the external switches. In consequence, an inductor current replication circuit has been implemented, which replicates I_L during both converter phases. Therefore, the zero-crossing can be detected with much higher precision and additional conduction losses are minimized.

C. INDUCTOR CURRENT REPLICA GENERATION

Fig. 6 shows the simplified inductor current replication circuit. The core consists of two voltage controlled current sources, dependent on V_{in} and V_{out} and the integration capacitor C. Consequently, both g_m-stages represent the inductor, by generating a current proportional to the voltage across L. During the magnetization phase it is equal to V_{in}, whereas L is demagnetized by $V_{\text{out}} - V_{\text{in}}$. Fig. 7 illustrates the different phases of a full switching cycle during DCM operation graphically. In fact, the LS integration phase is split into two sub-steps. For the first half, the capacitor is shorted by M8 and thus, V_C stays at 0 V. During the second phase, namely LS2, the integration capacitance is charged with twice the current. I_{up} measures:

$$I_{\text{up}} = I_2 + I_3 = 2 \cdot g_m V_{\text{in}}. \tag{8}$$

LS2 is triggered by the main comparator of the current loop, which compares the measured inductor current with $V_{peak,half} = 0.5 \cdot I_{peak}$, cf. Fig. 4. Once surpassed, M8 is turned off and C is charged by I_{up}. Additionally, the comparator reference is switched to the full peak inductor current value. When the output stage enables the HS transistor, M5 isolates I_2 from I_{up}, whereas M7 is turned on. Therefore, C is discharged by $I_{dn} = g_m \cdot V_{\text{out}}$. During the HS-phase the overall capacitor current measures:

$$I_C = I_{\text{up}} - I_{dn} = g_m \cdot (V_{\text{in}} - V_{\text{out}}). \tag{9}$$

When the capacitor voltage crosses 0 V, $V_{C,\text{ramp}}$ reaches its initial value of 500 mV, which is detected by the connected comparator. Consequently, the inductor current has reached 0 A and the controller can switch the output stage to high impedance – idle state. At the same time the integration capacitor is discharged through M8 again.

The reason for the chosen modified LS-integration time LS2 is to switch off the HS at precisely 0 A. Otherwise, the HS would be turned off with the exact same offset current which is present during the start of the LS-phase, induced by the inevitable inductor current ringing in idle state. Dependent on the exact input and output voltages, the ringing magnitude ΔI would significantly influence the HS switch off point from cycle to cycle and therefore the body diode conduction time. Fig. 8 depicts the timing relationship of the modified implementation. By adding the additional inductor threshold

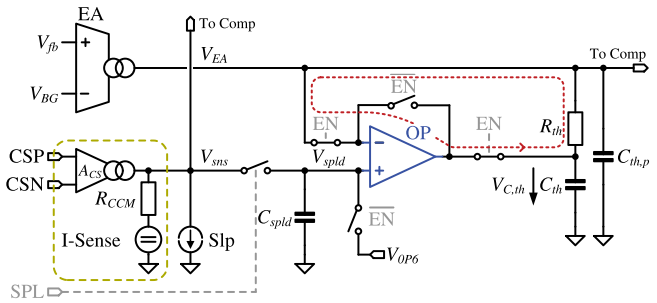


FIGURE 9. Compensation capacitance pre-charge loop for mode change.

current as a second timing reference, the integration time can be connected to the exact difference in $I_L - 0.5 \cdot I_{peak}$, which eliminates any initial offset.

It has to be mentioned that both comparators introduce a propagation delay, which affects the exact timing. The main current comparator features a comparably small delay of 45 ns, which nearly cancels out, because it occurs at both comparator tripping points. However, the comparator of the inductor current replication circuit is slower – 200 ns across PVT – due to its power-saving design. For that purpose, a compensation feedback loop has been designed, which regulates the propagation delay to less than 5 ns.

The current sources – M2, M3 and the output related g_m-stage – are not switched to minimize any disturbance during operation. Instead, all nodes are automatically precharged to the correct potential. Moreover, compensation switches were added to minimize critical charge injection.

D. MODE CHANGE INTO CCM

As presented in the previous subsection, the EA is not part of the feedback loop during DCM operation. Therefore, V_{EA} does not match to the actual peak inductor current, moreover the EA saturates to $V_{EA,\min} = 500\,\text{mV}$.

For a smooth transition into CCM operation, the compensation network is pre-charged to the matching sensed inductor peak current, including the slope compensation fraction. To achieve this, the output stage is operated with a fixed duty-cycle, calculated on-the-fly for five switching periods. The peak inductor current is sampled and stored, whereas an additional buffer charges the compensation capacitance. Fig. 9 depicts the corresponding circuit implementation at system level, whereas Fig. 10 illustrates the simulated transient waveforms during the mode transition from DCM to CCM. The feedback voltage V_{fb} is deliberately connected to 1.5 V to saturate the EA at 500 mV. With the activation of the pre-charge system, V_{fb} is reconnected to the input voltage divider. By observing V_{spld}, the capacitive loading of the comparably high impedance V_{sns}-node is clearly visible. Nevertheless, after five sampling events V_{spld} is equal to V_{sns} as well as the reference voltage V_{thres}.

After the successful mode change to the DCM, the pre-charge circuit is powered down into standby operation with only 20% current consumption. However, the amplifier is kept

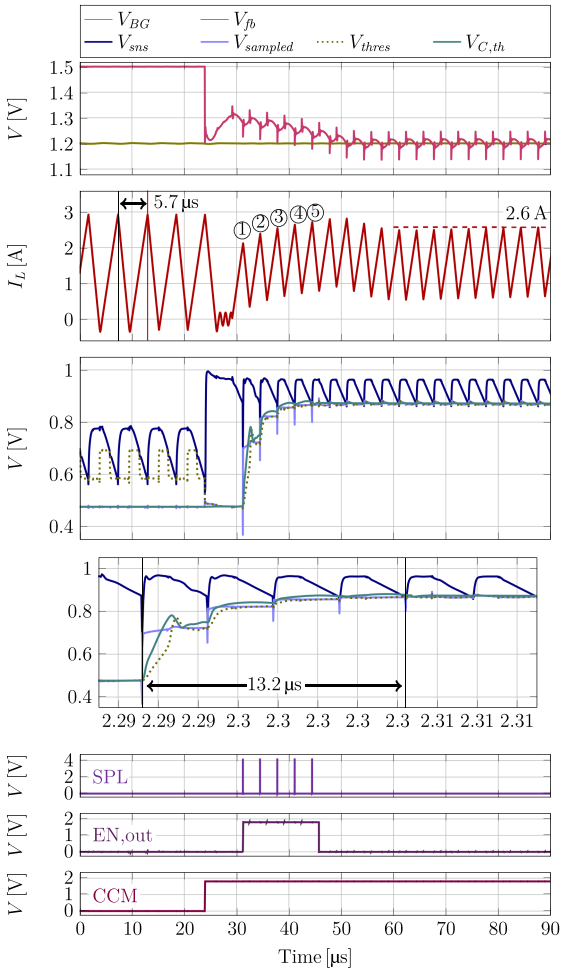


FIGURE 10. Simulated transition into CCM – the compensation capacitance pre-charge technique enables a smooth mode change.

in closed negative feedback operation, to shorten the startup time of the next transition into CCM.

E. OPERATIONAL AMPLIFIER DESIGN

R_{th} and $C_{th,p}$ of the compensation network form a mid frequency pole at the input of the amplifier which confines the achievable bandwidth of the closed feedback loop substantially. The sampling rate is equal to the 300 kHz switching frequency and thus, defines the settling time of the amplifier. However, the slew rate is very much limited by the 70 pF output capacitance. For that reason, the output of the operational amplifier is connected directly to the main compensation capacitance, whereas the feedback potential is taken from the actual EA output.

Fig. 11 pictures the circuit implementation of the pre-charge amplifier. The architecture is based on a folded cascode with a PMOS input pair to enable low input voltages and high loop gain. The current sources provide 1 μA tail current and are also implemented with PMOS transistors. In contrast to NMOS current sources, the power supply rejection ratio (PSRR) for the node $V_{\text{out},fc}$ is improved significantly.

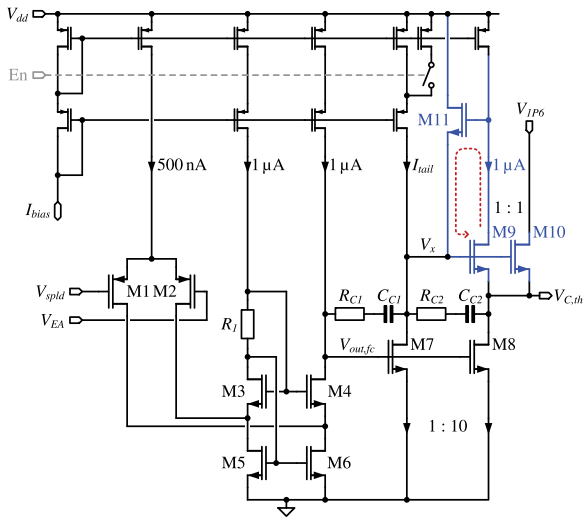


FIGURE 11. Circuit implementation of the pre-charge amplifier.

TABLE 1. Discrete Key Components of the Prototype

Component	Model/Value	Quantity
Output stage FETs M1, M2	4.3 mΩ, NVMFS5C645NL	2
MPPT FET M3	1.4 mΩ, PSMN1R2-25YLD	1
Inductor	8.2 µH, SER2211-822MED	1
C_{in}	4.7 µF, 50 V	4
C_{out}	2.2 µF, 100 V	4
R_{sense}	10 mΩ, 2 W	1
Gate resistor	4.7 Ω	2
Diode D	Schottky, STPS30H100DJF	1

The design uses an additional output stage, represented by M7-M11, to achieve larger positive and negative slew rates ($\pm 0.25\,\mathrm{V}/\mu\mathrm{s}$), combined with a current efficient design. All static branch currents are well defined by current sources. The extra feedback loop formed by M9 and M11 eliminates undershoots of V_{EA} for decaying input signals, by avoiding saturation effects of V_x. A conventional compensation technique would not be sufficient at this point, or would slow down the overall loop response excessively.

IV. MEASUREMENT RESULTS

In the following section, measurement results of a single boost converter are presented. A Keysight E4360 A solar simulator is used as a PV-source. The device maps the *IV*-curve of a 20-cell sub-string from an LG NeOn2 module (LG370N1C-N5). The converter output is connected to an electronic load in constant voltage operation. In the second part, field measurements of multiple in series connected MPPB converters under partial shaded conditions are shown. These results are further compared against the bypass diode approach, which has become standard practice in modern PV-panels. Table 1 lists the key components of the measurement prototype.

A. MODE CHANGE INTO CCM

Fig. 12 shows the measured switching waveforms of a single boost converter during the mode transition from DCM to

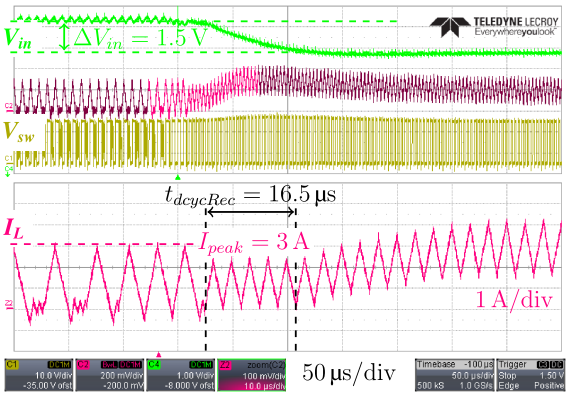


FIGURE 12. V_{in}-Step: Mode transition from DCM to CCM.

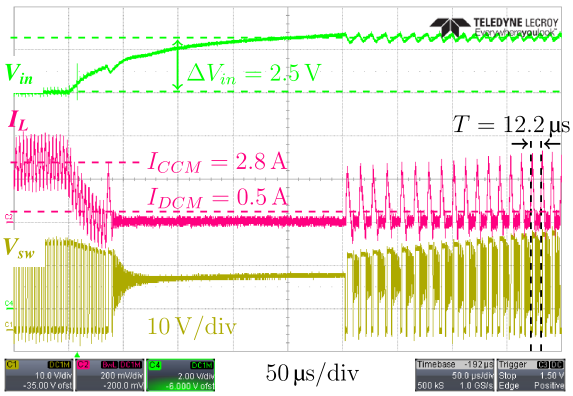


FIGURE 13. V_{in}-Step: Mode transition from CCM to DCM.

CCM. The operation mode change is caused by lowering the V_{in} set voltage. For that purpose, the current DAC is adjusted via the SPI interface. V_{in} thereby drops by 1.5 V to 9.9 V. The controller transitions into CCM operation, because a new LS pulse is scheduled – V_{fb} exceeds V_{BG} – before the HS phase has finished completely and is turned off by the control logic. The magnified section of I_L shows the increasing switching frequency, until the high impedance duration in DCM vanishes. The first five switching cycles are performed with the on-the-fly calculated duty-cycle. Afterwards, the compensation capacitance has reached the final current sense voltage and the current feedback loop is closed again, as described in Section III-D. This technique achieves a smooth transient response without undershoot of V_{in}. For 11.4 V V_{in} and 20 V output voltage, the peak inductor current measures 3 A in DCM. Due to the diode characteristic of the PV-panel, the input current rises when the string-voltage decreases. The settling behavior of V_{out} and thus, the switch pin voltage, is caused by the limited bandwidth of the electronic load used.

B. MODE CHANGE INTO DCM

The mode transition from CCM into DCM operation is illustrated in Fig. 13. The mode change is initiated by adjusting the feedback DAC via SPI, which leads to the depicted step

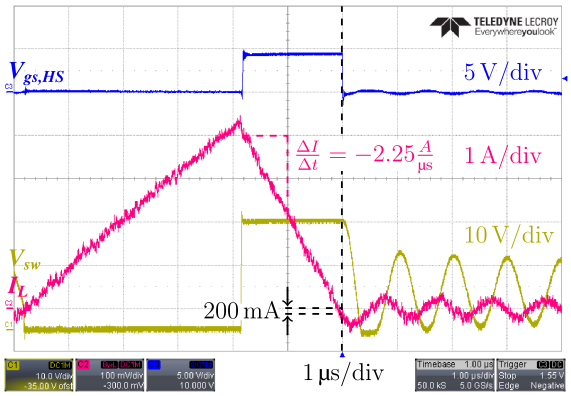


FIGURE 14. High-side turn-off in DCM based on replicated I_L.

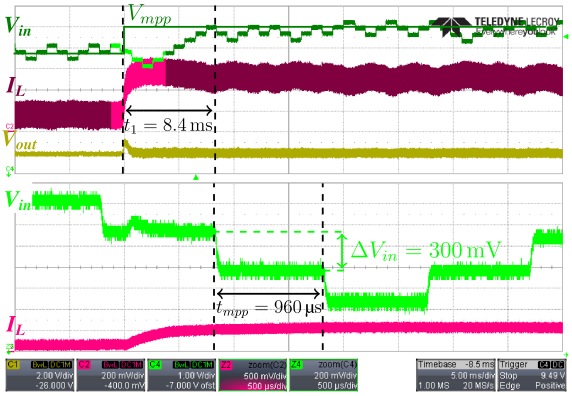


FIGURE 15. Active MPP-tracking: P_{in}-step from 20% to 60%.

response. The inductor current drops to nearly 0 A in approximately 35 μs. As a consequence, the panel-voltage rises. When the DCM-detection circuit indicates the threshold for mode change, the converter stops switching. The next LS-pulse is scheduled after V_{in} exceeds the target voltage. This is the most extreme example concerning a fast mode change. In general, the V_{in} change would take place much slower, in conjunction with a smaller ΔV_{in}. However, the measured response shows a stable transition without I_L undershoot. The inductor current drops from 2.8 A to 0.5 A, whereas the switching frequency decreases to 82 kHz. Moreover, the input voltage ripple increases from 100 mV to 500 mV, due to the increased switching period.

C. PRECISE HS TURN-OFF IN DCM

Fig. 14 pictures the HS turn-off moment in DCM. The inductor current I_L is shown as well as the switch pin voltage together with the gate source voltage, $V_{gs,HS}$, of the HS switch. The inductor current measures approx. −200 mA when the HS is switched off. With a current slope of −2.25 A/μs, this is equivalent to 80 ns overall delay. The deviation from the ideal delay-free implementation can be explained by mismatch in the inductor current replication circuit and delay between digital control signals of the power stage and the actual driver output. However, a delayed turn-off is not very critical, because the inductor current is going to drop even further below zero, which can be clearly observed in the figure, as well. This is due to the parasitic capacitance at the switch pin, which has to be discharged to V_{in} first. Therefore, a prolonged HS phase leads to a slightly more negative inductor current, which in turn discharges the switch node capacitance faster. However, the delay should not be too large, otherwise the PV-panel current would be lowered and the mode change hysteresis would be affected too much.

D. MPP-TRACKING: INPUT POWER STEP RESPONSE

Fig. 15 shows the input voltage and the inductor current during active MPP-tracking. The initial input power is raised from 15.1 W to 51.1 W. Thereby, V_{in} increases slightly from 8.7 V to 9.5 V, however I_L rises significantly from 1.73 A to 5.38 A, due to the diode characteristic of the PV-cell. Moreover, a small coupling to V_{out} is observable, which settles quickly. The MPP-tracking efficiency measures 99.9%, the ideal V_{in}-trace is added to Fig. 15 as well. The magnified section of the annotated measurement graphic shows the V_{in} perturbation steps. The step height is adjustable and measures 300 mV. Moreover, after 960 μs, the delta modulator is evaluated. Based on the relation of (1), the excitation direction is changed. After 8.4 ms the new MPP is found. By changing the MPP-tracking parameters – excitation step height, delta modulator evaluation time and step acceleration – the tracking behavior can be adjusted to fit different needs for various application scenarios. Therefore, a good trade-off between fast settling or slower, more noise-immune tracking for different panel technologies with diverse string-voltages can be realized. The tracking efficiency is the ratio of harvested power to the maximum available power $P_{in,max}$ delivered from the source. To obtain $P_{in,max}$ of the Keysight solar simulator for a programmed IV-curve, the converter was operated with deactivated MPPT. This method was chosen in favor of a DC input power sweep, because P_{in} with DC/DC converter measured larger than the DC measurement. This may be explained by the use of 4-wire sensing of the solar simulator as well as interfering of regulation loops. However, the measurement with deactivated MPPT shows repeatable results. The tracking efficiency also matches simulation results. The input voltage was altered by sweeping the DAC at the feedback divider, which changes V_{in} as described in (2).

E. SERIES CONNECTION OF TWO MPP-TRACKING BOOST CONVERTERS

The following subsection provides measurement results of multiple in-series connected MPP-tracking boost converters. The first configuration comprises two DC/DC converters, each connected to a single custom CIGS thin film solar module. The rated panel input power is 80 W. Fig. 16 shows the transient tracking behavior in very light load operation. The summed output voltage V_{out} is regulated by the connected

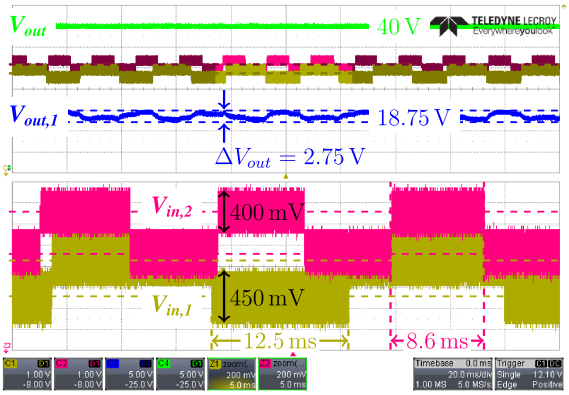
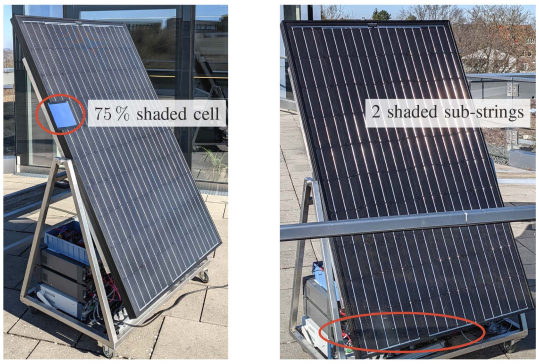


FIGURE 16. Two MPP-tracking boost converters connected in series with different P_{in} in very light load operation.



(a) 75 % shaded cell (b) 2 shaded sub-strings

FIGURE 17. Measurement setup of shaded PV-panel fitted with three in-series connected MPP-tracking DC/DC converters.

electronic load and measures 40 V. $V_{\text{out},1}$ represents the output of the first converter, whereas the average voltage lies at 18.75 V. The output current measures 80 mA. Therefore, the first converter delivers 1.5 W and the second DC/DC module 1.7 W to the total output power of 3.2 W. The output voltage of each converter inherently represents the fraction contributing to the total string power. Thereby, $V_{\text{out},1,2}$ automatically adjusts, due to the common string current. The output voltage ripple ΔV_{out} (2.75 V) consists of both converter fractions, due to the common ground measurement. The lower part of the figure shows the magnified input voltages which are approx. equal to the panel voltages. Both controllers operate in DCM, with comparable peak inductor current. Thus, the switching frequency differs, due to the unequal input power, caused by the very advanced sunset. For that reason, the MPP-tracking speed is also very different. The perturbation steps are clearly visible. The differing operating points also affect the V_{in} ripple voltage. Moreover, the ripple magnitude is comparably large regarding the averaged input voltage – $V_{\text{in},1}$ measures 8.75 V, the second PV-panel operates at 9.18 V. This is a direct consequence of the intentionally low switching frequency, to boost the efficiency at light load operation.

F. FIELD MEASUREMENTS OF THE MPP-TRACKING BOOST CONVERTER SYSTEM

The following results are collected from outdoor measurements of a 250 W rated 60-cell BOSCH *c-SI M 60 S EU42117* PV-panel. The module has been split up into three sub-strings, consisting of 20 cells each, which are connected to three MPP-tracking ASICs and was used with the original three bypass diodes.

Fig. 17 shows the setup of the field measurement under partial shading, whereas the ASIC and all supplementary devices are located behind the panel. Fig. 18 pictures the panel current as a function of V_{panel} as well as the *PV*-curve. The unshaded panel generates 124.5 W in MPP at 530 W/m^2 solar insolation. The second measurement shows two maxima of the *PV*-curve, at which a single cell is shaded by 65%. The

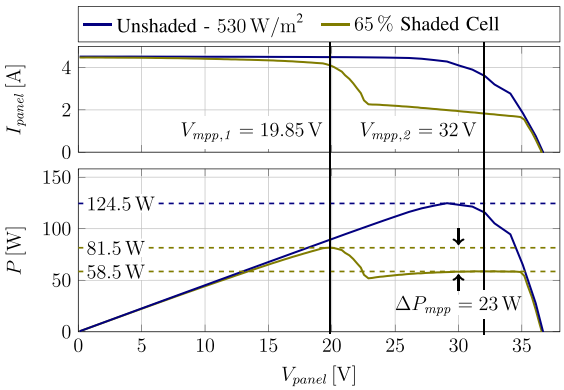


FIGURE 18. *PV*-curve of unshaded and partially shaded PV-panel.

panel insolation is identical to the unshaded case. Moreover, the curve characteristic is typical of shaded, in series connected PV-cells with bypass diodes, in which the total number of possible maxima is equal to the number of diodes. The bypass diode conducts for small module voltages, and therefore shorts the shaded sub-string. Hence, the larger current of the unshaded cells is not limited by the single shaded cell. However, the shorted sub-string does not contribute to the output power and even consumes a small amount of power, due to the bypass diode voltage drop. When V_{panel} increases, the cell current decreases, due to the diode nature. Hence, at approx. 23 V, the diode disengages. At that point, I_{panel} can also be delivered by the shaded string. Consequently, the generated power increases again and forms the second MPP at 32 V with 58.5 W, which is 23 W less than the global MPP under shading. The difference in power depends on the shading difference between sub-strings. Completely uniform shading of all sub-strings results in a single MPP, whereas a single shaded cell shows two MPPs with the largest power difference.

Today's central inverter topologies are capable of detecting local MPPs and adjusting to the global MPP by periodically testing the full *PV*-curve. However, this is generally a slow process – a global search is executed every 6 min for an SMA

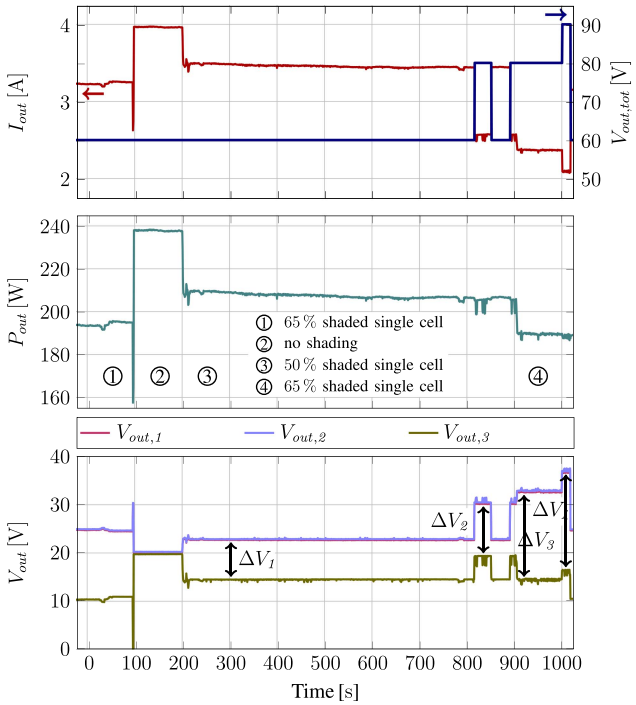


FIGURE 19. Output power and individual V_{out} of three in-series connected MPP-tracking DC/DC converters for different shading scenarios.

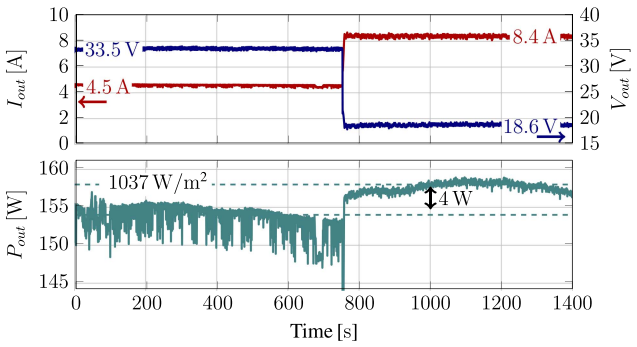


FIGURE 20. Output power, V_{out} and I_{out} of the original PV-panel with a 50%-shaded cell. MPP difference with engaged/disengaged bypass diode.

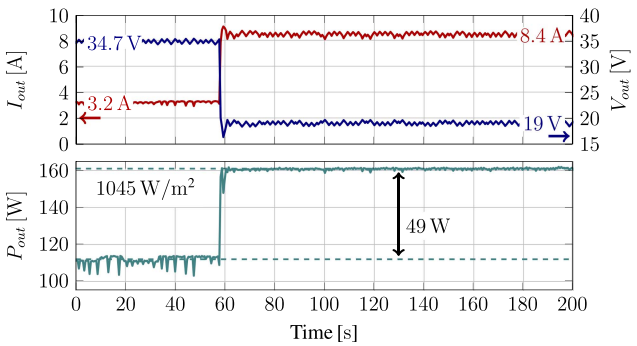


FIGURE 21. Output power, V_{out} and I_{out} of the original PV-panel with a 65%-shaded cell. MPP difference with engaged/disengaged bypass diode.

Sunnyboy [5]. The presented MPP-tracking DC/DC converter is capable of using the entire available power of each sub-string. Instead of losing the energy of the shaded string like in case of an active bypass diode, the sub-string can still contribute to the total module output.

Fig. 19 depicts the measured output characteristics of three in-series connected boost converters for different shading scenarios and output voltages. The first time slot until 100 s shows a measurement with a single cell shaded by 65%. The system output voltage is set by the electronic load to $V_{\text{out,tot}} = 60$ V. This is not enough to balance the output current of all MPP-tracking converters. Consequently, the shaded DC/DC sub-string converter is not switching. V_{out3} lies at 11 V and the HS body diode of the power stage conducts. The shaded string still adds to the total 194 W P_{out}, but the diode drop introduces losses. The first and second converter contribute equally, which can be seen in the equality of V_{out1} and V_{out2}.

In phase 2, the PV-module is not shaded, all converters generate 80 W. The system output current measures 4 A, whereupon the individual $V_{\text{out},1,2,3} = 20$ V add up to 60 V.

From 200 s to 810 s one cell in sub-string 3 is shaded by 50%. Therefore, the total output power drops by 30 W. However, in contrast to phase 1, all DC/DC converters are switching and are regulating their respective sub-string in MPP. Converter 1 and 2 generate the same power – 80 W, like in the unshaded case. Consequently, the shaded string still contributes 50 W to P_{out}.

The system output voltage $V_{\text{out,tot}}$ can be set to a wide range. However, for large sub-string mismatch, $V_{\text{out,tot}}$ is limiting the overall system shading tolerance, instead of the converter output voltage range. This can be seen in phase 1, where $V_{\text{out},3}$ is forced too low, which turns off the boost converter. Although the power ratio between shaded and unshaded sub-string lies at only $V_{\text{out},2}/V_{\text{out},3} = 2.3$, which is much smaller than the theoretical limit of 5, sub-string 3 is not in MPP. To avoid this, the system voltage V_{out} must be increased, whereby $V_{\text{out},3}$ rises as well. This is shown in phase 4 in Fig. 19. The system voltage is increased to 80 V which leaves enough margin for the shaded sub-string converter to operate with the same 65% shaded cell as in phase 1. Nevertheless, the total output power decreases by 4 W, which is a combination of slightly lower insolation and increased DC/DC switching losses, due to the larger output voltage of all converters.

To illustrate the benefit of the proposed system with partial shading, Fig. 20 and Fig. 21 show the generated power of the original PV-panel, fitted with bypass diodes for 50% and 65% shading of a single cell. The MPPT is realized in MATLAB and is based on a perturb-and-observe algorithm. The panel voltage is adjusted approx. two times per second. The first part of the measurements shows the PV-panel operating at high output voltages where the bypass diodes are not active, while the second half documents the operation with active bypass diodes for the shaded sub-string. Both measurements demonstrate that the overall output power is increased by the use of bypass diodes for shaded strings. However, in case of 50%

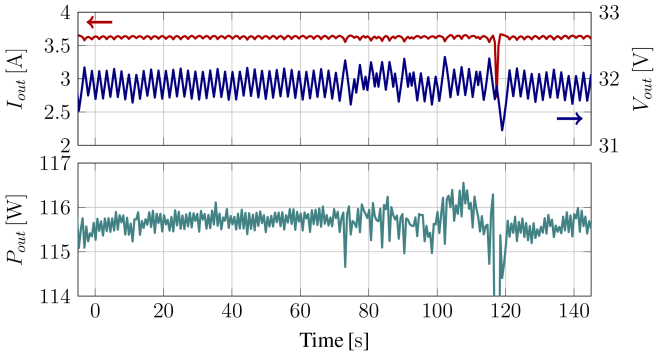


FIGURE 22. Output power, V_{out} and I_{out} of the original PV-panel with two shaded panel sub-strings operating in MPP.

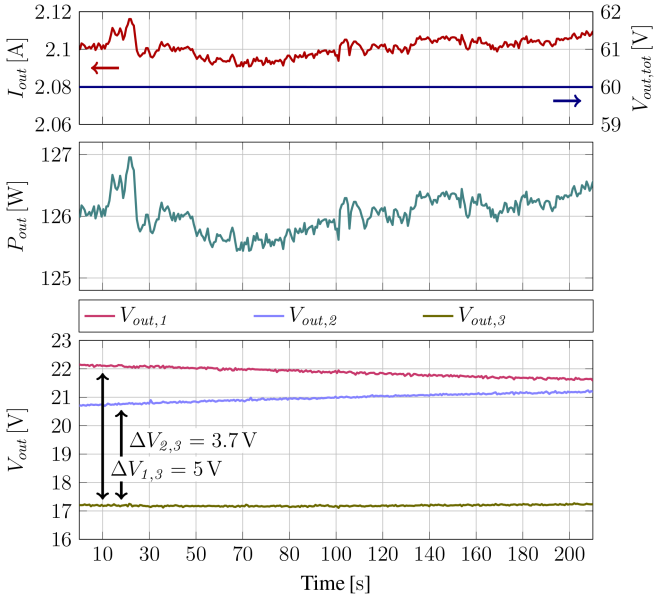


FIGURE 23. Output power, V_{out} and I_{out} of three in-series connected MPP-tracking DC/DC converters with two shaded sub-strings.

shading, the power advantage measures only 4 W compared to 49 W for 65% cell shade in Fig. 21. With these results in mind, the performance of the MPP-tracking sub-module converters show an increase from 158 W to 210 W and from 161 W to 190 W for 50% and 65% shading of a single cell. This means 33%, respectively 18% higher energy yield with the proposed concept compared to bypass diodes.

Due to soiling or cell failure, individual cells may be severely shaded. The following subsection evaluates and compares the proposed MPP-tracking DC/DC converter in a lower shading scenario, which may result from trees, chimneys or antennas. The insolation profile is depicted in Fig. 17(b); two sub-strings are lightly shaded. Fig. 22 shows the panel output power with traditional bypass diodes. Due to the small amount of shade, the MPP lies at higher panel voltages and measures 115.5 W. Thus, none of the bypass diodes short out a shaded sub-string.

Fig. 23 shows the result of the shaded PV-panel, fitted with three sub-module converters. The average output power amounts to 126 W, which is 10.5 W higher compared to the original bypass diode approach. The output voltage of each converter represents the power difference between the sub-strings. The partial shading reduces the ideal, unshaded panel power by only 8.5%, which results in 18.5% effective energy loss for the conventional system, whereas the proposed DC-DC converter solution loses only 11%. This leads to 9% higher energy yield and proves that even light partial shading results in significant losses with the industry standard bypass diode approach.

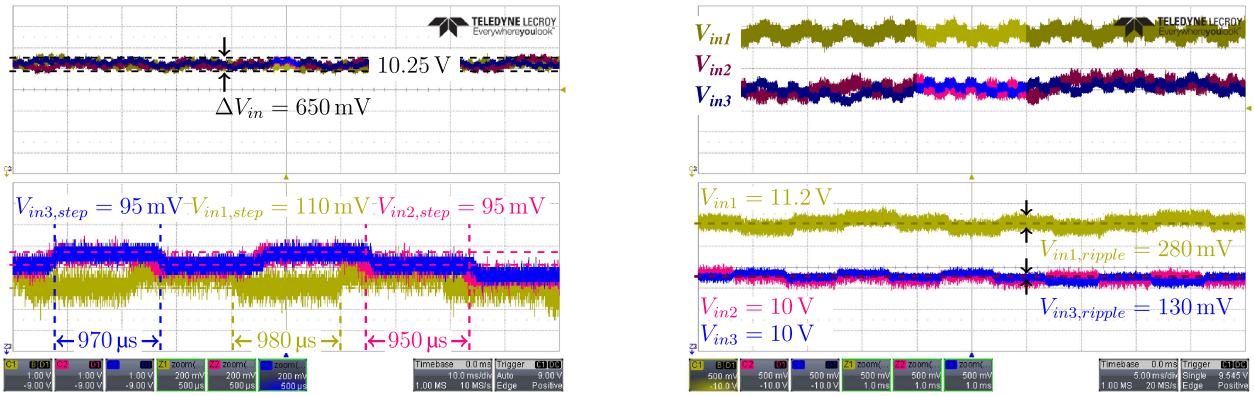
The following subsection provides another example of operation under partial shading. In addition to that, the measurement results focus on the ASIC input voltage, which is equal to the connected sub-string voltage. Hence, the tracking behavior is shown in more detail and the MPPT perturbation steps are highlighted.

Fig. 24(a) shows the sub-string voltages under unshaded conditions. All converter input voltages measure 10.25 V. The captured waveforms display 100 ms, in which V_{in} is adjusted approx. 100 times by the tracking circuit. The V_{in} ripple, including the MPP perturbation steps, stabilizes at 650 mV. The magnified part clearly shows the very well matched panel voltages of the second and third DC/DC converter. The excitation step height measures around 100 mV. Moreover, the MPP-tracking cycle is very similar for all circuits and lies around 970 μs. Fig. 24(b) depicts the input voltages for partial shading of the first PV sub-string. For that purpose, a single PV-cell has been darkened by 50%. Thus, the MPP-voltage increases to 11.2 V and therefore, lies about 1.2 V above $V_{\text{in},2}$ and $V_{\text{in},3}$. Moreover, the input voltage ripple of the shaded string doubles as well. All in all, the power of the shaded string drops by 38% or 25 W, which results in $V_{\text{out},1} = 14.3\,\text{V}$; V_{out} of the non affected sub-module converters measure 23 V and 22.8 V, respectively. Therefore, the total output power decreases from 200 W to 175 W at a solar insolation of 870 W/m^2. If no submodule DC/DC converters were applied, but only three string diodes, the maximum PV-power would drop to approx. 133 W – the shaded string would be shorted by one diode.

Fig. 25 illustrates the boost output voltages during transient shading of the first PV-panel sub-string. As a result V_{out}, of the shaded converter drops by 4.9 V to 14.5 V; hence converters two and three increase their output voltage by 2.45 V, each. The shading and transient settling takes 250 ms. The detailed view of the output voltages shows the remaining ripple, moreover all DC/DC converters still operate in CCM with a switching frequency of 300 kHz.

G. EFFICIENCY

Fig. 26 shows the efficiency curves of the MPPB for multiple output voltages. For that purpose, the *IV*-curve of a 20-cell sub-string from an LG NeOn2 module (LG370N1C-N5) was simulated with a Keysight E4360 A solar simulator. An insolation sweep was replicated with the maximum power limited to



(a) Unshaded PV-Panel (b) Shaded sub-string 1

FIGURE 24. Series connection of three MPP-tracking DC/DC converters connected to a three-string subdivided PV-panel. V_{in} during unshaded conditions and partial shaded operation of the first string.

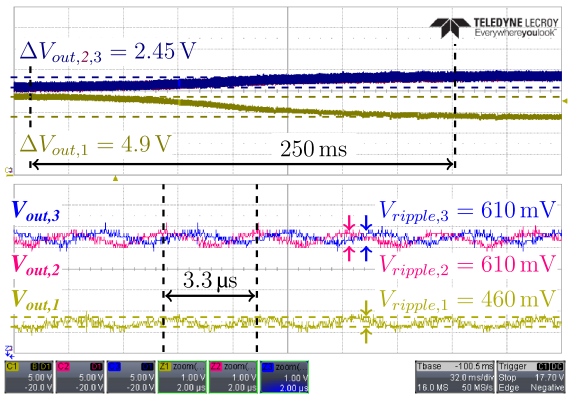


FIGURE 25. ASIC output voltage under transient shading of a single PV-panel sub-string in a series connection of three sub-strings.

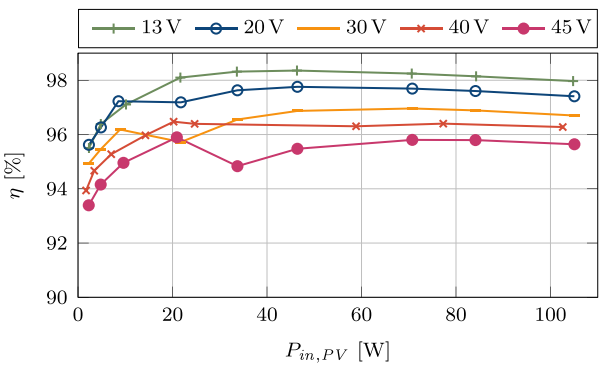


FIGURE 26. MPP-tracking boost converter – system efficiency for different V_{out} across input power range.

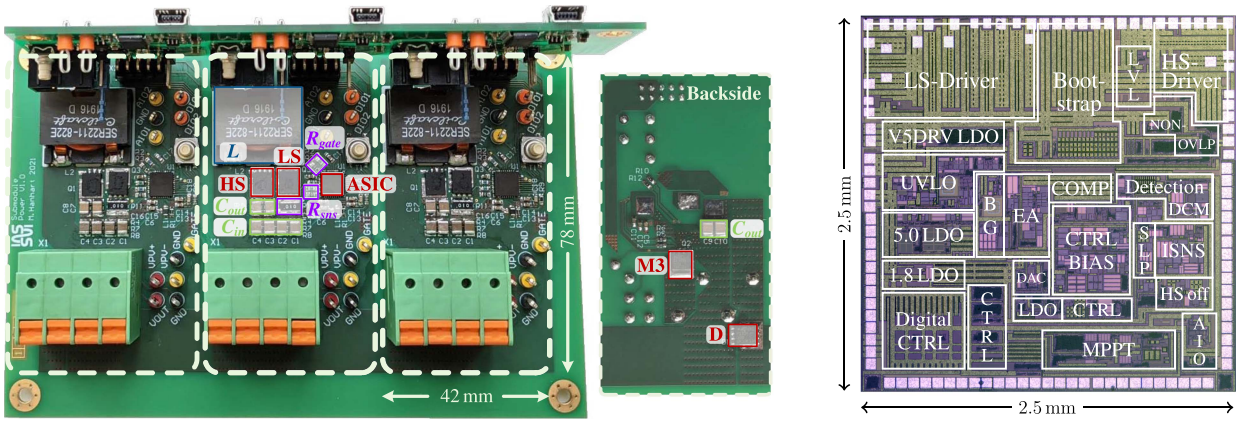
approx. 110 W instead of the peak sub-panel power of 125 W, due to the limited capabilities of the solar simulator used. The peak efficiency measures 98.4%.

The conversion efficiency at high insolation, and thus large PV currents, is limited by the conduction losses. For that reason, low-ohmic switches – *NVMFS5C645NL* from on-semi with an $R_{DS,\text{on}}$ of 4.3 mΩ – are used. However, the efficiency at small input power levels is restricted by the capacitive switching losses, especially at high output voltages. To achieve a good trade-off across the full insolation range, the aforementioned DCM implementation reduces the switching frequency significantly and thus enables excellent conversion efficiencies well above 93% down to P_{PV} as small as 2 W. In that case, an increased input voltage ripple – up to 1 V – is still favorable, despite it affecting the MPP-tracking precision slightly. However, the overall losses diminish in contrast to shorter switching periods with less V_{in}-ripple [20]. The constant voltage sensing MPPT principle reduces the efficiency by only 0.4%, independently of P_{in}. The current consumption of the microcontroller and its digital interface board is included in the efficiency calculation whereby the PV source acts as the only supply.

H. MEASUREMENT PCB AND PHYSICAL IMPLEMENTATION

Fig. 27(a) depicts the PCB which can be fitted to a PV-panel for submodular power optimization. The board contains three MPP-tracking DC/DC converters, where the outputs are connected in series as in Fig. 3. For the initial calibration of the ASIC, live debugging and for receiving internal status signals via the SPI interface, an additional vertically stacked microcontroller board has been attached to the main PCB. A production-ready design would neither need the digital daughter board, nor the test points. This would shrink the PCB to fit in the standard junction box found behind the Bosch panel. The ASIC can be controlled via MATLAB, hence allowing the integration in an automated measurement setup environment.

A single channel occupies 42 mm × 78 mm PCB area. The sense FET for the MPPT (M3) is mounted on the backside of the PCB, as is the bypass diode *D*. Each microcontroller is supplied by the 5 V regulator of the ASIC. This enables a fully standalone operation. The layout has been designed to route the switching loops as compactly as possible. This reduces the effects of electromagnetic interference, as well as



(a) PCB, front side and back side of a single converter

(b) Die micrograph

FIGURE 27. PCB with three MPP-tracking DC/DC converters connected in series together with the annotated die micrograph.

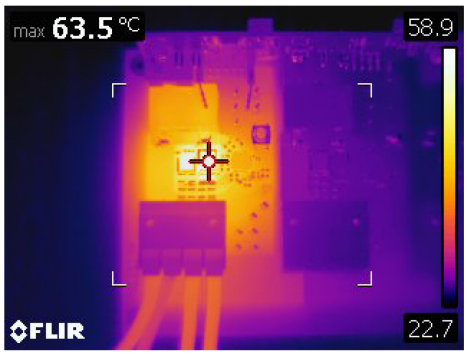


FIGURE 28. Thermal Image of the board with a single channel operating near maximum rating.

minimizing conduction losses. Nevertheless, attention has to be paid to the total heat dissipation capabilities of the board, especially regarding the MOSFETs. Fig. 28 show a thermal image of the PCB under sustained 135 W load on a single channel. The prototype board uses the components listed in Table 1. However, it can be fitted with different MOSFETs, optimized for the given application and PV-panel.

Fig. 27(b) shows the annotated micrograph of the ASIC. The die measures 2.5 mm × 2.5 mm. It has been fabricated in an 0.18 μm high voltage BCD process and is wire-bonded in a QFN36 package with 6 mm edge length.

I. COMPARISON

Table. 2 provides a performance comparison to similar state-of-the art converter topologies. The ratio of output to input voltage plays an immanent role for all DC/DC converter architectures which are directly connected to a PV-panel in terms of shading tolerance, in contrast to the DPP approach of [12], [21] and [22]. Thus, in DPP architectures, the operable current range determines the overall system performance for nonuniform insolation. Buck architectures generally have a better efficiency than boost converters, however the conduction losses related to module and central inverter wiring increase, due to the larger output current. The efficiency of the DC/DC converter is therefore only one part of the overall system. In addition, the proposed design is optimized for medium input power levels. Because of the aggressive switching frequency reduction for low insolation, the proposed system outperforms [14] by multiple efficiency percentage points. Due to the controller architecture, the use of smaller $R_{DS,\mathrm{on}}$ MOSFETs allows the peak efficiency to be adapted to higher power levels, with compromising efficiency at lower P_{in}. The DPP architectures can have very good system efficiencies under lightly shaded conditions, but suffer large losses at high mismatch conditions, due to poor efficiency of the DC/DC converter.

Moreover, the overall solution size is very much limited by the thermal heat dissipation capabilities. Very small solutions, like [24] need further cooling mechanisms, especially during operation at high temperatures in harsh environmental conditions. A larger switching frequency enables smaller passive filter components, however, the dynamic losses increase, particularly at higher voltages. In addition, the MPP-tracking speed is always restricted by the converter transition frequency – f_t – and hence, benefits from faster switching as well. The proposed MPPT is capable of very fast tracking and can be used in rapidly changing operating conditions, such as moving cars or cast shadow scenarios. The implemented MPPT achieves 99.9% tracking efficiency (η_{MPPT}) for the mentioned operating points. However, a physical implementation issue – additional resistance from $VSNS+$ and $VSNS-$ to the internal circuitry – limits the tracking efficiency to slightly lower values at specific operating points. This has been verified with post silicon simulations and can be fixed in silicon easily. However, the MPP-tracking principle does not lose tracking resolution, and thereby tracking efficiency, at low input power levels, which is a major advantage over implementations based on absolute power measurements with ADCs, like [15]. [23] and [21] observe the difference in

TABLE 2. Performance Comparison to Similar State-of-The-Art Publications

Parameter	This work	MAX20801 TPBD [14]	SPV1020 [15]	Discrete GaN [23]	Discrete Buck [24]	Discrete DPP [12]	Discrete DPP [21]	Cell-Level DPP [22]
Topology	Boost Controller	Buck Converter	4-phase Boost Converter	Boost Converter	Buck Converter	Buck-Boost	Buck-Boost	Buck-Boost
Inductor	1	1	4	1	1	1	2 (+)	1
V_{in}	7 - 24 V	6.5 - 15.5 V	6.5 - 40 V	$\leq$ 15 V	5 - 27 V	3 - 13.4 V	36 V-panel	1.1 - 3.3 V
V_{out}	1.1 V_{in} - 50 V	$<$ 1 V$-$11.7 V	V_{in} - 40 V	-	0.8 V - 20 V	-	-	$V_{in}/2$
η_{peak}	98.4 %	99.1 %	98.4 %	97 %	98.2 %	95 %	92.3 % (+)	83.7 %
P_{max}	144 W	143 W	320 W	100 W	80 W	60 W	200 W	13.3 W
Quiescent Current	680 µA	60 mA	5 mA	-	-	-	-	$<$20 mA (‡)
f_s	250 - 400 kHz	-	50 - 200 kHz	250 kHz	250 kHz	100 kHz	100 kHz	3 MHz
MPPT t_{step}	0.15 - 1 ms	0.4 ms	1.28 - 5.1 ms	$\approx$ 56 ms	100 ms	$\approx$ 2 s	-	-
η_{MPPT}	99.9 % (*)	99.9 % (†)	-	-	-	-	-	no MPPT
Die	6.25 mm^2	-	-	-	-	-	-	4 mm^2
Package	6 $\times$ 6 mm^2	10.3 $\times$ 5.8 mm^2	3 $\times$ 7.5 mm^2	-	-	-	-	-
Process	0.18 µm	-	-	discrete	discrete	discrete	discrete	0.13 µm

(*) measured at 15 W and 51 W, simulated for $P > 3$ W (†) $I_{MPP} > 5.5$ A (+) per panel (‡) calculated from 40 mW

V_{out}, after perturbing the module voltage, which also requires an ADC with sufficient resolution. In addition, this technique is susceptible to noise from adjacent converters. The MPPT implementation of [24] maximizes the duty cycle of all converters and thus their output voltage, but this approach requires an additional global MPPT for the whole system. Simpler implementations, such as [22] equalize the voltage of all PV-cells, which is no true MPP-tracking and less accurate. Reference [14] reaches 99.9% tracking efficiency only for input power levels larger than 46% of P_{max}.

V. CONCLUSION

An integrated MPP-tracking boost controller and its application range has been demonstrated in this work. The digitally-assisted MPPT implementation omits the need for a high resolution ADC and achieves 99.9% tracking efficiency. The constant voltage sensing approach degrades the efficiency by only 0.4% across the full input power range. Therefore, a very high system efficiency is achieved – η_{peak} measures 98.4%. This is further enabled by the DCM implementation for light load operation, which incorporates the operating point for an adaptable peak inductor current. Thus, the switching frequency is significantly reduced compared to the 300 kHz peak-current-mode CCM operation. For a precise HS turn-off, the inductor current is replicated during DCM. Multiple DC/DC converters can be connected in series, to benefit from a larger string voltage for a single central inverter. In field measurements, the proposed solution shows up to 33% higher energy output under partial shaded conditions compared to the standard bypass approach for a standard PV-module.

All in all, the proposed MPP-tracking boost converter offers a very versatile solution for submodule PV-applications and is capable of reducing the influence of partial shading as well as intermodule-level degradation on output power significantly.

ACKNOWLEDGMENT

The authors would like to thank the HiSilicon sponsorship program for MPW prototyping for the ASIC fabrication sponsorship.

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