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Investigation Into Active Gate-Driving Timing Resolution and Complexity Requirements for a 1200 V 400 A Silicon Carbide Half Bridge Module

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ABSTRACT Silicon Carbide MOSFETs have lower switching losses when compared to similarly rated Silicon IGBT, but exhibit faster switching edges, larger overshoots and increased oscillatory switching behaviour, resulting in greater electro-magnetic interference (EMI) generation. Active Gate Drivers (AGD) can help mitigate these issues while maintaining low switching losses. Numerous AGD topologies have been presented with varying capabilities in terms of timing resolution and output stage complexity. This paper presents an experimental investigation into the influence these capabilities have on the switching performance of an AGD driven high current module, with the goal of advising future AGD designers on the performance trade-offs between signal resolution and complexity. A 2.5 ns resolution 6-level AGD was utilised in combination with parameter sweeps and a genetic algorithm to determine gate voltage patterns that provided improved switching performance. Results indicate that higher resolution (2.5–5 ns) provided the greatest improvements in switching performance, even utilising the simplest considered gate driving patterns, with the use of more complex patterns offering minimal additional improvements. However, at lower timing resolutions (10–40 ns) a stronger set-point dependence degradation in switching performance is observed when using simpler gate patterns, which can be mitigated by utilising more complex patterns.

INDEX TERMS Active gate driving, AGD, Silicon Carbide, SiC, EMI reduction, timing resolution, signal complexity, half bridge module, genetic algorithm.

I. INTRODUCTION

Silicon Carbide (SiC) MOSFET's have been supplanting Silicon (Si) IGBT's in the lower end of high-power hard-switched drive and inverter applications, with 1.7 kV 600 A devices commercially available [1]. The low switching losses of these devices and higher achievable switching frequencies have the potential to allow for more efficient power converters with reduced passive components, and therefore volume. SiC has an electric field strength breakdown value that is almost ten times that of Si and a thermal conductivity that is almost three times. These material properties facilitate smaller dies, with reduced channel lengths and reduced parasitic die capacitance's which, alongside a faster rate of minority carrier recombination, results in faster switching edges (dI/dt and dV/dt) for the drain current (I_D) and drain-source voltage (V_{DS}). These faster switching edges couple with the distributed parasitic inductance, illustrated in Fig. 1 for a typical half bridge module, to produce a significantly increased overshoot and oscillatory response during the switching transients compared to Si IGBT's [2]. This produces an increased level of electromagnetic interference (EMI) and transient over-voltage limit concerns that necessitates an increased safe-operating area,

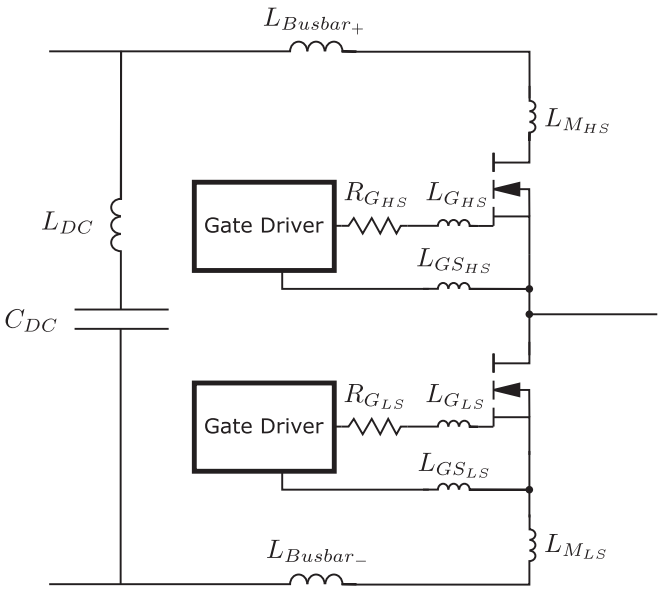

FIGURE 1. Illustration of the power loop and gate loop parasitic inductance of a typical half bridge module.

presenting serious barriers to the mass adoption of SiC devices [3], [4].

These issues can be partially mitigated by optimising the busbar layout to reduce stray inductance (cf. Fig. 1, L_{Busbar_+} and L_{Busbar_-}) and by designing high-quality decoupling capacitors with low equivalent series inductance (L_{DC}). Optimising these has the cumulative effect of reducing the power loop inductance which minimises the corresponding coupling with the fast switching edges of the SiC device, thereby partially mitigating the overshoot and oscillations issues present [2], [5]. However this solution is often limited by the device packaging, with SiC half bridge modules at the time of writing, having a package stray inductances ($L_{M_{HS}}$ and $L_{M_{LS}}$) of 3–10 nH without additional external fixings. A different solution to these problems, particularly for reducing both the conducted and radiated EMI is to increase the gate resistance [6]. This limits the gate current, thereby reducing the dI/dt and dV/dt observed in V_{DS} and I_D. This is a proven method of minimising the V_{DS} and I_D overshoot and oscillations though comes with the major penalty of significantly increased switching losses [7]. Another solution to improve the switching characteristics is the use of passive snubbers, however these come with the penalty of increased volume, complexity, cost and energy loss [8], [9].

Active gate drivers (AGD) are another potential solution to these issues and are the focus of this paper. AGDs function by manipulating either the gate-source voltage or gate current during the switching transient to improve the switching characteristics [2], [9], [10]. The AGD solutions presented in the literature vary widely in their capabilities, with the Gate Timing Resolution (GTR) and output stage complexity identified as primary distinguishing factors between different implementations within this paper. The GTR refers to the smallest discrete timing step which an AGD is capable of changing its output state and the output stage complexity refers to how many voltage/currents levels an AGD is capable of applying to a device during the switching transient. This paper aims to empirically assess, due to the lack of suitable nanosecond scale simulation models, the influence of these AGD capabilities on a 1200 V 400 A SiC half bridge module's switching performance in terms of energy loss, V_{DS}/I_D overshoot and V_{DS}/I_D oscillation. This was performed with an AGD referred to as the Modular Multilevel Gate-Driver (MMGD), which was capable of modulating its output voltage in 5 V increments from −5 V to 15 V, with a resolution of 2.5 ns as presented in [11]. This was used as a tool to generate the gate signal patterns studied in this investigation and is not considered a viable AGD for industrial applications due to its high cost and complexity. This was employed with variable sweeps and a Genetic Algorithm (GA) based automated searching method, which used an objective function to find well-performing gate-voltage patterns.

This investigation was undertaken with the aims of:

- Providing a novel understanding of how different combinations of AGD timing resolution and signal complexity affect the switching performance.
- Informing future AGD designs on the relative benefit of designing an AGD with a more complex output stage or higher GTR.
- Informing closed-loop AGD strategies, such as those detailed in [12], [13], [14], [15] of the required timing accuracy and signal complexity to achieve good switching performance improvements across varying load conditions.

The results from this investigation indicate that:

- At high GTR values (2.5–5 ns) there is little improvement in the switching performance that can be achieved by using an AGD with a more complex output stage.
- At lower GTR values (>10 ns) additional complexity in the AGD output stage can be used to provide significant improvements in switching performance.
- A GTR exists (approximately 5–10 ns), which varies with the switching transient and the parameters being optimised, where further increases in GTR provide minimal switching performance improvements.
- The GTR appears to be more critical during the turn-on switching transient. This criticality can be reduced by targeting just a reduction in I_D oscillation, rather than targeting both I_D oscillation and overshoot.
- In general, a lower complexity AGD with higher GTR outperforms or matches the performance of an AGD with higher output stage complexity but lower GTR.
- AGDs with lower GTR values may not provide consistent switching performance improvements as the load conditions change. This can be mitigated by using an output stage with higher complexity.

II. ACTIVE GATE-DRIVERS FOR SIC DEVICES

Multiple AGD topologies have been presented in the literature, these vary drastically in their capabilities and implementation. This section aims to provide a detailed overview of these topologies and the output signals they are capable of producing.

A. OVERVIEW OF ACTIVE GATE-DRIVERS

AGD's can broadly be categorised into one of three primary configurations: switched resistance, voltage-sourced and current-sourced [16]. These all fundamentally perform the same task of influencing the gate-source voltage/gate current of the device during a switching transition but vary in their implementation, efficiency, complexity, controllability and GTR [16]. The most basic form of AGD to implement is the switched resistance design, these allow for a high timing resolution but have higher driver losses than the other configurations [6], [16], [17]. This topology typically uses transistors to switch between gate resistances, reducing and increasing the gate current at set points during the switching transient to improve the performance. Voltage sourced drivers offer comparably reduced losses, utilising transistors to switch between different voltage levels/sources to control the gate current during the switching transient [7], [12], [16], [18], [19]. Current sourced drivers also offer comparably reduced losses by directly controlling the gate current by generating a digital signal which is then passed through an amplifier to the device's gate [2], [16], [20].

B. CLOSED LOOP ACTIVE GATE DRIVERS

One key challenge in implementing active gate-driving is the requirement to ensure a good performance under varying loading conditions, such as those present in AC-DC converters. Most proposals to achieve this include a closed-loop system that can adjust the timing/pattern of any modulated gate-source voltage based upon measurements. Notable examples of closed-loop AGD systems for SiC MOSFET's have been presented in the publications [12], [13], [14], [15]. The authors of [12] presented a closed loop voltage sourced AGD with the aim of optimising the trade off between between overshoot and switching losses. A PCB Rogowski coil was used to measure the rate of change of drain current, this was then fed into a control IC to adapt the gate pattern. The paper [13] introduced a closed loop AGD capable of being retrofitted onto a commercially available 1.2 kV 180 A module, it utilised gate voltage control to limit the slew rate and used a feedback voltage loop from Rogowski coils to improve the I_D and V_{DS} switching waveform quality. The authors of [14] presented a closed loop switched resistance style AGD for reducing the voltage overshoot during the turn off transient.

C. GATE TIMING RESOLUTION

Most AGD's utilise clocked digital logic which means their voltage/current output, both in terms of triggering point and duration, is limited by the switching speed of the controller and the output stage circuitry. The AGD's presented in the literature vary widely in their GTR, with typical values being in the region of 20–40 ns [21], [22], [23], [24], [25]. Greater GTR require the use of faster controller clock speeds which can be harder to implement, often requiring additional chips, an example being the MMGD presented in [11], which used a 200 MHz FPGA with an additional clock divider to give a GTR of 2.5 ns. Higher GTR of up to 100 ps have been demonstrated in the literature with custom ASIC designs, though these focused on Gallium Nitride (GaN) MOSFET's [26].

D. OUTPUT STAGE COMPLEXITY

An example of a relatively simple AGD is a design that produces a single pulse at its maximum drive strength (e.g positive or negative supply rail in a voltage-source AGD). An illustration of this gate pattern and an example of a topology capable of creating this is shown in Fig. 2(a). An AGD of this type was presented in [18], where a separate transistor was used to pull the driver output voltage to the negative supply rail for short periods during the switching transition. The authors of [19] presented a similar topology but with an additional transistor to pull the voltage to the positive maximum, allowing for active gate driving of both the turn off and turn on transients.

An increased level of output stage complexity is an AGD that is capable of producing a single pulse of intermediate drive strength during switching transitions. An example showing different gate patterns of this type and a topology capable of producing them is shown in Fig. 2(b). The authors of [6] and [17] presented an AGD of this type which utilised switched resistance style topologies to produce intermediate drive levels. There are also topologies capable of producing multiple drive strength, with these typically employing a similar design to the previous driver but with additional stages. An AGD that switches between independent voltage sources to produce varying drive strengths is detailed in [7]. Another example of this type of AGD is detailed in [27] where a switched resistance array is used. A digitally clocked AGD capable of producing 63 distinct drive-strength levels, generated by the parallel connection of 63 transistors, at a 40 ns GTR is detailed in [28], [29].

An example of further AGD output stage complexity is a driver which is capable of producing multiple pulses of varying drive strength during a single switching transient. This type of gate pattern is referred to in this paper as continuous modulation, with an example of this pattern type shown in Fig. 2(c) alongside a topology capable of producing it. Due to the increased number of potential gate patterns, this type of AGD requires a significantly more complex controller capable of providing much greater processing power compared to the single pulse examples previously detailed. An example of this type of design was presented by the authors of [21], [22], [23], where a 63-level driver (similar to that previously detailed and presented in [28], [29]) was given a continuous modulation signal with a GTR of up to 20 ns.

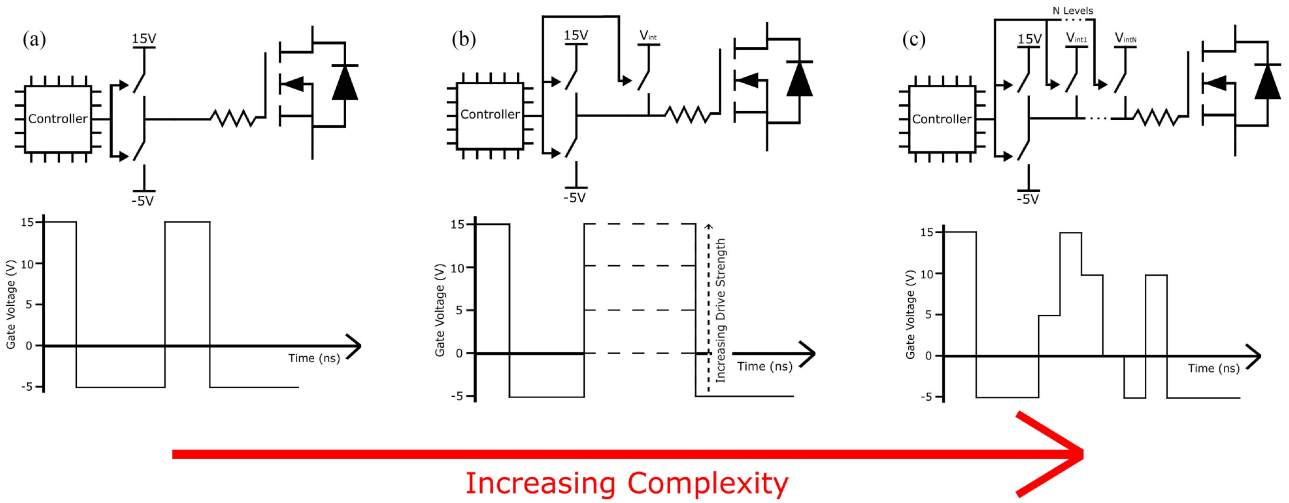

FIGURE 2. **Illustration of gate patterns and example gate drivers with increasing output stage complexity: (a) a single maximum drive strength pulse, (b) a single intermediate drive strength pulse and (c) continuously variable with multiple intermediate drive strength pulses.**

E. USE OF TRAJECTORY MODELS

Model based trajectory optimisation of AGD patterns has been previously proposed as a method of deriving AGD patterns. This has been demonstrated in the publication [27] for single-die SiC MOSFET device utilising a 3-level AGD with a 3.33 ns GTR. The focus of this research was placed on reducing the switching edge *dV/dt* and *dI/dt* magnitudes while retaining low turn-on/turn-on delay times. An online model based adaptive method for adjusting the driving settings of a 3-level AGD was presented in [30], again focusing on dV/dt and dI/dt reduction. The accurate modelling of devices under more complex AGD patterns, such as the multi-level waveforms presented in [21], [22], [23], remains challenging due to phenomena such as space charge trapping which results in threshold voltage hysteresis effects under short gate pulse conditions [31], [32], [33]. Attempts at modelling this gate voltage shift have been successful, though to the authors knowledge this has only been achieved to an accuracy of 100 ns, significantly lower than what is required for this study [34]. In addition, trajectory-based approaches do not capture the drain-source voltage and drain-current oscillation behaviour, which is a major concern for higher current multi-die modules, particularly with respect to EMI generation. Due to the difficulties modelling complex gate-voltage waveforms highlighted, it was concluded that an empirical study was required for this investigation.

F. MODULAR MULTI-LEVEL GATE DRIVER (MMGD)

As discussed in the introduction, this study utilised the Modular Multi-Level Gate Driver (MMGD), shown in Fig. 3 and presented in the publication [11], to perform investigations into how the GTR and output stage complexity influenced the achievable switching performance of SiC MOSFET modules. Its design was driven to be used as a highly flexible research tool that can be used to investigate various different gate-drive strategies, not as a practical solution for industrial

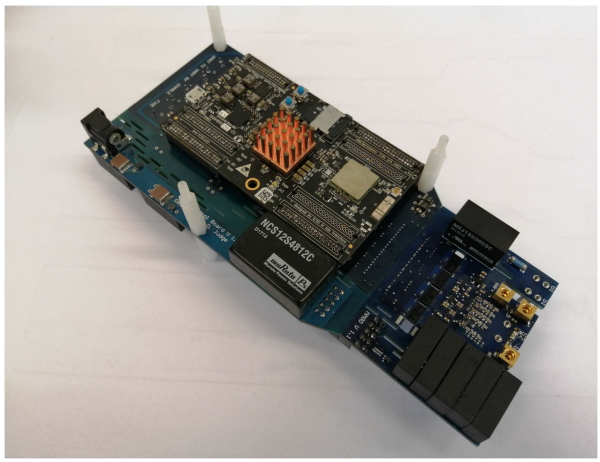

FIGURE 3. **Image of the modular multilevel gate-driver (MMGD).**

applications. The MMGD is a voltage sourced active gate driver capable of producing 6 voltage levels in 5 V increments from −5 V to 20 V with a 2.5 ns resolution, though in this study only 5 levels are utilised from from −5 V to 15 V, while achieving 16/10 A gate current source/sink capability. The control of the MMGD is achieved using a Xilinx Zynq 7020 FPGA SoC, mounted on a Snickerdoodle development board from KRTKL. The programmed patterns stored for both turn-on and turn-off can be updated over an optical UART link.

The MMGD control and output stage circuit design is shown in Fig. 4. The output stage is formed from a series connection of five sub-gate-drivers, each of which contains a paralleled pair of LMG1020 gate driver from Texas Instruments designed for driving Gallium Nitride devices. These individual sub-drivers are capable of producing pulse widths down to 1 ns, and are capable of sourcing/sinking 8/5 A

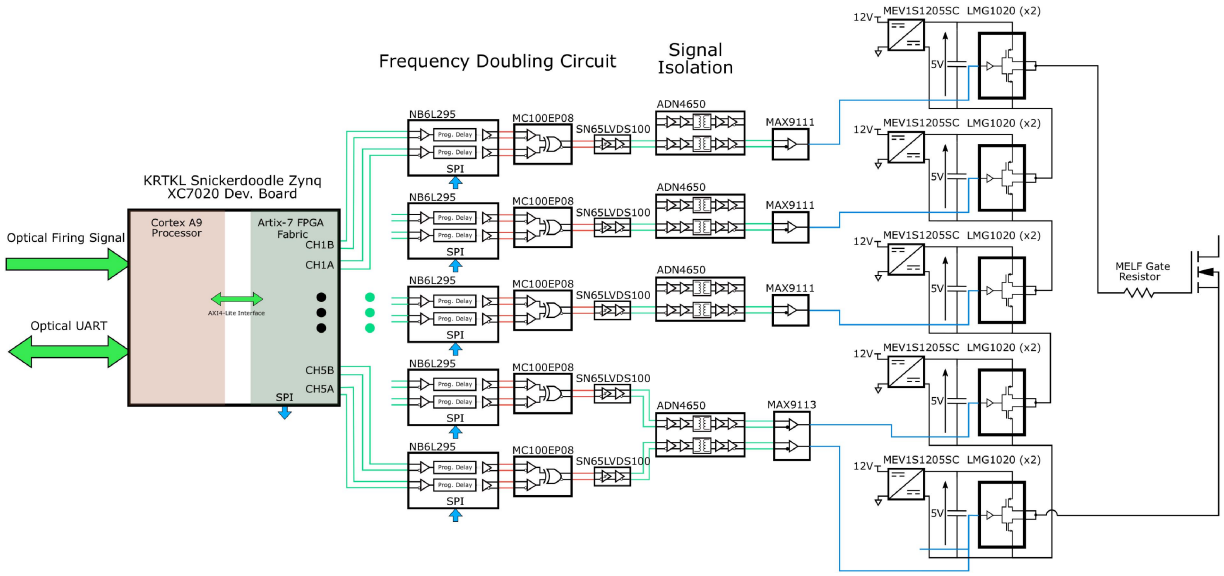

FIGURE 4. 6-Level Modular Multilevel Gate Driver (MMGD) Control & Output Circuit Diagram.

respectively. Paralleled pairs of LMG1020 drivers were used to ensure sufficient drive capability for high-current MOSFET modules, giving a 16/10 A gate current source/sink capability. Each sub-gate-driver had its own isolated 5 V Murata MEV1A1205SC power supply. Signal isolation and level shifting from the control board to each sub-gate-driver was achieved using dual channel ADN4650 LVDS isolators from Analog Devices rated for 600 MBPs data rates. Sub gate-drives 1 and 2 share an isolator as they both have common grounds. A frequency doubling circuit that utilises programmable delay chips was used to increase the effective clocking frequency to 400 MHz, from the 200 MHz clock used internally within the FPGA, giving the MMGD a GTR of 2.5 ns. Additional details of the MMGD's design process and capabilities can be found in the publication [11], where it was first introduced.

III. SWEEPED PARAMETER INVESTIGATION INTO AGD PERFORMANCE

This section presents an investigation into the use of different gate-voltage patterns by utilising parameter sweeps. First maximum drive strength single pulse signals are examined followed by signals of greater complexity which utilise additional drive strengths.

A. EXPERIMENTAL SETUP

Experimental results for this study were obtained using the custom built University of Edinburgh Double Pulse Test Rig (DPTR) shown in Fig. 5. Measurements of results were taken using Tektronix MSO64 1 GHz 25 GS/s and Teledyne LeCroy WaveRunner 604Zi 400 MHz 20 GS/s oscilloscopes. The use of two scopes was necessitated by the available probes. Gate voltage and current measurements were made using 1 GHz IsoVu probes that required the use of the Tektronix scope and measurement's of V_{DS} were made using a HVD3605 200 MHz 6000 V differential probe that required the use of the Teledyne LeCroy WaveRunner oscilloscope. I_D was measured using a PEM 50 MHz Rogowski coil with minimal temperature sensitivity (1.65% over the range −40 °C to 125 °C being the manufacturer stated variance). This current was also measured on the Teledyne LeCroy WaveRunner to eliminate the effects of jitter between the scopes (estimated to be around 2 ns) and its impact on the switching energy calculations. The two scopes were deskewed by the Tektronix MSO64 triggering the Teledyne LeCroy WaveRunner, with the fixed delay this introduced calculated and accounted for in the processing of the results. The device under test was the WolfSpeed CAB400M12XM3, the switching loss optimised version of it's module series, and representative of one of the best in-class 1200 V SiC MOSFET modules currently commercially available. This was mounted onto a low inductance custom built busbar also visible in Fig. 5. The CAB400M12XM3 is rated by the manufacturer to be used with external gate resistances down to 0 Ω, with an internal 1.4 Ω gate resistance included within the module. In addition to this a small 0.25 Ω external gate-resistor was included on the MMGD to faciliate the gate-current measurements using the IsoVu Probe. The V_{DS} measurements were made by attaching probes to tabs connected to the modules output terminals and the I_D measurements were taken by the Rogowski coil around the busbar at the point it connected to the module. Module temperature control was achieved using an Omega PID controller in conjunction with a heating pad and thermo-couple mounted to the base-plate of the module.

Several metrics were used to quantify the switching performance, the percentage overshoot of the V_{DS}/I_D waveform, the switching energy losses and a metric measuring the oscillations in the V_{DS}/I_D waveforms. Using the V_{DS} and I_D switching

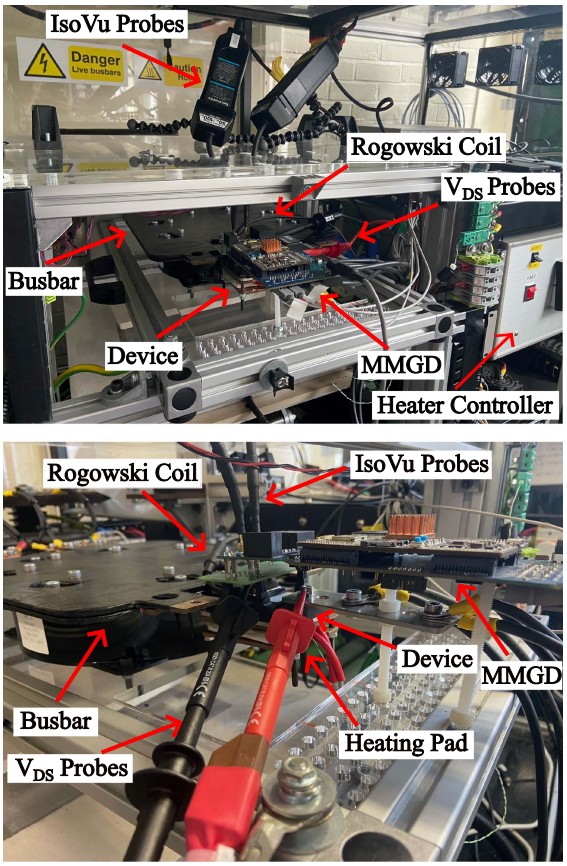

FIGURE 5. Labelled Images of the Double Pulse Test Rig (DPTR) with the busbar, CAB400M12XM3 device, MMGD and measurement equipment.

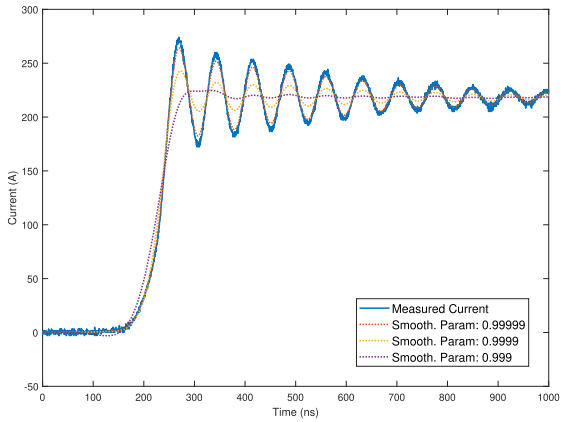

FIGURE 6. Fitted smoothing function with an increasing smoothing parameter on a 200 A 300 V turn-on transient without AGD.

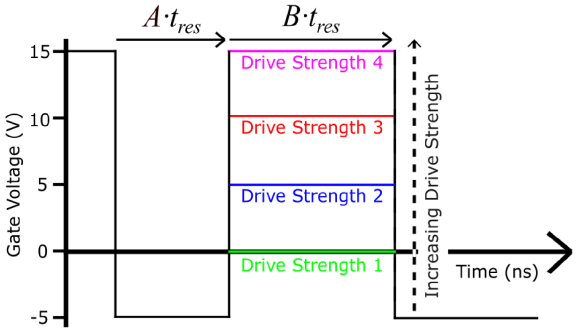

FIGURE 7. Different single pulse gate signal achievable on the MMGD for a turn off transition. Drive Strengths 1–4 for turn-off are defined in 5 V increments from the −5 V supply rail. Drive Strengths 1–4 for turn-on are defined in −5 V increments from the 15 V supply rail.

waveforms, the overshoot and switching energy were easily quantifiable. However quantifying the oscillation metric was comparably more complex. In this work it was performed by a smoothing function to damp the measured waveform, producing a more-idealised waveform while retaining sharp transition edges. The effect of applying various smoothing parameters to a 200 A hard switched turn-on current waveform can be observed in Fig. 6. The absolute difference between the measured and smoothed waveform was integrated to give the metric used for quantifying improvement in voltage/current oscillation reduction.

B. PARAMETER SWEEP

A single pulse AGD waveform, at maximum drive strength (i.e 20 V relative to the low voltage rail at −5 V) with pulses of 4 fixed widths (5 ns, 10 ns, 20 ns and 40 ns) were applied at the turn-off transient at the set point 600 V, 400 A at 80 °C while the switching delay was swept from 60 to 200 ns in 2.5 ns increments. A typical pulse is shown in Fig. 7, with the pulse being at drive strength 4. The V_{DS} waveform was measured and from this the percentage overshoot, energy loss and oscillation metric calculated. The results from these sweeps are plotted in Fig. 8 with time delay of the pulse used as the x-axis. The results for the 40 ns pulse in Fig. 8 appear different to the other results, having local minima and maxima in the region where the other pulses experienced improvement in overshoot and oscillations. This was attributed to the pulse being wide enough to cause the device to briefly turn back on, giving the V_{DS} waveform two rising edges.

Improvements in switching performance, compared to the hard switched case were observed to differing degrees when all the pulse widths were applied, with the 20 ns pulse width offering the greatest improvements of the set. The greatest decrease in overshoot was observed with a time delay of 100 ns, with the percentage overshoot and oscillation metric decreasing by 53.1% and 48.0% respectively when compared to the hard switched case, though this came with the cost of a 31.2% increase in switching energy. These results show that significant switching performance improvements are achievable using simple single pulse AGD output stages. A time domain plot of the waveform of a 20 ns pulse with a 100 ns delay is shown in Fig. 9 alongside a plot of the hard switched case for reference. It was also observed in Fig. 8 that the duration of significant improvement (greater than 25% reduction in metric) for the 20 ns pulse was 10 ns for overshoot, compared to 35 ns for the oscillation metric. This comparably wider region for the oscillation metric was observed in all the data

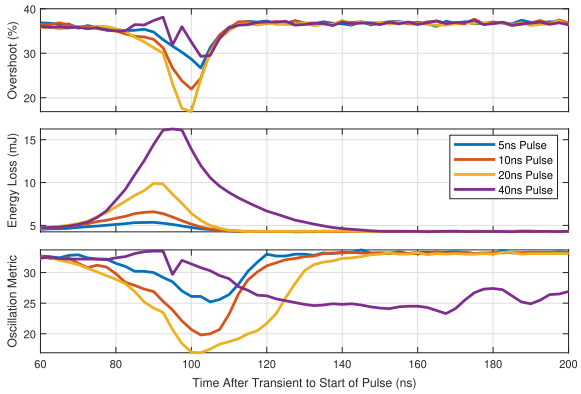

FIGURE 8. The percentage overshoot, energy loss and oscillation metric values of a turn-off transient from applying maximum drive strength (20 V) pulses of 5 ns, 10 ns, 20 ns and 40 ns to the gate at 2.5 ns increments from 60 ns after the start of the gate switching edge at 600 V, 400 A at 80 °C.

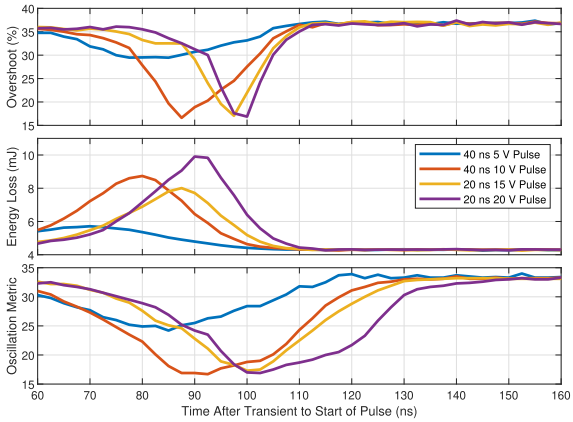

FIGURE 10. The best measured percentage overshoot, energy loss and oscillation metric values of a turn-off transient of each drive strength after applying pulses of 5 ns, 10 ns, 20 ns and 40 ns width to the gate at 2.5 ns increments. Tests performed at a set point 600 V, 400 A at 80 °C.

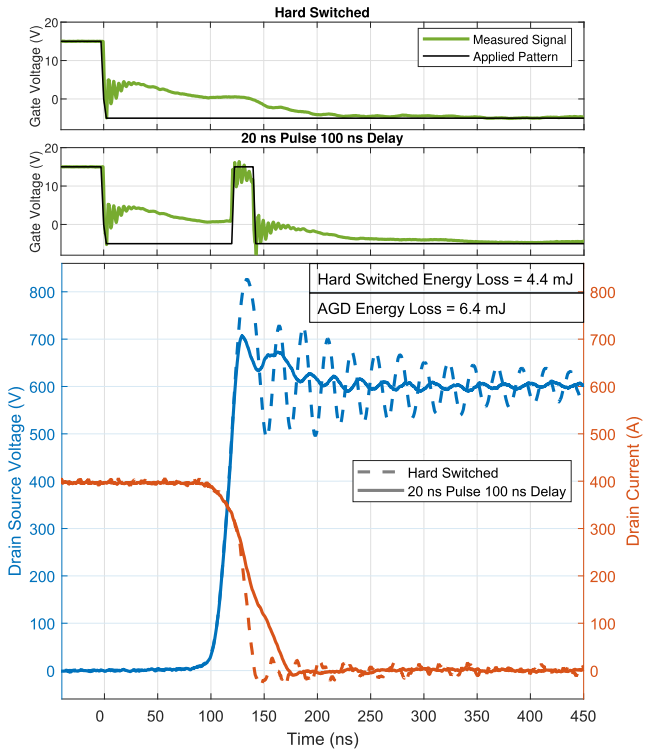

FIGURE 9. A waveform comparison between hard switched and the best result from the maximum drive strength single pulse sweep AGD patterns (20 ns duration with a 100 ns delay) at the set point 600 V, 400 A at 80 °C.

sets and indicates that the GTR of an AGD is less critical when reducing oscillations compared to when reducing overshoot.

The impact of utilising intermediate drive strengths was then investigated. Four pulses of fixed width were applied to a turn-off transient at the same set point as before with varying delays from 60 to 160 ns in 2.5 ns increments, though this time the pulses were implemented at 4 drive strengths (5, 10, 15 & 20 V pulses with respect to the −5 V supply rail) achievable on the MMGD. The corresponding pulses of these 4 drive strengths can be observed again in Fig. 7. Following this the drive-strength for each pulse width that provided the greatest reduction in overshoot at each drive strength were plotted for analysis in Fig. 10.

In Fig. 10 the maximum reductions in the percentage overshoot and the oscillation metric were similar for the pulses of 10–20 V, indicating that using an intermediate drive strength over the maximum drive strength offered negligible improvements in the maximum achievable waveform quality. However it was observed that the range of delay values that provided improvement in percentage overshoot (the metric most limited by GTR) was significantly increased at lower drive strengths, most visible moving from a single pulse of 20 V to 10 V, where the window of timing delays that provided a 25% improvement in overshoot increased from 10 ns to 20 ns. This observation suggests that the use of intermediate drive strengths has the potential to reduce the criticality of GTR by having a greater time window that a pulse can be triggered during to provide significant improvements when compared to higher drive strength pulses.

Additional tests over the temperatures 50 °C, 80 °C, 110 °C and 140 °C were undertaken using the best-performing 10 V and 15 V pulses from the previous investigation into drive strength, duration's 40 ns and 20 ns respectively. This was with the aim of investigating the impact of device junction temperature on the switching characteristic improvements recorded. The results of these tests are shown in Fig. 11. It was observed that as temperature increased the curves were shifted to the right with negligible changes to both the peak values and the duration of the window of timing delays that provided improvements. This aligns with the manufacturers data-sheet parameters that show minimal switching energy variance with temperature, the main impact of temperature observed was the change in turn-on and turn-off delay during switching caused by a shift in the threshold voltage. With the negligible effect on the window of timing delays that provided

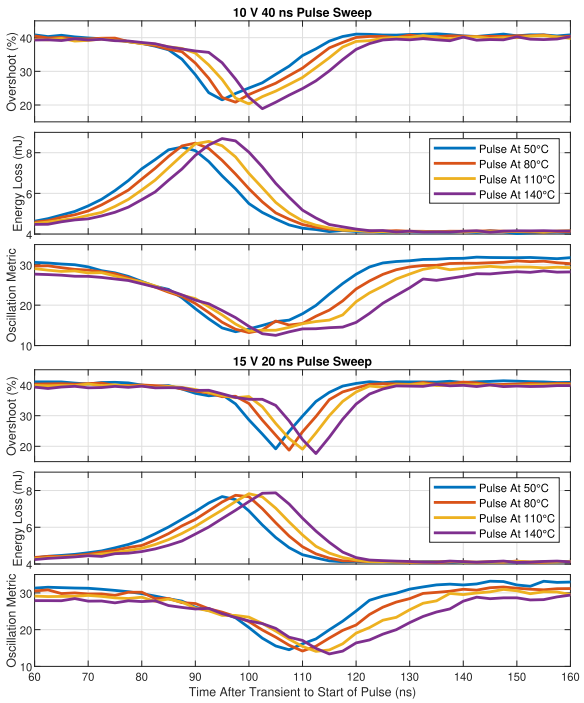

FIGURE 11. **The percentage overshoot, energy loss and oscillation metric values of a turn-off transient after applying a 40 ns 10 V pulse 20 ns 15 V pulse to the gate at 2.5 ns increments at the temperatures 50 °C, 80 °C, 110 °C and 140 °C at 600 V and 400 A.** **** These results were obtained through testing a different device of the same module type to the other results presented following a device failure.***

improvements established, in subsequent tests the temperature was kept constant at 80 °C.

IV. AUTOMATED GATE VOLTAGE PROFILING

When considering more complex AGD gate patterns, the potential number of patterns that can be created and the time required for each DPTR test to be performed, manual sweeping of pattern parameters becomes infeasible. For this reason an optimisation based approach for automatically searching for patterns was used to further investigate the influence of GTR and complexity on AGD patterns. This was implemented with a Genetic Algorithm (GA) from the built in GA solver in MATLAB's Global Optimisation Toolbox. This solver was capable of handling non-convex integer optimisation problems, and needs no information about the plant/process being optimised, making it a useful tool to find the good representative gate patterns.

A. PREVIOUS WORK IN THE LITERATURE

Automated AGD pattern searching has featured previously in the literature [21], [22], [23], [24], [25]. Some limited research has been previously undertaken into GTR and output stage complexity using a GA, though these studies have investigated these capabilities individually. To the authors knowledge there has been no study analysing and comparing both of these capabilities together, particularly at the high resolutions of up to 2.5 ns discussed in this paper. An investigation into the effects of the GTR in AGD's for Si IGBT was carried out in the publication [22]. The authors performed their experiments on a low current 8 A Si IGBT at resolutions of 400 ns, 100 ns and 40 ns while using only energy loss and overshoot as terms in the objective function. Another investigation into to the effect of using different drive strengths was performed by the authors of [29], the performance from using 9 and 63 level gate patterns was compared to hard switching at a 40 ns resolution. Previously in the literature the use of a continuous modulation signal was quantified by comparing an optimised pattern against a hard switched waveform for the case of a Si IGBT with an undefined timing resolution [21], [25].

B. GENETIC ALGORITHM IMPLEMENTATION

The genetic algorithm used in this work converges towards the solutions through the use of an objective function in the form detailed in (1) for the turn-off transient and (2) for the turn-on transient. The metrics of concern that made up the parameters for the objective function were: the switching energy (E_{switch}), the overshoot ($\frac{V_{DS}\hat{(}t)}{V_{DC}}$ and $\frac{I_D\hat{(}t)}{I_{DC}}$) and the oscillation metric ($\int_{t_1}^{t_2}(V_{DS}(t) - f_s(V_{DS}(t)))dt$ and $\int_{t_1}^{t_2}(I_D(t) - f_s(I_D(t)))dt$). The expressions for oscillation metric give the difference between the waveform and the smoothing spline introduced in Section III. Lower values of the objective function (J_{off} or J_{on}) in (1) and (2) mean that the sum of the individual cost elements representing the characteristics of concern have decreased and that ultimately the switching performance improved. The relative weight of each parameter in (1) and (2) was adjusted using scaling terms; Q_{os}, Q_E and Q_D for overshoot, energy and oscillations respectively to produce a balanced objective function capable of converging towards a good representative solution. These scaling terms were selected through pilot testing, in which these values were refined to provide convergence and a good trade-off between all the terms in the objective function. A flow chart depicting the method by which the genetic algorithm converges towards good representative gate patterns at each set point tested is presented in Fig. 12.

$$J_{off} = Q_{os}\frac{V_{DS}\hat{(}t)^2}{V_{DC}} + Q_E E_{switch}{}^2 \ldots + Q_D \int_{t_1}^{t_2}(V_{DS}(t) - f_s(V_{DS}(t)))^2 dt \quad (1)$$

$$J_{on} = Q_{os}\frac{I_D\hat{(}t)^2}{I_{DC}} + Q_E E_{switch}{}^2 \ldots + Q_D \int_{t_1}^{t_2}(I_D(t) - f_s(I_D(t)))^2 dt \quad (2)$$

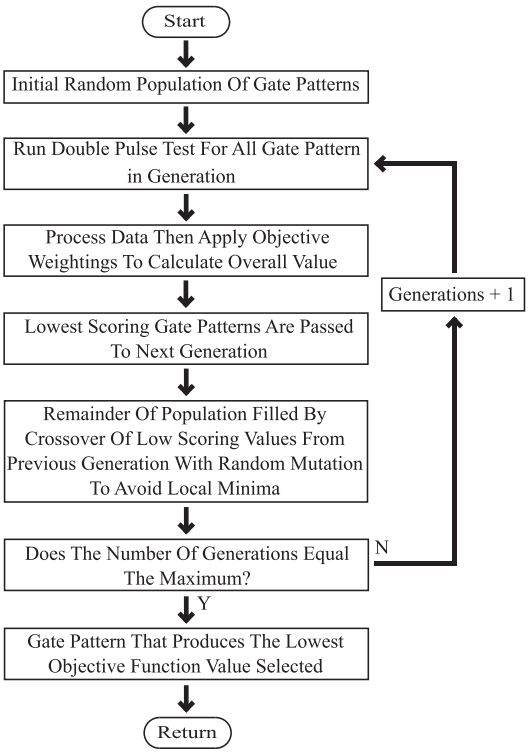

FIGURE 12. Flowchart depicting the method by which the genetic algorithm finds good representative gate patterns at each set point.

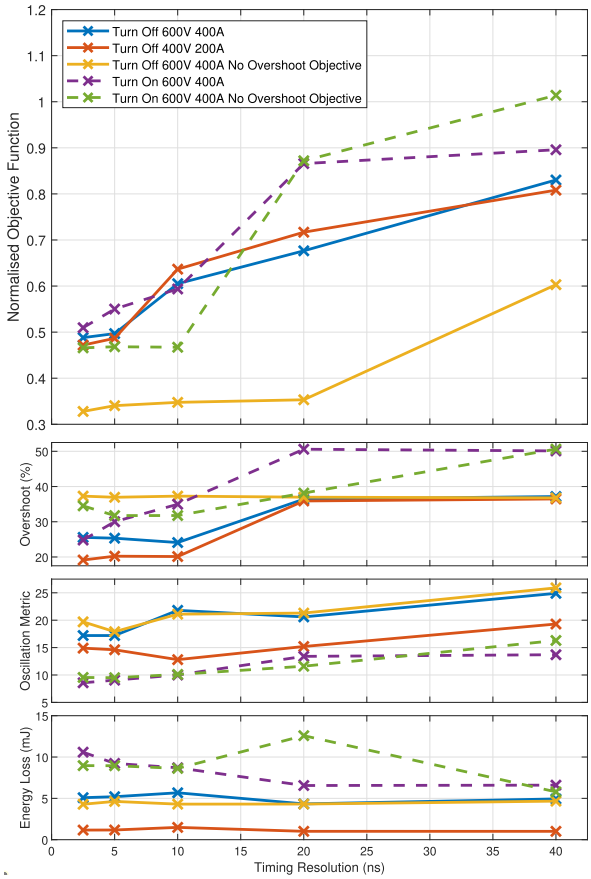

FIGURE 13. Objective function and constituent measurement plots for varying gate timing resolution values. The Objective function values are normalised using the objective function value of the hard switched case.

V. INFLUENCE OF GATE TIMING RESOLUTION ON AGD PERFORMANCE

The first AGD capability investigated using the genetic algorithm was the effect of the GTR. Initially the pattern was restricted to a single pulse of maximum drive strength to eliminate the influences of other gate drive parameters. An example of this type of pulse is shown in Fig. 7 in Section III, with drive strength 4. In this figure it can be observed that the GTR is broken down into the triggering timing resolution $A.t_{res}$ and the pulse duration timing resolution $B.t_{res}$, where A and B are integers and t_{res} is the GTR. The values of t_{res} tested were 2.5 ns, 5 ns, 10 ns, 20 ns and 40 ns.

The initial test conditions were 600 V, 400 A at 80 °C, for both turn-on and turn-off with objective function weightings of 20% switching energy, 50% overshoot and 30% oscillations for turn-off and 10% switching energy, 40% overshoot and 50% oscillations for turn-on. These weightings were selected from preliminary testing as values that ensured each parameter influenced the result. The best observed objective function value at each GTR with the corresponding overshoot, oscillation and energy loss values of these tests are displayed in Fig. 13. A supplementary test for turn-off was undertaken at 400 V and 200 A at 80 °C with the same objective function weightings as the previous turn-off test, with the results also given in Fig. 13.

For all three of these set points, displayed in Fig. 13, an overall negative correlation between the achieved objective function value and the timing resolution was observed. Alongside this for both of the turn-off set points a significant drop in gradient from 5 ns was also identified which was not observed during the turn-on tests. These results suggest that increasing the timing resolution improves the quality of the waveform to a limit where further increases in resolution provide little additional improvement. If the turn on transient follows the trend of turn off, the lack of a drop in gradient observed indicates that further improvements could potentially be obtained by utilising a higher GTR, and that the turn-on transient requires a greater GTR to produce similar improvements to those observed during turn-off.

Despite the significant improvements in the waveform quality over hard switching offered by the AGD during the turn-on transient (a 49.3% reduction in overshoot and a 50.1% reduction in oscillations), the increase in switching energy from 5.37 mJ to 10.59 mJ (a 97.2% increase) is significantly larger than the equivalent case for turn-off. An alternate objective function was investigated focusing on energy loss and oscillations, removing the overshoot objective. Two tests with this reduced objective function were undertaken at the set point

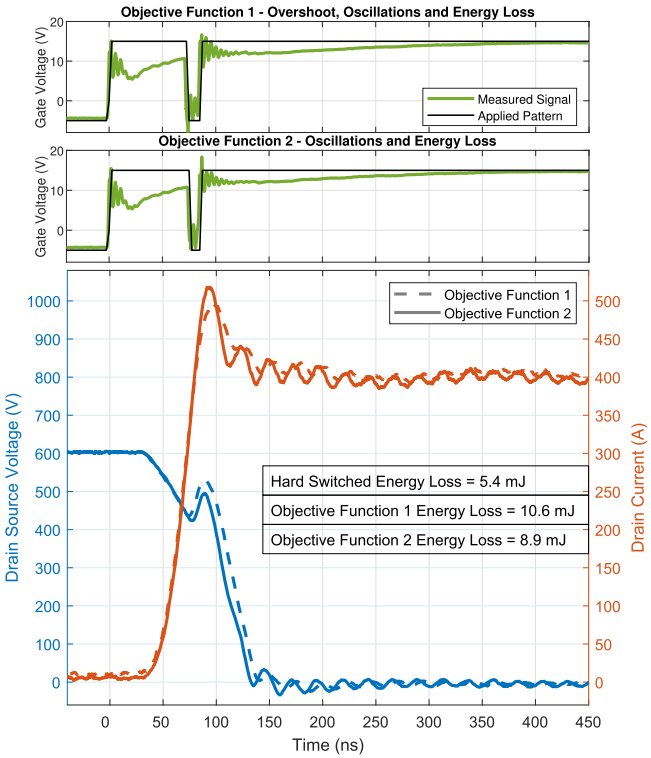

FIGURE 14. A comparison of the turn-on waveforms produced using the GA using two different objective functions at a 2.5 ns GTR and test conditions of 600 V, 400 A at 80 °C. Objective Function 1 placed weights on the switching energy, overshoot and oscillation, while Objective Function 2 included weights only on the switching energy and oscillation.

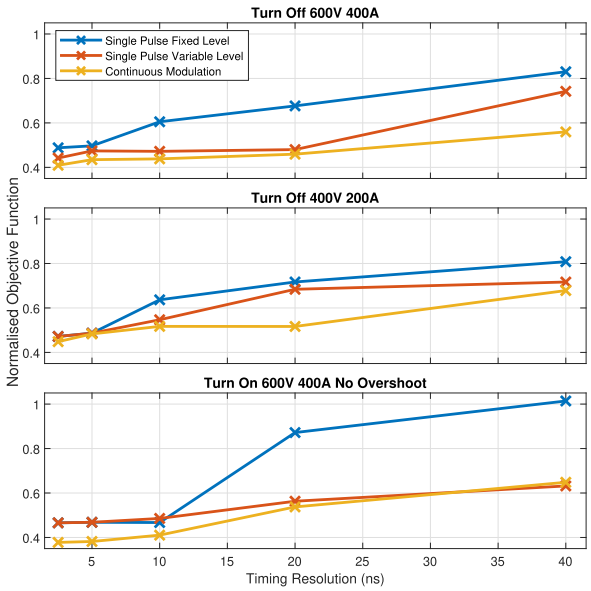

FIGURE 15. Comparison of the Objective Function value between single pulse 2 level, single pulse variable level and continuous modulation gate patterns.

600 V, 400 A at 80 °C with turn-off weightings of 25% switching energy and 75% oscillations and a turn-on weighting of 20% switching energy 80% oscillations, the results of these tests are displayed alongside the other results in Fig. 13. In addition to having the same negative correlation, they both showed a reduction in the rate of improvement previously only observed during the turn-off transient. For the turn-off test this started at a 20 ns resolution and for turn-on at 10 ns, much lower values than with an overshoot objective, indicating these values were less dependent on GTR. In addition this supports the earlier observation from Fig. 8 in Section III that the GTR is less critical to the oscillation metric than it is to the overshoot. It is suspected that this difference is due to the overshoot reduction requiring the AGD to influence the device during the relatively short overlap period, where the majority of switching energy losses occur, and so any error in timing caused by lower resolutions incurs a larger switching energy penalty. However to dampen the oscillations the larger and less energy critical time period after the overlap can be targeted instead, this period can be more easily influenced by lower resolution patterns and result in lower energy losses. The negative correlation observed in Fig. 13 also supports another previous observation that GTR is more critical for the turn-on transient, with a higher GTR required to reach the point of a reduced rate of change of improvement in the objective function, and therefore switching performance, compared to turn-off. The switching loss increase for this turn-on transient was 66.7% for a decrease in oscillations of 56.8% at 2.5 ns resolution. The resultant gate voltage, drain-source voltage and drain current waveforms produced by the GA for the turn-on transient at a GTR of 2.5 ns with and without an overshoot objective are displayed in Fig. 14 to illustrate the different solutions produced.

VI. INFLUENCE OF OUTPUT STAGE COMPLEXITY ON AGD PERFORMANCE

A. INTERMEDIATE LEVEL SINGLE PULSES

Following on from this the use of additional complexity in the AGD output stage was investigated using the GA. The use of intermediate level single pulses was investigated first, utilising the 4 drive strengths previously detailed and illustrated in Fig. 7, at the timing resolutions 2.5 ns, 5 ns, 10 ns, 20 ns and 40 ns. These tests were undertaken at 600 V, 400 A at 80 °C and 400 V, 200 A at 80 °C for turn-off with all 3 objective functions values; and at 600 V, 400 A at 80 °C for turn-on with an objective function targeting just oscillation and switching energy. The objective weightings employed in these experiments remained consistent with those used previously for the maximum drive strength single pulse tests in the Section V. The results from these experiments alongside those from the maximum drive strength single pulse tests are displayed in Fig. 15.

Fig. 15 shows that for lower GTR values (10–40 ns) the use of intermediate drive strengths offers significant improvements in achievable switching performance when compared to the maximum drive strength case. The same improvements

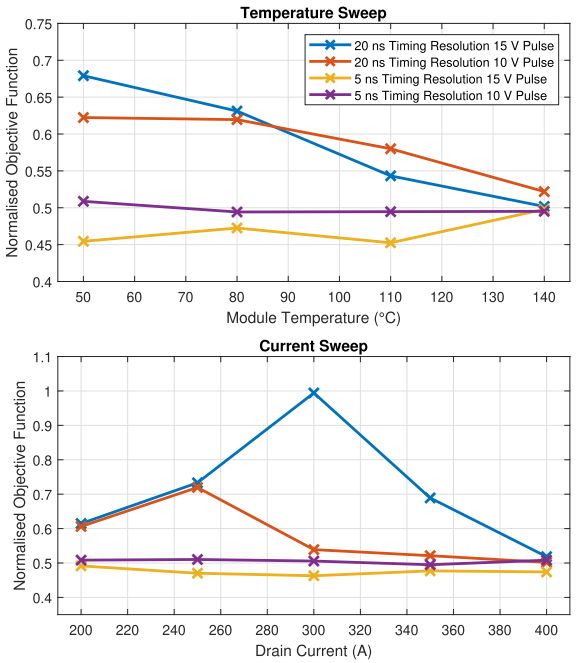

FIGURE 16. GA objective function results using 5 ns and 20 ns Gate Timing Resolution intermediate AGD pulses at a fixed current of 400 A with variation in temperature (upper), and at a fixed temperature of 80 °C with variation in current (lower).* *Temperature Sweep results were obtained through testing a different device of the same module type to the other results presented following a device failure.*

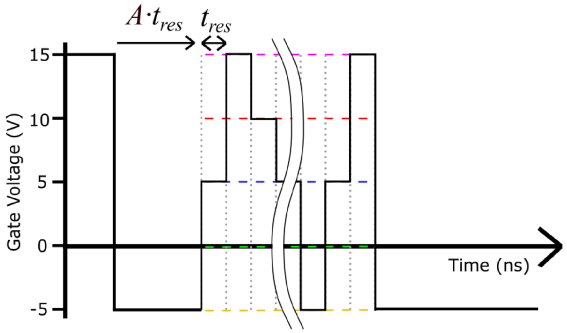

FIGURE 17. Example continuous modulation pattern achievable on the MMGD for a turn off transition displayed with the time to triggering, timing resolution, and achievable drive strengths.

were not observed at the higher GTR values (2.5–5 ns) with minimal differences in the objective function, and therefore achievable switching performance, recorded. These observations can be attributed to the effect discussed and illustrated in Fig. 10 in Section III, where the timing window in which an applied gate pattern provides significant improvement is comparably small (∼10 ns) at the maximum drive strength but increases with lower intermediate drive strengths. For lower GTR (<10 ns), the resolution is not sufficient to guarantee the pulse will be triggered within the timing window of improvement. However by utilising intermediate drive strengths, which result in greater timing windows of improvement, the probability of the pulse triggering at a good time and therefore achieving good switching characteristics increases. At higher GTR (>5 ns), with sufficient resolution to ensure the pulse is triggered within this window of improvement at maximum drive strength, the use of intermediate drive strengths and increasing the timing window of improvement offers little impact on performance.

To validate this observation a sweep of GA driven tests at different values of drain current and temperature was performed, utilising two intermediate drive strengths (10 and 15 V) and two GTR values (5 and 20 ns). The results from these tests are both given in Fig. 16, with the higher GTR (5 ns) pulses showing little variance in switching performance across the different current and temperature set points compared to the lower GTR signals (20 ns), supporting the observation that high GTR values are required to achieve consistently good results. Also observed in Fig. 16 was that the lower drive strength pulses had a smaller variance in switching performance when compared to the higher drive strength pulses at both GTR during both sweeps. This supports the observation that lower drive strength pulses, with the additional complexity they bring, can be used to reduce the criticality of GTR on providing consistently good results across different operating set points.

B. CONTINUOUS MODULATION

The final level of output stage complexity to be tested using the genetic algorithm was the use of continuous modulation, this comprised of multiple pulses of differing drive strengths, an example waveform is presented Fig 17. With the MMGD producing a continuously modulating output pattern, the GA experiments were repeated at the same GTR, objective function weightings and set points from the maximum and intermediate drive strength analysis for consistency. The objective function results obtained from these experiments were displayed alongside the previously obtained results in Fig. 15. The same general negative correlation observed earlier was also seen here though the switching characteristics were improved at all resolutions, showing this type of gate pattern gave the best overall switching characteristics at all GTR values. This observation was expected, with this output pattern having the greatest level of control to influence the gate-source voltage to produce a better switching performance. Figs. 18 and 19 show the measured external gate-source voltage, V_{DS} and I_D waveforms of the turn-on and and turn-off transients for the 2.5 ns resolution GA results of the gate patterns of a single pulse fixed level, a single pulse intermediate level and continuous modulation at 600 V, 400 A at 80 °C. The V_{DS}/I_D waveform show a minimal difference between the different AGD gate pattern types, particularly when they are compared to the hard switched case, indicating that the additional complexity above the simplest gate pattern of a single pulse at

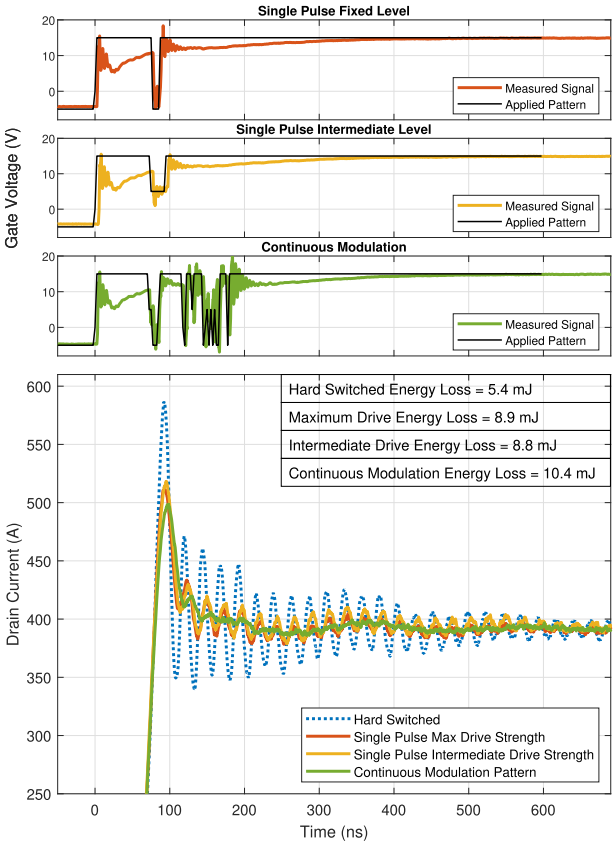

FIGURE 18. Comparison of I_D wavefroms from different gate signal complexities for the turn-on transient at 600 V, 400 A at 80 °C.

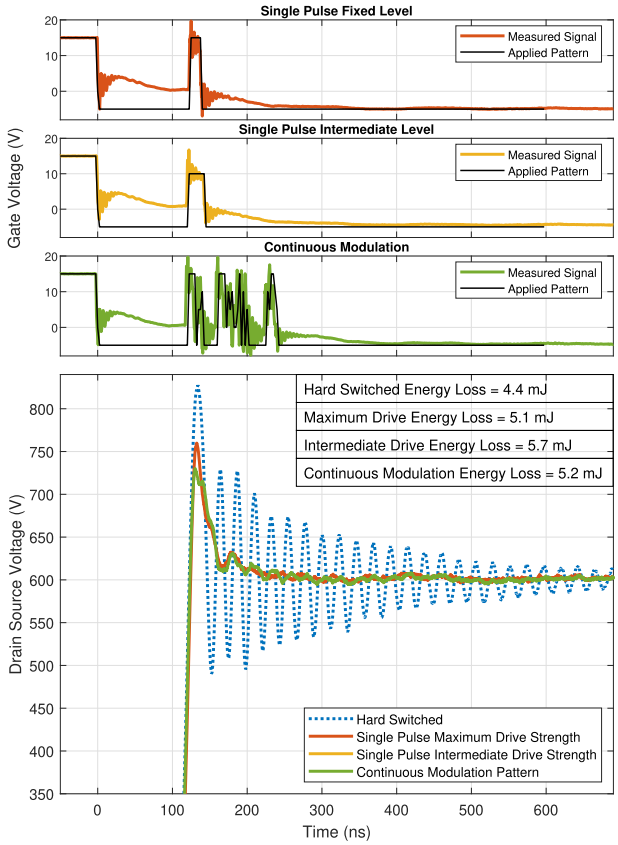

FIGURE 19. Comparison of V_{DS} waveforms from different gate signal complexities for the turn-off transient at 600 V, 400 A at 80 °C.

maximum drive strength adds only minor improvements to the switching performance.

However at lower GTR values, the results indicate that the use of additional output stage complexity has the potential to significantly improve the switching performance compared to single pulse maximum drive strength gate patterns. To demonstrate this Fig. 20 shows the measured gate-voltage, V_{DS} and I_D waveforms for the turn-off transient a hard switched case, a 2.5 ns resolution single pulse at fixed level (maximum drive strength), a 10 ns resolution single pulse at an intermediate level (drive strength 3) and a 20 ns continuous modulation gate pattern, all at 600 V, 400 A at 80 °C. Despite the large differences in resolution, the switching characteristics are similar showing that additional complexity in the driver output stage can be used to reduce the reliance on high GTR. This demonstrates that a design trade-off exists between the required GTR and the driver output stage complexity in a practical implementation of an AGD. This research can therefore be used as a guide to aid future AGD designers in finding a trade-off point for their specific application.

VII. DISCUSSION ON ACTIVE GATE DRIVE DESIGN

The previous sections have highlighted that good AGD performance can be achieved when using GTR values in the 5–10 ns range, even with simple AGD output stage designs. These values should be considered in the context of the achievable propagation delay of any AGD system. The estimated propagation delay of the existing MMGD, which achieves a GTR of 2.5 ns is detailed in Table 1, with an estimated total propagation delay of 13.6 ns from the output pins of the controlling ZYNQ-based controller to the gate-driver output connection. Conceptually an MMGD design that eliminates the frequency doubling circuit from the design would achieve a lower overall propagation delay of 7.8 ns, though this comes with the slower clock rate of 200 MHz and a GTR of 5 ns. The values detailed in Table 1 highlight the challenge of implementing a closed-loop AGD, particularly considering that a closed-loop controller will add additional detection and propagation delays to those presented in Table 1. Effective closed-loop AGD designs will likely require ASIC implementations of the controlling logic level-shifting and the AGD itself, rather than implementations formed of discrete components like the MMGD utilised in this study. Promising high-speed sub-nanosecond propagation delay level-shifters with high common-mode transient immunity have been presented [35], alongside high-frequency ASIC implementations of AGD's for Gallium Nitride devices [36].

Further potential barriers to the implementation of close-loop AGDs are illustrated in Fig. 21, which shows a closer

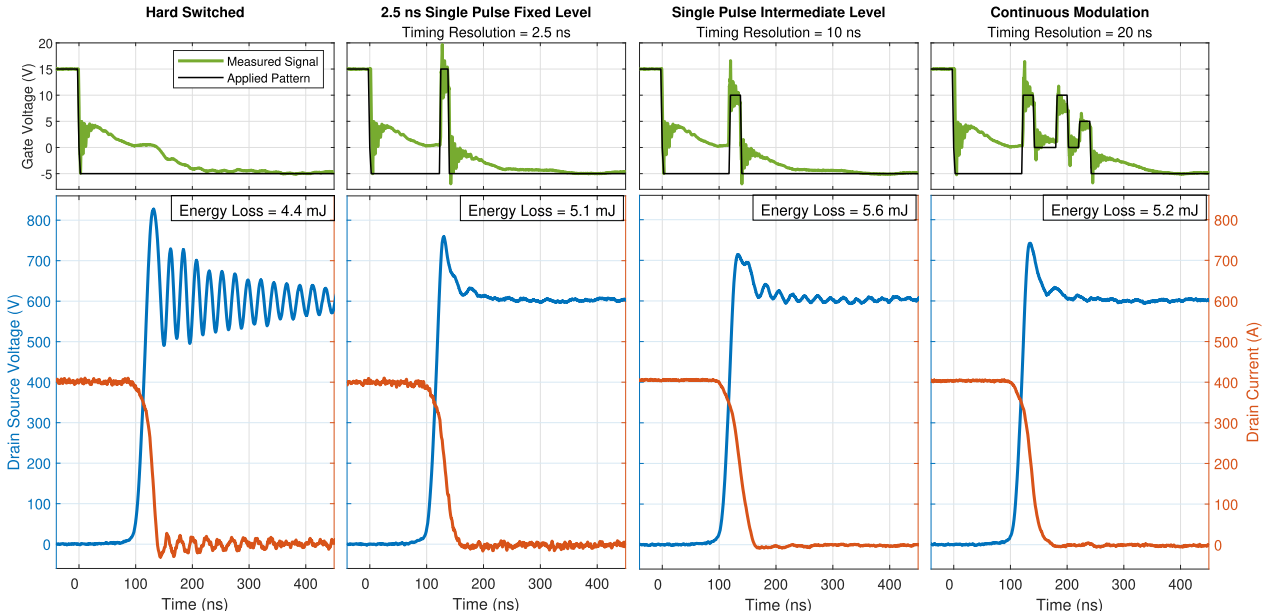

FIGURE 20. Comparison of hard switched, a 2.5 ns resolution single pulse at maximum drive strength, a 10 ns resolution pulse at an intermediate drive strength and a 20 ns resolution continuous modulation waveform for the turn-off transient at the set point 600 V, 400 A at 80 °C.

TABLE 1. Estimated Propagation Delay for the Existing MMGD Design and a Conceptual MMGD Design With Reduced Gate-Timing Resolution

Existing MMGD Design with GTR of 2.5 ns	
Component	**Propagation Delay**
NB6L295 Programmable Delay	3.1 ns
MC10EO08 XOR Gate	0.25 ns
SN65LVDS100 ECL-LVDS Converter	0.47 ns
ADN4650 LVDS Isolator Delay	4.5 ns
MAX9111/9113 LVDS Receiver Delay	1.8 ns
LMG1020 Gate Driver Delay	2.5 ns
PCB Signal Transmission Delay	0.9 ns
Total	**13.6 ns**
Conceptual MMGD Design with GTR of 5 ns	
Component	**Propagation Delay**
ADN4620 LVDS Isolator Delay	2.8 ns
MAX9111/9113 LVDS Receiver Delay	1.8 ns
LMG1020 Gate Driver Delay	2.5 ns
PCB Signal Transmission Delay	0.9 ns
Total	**8.0 ns**

view of the active gate driving region of the device waveforms for a hard-switched case and GA-optimised single-pulse patterns with GTR values of 2.5 ns drive strength 4 and 10 ns drive strength 3. These waveforms are for the turn-off transient at 600 V, 400 A at 80 °C. An approximate 4 ns delay between the edge of the modulated gate voltage applied by the MMGD (t_1 and t_3 on the diagram for the 10 ns and 2.5 ns GTR's respectively) and a measurable impact on the V_{DS} and I_D waveforms (t_2 and t_4 on the diagram for the 10 ns and 2.5 ns GTR's respectively) can be observed. This delay is proposed to be a consequence of space charge trapping which results in threshold voltage hysteresis effects [31], [32], [33]. This delay would add to any sensing and output propagation delay introduced by an AGD, adding a further challenge to closed loop AGD implementation. Accurate modeling of such effects at a nanosecond resolution is a potential future research task required to enable model-based optimization of gate-voltage patterns of the type discussed in this paper.

The GTR requirements of 5–10 ns to ensure good performance discussed in the previous section can be compared to an approximate 35 ns miller plateau time for the considered device, and a 22 ns resonance period between the commutation loop parasitic inductance and device output capacitance. To maximise efficiency it is desirable for the AGD pattern to be applied as late as possible during the miller period, this ensures the shortest transition time and minimises device switching losses while still significantly reducing overshoot and oscillations. This is highlighted in Fig. 21, where the AGD pattern with a 2.5 ns GTR single pulse maximum drive strength pattern is applied towards the end of the miller region. The AGD pattern with an intermediate drive-strength 3 pattern with a 10 ns GTR also given in Fig. 21 did not have the accuracy to be applied at the end of the miller region so was optimised by the GA to be applied earlier, sacrificing efficiency when compared to the 2.5 ns GTR case. Using a driver with increased output complexity beyond a single pulse maximum drive strength pattern, like the intermediate drive strength 3 pattern for the GTR 10 ns case, has previously been observed to significantly improve the switching performance at lower GTRs. This is thought to be a result of the lower drive strength pulses reducing the increase in transition time when compared to maximum drive strength pulses of the same

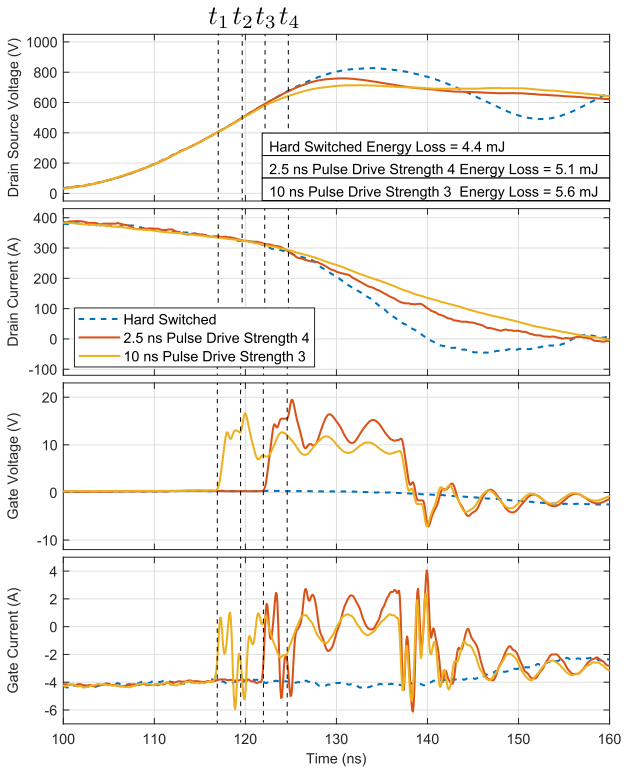

FIGURE 21. Close up view of the active gate driving region of the device waveforms with different gate signal GTR and complexities for the turn-off transient at 600 V, 400 A at 80 °C.

GTR, thereby reducing switching losses while still causing significant V_{DS}/I_D overshoot and oscillation reductions. Other parasitics such as the gate loop inductance may also influence the GTR required to give good performance, however the oscillation frequency observed in the gate-current is substantially higher than the I_D oscillation frequency, and is not reflected in the V_{DS} waveforms and so this is not suspected to have a major role.

VIII. CONCLUSION

This paper has investigated the effect that the active gate driving capabilities, gate timing resolution and signal complexity, had on the switching characteristics of a 1200 V 400 A Silicon Carbide half bridge module. A combination of parameter sweeps and a genetic algorithm were used to identify representative results to assess these capabilities. Firstly it was established that significant improvements in the switching characteristics could be achieved using active gate driving, with minor increases in energy loss. It was then observed that increasing the gate timing resolution (GTR) increased the switching performance to a point (approximately 5–10 ns), beyond which further increases in resolution provided little improvement in performance. This GTR requirement can be compared to an approximate 35 ns miller plateau time for the considered device, and a 22 ns resonance period between the commutation loop parasitic inductance and device output capacitance. Alongside this, these results suggested active gate driving during the turn-on transient results in a significantly increased energy loss and requires a greater timing resolution when compared to the turn-off transient. Furthermore it was observed that the criticality of gate timing resolution was significantly greater when attempting to reduce the overshoot compared to attempting to reduce voltage/current oscillations. This suggests that an AGD designed to target just voltage/current oscillations requires a lower timing resolution driver than one required for overshoot reduction. Improved switching characteristics were also observed when additional complexity was added to the gate voltage pattern. At higher gate timing resolutions the improvements offered by increased complexity were minimal so the simplest, single pulse maximum drive strength, pattern and associated driver are likely to be sufficient for most applications. However the reduced criticality of timing resolution observed when using more complex intermediate drive strengths suggest this could be used to facilitate the design of AGD's, capable of significantly improved switching characteristics, while being less dependent on high timing resolutions. In addition to all of these observations, this study has highlighted the need for device models that can accurately capture the behaviour of devices under nanosecond resolution AGD patterns as an important future research topic required for the successful implementation of closed loop AGD designs.

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