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Medium-Voltage Seven-Level Multiplexed Converter for AC Applications

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ABSTRACT After several decades of technological evolution, power electronics applications have become extremely important for electric/hybrid propulsion systems, smart grids, renewable energy systems, energy saving, and bulk energy storage, besides the typical applications in industrial automation and high-efficiency energy systems. In all these applications, a power conversion system with high efficiency and power density is required without sacrificing the system's power quality. The paper describes the specific characteristics and the scalar modulation strategy of a new multi-level multiplexed inverter topology for medium-voltage AC applications. The proposed power converter configuration is intended for high-power applications aiming to reduce the active device's voltage rating and losses exhibiting a resulting low switching frequency of the power switches. The proposed modulation strategy aims to reduce the computational burden and simplify the implementation process, which are at the basis of any possible industrial adoption. Simulation results and full Hardware-In-the-Loop verification support the analysis. The Hardware-In-the-Loop assessment has enabled the development of a suitable modulation strategy, and the testing of the power converter is a safe environment.

INDEX TERMS Multilevel, multiplexed, AC application, three-phase inverter.

I. INTRODUCTION

Multilevel and multicell power converters are currently considered one of the most promising industrial topology solutions thanks to the reduction of losses and, consequently, the efficiency improvement without sacrificing the system's power quality [1]. Over the years, several multilevel topologies, from the simplest to the most complex, have been introduced in literature [2], [3]. The fundamental characteristics of the multilevel converters, which determine their usability, such as DC bus neutral point voltage balancing and flying capacitor voltage control, are investigated in [4], [5].

New converter topologies have been introduced [6], presenting specific features for medium voltage applications. A review of Modular Multilevel Converters (MMC) has been presented in [7], where the application to medium voltage electric drives is illustrated in [8]. Concerning the MMC, a flying capacitor architecture has been described in [9]. Charging the floating capacitors is an issue that has been solved by adopting cost-effective solutions [10], gaining attention to the related converter topologies.

Multilevel based power converter architectures have also been investigated for DC-DC applications as in [11], [12]. It is imperative to choose the proper conversion topology and technology to enhance the characteristics of the multilevel converters, such as efficiency, power density, and quality of the input currents and output voltages. Concerning the choice of the conversion topology, size and weight of the system, its cost, energy efficiency, thermal efficiency, complexity, and electromagnetic interference are all factors that a designer should consider to achieve an optimal design [13], [14]. Naturally, it must be recognized that these factors are interdependent. For instance, a complex topology may exhibit more pronounced electromagnetic interference effects than a simpler one. Beyond the choice of the topology, there is another essential element in the hardware implementation of a power conversion system, such as the progress in new power

devices and/or technologies [15]. Today, for example, many converter designers rely on the use of new power semiconductors based on the Wide Bandgap Semiconductors (WBS), like Silicon Carbide (SiC) or Gallium Nitride (GaN) [1] which support much faster commutations than silicon power devices and can operate at higher temperatures [17]. This paper describes the three-phase 7-level Multiplexed Converter (3Φ7L M_LM_XC). The operation principles and the modulation strategy of the proposed converter are discussed, by proposing a carried-based modulation approach (i.e., effective to be implemented on industrial microcontrollers or FPGAs) and describing the commutation paths. The flying capacitor of the proposed converter requires an additional pre-charging circuit during the start-up process and balancing control during steady-state operation. The voltage balancing of flying capacitor at a steady-state can be solved by charging and discharging the capacitors using the redundant states. However, the problem of the unbalancing voltage across the flying capacitors is not addressed in this paper. The analysis is supported by simulation results and full Hardware-In-the-Loop (HIL) verification implementing the proposed modulation scheme on an industrial-grade control board. The Hardware-In-the-Loop assessment has enabled the development and testing of a suitable modulation strategy for the power converter in a safe environment, which is very close to the final usage being the code implemented in an industrial control platform.

This paper is organized as follows. In Section II, the 3Φ7L M_LM_XC topology is introduced and compared with other 7-level topologies. The carrier-based modulation strategy and the operating principle of the proposed converter are presented in Section III, including a detailed description of the commutation paths. The problem of the flying capacitor voltage balancing is addressed in Section IV. Section V presents the simulation results to verify the converter performance, while Section VI presents the experimental results using the Hardware-In-the-Loop system. A preliminary analysis of the conduction and switching losses of the 3Φ7L M_LM_XC topology is shown in Section VII. Finally, Section VI outlines the conclusion.

II. 3Φ7L M_LM_XC TOPOLOGY

The circuit diagram of the proposed topology is illustrated in Fig. 1. As can be seen, the 3Φ7L M_LM_XC is equipped with 24 switches, and it is the combination of two different topologies: the Flying Capacitor (FC) and the NPC (Neutral Point Clamped). The first FC on the top side of the power conversion is responsible for managing the upper DC-bus, while the second FC manages the lower part of the DC-bus.

Thus, the top side and the bottom side FCs work as DC-DC converters, and they play the role of the multiplexer, hence the name multi-level multiplexed converter. Both top and bottom FCs provide four voltage levels (0, $^1/_2V_{BUS}$, $^1/_3V_{BUS}$, $^1/_6V_{BUS}$, top side and 0, $-^1/_2V_{BUS}$, $-^1/_3V_{BUS}$, $-^1/_6V_{BUS}$ bottom side). Consequently, the single phase of the NPC topology can provide seven voltage levels, 0, $\pm 1/2V_{BUS}$, $\pm 1/3V_{BUS}$, $\pm 1/6V_{BUS}$. The main advantage of this configuration is that no filter

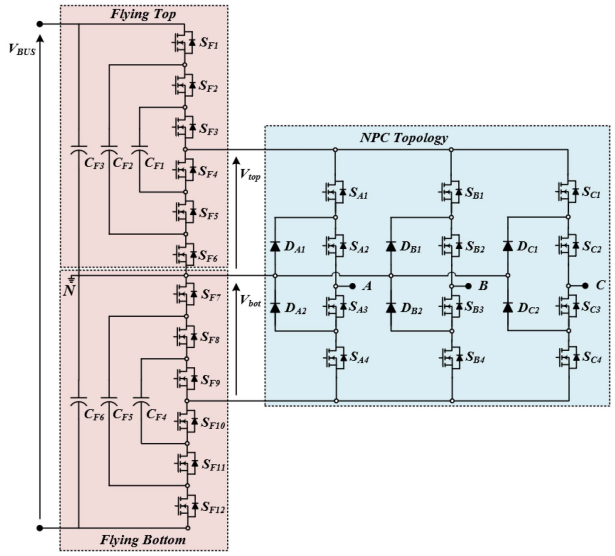

FIGURE 1. Circuit diagram of 3Φ7L M_LM_XC.

elements are used between the flying capacitor and the NPC topologies. Another benefit of the proposed topology is the low voltage stress across the power semiconductors, which enables to use low-cost silicon components or, in the alternative, SiC devices can be used to improve the efficiency and the power density. Several multilevel topologies able to provide 7 voltage levels at the output are proposed in the literature [18], [19], [20], [21], [22], [23], [19], [24], [25], [26], [27], [28], [29]. The comparison of the three-phase 7-level (7L) converter topologies in terms of the number of power semiconductors, including switches and diodes, the number of DC-bus capacitors and flying capacitors, as well as the maximum voltage stress across the components is shown in Table 1. As can be seen, the 7L Active Neutral point Clamped (ANPC) [22], the 7L Flying Capacitor NPC (FC-NPC) [24], and the proposed topology makes fewer power semiconductors compared to the other topologies. The 7L NPC [20], the Hybrid ANPC (H-ANPC) [25], as well as the 7L modular multilevel converter (MMC) [28] require a larger number of power semiconductors. The disadvantages of the 3Φ7L M_LM_XC are the voltage stress across the external flying capacitors C_{F3}, C_{F6} and the voltage across the power semiconductors located in NPC, which is equal to $^1/_2V_{BUS}$. However, the commutation of the power semiconductors placed into NPC of the 3Φ7L M_LM_XC can occur at zero current, and thus the switching losses can be drastically reduced.

III. MODULATION STRATEGY

Sinusoidal Pulse Width Modulation (SPWM) has been used to control the power semiconductors of the topology. Fig. 2 shows the implemented modulation scheme for the modulation depth M_0 below and above 0.5. When $M_0 \leq 0.5$, the top and bottom FCs provide $\pm 1/3V_{BUS}$ (given that S_{F3}, S_{F5}, S_{F6}, S_{F7}, S_{F8}, S_{F10} are in on-state conduction mode) and two carrier signals c_{Nt2}, c_{Nt3} are compared to the modulating signals,

TABLE 1. Number of Components in Three-Phase 7-Level Converter Topologies

	Number of power semiconductors	Number of DC-bus capacitors	Number of Flying Capacitors	Maximum Capacitors voltage stress	Maximum power semiconductors voltage stress	Number of power semiconductor with $^1/_6V_{BUS}$
7L NPC [20]	66	6	-	$^1/_6V_{BUS}$	$^1/_6V_{BUS}$	66
7L FC [21]	36	2	15	$^5/_6V_{BUS}$	$^1/_6V_{BUS}$	36
7L ANPC [22]	30	2	6	V_{BUS}	$^1/_2V_{BUS}$	12
7L HC [23], [24]	36	3	6	$^1/_3V_{BUS}$	$^1/_3V_{BUS}$	12
7L FC-NPC [25]	24	-	12	$^1/_2V_{BUS}$	$^1/_2V_{BUS}$	12
7L H-ANPC [26]	57	2	15	$^1/_2V_{BUS}$	$^1/_2V_{BUS}$	6
7L E-Type [27]	36	6	-	$^1/_6V_{BUS}$	$^2/_3V_{BUS}$	12
7L Generalized [28]	36	3	12	$^1/_3V_{BUS}$	$^1/_3V_{BUS}$	6
7L MMC [29]	72	-	36	$^1/_6V_{BUS}$	$^1/_6V_{BUS}$	72
7L Cascade [30]	36	6	-	$^1/_6V_{BUS}$	$^1/_6V_{BUS}$	36
7L M_LM_XC	30	-	6	$^1/_2V_{BUS}$	$^1/_2V_{BUS}$	12

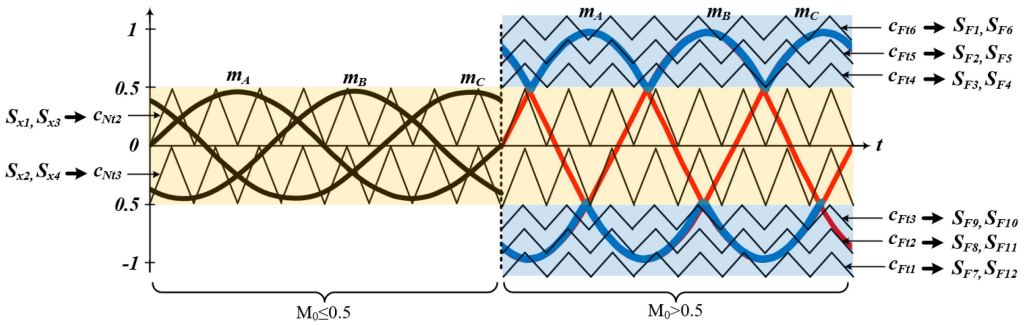

FIGURE 2. Carrier-based modulation scheme for the 3Φ7L M_LM_XC.

providing the control signals of the power semiconductors located in the NPC.

In case $M_0 > 0.5$, it is possible to notice that the top and the bottom part of the modulation signals (blue line) are managed by the FCs, as well as the transitions of the modulation signals (red line) are handled by the NPC converter. The control signals of the switches located in the bottom FC are generated by the comparison between the lower modulating signal (highlighted in blue) and three carrier signals, c_{Ft1}, c_{Ft2}, and c_{Ft3}, while the control signals of the power semiconductors placed into the top FC are provided through the comparison between the higher modulating signal (highlighted in blue) and three carrier signals c_{Ft4}, c_{Ft5}, c_{Ft6}. The comparison between the modulating signals highlighted in red and two carrier signals c_{Nt2} and c_{Nt3}, generate the power semiconductors' control signals in the NPC. Thus, the voltage provided by the proposed converter shows seven voltage levels in Fig. 3, in which the ten sectors are clearly visible at the bottom side.

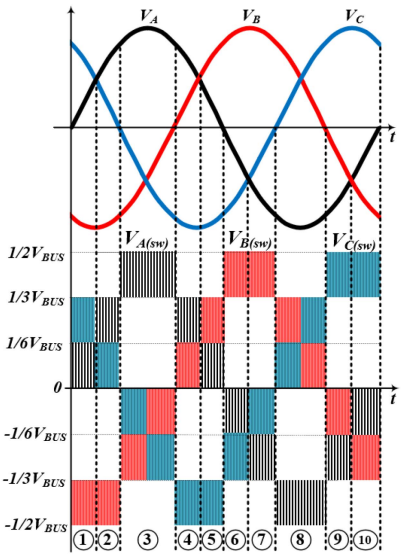

FIGURE 3. Voltage waveforms before and after the output filters.

A. FORBIDDEN STATES

The presented configuration exhibits inherent forbidden states, which must be avoided to not occur in catastrophic failure of the power converter. The proposed carrier-based modulation will be able to prevent such conditions thanks also to the FPGA implementation. The PWM modulation strategy has been implemented to stop any potentially dangerous state propagated by comparing the carrier and the modulating signal. The specific operating sector must be distinguished to detect the switching pulses that are not allowed. The modulating signals of the particular phase are split into ten different sectors. For instance, considering the phase A, it is possible recognize ten sectors, as shown in Fig. 3. Given that the positive DC-bus and the negative DC-bus are shared between the three phases of the NPC inverter, when the output voltage vector to be synthesized is inside a specific sector, the affected

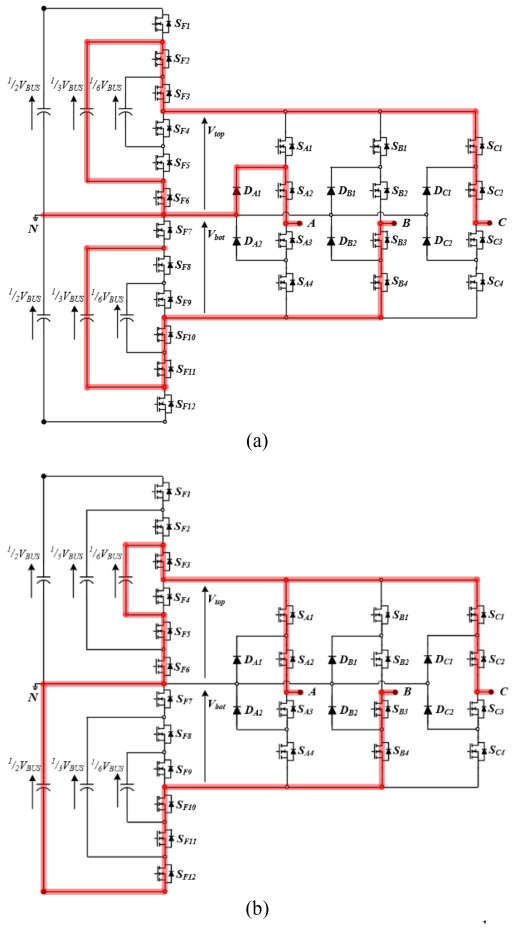

FIGURE 4. Commutation path in the sector 1: (a) $V_{A(sw)}=0$, $V_{B(sw)}=-{}^1/_3V_{BUS}$, $V_{C(sw)}={}^1/_3V_{BUS}$, (b) $V_{A(sw)}={}^1/_6V_{BUS}$, $V_{B(sw)}=-{}^1/_2V_{BUS}$, $V_{C(sw)}={}^1/_6V_{BUS}$.

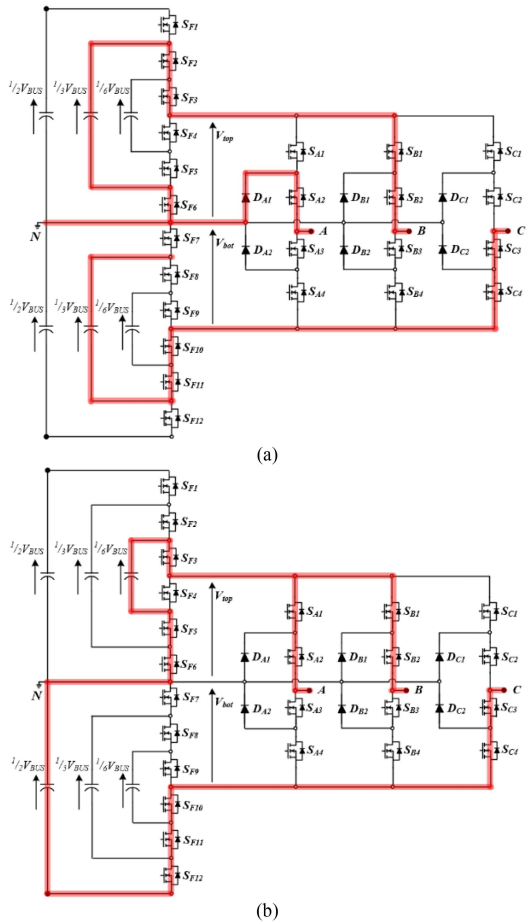

FIGURE 5. Commutation path in the sector 5: (a) $V_{A(sw)}=0$, $V_{B(sw)}={}^1/_3V_{BUS}$, $V_{C(sw)}=-{}^1/_3V_{BUS}$, (b) $V_{A(sw)}={}^1/_6V_{BUS}$, $V_{B(sw)}={}^1/_6V_{BUS}$, $V_{C(sw)}=-{}^1/_2V_{BUS}$.

switches are forced to their appropriate state. As seen in Fig. 3, in sector 1 the phase A commutates between 0 and ${}^1/_6V_{BUS}$, while the phase C and then the phase B commutate between ${}^1/_6V_{BUS}$ and ${}^1/_3V_{BUS}$ in the same sector. Thus, in sector 1, phase A of the NPC is kept to zero through the clamped diode when the top FC provides ${}^1/_3V_{BUS}$, as illustrated in Fig. 4(a), while in the other state, both phases A and C provide ${}^1/_6V_{BUS}$, as shown in Fig. 4(b).

In sector 2, there is the same situation as in sector 1, but with phases A and C reversed. In sector 4, the same situation occurs, but this time, it is phase B instead of phase C to share the positive DC-bus with phase A. Consequently, when the output of phase B provides ${}^1/_3V_{BUS}$, phase A is kept to zero, as shown in Fig. 5(a), whereas in the other instant, both phases A and B provide ${}^1/_3V_{BUS}$, as illustrated in Fig. 5(b).

In sector 5, there is the same situation as in sector 4, but with phases, A and B reversed. A similar situation occurs in sectors 6, 7, 9, and 10.

IV. SIMULATION RESULTS

The operation principle, including the modulation scheme of the 3Φ7LM$_L$M$_X$C, has been implemented in Matlab/Simulink

TABLE 2. Operating Point of the 3Φ7LM$_L$M$_X$C

DC-bus voltage V_{BUS}	11 kV
Line-to-line RMS voltage V_{xLL} with x∈{A, B, C}	6.6kV
switching frequency f_{sw}	5 kHz
fundamental frequency f_0	50 Hz
Output filter capacitance C_{0f}	20 µF
Output filter inductance L_{0f}	200 µH
Resistive load R_{Load}	10 Ω
Output Power P_0	3.8 MW

with a fully detailed model, which considers the physical realization of the modulation strategy on the control platform. The characteristic waveforms and the voltage stress of the power semiconductors have been evaluated according to the operating point listed in Table 2. Fig. 6 shows the voltage waveforms at steady-state under resistive load when the modulation depth M_0 is below (a) and above 0.5 (b).

As it can be seen, when $M_0 = 0.4$, the phase-to-neutral switching voltages $V_{xN(sw)}$, with $x\in\{A, B, C\}$, show three-voltage level, as well as the positive and negative DC-bus voltages V_{top} and V_{bot} are equal to $\pm{}^1/_6V_{BUS}$, respectively. When $M_0 = 0.94$, the phase-to-neutral switching voltages $V_{xN(sw)}$ show seven voltage levels, and the output voltages

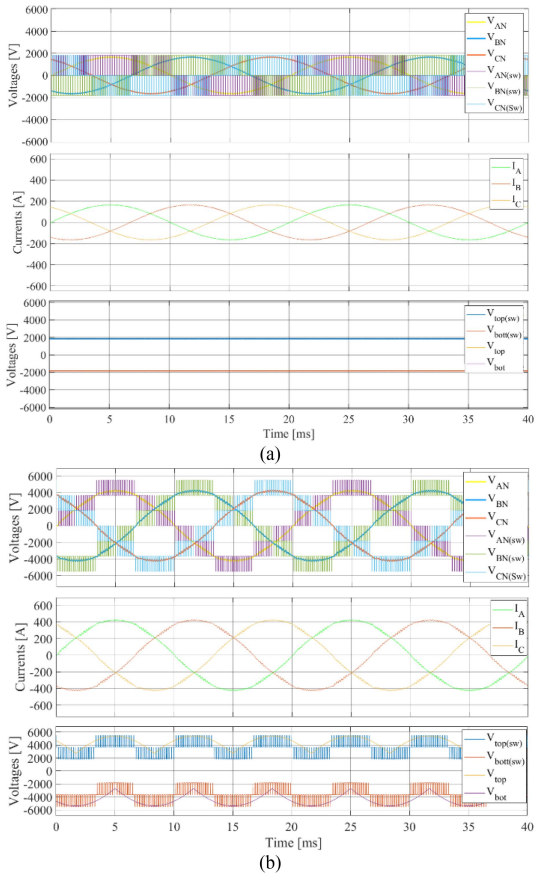

FIGURE 6. Waveforms at a steady state, from top to bottom: Phase-to-neutral before and after filter V_{xN}, $V_{xN(sw)}$, three-phase currents i_x and top and bottom DC-bus voltages $V_{top(sw)}$ and $V_{bot(sw)}$: (a) M_0=0.4, (b) M_0=0.94.

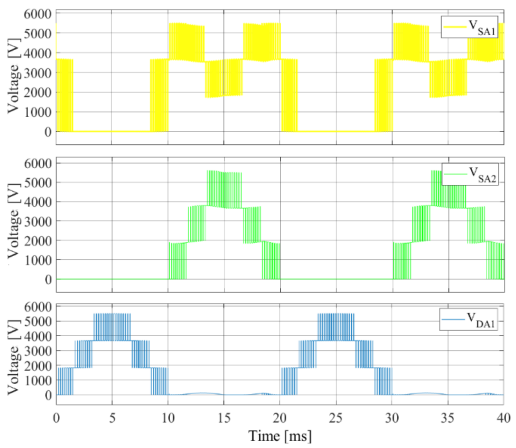

FIGURE 7. Voltage stress across the NPC power semiconductors S_{A1}, S_{A2}, D_{A1}.

provided by the top and the bottom FCs (V_{top} and V_{bot}) draw three voltage levels. The voltage across the power semiconductors of the top side of the NPC phase leg A S_{A1}, S_{A2}, D_{A1} are illustrated in Fig. 7. Fig. 8 shows the power semiconductors' voltage stress in the top FC and bottom FC, S_{F1}, S_{F2}, S_{F3}, S_{F10}, S_{F11}, S_{F12}. From this analysis, it is possible to state that the maximum voltage stresses of power semiconductors placed into NPC and FCs are $^1/_2V_{BUS}$ and $^1/_6V_{BUS}$, respectively.

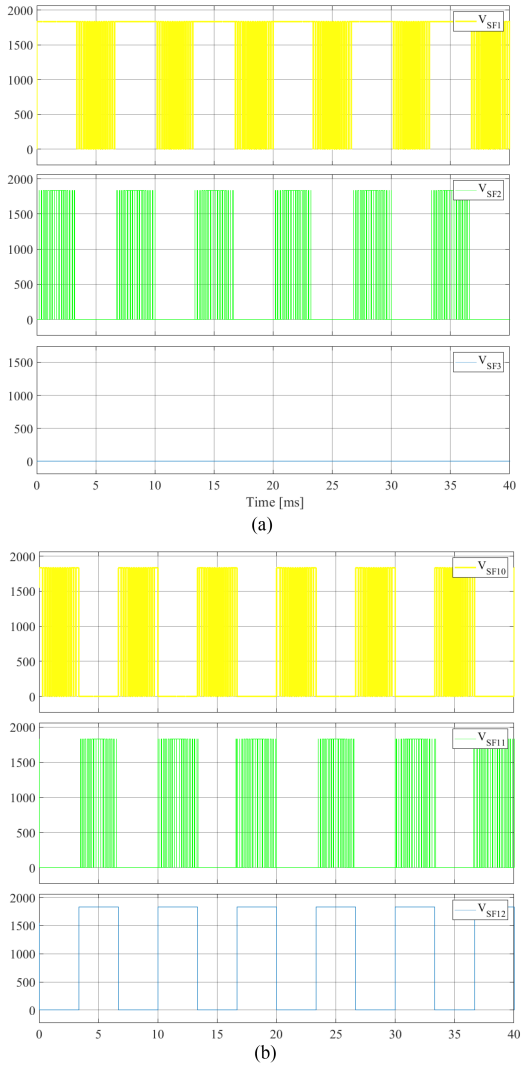

FIGURE 8. (a) Voltage stress across the power semiconductors: (a) Located in the top FC S_{F1}, S_{F2}, S_{F3}. (b) Located in the bottom FC S_{F10}, S_{F11}, S_{F12}.

V. CAPACITORS VOLTAGE BALANCING AND DESIGN

The flying capacitors can be balanced starting from the proposed modulation control scheme. The external flying capacitors C_{F3} and C_{F6} can be balanced by adding the offset in the modulation signals [30]. The control signals are written in (0), where m_0 is the offset of the signals, M_0 is the modulation depth and ξ=01,2.

$$m_{A,B,C}(t) = m_0 + \frac{1}{2}\left[1 + M_0 \sin\left(\omega_0 t - \xi\frac{2\pi}{3}\right)\right] \quad (1)$$

It can be proven that the average current into the neutral point N depends on the offset m_0. Thus, by controlling the modulation index offset m0, it is possible to achieve an

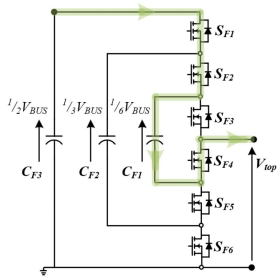

FIGURE 9. Charging path for the flying capacitors C_{F1}.

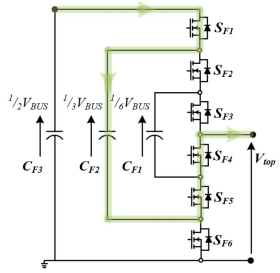

FIGURE 10. Charging path for the flying capacitors C_{F2}.

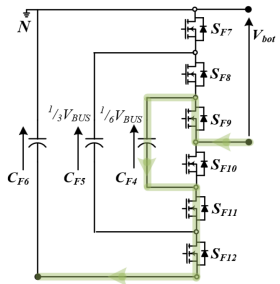

FIGURE 11. Charging path for the flying capacitors C_{F4}.

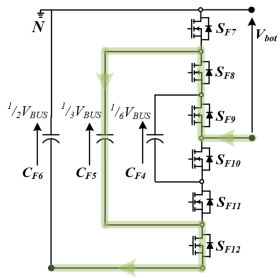

FIGURE 12. Charging path for the flying capacitors C_{F5}.

equal voltage distribution among the capacitors C_{F3} and C_{F6}. Regarding the flying capacitors C_{F1}, C_{F2}, C_{F4} and C_{F5}, the situation is different. The main idea is to exploit some commutation instants to charge the capacitors in each sector, as shown respectively in Fig. 9 for C_{F1} and in Fig. 10 for C_{F2}.

When the capacitor C_{F1} is charged, the top FC provides $^1/_3V_{BUS}$, while the top FC provides $^1/_6V_{BUS}$ when the flying capacitor C_{F2} is charged. The same happens to the flying capacitors C_{F4} and C_{F5}, as shown in Figs. 11 and 12, respectively. If the capacitor C_{F5} is charged, the bottom FC provides $-^1/_6V_{BUS}$. As can be noticed, the flying capacitor voltages are self-balanced without additional balancing circuits.

Since the load current flow through the flying capacitors, film capacitors must be used. Film capacitors have a much lower ESR than electrolytic capacitors but are bulkier. The minimum required value of the flying capacitors depends on several factors, such as maximum permissible voltage ripple, switching frequency, and current flowing through the flying capacitors. Consequently, the choice of the flying capacitors to be used can be made on two criteria: 1) current stress and 2) minimizing the peak value of the output voltage ripple. In particular, the voltage ripple is related to the current and the capacitor by the relationship in (2), where I_{FC} is the current flowing in the flying capacitor and d_{FC} is the duty cycle of the flying capacitor current. The maximum voltage ripple $\Delta V_{FC\_\max}$ occurs in a switching period when $d_{FC} \cdot I_{FC}$ is maximum.

$$\Delta V_{FC\_\max} = \frac{\max\left(d_{FC} I_{FC}\right)}{2 f_{sw} C_{FC}} \tag{2}$$

To simplify the design process, for a given power factor, the worst-case scenario for maximum voltage ripple is considered, i.e.,:

$$\Delta V_{FC\_\max}\big|_{(worst\,case)} = \frac{\max\left(d_{FC}\right)\max\left(I_{FC}\right)}{2 f_{sw} C_{FC}} \approx \frac{I_{BUS}^{pk}}{2 f_{sw} C_{FC}} \tag{3}$$

Consequently, the minimum flying capacitor value can be calculated considering the (4).

$$C_{FC} \geq \frac{I_{BUS}^{pk}}{2 f_{sw}\, \Delta V_{FC\_\max}\big|_{(worst\,case)}} \tag{4}$$

To precharge the flying capacitors, resistors can be installed in parallel. There is no specific formula for calculating these resistor values. Still, they should be selected so that when no power semiconductors are switching, and the general circuit behaviour is similar to an RC network, the steady state value of the flying capacitor voltages are within 5% of their nominal value.

VI. EXPERIMENTAL VERIFICATION

Complete power converter configuration has been real-time emulated by the eHS64 FPGA solver from OPAL-RT. The high-fidelity, high-performance OP4610XG Hardware-In-the-Loop allowed to correctly represent the power converter behavior under the proposed modulation strategy. Inverter switches' commutation patterns are provided by an industrial control platform directly connected to the HIL system. The modulation scheme has been implemented on the PED-Board controller directly on the FPGA taking advantage of the LabVIEW graphical environment. Thanks to the FPGA implementation, the carrier-based approach was possible due

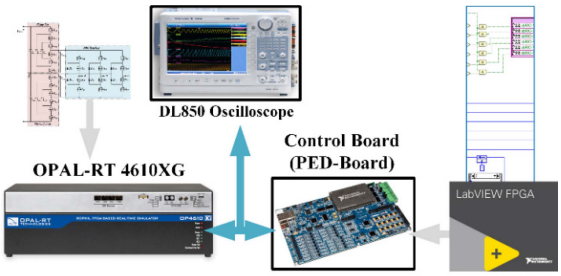

FIGURE 13. Real-time arrangement for testing the 3Φ7L M_LM_XC modulation strategy.

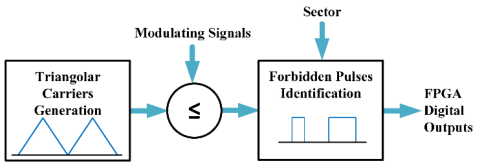

FIGURE 14. Block diagram for the suppression of the prohibited switching pulses.

to the possibility of stopping the forbidden states straightforwardly. The experimental set-up used for the final verification is shown in Fig. 13.

A. FPGA IMPLEMENTATION FOR THE FORBIDDEN STATES

As previously described, a pure carrier-based PWM modulator generates specific switching configurations that must be avoided to save the converter from dangerous and catastrophic situations. Accordingly, the FPGA checks for every switching pulse when it falls in the forbidden list. Consequently, the prohibited impulses will be inhibited, as shown in Fig. 14. Sector identification is performed continuously with a time resolution of 25 ns, which is the FPGA base clock.

B. STEADY-STATE TEST

The experimental verification of the 3Φ7LM_LM_XC has been performed according to the operating point of Table 2. Fig. 15 shows the phase-to-neutral switching voltage $V_{A(sw)}$ (violet line), the phase voltage V_A (yellow line), the top DC-bus voltage $V_{top(sw)}$ (green line) and the bottom DC-bus voltage $V_{bot(sw)}$ (cyan line) for different values of the modulation depth.

It is easy to recognize the seven voltage levels provided by the phase A. Moreover, as it results in Fig. 6, the voltages $V_{top(sw)}$ and $V_{bot(sw)}$ show three voltage levels. The three-phase voltages V_A, V_B and V_C are illustrated in Fig. 16, whereas the normalized harmonic content of the phase-to-neutral voltage related to the phase A, V_A, is illustrated in Fig. 17. As can be seen, the 5th and 7th harmonics are dominant at low frequencies.

Fig. 18 shows the THD of the phase-to-neutral voltage V_A as a function of the modulation depth M_0. As can be seen, the THD exhibits a relatively high value when M_0 is close to *0.6* since the duty cycle of the switches into NPC is

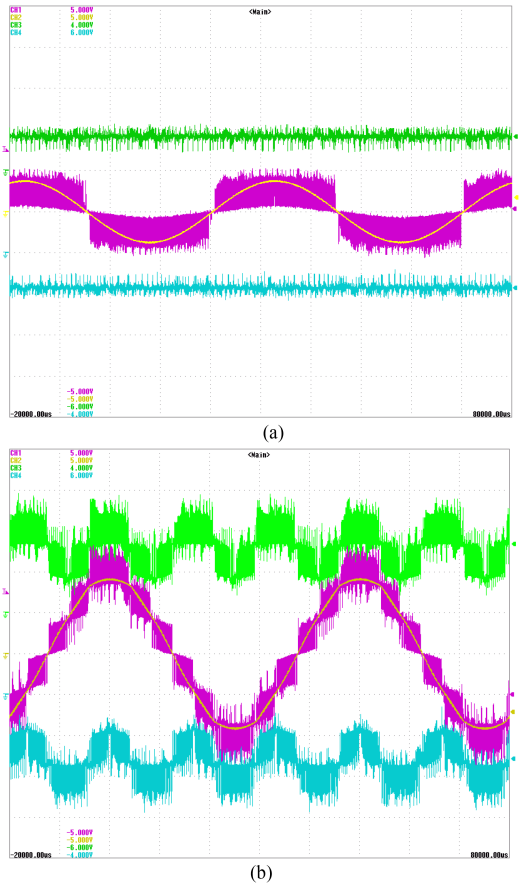

FIGURE 15. Phase-to-neutral switching voltage $V_{A(sw)}$ (violet line), phase voltage V_A (yellow line), top DC-bus voltage $V_{top(sw)}$ (green line) and bottom DC-bus voltage $V_{bot(sw)}$ (cyan line): (a) M_0=0.4, (b) M_0=0.94. 2500 V/div, 4 ms/div.

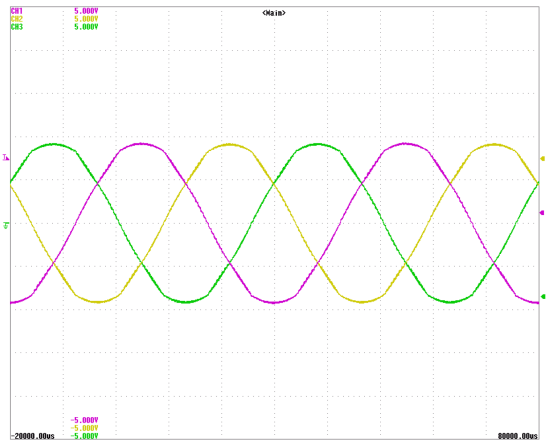

FIGURE 16. Three-phase voltages waveforms V_A (violet line), V_B (yellow line), V_C (green line) when M_0=0.94. 2500 V/div, 4 ms/div.

different if the transition happens when the voltage is high or low. The three-phase currents flowing into output inductances are shown in Fig. 19. It can be noticed that the three-phase voltages and currents are perfectly symmetrical and balanced. The Total Harmonic Distortion (THD) estimated up to the 50^{th} harmonic is *1.52%*.

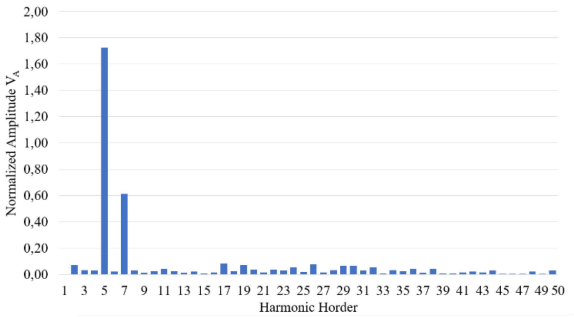

FIGURE 17. Normalized phase-to-neutral voltage V_A harmonic content when M_0=0.94.

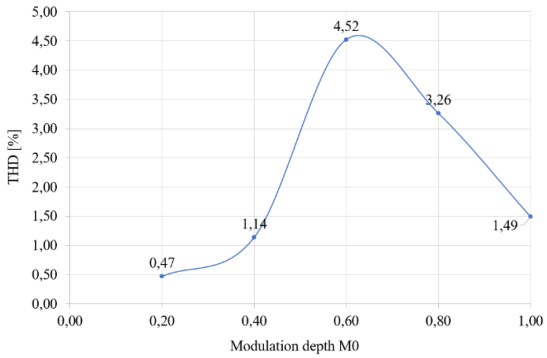

FIGURE 18. Total harmonic distortion of the phase-to-neutral voltage V_A as a function of modulation depth M_0.

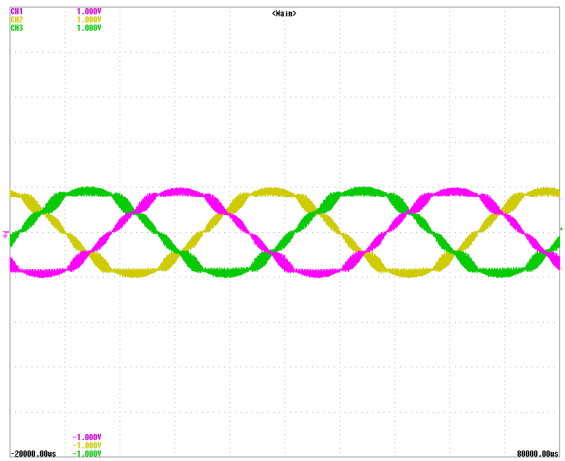

FIGURE 19. Three-phase inductor currents waveforms I_A (violet line), I_B (yellow line), I_C (green line) M_0=0.94. 400 A/div, 4 ms/div.

Fig. 20 illustrates the voltage waveforms across the power switches S_{A1}, S_{A2}, and the power diode D_{A1}. As can be seen, these waveforms are coincident with those of Fig. 7. Finally, Figs. 21 and 22 show the voltage stress of the power semiconductors located in the top FC S_{F1}, S_{F2}, S_{F3} and the voltage stress found in the bottom FC S_{F10}, S_{F11}, S_{F12}.

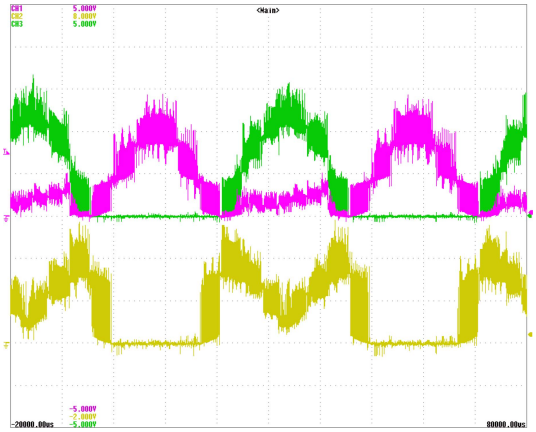

FIGURE 20. Voltage stress across the NPC power semiconductors S_{A1} (yellow line), S_{A2} (green line), D_{A1} (violet line). 2500 V/div, 4 ms/div.

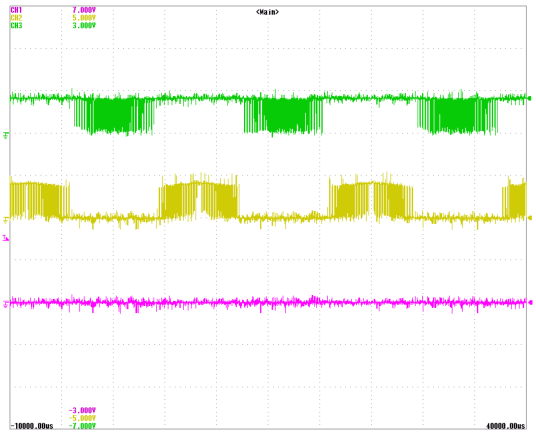

FIGURE 21. Voltage stress across the top FC power semiconductors S_{F1} (green line), S_{F2} (yellow line), S_{F3} (violet line). 2500 V/div, 4 ms/div.

VII. PRELIMINARY ANALYSIS OF THE CONVERTER LOSSES

The power losses are evaluated in the Plexim/Plecs environment, where the thermal model of power semiconductors has been created, producing multi-dimensional lookup tables based on the parameters provided by the manufacturers. In this case, the losses have been evaluated considering the use of the 3300V IGBT module (manufacturer Infineon, part number FZ2400R33HE4) and for the FCs the 2300V IGBT module (manufacturer Infineon, part number FF1800R23IE7P).

Assuming the DC-bus voltage $V_{BUS} = 11\ kV$, line-to-line RMS voltage $V_{xLL} = 6.6\ kV$, switching frequency $f_{sw} = 5\ kHz$, fundamental frequency $f_0 = 50\ Hz$, modulation depth $M_0 = 0.94$, output filter capacitance $C_{0f} = 20\ mF$, output filter inductance $L_{0f} = 200\ mH$, Fig. 23(a) illustrates the conduction and switching losses in both top and bottom FCs as a function of the output power, while Fig. 23(b) shows the conduction and switching losses in the NPC as a function of the output power. As can be seen, the switching losses are higher than the conduction losses since the power switches commutate at high DC-bus voltage. Fig. 24 shows the efficiency and power

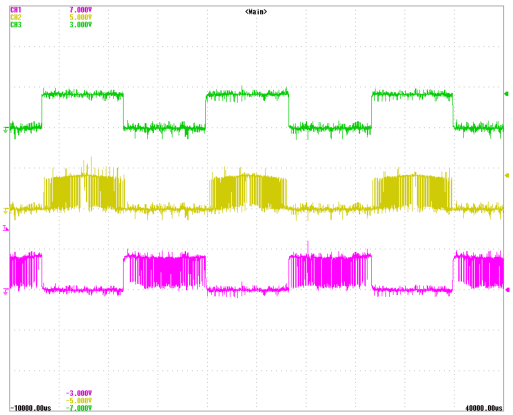

FIGURE 22. Voltage stress across the bottom FC power semiconductors S_{F10} (violet line), S_{F11} (yellow line), S_{F12} (green line). 2500 V/div, 4 ms/div.

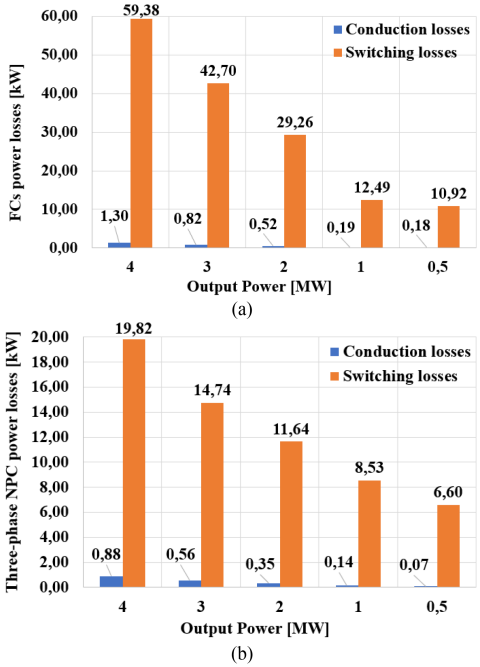

FIGURE 23. Power losses distribution of the power semiconductors located in: (a) Top and bottom FCs, (b) Three-phase NPC.

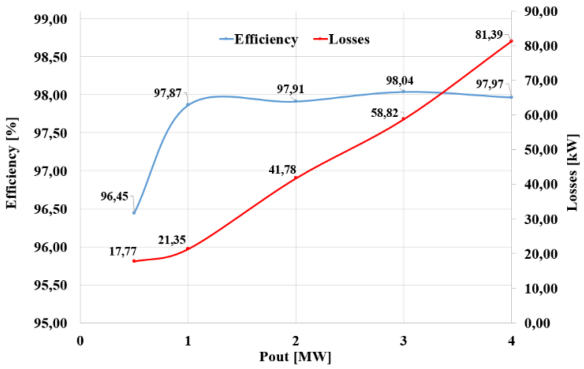

FIGURE 24. Estimated power efficiency and losses as a function of the power.

losses distributions as a function of the output power. It can be seen from Fig. 24 that the efficiency is above 97.5% in the power range between 1 and 4 MW.

VIII. CONCLUSION

A three-phase multi-level multiplexed converter for medium voltage has been discussed in this paper. The 3Φ7L M_LM_XC topology, modulation strategy, and operating principle have been explained. The modulation strategy has been implemented in Matlab/Simulink environment to verify the proposed analysis. Experimental waveforms obtained using the high-fidelity Hardware-In-the-Loop real-time emulator have been illustrated to prove the correct operation and performance of the proposed topology. The achieved results show the excellent quality of the converter's output waveforms even in the case of low switching frequency.

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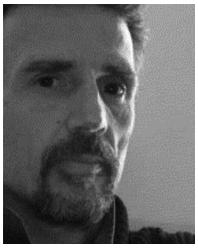

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