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Parasitic Component Inclusive Optimum Phase-Frequency Contour Enabled Synchronous Rectification of Asymmetric CLLC Resonant Converter

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ABSTRACT With an objective to reduce the switching losses in a bidirectional resonant CLLC DC/DC converter for electric vehicle (EV) charging applications, this paper presents an elaborate frequency dependent general harmonic approximation (GHA) based secondary side turnoff current minimization technique by investigating the optimum operating point to achieve synchronous rectification (SR). Formulation of an accurate all-inclusive gain model is presented, specifically focusing on effect of parasitic components on the resultant gain-frequency trend, backed with thorough experimental validation. Further, meticulous modeling of the GHA based state equations is presented to obtain a contour of feasible operational frequencies and corresponding phase shifts to ascertain accurate SR operation with a multi-dimensional optimization technique to ensure reduced switching losses. In addition to that, to precisely characterize the resonant tank equivalent circuit, stressing on its effect on SR phase calculation, a detailed 3D finite element analysis (FEA) based R-L-C modelling of the employed high frequency planar transformer (HFPT) is explained. To validate and benchmark the performance of the proposed gain model while ensuring accurate SR operation, a 1 kW all-GaN based CLLC experimental prototype is developed for a resonant frequency of 500 kHz, with a power density of 106 W/inch^3. Experimental waveforms at corner conditions are presented for a wide-gain bidirectional operation, portraying a peak converter efficiency of 98.49%.

INDEX TERMS EV charging, resonant converters, synchronous rectification, switching losses.

I. INTRODUCTION

Resonant CLLC DC/DC converters have found widespread acceptance in the field of EV onboard and wireless charging [1], more-electric-aircrafts (MEA), and naval power supplies due to their well research merits like high efficiency, wide voltage gain range, bidirectional power flow capability and zero voltage switching (ZVS) for the primary side bridge [2], [3]. Additionally, with an aim to achieve superior power density for such converters, various research works have been published that aim at increasing the operational frequency of the converters, thus enabling reduction in size for magnetic components [4]. However, increasing the frequency inherently leads to increased AC losses in the transformer windings and higher switching losses leading to significant degradation in the converter efficiency. In that context, facilitating soft switching for the secondary side by enabling SR [5] is a necessity for efficient power conversion.

Several studies have been published in the literature that have implemented various techniques to correctly realize SR. A summarized comparison is presented in Table 1 that qualitatively compares the most leading state-of-the-art works by elaborating on various metrics of performance and implementation. The method explained in [6] senses the voltage across the body diodes of the switches, based on the reverse current

TABLE 1. Merit Review of Different State-of-the-art Works on SR Implementation

Criteria	[6]	[7]	[8]	[9]	[10]	[11]	[12]	[13]	[14]	[15]	[16]	Proposed Method
Method	Voltage Detection	Current Detection		Time Domain Modeling				FHA			EHA	GHA based optimization
Accuracy of Estimation	◇◇◇	◇◇◇◇	◇◇◇	◇◇◇◇	◇◇◇◇	◇◇◇	◇◇◇◇	◇◇	◇	◇	◇◇◇◇	◇◇◇◇◇
Computational Workload	◇◇	◇◇◇	◇	◇◇	◇◇◇◇	◇◇◇◇	◇◇◇	◇	◇	◇	◇◇	◇◇◇
Difficulty in Realization	◇◇◇	◇◇	◇◇◇	◇◇◇◇	◇◇◇◇	◇◇◇	◇◇◇	◇◇	◇	◇◇	◇◇	◇◇
Sensor Requirement	Yes	No (indirect)	Yes	Yes	Yes	No	Yes	No	No	No	No	No
Peak Efficiency	96.20%	~97.2%	98.30%	~91%	97.05%	N/A	97.60%	~96.8%	~95.5%	97.50%	97.24%	98.49%

flow, to detect the turn-on instant. The study mentioned in [7] is based on resonant inductor voltage sensing which is used to formulate the instantaneous current flowing through it, which is used to actively detect the turn-on instants corresponding to current zero-crossings. Zhuoran et al. in their study [8] utilize a Rogowski coil and a zero-crossing detector (ZCD) to synthesize the switching instants. However, all the above-mentioned methods utilize an extra voltage/current sensor to realize SR, which increases the overall cost and losses in the circuit. Further, in these cases, accuracy of SR highly depends on the sampling frequency of the sensor, which limits their use for high frequency application. In addition, intermediate failure in the auxiliary sensing circuit might adversely affect the power stage due to damage caused due to inaccurate phase tracking.

The studies presented in [9], [10], [11], [12], [13] provide an elaborated time-domain model highlighting the switching instants and formulating detailed system equations, to analytically calculate the required phase for enabling SR. These methods portray superior tracking accuracy, which is sufficiently backed by detailed sensitivity analysis corresponding to change in system parameters. However, these methods include relatively complex mathematical synthesis and solving complicated differential equations for each switching instants with several small signal approximations, limiting its widespread acceptance. In addition to that, these methods do not account for the stray components appearing in the resonant tank, thus rendering the work deficient.

Addressing the limitations of time domain models, the works in [13], [14], [15] utilize frequency dependent first harmonic approximation (FHA) model to synthesize the state equations and corresponding obtain the required phase to enable SR. However, FHA ignores the effect of higher order harmonics in formulating the system equations, thus limiting the accuracy of presented analysis. Further, inaccurate phase tracking based on FHA results in a degraded efficiency due to higher mismatch between the secondary current zero-crossings, leading to higher switching losses. To address the limitations of FHA, the study presented in [16] utilizes an extended harmonic approximation (EHA) strategy to synthesize the phase shift for ensuring minimal switching losses. In addition, detailed sensitivity analysis is also presented which highlights the accuracy of the proposed method for significant changes in resonant tank parameters. However, this method, like all the previously referred works, does not account for the stray components: (a) winding resistance and (b) inter and intra-winding capacitance of the HFPT, leading to inaccuracy in terms of frequency modulation to achieve a particular gain, which significantly affects the resultant phase tracking accuracy.

Addressing the aforementioned limitations pertaining to the state-of-the-art methods of enabling SR, the key contributions of this paper are as follows: (a) Intricately curated all-inclusive GHA based modeling of CLLC converter with asymmetric tank accounting for stray parameters and their effect on the resultant gain trend, highlighting the experimental accuracy of the presented analysis, (b) A non-approximated frequency domain model-derived formulation of required phase shift enabling SR, accounting for the stray parameters and corresponding minimization of turnoff current based on multi-dimensional optimization approach, and (c) Precise parameterization of frequency dependent winding losses in conjunction with thorough analytical characterization of leakage inductance, winding resistance and stray capacitances based on 3D FEA for multiple winding configurations of HFPT.

The rest of the paper is structured as follows: Section II presents the GHA based model of CLLC topology with detailed analysis on the gain derivation accounting for the stray components of the resonant tank. A comprehensive analysis turnoff current minimization approach enabling SR for the secondary side switches is presented in Section III. Section IV characterizes the tank parameters emphasizing the analytical modelling of stray parameters. Further, Section V provides various experimental analysis at different operating conditions to validate the presented analysis. Finally, Section VI points out some conclusive points with relevant discussions.

II. FREQUENCY DOMAIN GHA BASED EQUIVALENT CIRCUIT SYNTHESIS AND MODELING FOR ASYMMETRIC CLLC

Fig. 1 shows the bidirectional CLLC DC/DC converter topology operating at a resonant frequency $f_r = \frac{1}{2\pi\sqrt{L_pC_p}} = \frac{1}{2\pi\sqrt{L_sC_s}}$, where C_p and C_s denote the resonant capacitors for the primary and secondary side, respectively and L_p and L_s denote the resonant inductors obtained as integrated leakages

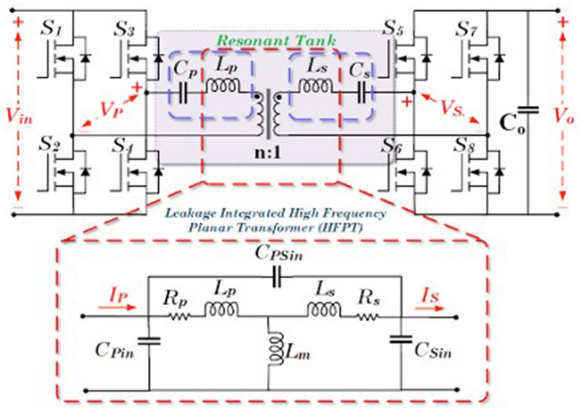

FIGURE 1. CLLC topology with zoomed in comprehensive HFPT circuit model.

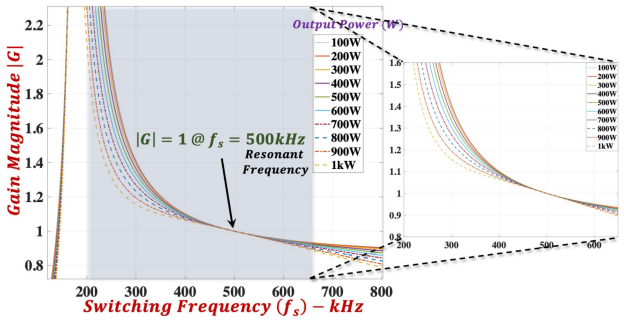

FIGURE 2. Voltage gain versus frequency trend of the designed CLLC converter.

from the HFPT designed with a turns ratio of $n:1$ and magnetizing inductance L_m.

Referring to the application of auxiliary charging systems corresponding to (400-600 V) to (24-28 V) conversion, a turns ratio (n) of 22:1 is selected based on the trade-offs between the core loss and winding loss, to adhere to the unity nominal gain requirement of the CLLC converter resulting in efficient voltage regulation [7], [9], [17], [18]. Fig. 2 shows the FHA based voltage gain magnitude versus the switching frequency (f_s) trend of the designed CLLC converter for the design specifications mentioned in Table 5. As observed, for a design gain range from G = 0.88 (for 600V − 24V conversion) to G = 1.54 (for 400V − 28V conversion) corresponding to the corner operating conditions, with the selected turns ratio and resonant tank parameter selection, the gain modulation is seamlessly achieved by varying the operational frequency between 200 kHz and 650 kHz.

Please note the tank is considered asymmetric (i.e., $L_p \neq n^2L_s$, $C_p \neq n^2C_s$) to bring in more design flexibility in terms of supporting wider gain range for both forward and reverse power flow. Also, it is practically difficult to ensure that the designer would be able to fabricate a leakage inductance of $L_s = L_p/n^2$, which is in the range of ∼100nH for the high step-down transformer under this study. The advantage of having asymmetric tank structure in CLLC converter is extensively discussed in [18], [19], [20]. As discussed in the

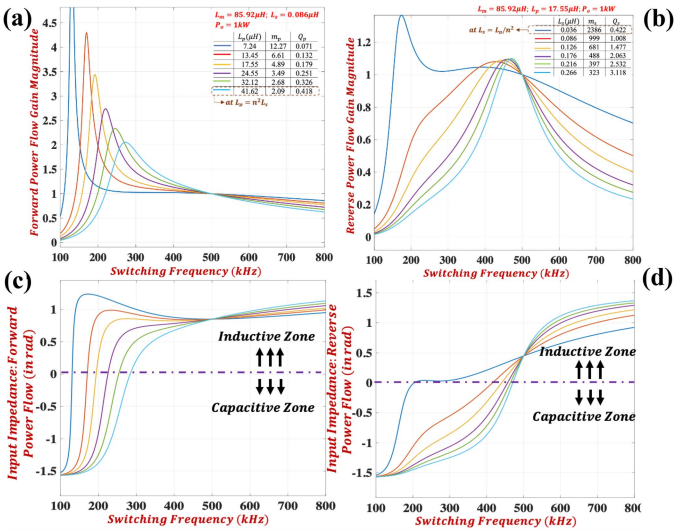

FIGURE 3. Gain and Input Impedance graphs (a)–(b): Forward and Reverse Power Flow Gain Magnitude versus switching frequency trend; (c)–(d) Input Impedance for Forward and Reverse Power Flow for varying m_p, m_s, Q_p, Q_s.

referenced works, due to asymmetric nature of L_p and L_s, the quality factors (Q_P and Q_S) (as shown in (1)) and corresponding resonant inductance ratios (m_P and m_S) (as shown in (2)) are different for forward and reverse power flows. Further, as observed in [21], [22], the values of Q and m play a crucial role in deciding the profile of the gain curve.

$$Q_P = \frac{\sqrt{\frac{L_p}{C_p}}}{n^2 R_{seq}};\ Q_S = \frac{n^2\sqrt{\frac{L_p}{C_p}}}{R_{peq}} \tag{1}$$

$$m_P = \frac{L_p}{L_m};\ m_S = \frac{L_s}{L_m} \tag{2}$$

$$R_{peq} = \frac{8V_{in}^2}{\pi^2 P_{in}};\ R_{seq} = \frac{8V_o^2}{\pi^2 P_o} \tag{3}$$

To illustrate the variation of gain trends with respect to different values of Q and m factors, Fig. 3(a)–(b) portray the FHA based gain versus frequency obtained by varying L_p and L_s, while Fig. 3(c)–(d) portray the input impedances perceived for forward and reverse power flow respectively. Further, as observed, the variations in the leakage inductances affect the maximum achievable gain, the frequency range for the gain requirement, and the gain gradient (dG/df) for a particular loading condition for forward and reverse power flow. Based on this trend, an iterative design analysis is carried out to comprehend the aspects pertaining to the frequency modulation range for accurate voltage regulation (adhering to the least count precision of the microcontroller) [23], loss budget for understanding the switching/conduction losses at different operational frequencies (based on the RMS values of tank currents) and ensuring inductive operative zone for ZVS (decided by the selection of L_m) [24]. Following this analysis, the specifications as mentioned in Table 5 were selected for ensuring superior efficiency and desired voltage regulation

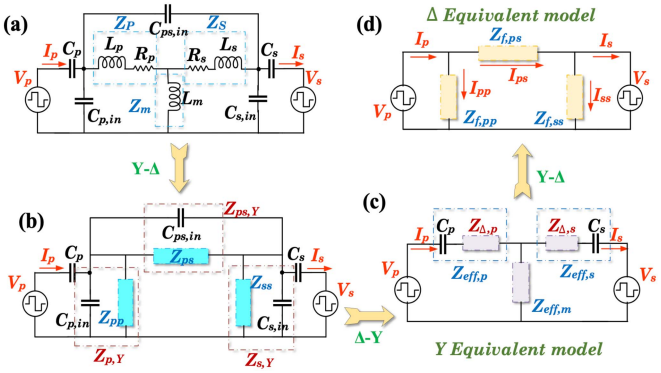

FIGURE 4. Reconfiguration of CLLC equivalent circuit accounting for stray components,.

for both forward and reverse power flow by implementing asymmetric tank structure.

Further, to provide intricately curated realistic model highlighting the stray components, a comprehensive HFPT circuit representation is highlighted in Fig. 1 and thoroughly explained in Section IV. As observed, R_p and R_s signify the effective winding resistances of the HFPT employed. Further, $C_{p,in}$ and $C_{s,in}$ denote the intra-winding capacitances of the primary and secondary windings of HFPT, while $C_{ps,in}$ signifies the inter-winding capacitance between the two windings.

To account for the influence of the above-mentioned stray components on the system performance, the equivalent tank structure shown in Fig. 1 is remodeled using a series of star (Y)-delta (Δ) conversions to obtain the effective impedance parameters in equivalent Y and Δ models, as shown in Fig. 4.

$$Z_p = R_p + j\omega L_p;\ Z_s = n^2\left[R_s + j\omega L_s\right];\ Z_m = j\omega L_m \tag{4}$$

$$\left.\begin{aligned} Z_{pp} &= Z_p + Z_m + \frac{Z_p Z_m}{Z_s} \\ Z_{ps} &= Z_p + Z_s + \frac{Z_p Z_s}{Z_m} \\ Z_{ss} &= Z_s + Z_m + \frac{Z_s Z_m}{Z_p} \end{aligned}\right\} \tag{5}$$

$$\left.\begin{aligned} Z_{p,Y} &= X_{C_{p,in}} || Z_{pp} \\ Z_{ps,Y} &= X_{C_{ps,in}} || Z_{ps} \\ Z_{s,Y} &= X_{C_{s,in}} || Z_{ss} \end{aligned}\right\} \tag{6}$$

$$\left.\begin{aligned} Z_{\Delta,p} &= \frac{Z_{p,Y} Z_{ps,Y}}{Z_{p,Y}+Z_{ps,Y}+Z_{s,Y}} \\ Z_{\Delta,s} &= \frac{Z_{s,Y} Z_{ps,Y}}{Z_{p,Y}+Z_{ps,Y}+Z_{s,Y}} \end{aligned}\right\} \tag{7}$$

$$\left.\begin{aligned} Z_{eff,m} &= \frac{Z_{p,Y} Z_{s,Y}}{Z_{p,Y}+Z_{ps,Y}+Z_{s,Y}} \\ Z_{eff,p} &= Z_{\Delta,p} + X_{C_p} \\ Z_{eff,s} &= Z_{\Delta,s} + X_{C_s} \end{aligned}\right\} \tag{8}$$

$$\left.\begin{aligned} Z_{f,pp} &= Z_{eff,p} + Z_{eff,m} + \frac{Z_{eff,p} Z_{eff,m}}{Z_{eff,s}} \\ Z_{f,ps} &= Z_{eff,p} + Z_{eff,s} + \frac{Z_{eff,p} Z_{eff,s}}{Z_{eff,m}} \\ Z_{f,ss} &= Z_{eff,s} + Z_{eff,m} + \frac{Z_{eff,s} Z_{eff,m}}{Z_{eff,p}} \end{aligned}\right\} \tag{9}$$

To formulate an all-inclusive GHA based gain equation, a detailed multi-harmonic AC equivalent impedance model

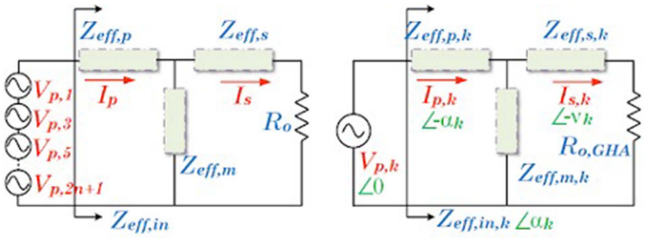

FIGURE 5. GHA equivalent model for CLLC converter for forward power flow.

based on the equivalent tank model is shown in Fig. 5. The resonant tank is excited by a square-wave voltage of magnitude corresponding to the DC input that can be decomposed into a series of multiple sinusoidal voltage sources that essentially accounts for the fundamental and higher order harmonics. Considering G2V operation, for finding the gain equation considering the inclusion of higher order harmonics and the parasitic components, with a constant input voltage source V_{in}, the reactive power flow in the system is assumed to be negligible. This assumption is realized as the tank parameters (mentioned in Table 5) are designed in a way that the superimposed phase lag between V_S and I_S (obtained as a GHA based superposition of phase lags between fundamental and higher order harmonic components) at operating conditions corresponding to $f_s > f_r$ and $f_s < f_r$ is restricted within $\pm 2.5°$ at all the corner conditions, which results in the amount of reactive power to be under 4.3% of the total apparent power. Thus, the secondary side can be modelled as a load with equivalent resistance $R_{o,GHA}$ [16], as shown below:

$$R_{o,GHA} = \frac{8n^2 R_o}{\pi^2} \sum_{k=13,5,\ldots}^{2m+1} \frac{1}{k^2} \tag{10}$$

As observed in Fig. 5, GHA enables the designer to analyze the effect of each harmonic component on the resultant gain by individually formulating the system equations for each component and superposing them to synthesize the equivalent gain. In that context, the input voltage ($V_p(t)$) and corresponding input current ($I_p(t)$) to the resonant tank can be written as summation of 'k' harmonic components as shown below:

$$V_p(t) = \sum_{k=13,5\ldots}^{2m+1} V_{p,k} \frac{\sin(k\omega_s t)}{k} = \frac{4V_{in}}{\pi} \sum_{k=13,5\ldots}^{2m+1} \frac{\sin(k\omega_s t)}{k} \tag{11}$$

$$I_p(t) = \sum_{k=13,5\ldots}^{2n+1} V_{p,k} \frac{\sin(k\omega_s t - \alpha_k)}{k} \frac{1}{\left|Z_{eff,in,k}\right|} \tag{12}$$

where, $Z_{eff,in,k} = Z_{eff,p,k} + Z_{eff,m,k} || (Z_{eff,s,k} + R_{o,GHA})$ denotes the input impedances and $\alpha_k = \angle Z_{eff,in,k}$.

Referring to (11)–(12), the cumulative power input accounting for the series connected voltage sources signifying

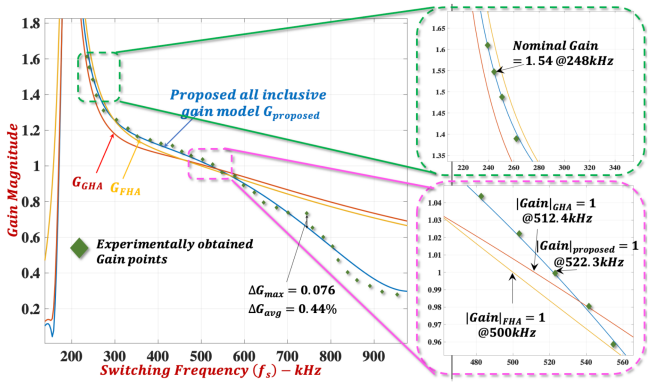

FIGURE 6. Gain comparison of FHA, GHA [16], and presented gain model, with experimental obtained gain versus frequency trend.

summation of k harmonic components can be written as:

$$P_{in} = \frac{1}{2} \sum_{k=\ 13,5...}^{2m+1} V_{p,k} I_{p,k} \cos(\alpha_k) \tag{13}$$

Further, substituting (11)–(12) in (13), the input power is formulated as shown below:

$$P_{in} = \frac{1}{2} \sum_{k=\ 13,5...}^{2m+1} \frac{V_{p,k}^2}{|Z_{eff,in,k}|} \cos(\alpha_k) \tag{14}$$

$$= \frac{8V_{in}^2}{\pi^2} \sum_{k=13,5,...}^{2m+1} \frac{1}{k^2} \frac{1}{|Z_{eff,in,k}|} \cos(\alpha_k) \tag{15}$$

The GHA based gain ($|G|\angle\varphi_g$) accounting for all the stray components is derived by equating (15) to $\frac{V_o^2}{R}$, invoking the power balance condition as shown below:

$$|G| = \frac{nV_o}{V_{in}} = \frac{2\sqrt{2}}{\pi} n \sqrt{R_o \sum_{k=13,5,...}^{2m+1} \frac{1}{k^2} \frac{1}{|Z_{eff,in,k}|} \cos(\alpha_k)} \tag{16}$$

where, φ_g is the gain angle which is obtained by finding the angle of equivalent impedance networks used to obtain the gain magnitude (nV_o/V_{in}).

Fig. 6 elucidates the gain versus frequency curves for first harmonic approximation (FHA), GHA [16], and the proposed gain model as shown in (16) with the experimentally obtained gain modulation trend for the design specifications mentioned in Table 5. As observed, due to intricately curated gain characteristics accounting for all the stray components in the asymmetric CLLC under study, the presented gain model follows the experimentally obtained gain model with an average mismatch of 0.44%, thus validating the exactitude of presented analysis.

In addition to that, it is worthwhile to note that the accuracy of the proposed all-inclusive gain model depends on the amount of harmonics considered while formulating the analytical model. To understand this dependency, Table 2 elucidates the effect of increasing number of harmonic components included in the analytical model of the proposed method and correspondingly compares the resultant error between the analytical and experimental gain points for four cases.

TABLE 2. Accuracy Comparison for Increasing Order of Harmonics Included in the Proposed Model

Case	Switching Frequency	Order of Harmonics Considered	Resultant Gain		% Mismatch
			Analytical	Experimental	
(a)	248 kHz	1	1.4467	1.541	9.43%
		5	1.4896		3.33%
		13	1.4922		3.16%
		21	1.5215		1.26%
		31	1.5402		0.052%
(b)	373 kHz	1	1.0935	1.121	2.45%
		5	1.1032		1.58%
		13	1.1063		1.31%
		21	1.1117		0.83%
		31	1.1201		0.081%
(c)	500 kHz	1	1.0051	1.024	1.84%
		5	1.0112		1.25%
		13	1.0196		0.43%
		21	1.0215		0.24%
		31	1.0230		0.094%
(d)	624 kHz	1	0.9126	0.864	-5.62%
		5	0.9014		-4.32%
		13	0.8911		-3.13%
		21	0.8725		-0.98%
		31	0.8636		0.046%

As observed in Table 2, with a defined mismatch threshold of <0.1% between the analytically formulated and experimental gain values, the order of harmonics considered in the proposed model is limited to $k = 31$. Further, to prove the accuracy of the proposed all-inclusive gain model, zoomed in snapshots of two instances of the gain plot comparison are presented in Fig. 6. As observed, implementing FHA based modeling, the unity gain point appears at operational switching frequency equal to the resonant frequency (500 kHz). However, when verified experimentally, the unity gain point shifts to 522.3 kHz, which matches the response portrayed by the proposed all-inclusive gain model. This occurs to due to the effect of parasitic components and higher order harmonics present in the system, which is encompassed by the proposed all-inclusive GHA based gain model. In addition to that, the nominal gain point ($|G|$=1.54) occurs at 248 kHz switching frequency, which also coincides with the plot elucidated by the proposed gain model. The above two instances indicate that the inclusion of parasitic components in the gain

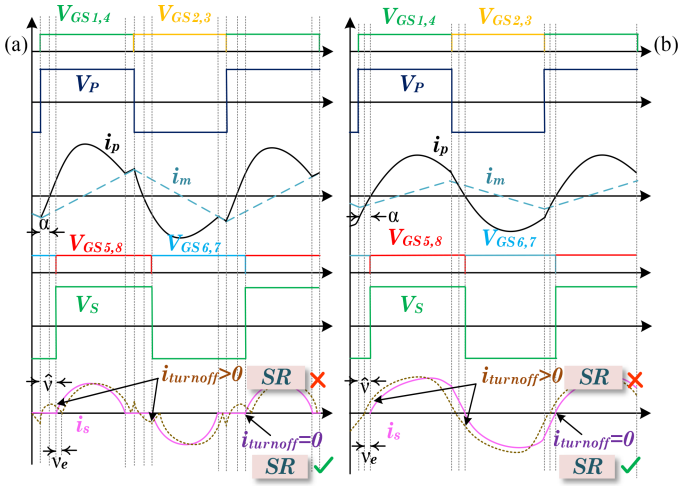

FIGURE 7. Waveform comparison for (a) $f_s < f_r$ and (b) $f_s > f_r$.

modeling plays a crucial role to obtain accurate output voltage regulation.

III. OPTIMUM PHASE-FREQUENCY CONTOUR-ENABLED SR BASED TURNOFF CURRENT MINIMIZATION

With an objective to reduce the on-state conduction losses in conventional diode based secondary side bridge, the use of active switches operating with phase shift (ϑ) with respect to the primary side gate pulses facilitates accurate phase tracking with the switch voltage, resulting in reduced turn-off losses. Further, precise estimation of the mentioned phase shift is quintessential for enabling SR; the failure to do so results in significant turnoff losses, which is directly proportional to the error in phase tracking (ϑ_e). Fig. 7 elaborates on this phenomenon by depicting the inaccurate phase tracking for two cases: (a) $f_s < f_r$ and (b) $f_s > f_r$ and compares it with an accurately estimated SR operation.

As observed, due to inaccurate phase shift provided to switch S_5 (represented by dotted lines), the current at turnoff instant is not zero, leading to additional switching losses as seen in (17)–(18).

$$i_{turnoff} = |I_s| \sin \vartheta_e \tag{17}$$

$$P_{turnoff} = 2 \cdot \frac{1}{2} V_o i_{turnoff} f_s t_{off} = V_o |I_s| f_s t_{off} \sin \vartheta_e \tag{18}$$

For cases including operation at $f_s < f_r$ or $f_s > f_r$, a gain angle (φ_g) between V_P and V_S will exist, which needs to be factored in for maintaining the resultant gain for SR operation. In that context, a combination of $\{f_s, \vartheta\}$ operating points corresponding to the desired gain and connected load will be required to ensure the required phase shift between the primary (V_P) and secondary (V_S) bridge voltages. In order to synthesize the required phase shift ($\hat{\vartheta}$) to alleviate the turnoff losses through SR, a detailed analysis elaborating on the system equations incorporating the effect of stray parameters is presented in this section. Referring to the Δ equivalent model as shown in Fig. 4(d), the secondary voltage can also be synthesized as a combination of 'k' voltage sources, each corresponding to the harmonic content of the quasi-square waveshape, as shown below:

$$V_s(t) = \sum_{k=\,13,5\ldots}^{2m+1} V_{s,k} \frac{\sin k(\omega_s t - \varphi_g)}{k} = \frac{4nV_o}{\pi} \sum_{k=\,13,5\ldots}^{2m+1} \frac{\sin k(\omega_s t - \varphi_g)}{k} \tag{19}$$

where, φ_g is the gain angle that essentially represents the phase difference between primary and secondary bridge voltages at a particular loading condition.

Utilizing (11) and (19), the current equations in the system can be formulated as follows:

$$i_{pp}(t) = \frac{4V_{in}}{\pi} \sum_{k=\,13,5\ldots}^{2m+1} \frac{\sin\left(k\omega_s t - \angle Z_{f,pp,k}\right)}{k} \frac{1}{|Z_{f,pp,k}|} \tag{20}$$

$$i_{ss}(t) = \frac{4nV_o}{\pi} \sum_{k=13,5\ldots}^{2m+1} \frac{\sin\left(k(\omega_s t - \varphi_g) - \angle Z_{f,ss,k}\right)}{k} \frac{1}{|Z_{f,ss,k}|} \tag{21}$$

$$i_{ps}(t) = \frac{4V_{in}}{\pi} \sum_{k=\,13,5\ldots}^{2m+1} \frac{\sin\left(k\omega_s t - \angle Z_{f,ps,k}\right)}{k} \frac{1}{|Z_{f,ps,k}|} - \frac{4nV_o}{\pi} \sum_{k=13,5\ldots}^{2m+1} \frac{\sin(k(\omega_s t - \varphi_g) - \angle Z_{f,ps,k})}{k} \frac{1}{|Z_{f,ps,k}|} \tag{22}$$

Referring to Fig. 4(c), the secondary bridge current $i_s(t)$ can be synthesized (as shown in (24)) as a sinusoidal waveform having a zero crossing at $\omega_s t = \vartheta$, where ϑ accounts for the effect of additional phase shift required.

$$i_s(t) = i_{ps}(t) - i_{ss}(t) \tag{23}$$

$$i_s(t) = \frac{4nV_o}{\pi} \sum_{k=\,13,5\ldots}^{2m+1} (A_k - B_k) \sin(k\omega_s t - \vartheta_k) \tag{24}$$

where, $\vartheta_k = \delta_k - \angle Z_{f,ps,k}$, $\delta_k = \tan^{-1} \frac{G\cos\beta}{1 - G\sin\beta}$, $\beta_k = \frac{\pi}{2} - k\varphi_g$, $A_k = \frac{\sqrt{1+G^2-2G\sin\beta_k}}{k|Z_{f,ps,k}|}$ and $B_k = \frac{1}{k|Z_{f,ss,k}|}$.

The analytical model developed for $i_s(t)$ provides a generic correlation of operating points (V_{in}, V_o, P_o) and is valid for any given set of phase and operational frequency set, where its practical amplitude limit is decided by the load power level. Fig. 8 portrays a phasor diagram elucidating the above-mentioned phase relationships between the port voltages and current for 'kth' harmonic component.

Please refer to the terms A_k and δ_k in (24), which have implicit dependence on the voltage gain magnitude (G) and gain angle (φ_g), so the SR accomplishment i.e., the solution of $i_s(t) = 0$ inherently incorporates the voltage gain constraint. Additionally, the function of i_s includes the effects of the operating frequency (ω_s) and SR enabling phase shift (ϑ_k).

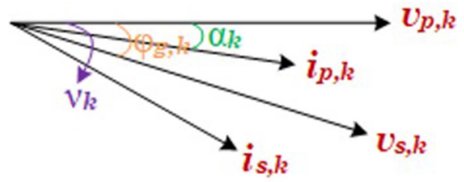

FIGURE 8. Phasor diagram explaining the phase relationship for kth harmonic component.

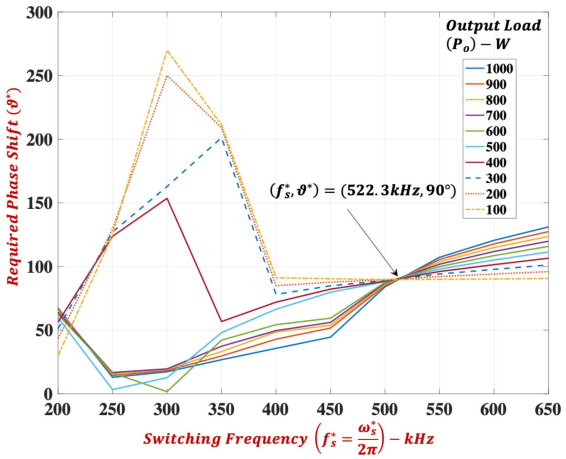

FIGURE 9. Plot of f_s^* versus ϑ^* for different loading conditions.

To obtain the required phase shift between the primary and secondary side gate pulses, the zero crossing of (24) is analyzed for one switching cycle ($t \in \{0, 2\pi\}$) by numerically solving the equation by substituting the values of $\{\omega_s, \vartheta\}$ in an iterative loop. For a defined nominal voltage gain, the solution of $i_{turnoff} \rightarrow F(i_s) = 0$ results in a contour of feasible solutions of $\{\omega_s^*, \vartheta^*\}$ corresponding to the rated load, all resulting in near-zero turnoff current. To elucidate this phenomenon, Fig. 9 shows the set of possible combinations of $\{f_s^* = \frac{\omega_s^*}{2\pi}, \vartheta^*\}$ plotted for different load powers.

A. NEWTON BASED TURNOFF CURRENT MINIMIZATION FOR OPEN LOOP OPERATION

To obtain the most optimum operating point resulting in minimum value of $i_{turnoff}$, an iterative multi-dimensional Newton method [25] using minimization approach with a residual error margin (ϵ) of 0.1%, as shown below:

$$\min i_{turnoff} \rightarrow \underset{\{\widehat{\omega_s}, \hat{\vartheta}\}}{solve} \; \boldsymbol{F}\left(i_s\{\boldsymbol{X}\}\right) = 0 \tag{25}$$

where, $\boldsymbol{X}$ denotes a matrix of all the feasible values of $\{\omega_s^*, \vartheta^*\}$ and $\boldsymbol{F}$ is the set of non-linear function depicting the values of i_s at the switching transition corresponding each possible value of $\{\omega_s^*, \vartheta^*\}$ for one switching cycle ($t \in \{0, 2\pi\}$),

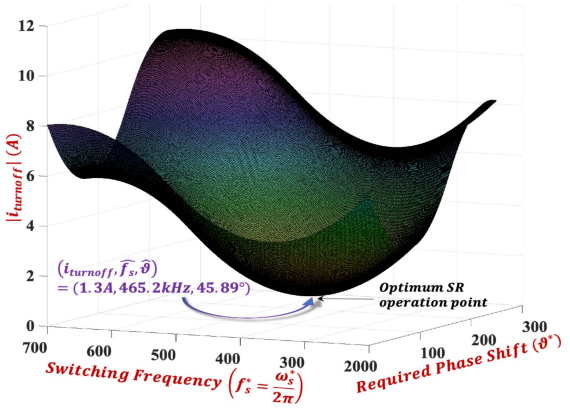

FIGURE 10. Plot of turnoff current cost function with respect to f_s^* and ϑ^* at 1 kW loading and output voltage – 28 V.

as shown below:

$$X = \begin{bmatrix} \{\omega_{s,1}^*, \vartheta_1^*\} \\ \{\omega_{s,2}^*, \vartheta_2^*\} \\ \vdots \\ \{\omega_{s,n}^*, \vartheta_n^*\} \end{bmatrix}; \boldsymbol{F}\left(i_s\{\boldsymbol{X}\}\right) = \begin{bmatrix} i_{s,1}\{\omega_{s,1}^*, \vartheta_1^*\} \\ i_{s,2}\{\omega_{s,2}^*, \vartheta_2^*\} \\ \vdots \\ i_{s,n}\{\omega_{s,n}^*, \vartheta_n^*\} \end{bmatrix} \tag{26}$$

Iteratively solving (25) for u iterations, the $(u+1)th$ solution set is formulated as shown below:

$$\boldsymbol{X}^{(u+1)} = \boldsymbol{X}^{(u)} - \boldsymbol{J}^{-1}(\boldsymbol{X}^{(u)})\boldsymbol{F}\left(i_s\{\boldsymbol{X}^{(u)}\}\right) \tag{27}$$

$$\boldsymbol{J}\left(\boldsymbol{X}^{(u)}\right) \boldsymbol{\epsilon}\left\{\boldsymbol{F}\left(i_s\{\boldsymbol{X}\}^{(u)}\right)\right\} = -\boldsymbol{F}\left(i_s\{\boldsymbol{X}^{(u)}\}\right) \tag{28}$$

where,

$$\boldsymbol{J}\left(\boldsymbol{X}^{(u)}\right) = \begin{bmatrix} \frac{\partial \boldsymbol{F}(i_{s,1})}{\partial \boldsymbol{X}_1} & \frac{\partial \boldsymbol{F}(i_{s,1})}{\partial \boldsymbol{X}_2} & \cdots & \frac{\partial \boldsymbol{F}(i_{s,1})}{\partial \boldsymbol{X}_n} \\ \frac{\partial \boldsymbol{F}(i_{s,2})}{\partial \boldsymbol{X}_1} & \frac{\partial \boldsymbol{F}(i_{s,2})}{\partial \boldsymbol{X}_2} & \cdots & \frac{\partial \boldsymbol{F}(i_{s,2})}{\partial \boldsymbol{X}_n} \\ \vdots & \vdots & \ddots & \vdots \\ \frac{\partial \boldsymbol{F}(i_{s,n})}{\partial \boldsymbol{X}_1} & \frac{\partial \boldsymbol{F}(i_{s,n})}{\partial \boldsymbol{X}_2} & \cdots & \frac{\partial \boldsymbol{F}(i_{s,n})}{\partial \boldsymbol{X}_n} \end{bmatrix} \tag{29}$$

$$\boldsymbol{\epsilon}\left\{\boldsymbol{F}\left(i_s\{\boldsymbol{X}\}^{(u)}\right)\right\} = \boldsymbol{F}(i_s\left\{\boldsymbol{X}^{(u+1)}\right\} - \boldsymbol{F}\left(i_s\{\boldsymbol{X}\}^{(u)}\right) \tag{30}$$

$\boldsymbol{J}(\boldsymbol{X}^{(u)})$ denotes the Jacobian matrix, while $\boldsymbol{\epsilon}\{\boldsymbol{F}(i_s\{\boldsymbol{X}\}^{(u)})\}$ represents the residual error of the *uth* iteration. Further, applying the constraint $\boldsymbol{\epsilon}\{\boldsymbol{F}(i_s\{\boldsymbol{X}\}^{(u)})\} < 0.1\%$, results in optimum set of solution $\rightarrow \{\widehat{\omega_s}, \hat{\vartheta}\}$. It is worthwhile to note that as the formulation of $i_s(t)$ (as seen in (24)) includes the influence of higher order harmonics due to adoption of GHA based approach and the effect of parasitic components in the resonant tank, the solution set ($\{f_s^* = \frac{\omega_s^*}{2\pi}, \vartheta^*\}$) obtained provides an accurate estimate of optimum operating points, resulting in significantly reduced turnoff losses.

Fig. 10 graphically shows the contour of the minimization function by plotting $\boldsymbol{F}(i_s\{\boldsymbol{X}\})$ with respect to varying values of $\{f_s^* = \frac{\omega_s^*}{2\pi}, \vartheta^*\}$, highlighting the optimum operating point for

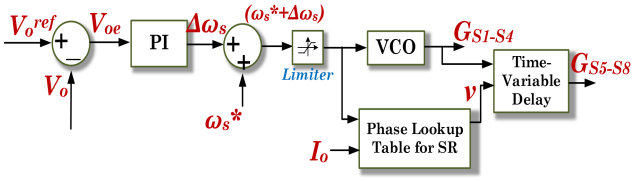

FIG. 11. Closed loop voltage regulation through PFM.

a rated load of $P_o = 1\,\text{kW}$ for a voltage conversion of 400-28 V. As observed, the global minima of the function lies at $\{i_{turnoff}, \hat{f}_s, \hat{\vartheta}\} = \{1.3\,A,\ 465.2\,\text{kHz},\ 45.89^\circ\}$ which ensures minimal switching losses due to implementation of SR. An additional constraint ($200\,\text{kHz} < \widehat{f_s} < 650\,\text{kHz}$) for forward power flow and ($430\,\text{kHz} < \widehat{f_s} < 650\text{kHz}$) for reverse power flow, corresponding to the selected design parameters, is enforced for limiting the solution of the minimization function to the frequency operating points adhering to the ZVS (i.e., inductive zone) occurrence, as obtained from the all-inclusive gain graph. Applying this constraint, if the solution set adheres to the ZVS range for the designed specifications, the result is deemed to be optimal.

B. SR ENABLED PULSE-FREQUENCY MODULATION (PFM) BASED CLOSED LOOP REGULATION

The closed loop regulation of the CLLC converter to achieve the voltage regulation and SR action is shown in Fig. 11. As observed, the sensed output voltage (V_o) is compared with its reference value (V_o^{ref}) to generate the error (V_{oe}), which is then processed in a PI controller to obtain the value of the frequency shift ($\Delta\omega_s$). The frequency perturbation is then added to ω_s^*, which portrays an initial estimate of the switching frequency (generally obtained from open loop gain plots), to obtain the required modulated frequency ($\omega_s^* + \Delta\omega_s$). A limiter is used to constrain the operational frequency ($200\,\text{kHz} < f_s^*(= \frac{\omega_s^*+\Delta\omega_s}{2\pi}) < 650\,\text{kHz}$) to stay in the limits based on the ZVS criteria, gain requirements and device stresses for forward power flow, while the limiter is set to $430\text{ kHz} < f_s^* < 650\text{ kHz}$ for reverse power flow. This is done by setting the time base period (TBPRD) register limits in the microcontroller employed. Further, a voltage-controller oscillator (VCO) is used to generate the gate pulses for the primary side switches ($S_1 - S_4$) corresponding to the modulated frequency signal. To enable SR for the secondary side switches ($S_5 - S_8$), an additional phase shift (ϑ) is added based on the look-up table (corresponding to Fig. 9) that encompasses the information pertaining to the connected load, realized using a time-variable delay block.

IV. PARAMETRIC R-L-C MODELING OF HFPT FOR ALL-INCLUSIVE GAIN MODEL ESTABLISHMENT

Following the comprehensive gain model highlighting the effect of stray components ($C_{p,in}$, $C_{s,in}$ and $C_{ps,in}$) in the resultant gain versus frequency trend presented in Section II and corelating its dependency on switching loss minimization using SR, it is hence noteworthy to study the effect of different

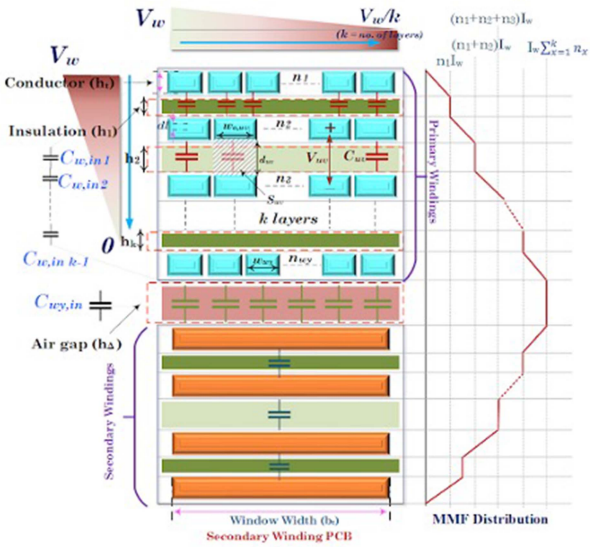

FIG. 12. Generic HFPT model to analyze the R-L-C parameters.

winding configurations based on the structural configuration of the windings. In addition to that, accurate characterization of effective winding resistance to yield minimum winding losses is also essential for ensuring high efficiency power conversion, specifically at higher operational frequencies. It is well established [26], [27] that interleaved winding configurations result in minimized winding losses due to relatively even current density distribution. However, interleaved configurations result in significantly lesser values of leakage inductances, thus rendering it infeasible for the mentioned leakage integrated CLLC converter design. Referring to the above-mentioned objectives, a detailed 3D FEA based R-L-C analytical modelling and quantification is presented in this section for non-interleaved winding configurations (see Fig. 12).

A. ANALYTICAL MODELLING FOR R-L-C SYNTHESIS

Complying to the objective of achieving higher power density, thus eliminating the external resonant inductors, adjustable air gaps between the core (h_w) and the windings (h_g) are provided to enable intentional flux leakage in a controlled manner. Corresponding to this leakage flux, the linked electromagnetic energy ($\in$) is used to analytically quantify the leakage inductance as shown as follows:

$$\in_w = \frac{\mu_o}{2} \sum \int_0^{h_t} H^2 l_w b_w dl = \frac{1}{2} L_w I_w^2\ ;\ w \in \{P, S\} \quad (31)$$

where, μ_o represents the permeability of the core, H denotes the field strength, which is formulated by the ampere turns linked, l_w is the length of each winding, b_w is the window width of the core and h_t is the thickness of the conductor. Further, dl is the incremental thickness situated at a distance of l from the inner surface of the conductor, as observed in

Fig. 12. Utilizing (31), the leakage inductance can be analytically formulated as:

$$\in_w = \frac{\mu_o}{2} l_w b_w \left[n \int_0^{h_t} \left(\frac{I_w l}{b_w h_w} \right)^2 dl + \left(\frac{n_1 I_w}{b_w} \right)^2 (h_t + h_1 + h_w) + \left(\frac{(n_1 + n_2) I_w}{b_w} \right)^2 (h_t + h_2 + h_w) + \left(\frac{(n_1 + n_2 + n_3) I_w}{b_w} \right)^2 (h_t + h_3 + h_w) + \ldots \text{for k layers} \ldots + \left(\frac{n I_w}{b_w} \right)^2 (h_t + h_w) \right] \quad (32)$$

$$L_w = \frac{2 \in_w}{I_w^2} \quad (33)$$

where, I_w represents the RMS value of primary/secondary winding current, $n_x; x \in \{12, 3..k\}$ denote the number of windings in each layer.

Further, to quantify the AC winding losses in the HFPT analytically, Dowell's equation [28] is employed, that formulates the ratio of AC resistance (R_{ac}) to the winding DC resistance (R_{dc}) for different winding configurations, as shown below:

$$\frac{R_{\text{ac}}}{R_{\text{dc}}} = \frac{\gamma}{2} \left[\frac{\sinh \gamma + \sin \gamma}{\cosh \gamma - \cos \gamma} + (2m - 1)^2 \frac{\sinh \gamma - \sin \gamma}{\cosh \gamma + \cos \gamma} \right] \quad (34)$$

$$m = \frac{MMF\,(k)}{MMF\,(k) - MMF\,(k-1)}; R_{\text{dc}} = \frac{\rho l_w}{h_w b_w} \quad (35)$$

where, *MMF(k)* denotes the magnetomotive force (MMF) of windings in layer k, ρ is the resistivity of the conductor and $\gamma = \frac{h_t}{\delta}$, where δ is the skin depth. As observed in Fig. 12, the MMF increases linearly proportional to the NI product of the winding layers, which results in higher $\frac{R_{\text{ac}}}{R_{\text{dc}}}$ for the inner PCB layers.

Fig. 12 also shows the voltage distribution of the primary winding which is assumed to vary linearly according to the turn distribution for each layer. Thus, the potential at each turn of the winding (V_u) can be formulated as:

$$V_u = \frac{(n+1) - u}{n} V_w; u \in \{12, 3 \ldots n\} \quad (36)$$

Referring to the voltage difference (V_{uv}) between two adjacent winding or windings in two adjacent layers, a virtual capacitor is created accounting for the overlapping surface area of the conductors and corresponding distance between them.

$$C_{uv} = \frac{\varepsilon_o \varepsilon_r S_{uv}}{d_{uv}}; S_{uv} = \int_0^{l_t} w_{o,uv} dl \quad (37)$$

Where, $\varepsilon_o$and ε_r denote the permittivity of air and relative permittivity of the dielectric material respectively, S_{uv} is the overlapping area between turns u and v as observed in Fig. 12 d_{uv} denotes the spacing between the two conductors, $w_{o,uv}$ is the overlapping conductor width and dl represents an infinitesimally small sectional length of a turn, which is integrated over the entire circumference to form a complete turn of length l_t. Thus, the inter ($C_{wy,in}$) and intra-winding ($C_{w,in}$) capacitance can be formulated as follows:

$$C_{w,in} = \sum_{x=12,3\ldots}^{k-1} C_{w_x} = \sum_{x=12,3\ldots}^{k-1} \varepsilon_o \varepsilon_r \int_0^{l_t} dl \sum_{y=1}^{q} \frac{w_{o_q}}{h_x} \quad (38)$$

$$C_{wy,in} = \varepsilon_o \varepsilon_r \frac{n_{wy} w_{wy}}{h_\Delta} \int_0^{l_t} dl \quad (39)$$

where, q denotes the number of conductor overlaps, n_{wy} is the number of windings in the last layer of primary winding and w_{wy} is the width of each winding.

B. 3D FEA MODELING, VERIFICATION, AND COMPARATIVE ANALYSIS

To verify the analytical formulations presented to characterize the HFPT parameters and to choose the most optimum winding configuration resulting in minimum winding losses, three winding configurations are compared in Table 2 for a 4-layer PCB for primary (connected in series) and secondary (connected in parallel) winding by solving the FEA model in ANSYS Maxwell electrostatic and eddy current solver. As observed in Table 3, winding configuration {7P-4P-4P-4P},{1S-1S-1S-1S} results in minimum value of winding resistances, while achieving the required leakage inductance required to satisfy the ZVS constraint, thus rendering it the most optimum winding configuration. (Please note the selected design specifications of HFPT are as follows: $h_w = 1.9$ mm, $h_g = 0.5$ mm, $h_t = 70\,\mu m$ (2oz. of Cu), $\{h_1, h_2, \ldots\}$ depending on standard 1.6 mm 4-layer PCB [21], $l_t = 90$ mm, $b_w = 20$ mm).

C. SENSITIVITY ANALYSIS OF THE HFPT COMPONENTS

As the HFPT parameters are prone to change in temperature, operating condition and layout, it is important to understand the effect of variation of the tank parameters with respect to change in resultant gain, optimum phase and operational frequency of the system. To elucidate this change, a sensitivity term (S_N^M) [29] is introduced, that is defined as the relative change in the parameter M with respect to relative variation in parameter N.

$$S_N^M = \frac{\frac{\text{dM}}{\text{M}}}{\frac{dN}{N}} \quad (40)$$

Further, Table 4 shows the analytically calculated sensitivity of resultant gain (G), the optimum phase shift $\hat{\vartheta}$ and the operating frequency ($\widehat{\omega_s}$) with respect to ±15% variation in the tank parameters. As observed in Table 4, the change in the resultant operating points (G, $\hat{\vartheta}$ and $\widehat{\omega_s}$) is relatively small for changes in the tank parameters. On the other hand, the sensitivity of stray capacitances is relatively larger that might lead to considerable changes in the optimum operating points. However, as observed in (38) and (39), the values

TABLE 3. Analytical and Simulation Findings For Winding Configurations Under Study

Winding Configuration	n	$L_p(\mu H)$		$L_S(nH)$		$C_{p,in}(nF)$		$C_{s,in}(nF)$		$C_{ps,in}(pF)$		$R_p(m\Omega)$		$R_s(m\Omega)$		P_{wind} (W)	P_{core} (W)	P_{total} (W)
		A	S	A	S	A	S	A	S	A	S	A	S	A	S			
{8P-3P-3P-8P}, {1S-1S-1S-1S}	22	27.2	26.7	85.3	85.2	0.51	0.58	0.66	0.7	23.1	23.9	102.6	91.7	0.82	0.81	7.16	5.2	11.36
{7P-4P-4P-4P}, {1S-1S-1S-1S}		17.8	17.1	87.5	87.5	0.55	0.61	0.66	0.67	23.7	24.5	82.5	87.2	0.82	0.79	4.41	5.2	8.61
{6P-5P-5P-6P}, {1S-1S-1S-1S}		10.6	11.0	87.9	87.4	0.55	0.59	0.66	0.68	24.5	25.5	91.2	92.8	0.82	0.79	6.52	5.2	10.72

TABLE 4. Sensitivity of Tank Parameters

Sensitivity	L_p	L_s	C_p	C_s	R_p	R_s	$C_{p,in}$	$C_{s,in}$	$C_{ps,in}$
S_x^G	$6.25\text{x}10^{-3}$	-0.1458	$5.2\text{x}10^{-2}$	0.117	-0.1513	-0.2114	0.0258	0.0161	-0.051
S_x^{ϑ}	1.4577	1.1683	0.5271	0.8915	0.5161	0.934	7.117	18.512	1.252
$S_x^{\bar{\omega}_s}$	-0.623	-0.0136	-0.887	-0.052	-1.273	-1.781	-12.152	-11.836	-2.527

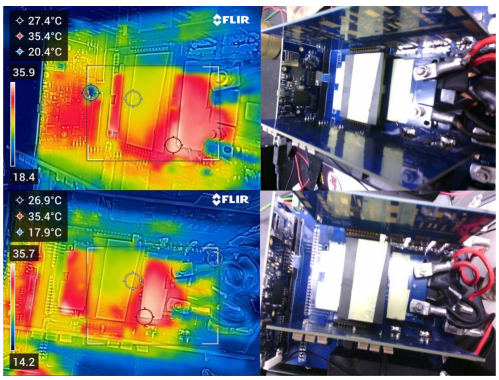

FIG. 13. Thermal image of the HFPT assembly during rated load operation.

of stray capacitance depend on the dielectric constant of the insulation used and the overlapping conductor thickness and relative distance between them. As the copper windings are fabricated in the PCB, their thickness and dimensions are relatively constant for any given operation status, temperature, or aging. Further, the dielectric coefficient of the FR4 material also remains constant with temperature (typical range of operation: $-20\,^{\circ}$C to to $170\,^{\circ}$C) as verified in [30], [31]. It is also ensured that the thickness of the windings of the HFPT are selected in such a way that at rated load condition, the temperature rise is limited to 40° adhering to IPC 2221 [32]. To validate the same, a thermal image depicting the winding temperature at the rated loading condition is shown in Fig. 13. Thus, the values of stray capacitances are relatively unfazed with change in temperature, aging or operation status, thus leading to minimal effect on the resultant gain, optimum SR phase shift and the operating frequency.

In addition to that, the value of magnetizing inductance (L_m) depends on the selected magnetic core which portrays non-linear relation in permeability with change in operational frequency [33]. In that context, the resultant value of L_m depends on the reluctance ($\Re$) offered by the core, and can be analytically formulated as:

$$\Re = \frac{1}{\mu_o A_e}\left[h_g + \frac{l_e}{\mu_r}\right] \tag{41}$$

$$L_m = \frac{n^2}{\Re} \tag{42}$$

where, A_e and l_e denote the effective area and length of the core respectively and μ_r is the relative permeability of the core. Please note that for the selected magnetic core (FR45810EC) with a specific value of h_g, μ_r varies non-linearly with the operational frequency (f_s), which for the CLLC resonant converter topology is modulated as per the loading conditions, due to its dependency with the resultant gain (G). Referring to the material properties of R-material [34], it was observed that the sensitivity of μ_r with respect to frequency variation for the required gain range at all loading conditions ($G \in [0.88 \text{ to } 1.54]$ for $f_s \in [200650]$ kHz) is $S_f^{\mu_r} = \frac{d\mu_r/\mu_r}{df_s/f_s} < 1.29\%$, leading to a sensitivity in resultant L_m with respect to μ_r to be $S_{\mu_r}^{L_m} = \frac{dL_m/L_m}{d\mu_r/\mu_r} < 1.62\%$. Utilizing this dependency, the gain trend for selected specifications experiences a variation of $<1.85\%$, which validates the core selection and its variation with a negligible effect on the output voltage regulation and corresponding SR action.

V. EXPERIMENTAL VERIFICATION AND BENCHMARKING

To validate the findings and analysis presented in the previous sections, an experimental prototype (as shown in Fig. 14) is developed for the specifications corresponding to auxiliary charging systems for ground military vehicles [35], [36] as mentioned in Table 5, and detailed analysis elucidating results obtained for both light and heavy loading conditions are presented. This prototype is developed with a targeted application of bidirectional EV charging, where the high voltage side corresponds to a DC link voltage of 400 V-600 V nominal, while the low voltage side corresponds to a battery at 28 V nominal with a depletion threshold of 24 V [37], [38]. In addition to that, following similar investigation pertaining to the gain

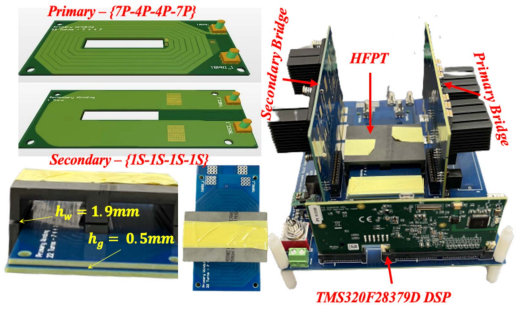

FIG. 14. Experimental proof-of-concept for developed CLLC converter.

TABLE 5. Design Specifications For Bidirectional CLLC

Parameters	Values
Primary input voltage (V_{in})	400-600V
Secondary output voltage range (V_o)	24-28V
Rated Power (P_o)	1kW
Transformer Turns Ratio (n)	22:1
Tank Leakage Inductances (L_p,L_s)	17.55μH, 0.086μH
Magnetizing Inductance (L_m)	85.92μH
Tank Capacitors (C_p,C_s)	5.77nF, 1.173μF
Resonant frequency (f_r)	500 kHz

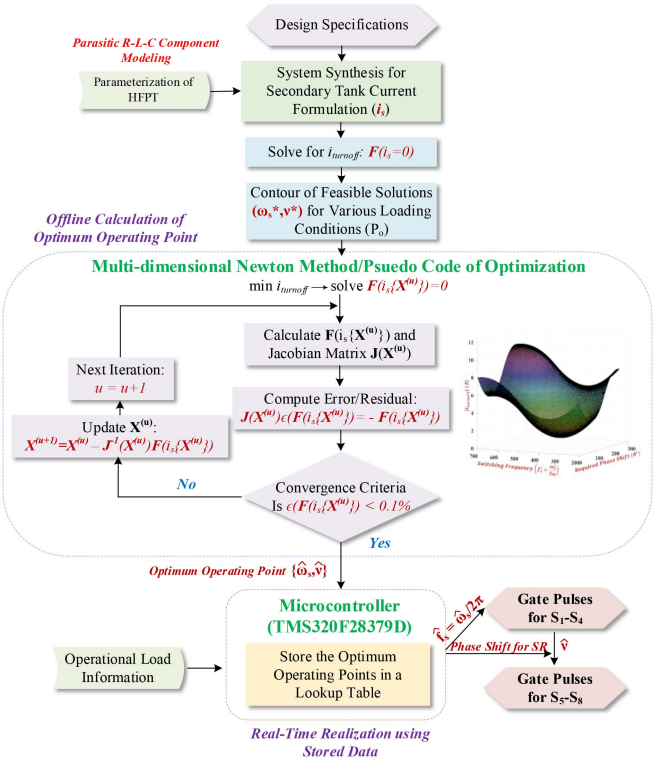

FIG. 15. Implementation of the proposed algorithm for turnoff current minimization.

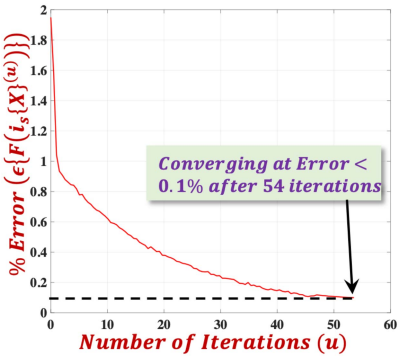

FIG. 16. Function convergence plot with respect to number of iterations.

and phase shift requirement, experimental results of reverse power flow are also presented accounting for the switching loss minimization objective. The required gate pulses with a phase shift enabling SR are provided using TMS320F28379D dual-core digital signal processor. The primary side bridge is realized using Transphorm TP90H050WS (900 V, 22 A, 63 $m\Omega$) cascode GaN-FETs, while the secondary side consists of four EPC2020 (60 V, 90 A, 2.2 $m\Omega$) switches connected in parallel, thus enabling an all-GaN power converter solution, ensuring a superior power density of 106 W/inch^3. Following the analysis presented in Section IV, an accurately modelled HFPT is fabricated using {7P-4P-4P-7P, 1S-1S-1S-1S} winding configuration, thus facilitating reduced winding losses and achieving required integrated leakage inductance. Magnetic planar EE core FR45810 from Mag Inc. is used to realize the HFPT, that results in a core loss of 4.2 W for an operational frequency of 500 kHz.

A comprehensive flowchart to elucidate the optimization approach and its implementation is presented in Fig. 15. As observed, with the knowledge of the design specifications and HFPT parasitic components, an offline calculation of optimum operating points is executed using multi-dimensional Newton optimization method. With respect to the cost function (min $i_{turnoff}$) defined, the function $F(i_s\{X^{(u)}\})$ is solved iteratively and corresponding error $\epsilon\{F(i_s\{X\}^{(u)})\}$ is calculated for every iteration. The algorithm converges when the criteria: $\epsilon\{F(i_s\{X\}^{(u)})\} < 0.1\%$ is satisfied (which indicates that the function has reached its minimum value), resulting in operating points $\{\hat{\omega_s}, \hat{\vartheta}\}$ that correspond to minimum turnoff current. To quantify the stop criteria for the optimization algorithm, Fig. 16 portrays the plot of the error with respect to number of iterations. As observed, the function converges after 54 iterations, when the error values satisfy the convergent criteria ($\epsilon\{F(i_s\{X\}^{(u)})\} < 0.1\%$). The number of iterations can be further reduced by adding a learning coefficient α_k in the optimum point tracking process [25]. These optimum points are stored along with the load information in the microcontroller (TMS320F28379D) as a lookup table. The number of entries in the lookup table significantly affects the accuracy of SR control, which is selected by analyzing the storage space and corresponding computation time of the microcontroller and % efficiency degradation (as compared to 1% variation in load) on account of linear interpolation applied to the nearest entry in the lookup table. In that context, Table 6 provides the

TABLE 6. Accuracy Comparison for Increasing Order of Entries in Lookup Table and Corresponding Efficiency Degradation

Number of Lookup Table Entries	Average % mismatch due to linear interpolation	% Degradation in efficiency
5	13.56%	3.01%
10	11.77%	2.72%
15	8.19%	2.51%
20	4.64%	2.11%
25	2.97%	1.83%
30	2.27%	1.26%
33	0.89%	0.84%

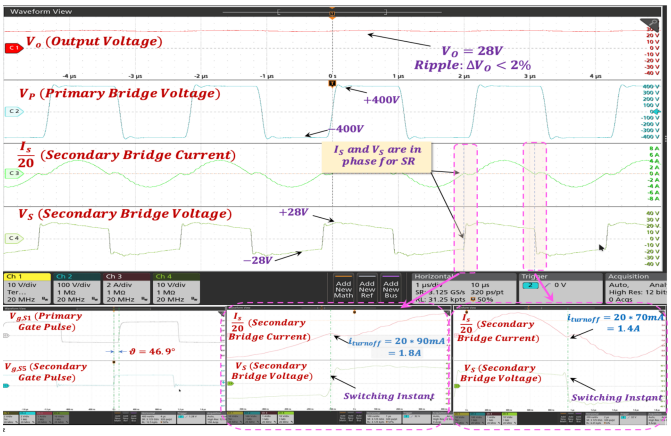

FIG. 17. Experimental Waveforms for 400-28 V conversion at 1 kW elucidating SR.

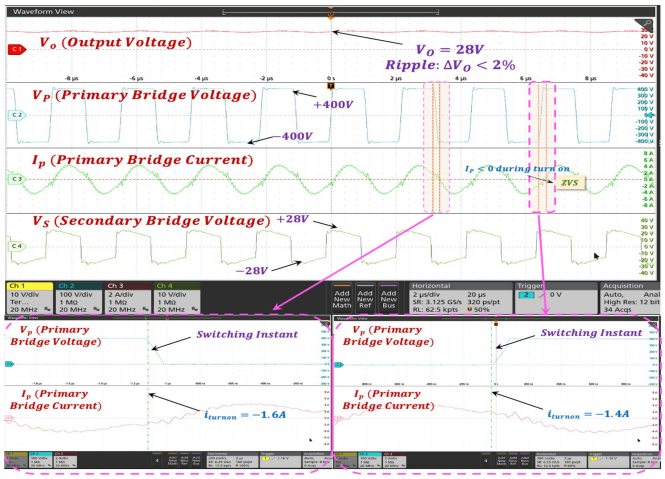

FIG. 18. Experimental Waveforms for 400-28 V at 1 kW elucidating ZVS.

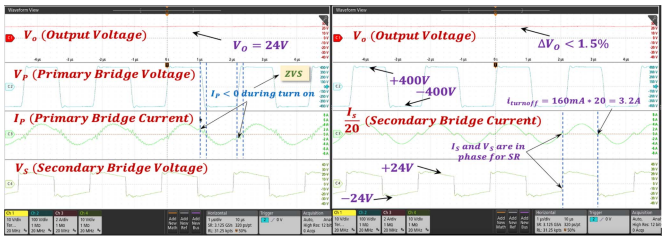

FIG. 19. Experimental Waveforms for 400-24 V conversion at 1 kW.

analytical comparison of increasing number of lookup table entries with respect to accuracy of SR tracking.

As observed in Table 6, by restricting the mismatch to <1% (avg.) corresponding to an efficiency degradation of 0.84%, the number of lookup table entries can be restricted to 33, thus ensuring accurate SR tracking while avoiding any additional computational burden to the microcontroller employed. For open loop operation of the developed converter at the optimal operating point, the load information is sensed, and corresponding gate pulses are given to switch S_1 to S_4 having a switching frequency of $\widehat{f_s} = \frac{\widehat{\omega_s}}{2\pi}$. In addition to that, the gate pulses are shifted by a phase of $\hat{\vartheta}$ and are applied to secondary side switches (S_5 to S_8) to obtain the required SR action.

Please note, due to significantly high magnitude of I_s, the interface between the HFPT and secondary bridge PCB is made using 20 Litz wires of same specification, connected in parallel to (a) facilitate near-equal sharing of current amongst all the wires and (b) to minimize any additional stray inductance, thus ensuring optimal tank design. Relevant experimental results for I_s have been obtained by probing one of the Litz wire.

Figs. 17–18 show the experimental results obtained for forward power flow for a voltage conversion of 400-28 V, obtained at 462.9 kHz with a SR phase shift of $\vartheta = 46.9°$, resulting in minimum switching losses (of 62 mW), portraying a strong agreement with the presented analysis, having a mismatch of 0.29% only. As observed, the instantaneous current at turn-off instant is significantly less (∼1.4A), which ensures ominously reduced turnoff losses for the secondary side switches. Further, as observed in Fig. 18, the primary current lags the primary bridge voltage thus achieving ZVS operation [39] ($i_p < 0$ at turn-on), which matches the presented analysis and justifies the winding selection and ZVS based constraint.

$$P_{turnoff} = 2\frac{1}{2}V_o i_{turnoff} f_s t_{off} = 62mW \tag{43}$$

In addition to that, as observed in Fig. 17, as the optimum operating point occurs at $f_s < f_r$, there is a small phase lag (<1.7°) between V_S and I_S , where the reactive power (Q) of the system is not zero. This phase refers to the superimposed phase lag obtained as cumulative phase difference between fundamental and higher order harmonic components obtained by GHA based harmonic decomposition of V_S and I_S. But, as this lag is relatively small and falls in the ±2.5° limit as discussed in the initial assumption adopted (10), the Q due to this phase lag is negligible and does not interfere with the SR action, maintaining reduced switching losses at the secondary side.

To elucidate the wide-gain capability of the designed converter, Fig. 19 shows experimentally obtained waveforms for 400-24 V conversion, with its optimum operating point

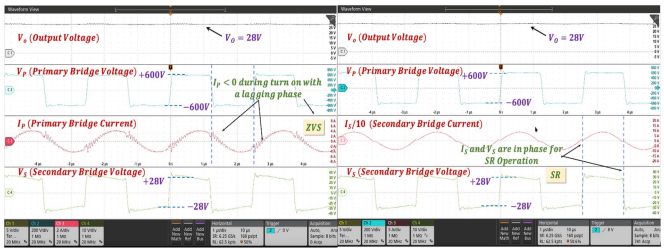

FIG. 20. Experimental Waveforms for 600-28 V conversion at 1 kW.

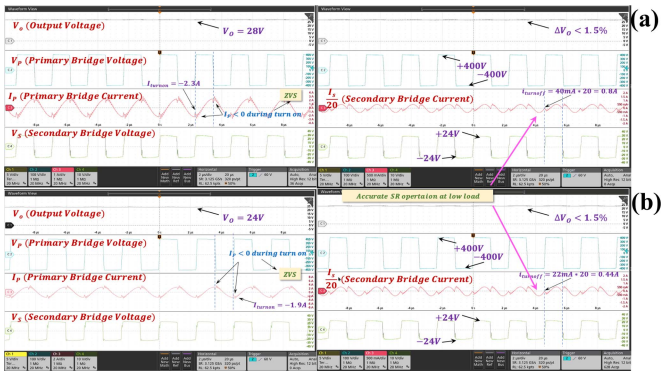

FIG. 21. Experimental Waveforms for (a) 400-28 V (b) 400-24 V conversion at 100W.

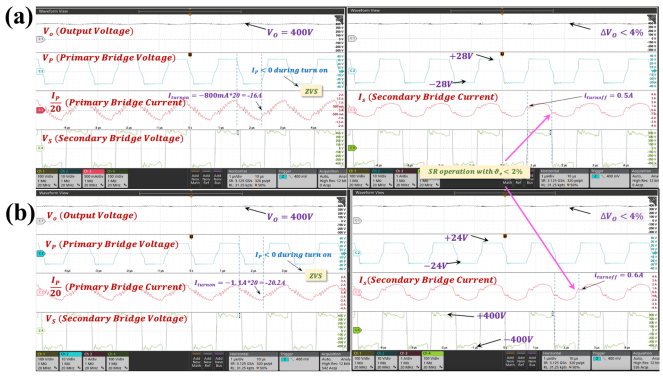

FIG. 22. Experimental Waveforms for reverse power flow (a) 28-400 V (b) 24-400 V conversion.

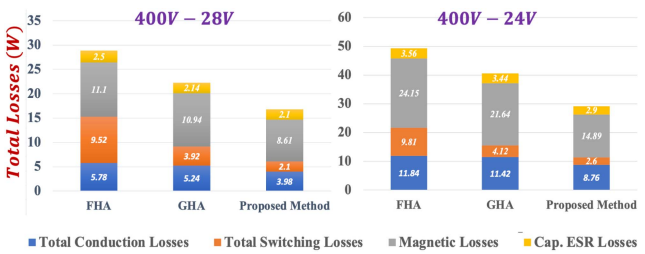

FIG. 23. Loss breakdown and comparison of 400-28 V and 400-24 V conversions.

located at $\{f_s, \vartheta\} = \{452.5\,\text{kHz},\ 42.2^\circ\}$. As observed, the primary switches undergo ZVS turn-on, while the secondary side switches experience minimal switching losses (84 mW) accounting for the comprehensive phase identification method used to enable SR.

Further, to elucidate the optimum SR phase and frequency tracking for a higher voltage step down condition, Fig. 20 portrays the experimentally obtained waveforms for 600 V-28 V conversion at the rated load of 1 kW. As observed, the ZVS and SR operations are retained, thus also achieving superior efficiency for a wide input voltage gain range.

While adhering to the efficiency maximization objective by reducing the secondary side switching losses at higher loading conditions, the presented analysis also portrays its effectiveness in light loading conditions. Fig. 21(a)–(b) illustrates the converter operation at 10% load, while achieving the required gain range to obtain $V_o = 28\,V$ and $V_o = 24V$, respectively. As observed, ZVS operation is maintained, while the turnoff losses at the secondary side are limited to 59 mW due to accurate SR tracking.

Further, to portray the feasibility of efficient reverse power flow for V2G applications, Fig. 22 shows experimentally obtained waveforms implementing the optimal phase detection method as explained in Section III. As observed, the turnoff current is reduced to $\sim 0.5A$ that corresponds to switching losses of only 62 mW in the secondary side, in addition to ZVS at the primary side, leading to reverse power peak efficiency of 96.2%.

To benchmark the efficiency improvement of the proposed SR method for 400 V-28 V and 400 V-24 V conversion, a detailed analytical loss breakdown at rated load of 1kW is provided in Table 7, that compares the various aspects of system losses for FHA, GHA, and the proposed method. As the SR action maintains a near-zero phase angle between secondary current and bridge voltage fundamental, it results in the least RMS current for a specific power transfer amount and reduces the device and winding conduction losses, when compared to other conventional FHA and GHA methods. Therefore, an illustrative loss breakdown for 400 V-28 V and 400 V-24 V conversion is graphically presented in Fig. 23. As observed, due to the accurate characterization of the system parasitics and inclusion of all the higher order harmonic components in the analytical model, the steady state values of SR enabling phase shift (ϑ) and operational frequency (f_s) obtained from the turnoff current minimization algorithm result in significant reduction of the SR phase tracking error (ϑ_ε) (less than 0.1%), as compared to the FHA and GHA based approaches (∼12% and ∼4% respectively). This ensures substantial reduction in the switching losses incurred in the secondary side, thus portraying a reduction of 77.9% and 46.4% in the overall switching losses for a 400 V-28 V conversion as compared to FHA and GHA based approaches respectively. Moreover, as observed in (44), for the same amount of output power (P_o) processed in the converter, as the phase lag error (ϑ_ε) is reduced, the RMS value of secondary side bridge current is also reduced, which results in reduction in the conduction losses of the switches (31.1% and 23.4% as compared to FHA and GHA respectively) and AC winding losses of the HFPT (22.4% and 21.3% as compared to FHA and GHA

TABLE 7. Comprehensive Loss Breakdown and Comparison for FHA, GHA and The Proposed Method

Loss category	Loss sub-category	Formulation	Comments	FHA	GHA	Proposed Method
Semiconductor Losses	Switch Turn on losses	$P_{sw,on\,(S_X)} = \frac{1}{2}V_{DS\,(S_X)}I_{D\,(S_X)}\left(t_{1,on\,(S_X)} + t_{2,on\,(S_X)}\right)f_s$ Where, $t_{1,on\,(S_X)} = R_{g\,(S_X)}C_{in(S_X)}\ln\left(\frac{V_{Dr(S_X)} - V_{th(S_X)}}{V_{Dr(S_X)} - V_{pl(S_X)}}\right)$ $t_{2,on(S_X)} = \frac{C_{gd\,(S_X)}\left(V_{DS\,(S_X)} - I_{D(S_X)}R_{DS,on\,(S_X)}\right)R_{g(S_X)}}{V_{Dr(S_X)} - V_{pl(S_X)}}$	Primary Side Switches $(S_1 - S_4)$ will undergo ZVS due to operation in inductive region. However, they will still incur turnoff losses. The secondary side switches $(S_5 - S_8)$ will incur turnoff losses corresponding to the error in the phase calculation. For FHA and GHA based methods the inaccuracy in the phase estimation was ~4% and ~12% respectively, as compared to the proposed model, leading to higher switching losses.	9.52W (400-28V) 9.81W (400-24V)	3.92W (400-28V) 4.12W (400-24V)	2.14W (400-28V) 2.6W (400-24V)
	Switch Turn off losses	$P_{sw,off\,(S_X)} = \frac{1}{2}V_{DS\,(S_X)}I_{D(S_X)}\left(t_{1,off\,(S_X)} + t_{2,off\,(S_X)}\right)f_s$ Where, $t_{1,off\,(S_X)} = R_{g(S_X)}C_{in(S_X)}\ln\left(\frac{V_{pl(S_X)}}{V_{th(S_X)}}\right)$ $t_{2,off(S_X)} = \frac{C_{gd(S_X)}\left(V_{DC(S_X)} - I_{D(S_X)}R_{DS,on(S_X)}\right)R_{g(S_X)}}{V_{pl(S_X)}}$				
	Conduction Losses	$P_{cond\,(S_X)} = I^2_{D,RMS\,(S_X)}R_{DS,on\,(S_X)}$	The conduction losses in the switches depend on the tank currents, which are a function of the operating frequency and the phase shift.	5.78W (400-28V) 11.84W (400-24V)	5.24W (400-28V) 11.42W (400-24V)	3.98W (400-28V) 8.76W (400-24V)
Capacitor ESR Losses	-	$P_{Cap,ESR} = I^2_{O,ripple\,(RMS)}R_{C_O,ESR}$	The capacitor ESR losses remain relatively unchanged in all the cases.	2.5W (400-28V) 3.56W (400-24V)	2.14W (400-28V) 3.44W (400-24V)	2.12W (400-28V) 2.9W (400-24V)
Magnetics	Core Losses	$P_{core} = \frac{1}{T}\int_0^T k_i \left\|\frac{dB}{dt}\right\|^{\alpha}(\Delta B)^{\beta-\alpha}dt$ Where, $k_i = \frac{k}{(2\pi)^{\alpha-1}\int_0^{2\pi}\|\cos\theta\|^{\alpha}2^{\beta-\alpha}d\theta}$	The RMS values of the tank current are different for FHA, GHA, and proposed method due to different operating frequencies. With the accurate phase and frequency calculated, the winding losses are least in the proposed method.	11.1W (400-28V) 24.15W (400-24V)	10.94W (400-28V) 21.64W (400-24V)	8.61W (400-28V) 14.89W (400-24V)
	Winding Losses	$P_{winding} = I^2_{p,RMS}R_p + I^2_{s,RMS}R_s$				

For any switch $S_{X;\,X\in\{1,2,\ldots8\}}$: -
$V_{pl\,(S_X)}$ = Gate plateau voltage
$R_{DS,on\,(S_X)}$ = On-state resistance of the switch
$R_{g\,(S_X)}$ = External gate resistance
$I_{D\,(S_X)}$= Instantaneous drain current of the switch
$I_{D,RMS\,(S_X)}$= RMS drain current of the switch
$C_{gd\,(S_X)}$= Gate to drain capacitance of the switch
$C_{in\,(S_X)}$ = Input capacitance of the switch
$C_{gs\,(S_X)}$= Gate to source capacitance
$R_{C_O,ESR}$ = ESR of the output capacitor
$V_{th(S_X)}$ = Threshold voltage
k, α, β = Steinmetz equation parameters
ΔB = peak to peak flux density
$t_{1,on(S_X)}$ = Time required for I_D to reach its rated value
$t_{2,on(S_X)}$ = Time required for V_{DS} to drop down to zero
$t_{1,on(S_X)}$ = Time required for V_{DS} to reach its rated value
$t_{2,on(S_X)}$ = Time required for I_D to drop down to zero

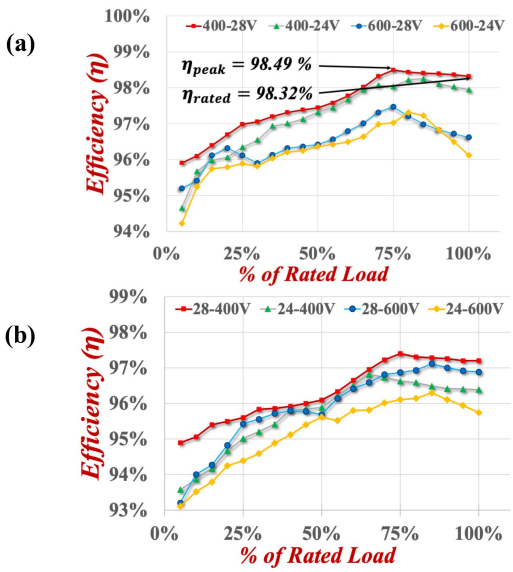

FIG. 24. Efficiency trend for various loading conditions (a) Forward Power Flow; (b) Reverse Power Flow.

respectively) for a 400-28 V conversion.

$$P_o = \frac{1}{2}\sum_{k=\,13,5\ldots}^{2n+1} V_{s,k}I_{s,k}\cos(\vartheta_\varepsilon) \tag{44}$$

Further, Fig. 24(a) compares the forward power flow efficiency trend, while Fig. 24(b) portrays the reverse power flow efficiency trend for various loading and corner gain conditions. As observed, due to elaborate and precise modelling accounting for the stray components affecting the system operating point, the proposed model yields a peak efficiency of 98.49% at an ambient temperature of 22 °C , depicting its superiority even at a high operational frequency. The main reasons leading to this enhanced efficiency profile trace back to the aspects including the employment of GaN devices that portray ultra-low body capacitors [40] and low $R_{ds,on}$ [41] resulting in reduced switching and conduction losses, optimized selection of phase-frequency operating point to facilitate reduced turn-off losses in the secondary bridge, and an optimum HFPT winding selection leading to reduced winding resistance and corresponding high-frequency AC losses.

VI. CONCLUSION

Meticulously considering the effect of stray parameters on the performance of a bidirectional asymmetric CLLC DC/DC converter, a comprehensive GHA based modeling and analysis is presented in this paper. Stressing on the influence of the stray components, a detailed all-inclusive gain model is derived, which is further validated with several experimentally obtained gain points, portraying an average mismatch

in gain modulation trend of 0.44% only, thus confirming its accuracy. Unlike other state-of-the-art methods focusing only on phase modulation or frequency modulation, the proposed SR phase detection technique provides a contour of feasible $\{\omega_s^*, \vartheta^*\}$ points for different gain/load operations. Further, a non-linear multi-dimensional minimization function for the secondary current zero crossing is defined with an error margin of 0.1%, that tracks the phase required to facilitate SR, and is experimentally verified elucidating a phase error of 0.29%. To facilitate the proposed SR tracking method and to ensure optimum transformer design, a thorough parametric RLC modeling of HFPT aided with detailed 3D FEA analysis is presented. To validate the presented model and SR phase detection method, exhaustive experimental analysis for a 1kW prototype operating at 500 kHz resonant frequency with results at various corner conditions are presented. Experimental results for forward power flow for 400-28 V and 400-24 V are provided which portray a turnoff current of ∼1.4A, highlighting reduction in switching losses, thus achieving a peak efficiency of 98.49%. In addition to that, the reverse power flow capabilities of the designed converter are also verified for different conditions (28-400 V and 24-400 V), which due to accurate phase detection, portrays a peak converter efficiency of 96.2%.

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