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Multilevel Switched Capacitor LLC-DCX Converter With Embedded Filter

SHOTA OKUTANI (Graduate Student Member, IEEE), RYO NISHIYAMA (Graduate Student Member, IEEE), PIN-YU HUANG (Member, IEEE), AND YUICHI KADO (Member, IEEE)

Graduate School of Science and Technology, Kyoto Institute of Technology, Kyoto 606-8585, Japan

CORRESPONDING AUTHOR: SHOTA OKUTANI (e-mail: s.okutani.kit@gmail.com)

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ABSTRACT A multilevel switched capacitor LLC-DC transformer (LLC-DCX) converter with an embedded filter is presented for a power module of solid-state transformers. The proposed converter is a hybrid converter composed of resonant switched capacitor converters (RSCCs) and a previously reported ripple-cancel converter. In contrast to the conventional SCC, which faces the issue of an inrush hard-charging current during switching transition, the proposed converter can be implemented using a soft-charging operation without additional inductors. Further, it inherits the advantages of the two converters, including load-independent soft switching, automatic voltage sharing, automatic current sharing, reduction of the current ripple, an embedded filter function, constant voltage gain, and flexible extensibility. This paper comprehensively analyzes these characteristics and the conditions for soft-charging operation. The design theory based on the analysis is also presented. We fabricated a prototype of the proposed converter with input and output voltages of 900 V and 150 V, respectively and the rated output power of 2 kW to demonstrate the validity of the analysis and design.

INDEX TERMS LLC resonant converter, switched capacitor, embedded filter, high-voltage application, soft switching, hybrid converter, solid-state transformer, DC transformer (DCX).

I. INTRODUCTION

Solid-State transformers (SSTs) are promising technologies to replace the bulky and heavy line frequency transformers (LFTs) for medium voltage (MV) applications, such as distribution systems, traction systems, wind or photovoltaic (PV) renewable energy systems, battery energy storage systems (BESS), shipboard-distribution systems, and even future electric aircraft systems [1], [2], [3], [4], [5], [6]. One of the major challenges with SSTs is the high voltage stress on the MV side. Several studies have focused on two-level converters utilizing MV power devices (10 kV–15 kV) [7], [8], which feature a simplified and mature configuration. However, soft switching on the MV side is difficult to achieve, and electromagnetic interference (EMI) becomes severe. In addition, the highest blocking voltage of SiC-MOSFETs in the distribution market is around 3.3 kV at present [9]. Thus, using low voltage (LV) power devices to handle the high voltage stress on the MV side is considered effective in terms of soft switching, cost, and EMI.

The majority of the existing SSTs consist of a modular multilevel converter (MMC) or cascaded modular converter (CMC) to handle high voltage stress on the MV side. With an MMC, stacked half-bridge modules effectively reduce the voltage stress [10], [11], but designing an MV medium frequency transformer (MFT) with a large turn ratio has challenges related to compatibility between the insulation and thermal management [12]. As for a CMC, stacked power modules (PMs) also effectively share the voltage stress while avoiding the difficulty of designing MVMFT [13], [14], [15], [16].

Although there are several circuit topologies for an isolated bidirectional DC/DC converter (IBDC) in a PM, the LLC-DC-transformer (LLC-DCX) converter is an outstanding candidate thanks to its load-independent soft switching, small turn-off switching loss, small harmonic component by quasi-sinusoidal current, and constant voltage gain against the load variation without a closed loop voltage control. Furthermore, modular SSTs consisting of LLC-DCXs feature automatic

input voltage sharing without a closed-loop voltage control, yielding a small control complexity [14], [15], [16]. For these reasons, LLC-DCX is widely utilized in SST applications [7], [8], [12], [14], [15], [16].

One of the challenges with LLC converters is that the current ripples are generally high. Although the modular configuration can mitigate the output current ripple by using multiple-phase control between modules, the input current ripple of each module remains. This input current ripple has negative effects on both the reliability and the power density of the SST. The reliability of DC-link capacitors is a particularly pressing concern in power electronic systems because they account for about 30% of converter failures [17]. Generally, an electrolytic capacitor bank is utilized as the DC-link capacitor, but the lifetime of the electrolytic capacitor is shorter than that of film or ceramic capacitors due to the evaporation of the electrolyte stemming from the power dissipation loss of the current ripple. A hybrid capacitor bank can resolve this problem to some extent, but there is still a certain amount of high-frequency current ripple flowing into the electrolytic capacitors [18], [19]. Thus, the standard solution is to utilize the film capacitor bank at the cost of power density. Furthermore, the input current ripple causes a reduction in the output power of PV systems [20], [21], [22]: in [20], experiments showed that the ripple reduction technology increased the average output power from the PV modules by 7%. This problem may also happen in the cascaded modular large-scale PV systems, where SST is applied [23], [24], [25].

In addition to reducing the current ripples, the number of PMs should be reduced by increasing the voltage rating of PMs to improve the power density of the SST. In fact, the overall power density of the SST decreases significantly compared to the power density of the PM converter as the number of PMs increases [26], [27], which reinforces the fact that a high-voltage LLC converter is required.

In response to the above two challenges, a multilevel Dickson-type ripple-cancel LLC (DRCLLC) converter is proposed for the PM. The proposed converter is a hybrid converter consisting of a ripple-cancel circuit and Dickson-type resonant switched capacitor converters (RSCCs). The general switched capacitor converter (SCC) has an inrush hard-charging current due to the charge redistribution, and the proposed converter can solve this problem without an additional inductance. In addition, it inherits the advantageous characteristics of the two converters, namely, load-independent soft switching, automatic voltage sharing, automatic current sharing, reduction of the current ripple, embedded filter function, constant voltage gain, and flexible extensibility.

Section II of this paper presents an overview of the conventional solutions for the two challenges discussed above to clarify their inherent limitations. The derivation of the proposed converter is introduced in Section III. In Section IV, the proposed converter is analyzed in detail, and in Section V, its design methodology is presented. Experimental results are provided in Section VI. Section VII presents a topology comparison. We conclude in Section VIII with a brief summary.

II. REVIEW OF CONVENTIONAL SOLUTIONS

In this section, we present a brief overview of the conventional solutions for the challenges pertaining to ripple reduction and the high-voltage LLC converter. We also introduce the motivation underlying the proposed converter.

A. RIPPLE REDUCTION

Several topologies have been proposed to mitigate current ripples, such as the interleaved converter [28], [29] and the passive ripple-cancel circuit [20], [30], [31]. The interleaved converter can effectively mitigate the current ripples, but it requires multiple phases, which results in lower power density. In addition, it is difficult to apply the interleaved technique to an LLC-DCX without closed-loop control due to the resonant parameter mismatch [29], thus making it unsuitable for a PM. As for the passive ripple-cancel circuit, while it can cancel out the input current ripple without affecting the original converter's operation, it requires additional magnetic components (e.g., transformers and coupled inductors) and thus also reduces the power density. In addition, since this circuit can be applied only to a current-fed converter, it cannot be used with an LLC converter and thus is also unsuitable for a PM. We previously proposed a ripple-cancel technique [32] and applied it to a dual active bridge converter and CLLC converter [33], [34]. As these converters require only an additional clamping capacitor on each port and no extra magnetic components for canceling current ripples, they can improve the power density compared to a CLLC converter with LC filters while maintaining the same current ripple mitigation [34].

B. HIGH-VOLTAGE LLC CONVERTER

Three-level LLC converters are candidates to reduce high voltage stress [35], [36], [37], [38]. [35], [36] proposed neutral-point clamped (NPC) three-level LLC converters in which the voltage stress can be halved by dividing the input voltage equally into two series of DC-link capacitors. However, the inner switches suffer from a high voltage stress equal to the input voltage when their driving signal turns off earlier than that of the outer switch. To avoid this issue, the gate driving signal of the outer switch can be turned off earlier than that of the inner switch, but this is more complicated than the simple driving signal with a duty ratio of 50% and complicates the ZVS condition. In addition, the neutral point voltage should be balanced for proper operation. The proposed in [37], [38] feature a series half-bridge (SHB) that halves the voltage stress on the switches with a simple duty ratio of 50%. However, as this creates an imbalance in the neutral point voltage, active voltage control is required [38]. In addition, there is no simple way to extend the three-level converters to higher levels due to the complicated gate driving signals and the voltage imbalance between series of DC-link capacitors. [39], [40] proposed ladder SCC hybrid LLC converters to automatically share the input voltage equally among two series of DC-link capacitors. Despite the gate driving signals of the switches being merely a duty ratio of 50%, the input

voltage can be naturally shared among the two series thanks to the SCC characteristics. Inspired by this technology, we previously proposed a ripple-cancel multilevel converter with automatic voltage/current sharing and flexible extensibility [41]. However, the major challenge with the SCC is the inrush hard-charging current due to the charge redistribution, and to limit this current, a sufficiently large on-resistance of the power devices or capacitance of the switched capacitors is required, which sacrifices either the efficiency or the power density or both. Thus, it may be difficult to maintain high efficiency and high power density in high-power applications over 50 kW, such as SSTs. Alternatively, an RSCC can limit the inrush hard-charging current by utilizing the small inductance, which is a technique known as soft-charging operation [42], without the expense of efficiency and power density. Thus, RSCC topologies have recently been applied to high-power applications over 50 kW, and the reported efficiencies have been as high as 97% [43], [44], [45]. A flying-capacitor-based hybrid LLC converter based on the ladder RSCC has been proposed [46]. This converter features automatic voltage and current sharing and can easily be extended for the M series of DC-link capacitors. However, an additional inductor is required in each switched capacitor loop to suppress the inrush current. As a result, the number of necessary inductors increases as the level increases, and these additional inductors must have the same inductance value in order to share the switch currents. Thus, the converter is sensitive to component tolerance.

C. MOTIVATION UNDERLYING PROPOSED CONVERTER

Our review of the two issues above indicates that integrating the previously proposed ripple-cancel technique and RSCCs is a good candidate for achieving a high-voltage LLC converter suitable for high-power applications. However, as stated, the general ladder RSCC is sensitive to component tolerance and requires more inductors as the level increases. Thus, it is attractive to ensure that no inductors are added except resonant inductors for transferring power. According to [42], the Dickson-type RSCC with clamping capacitors can overcome this issue simply by utilizing an aggregated resonant inductor. Thus, this paper proposes a hybrid converter consisting of the ripple-cancel LLC-DCX and Dickson-type RSCCs.

III. CIRCUIT DERIVATION

Fig. 1 depicts the circuit diagram of (a) the 4-to-1 step-down Dickson-type RSCC-based hybrid LLC converter and (b) its mirrored converter, respectively. In the circuit diagrams, L_{ri} ($i = 1, 2$) is a resonant inductor, C_{ri} ($i = 1, \ldots, 4$) is a resonant capacitor, and C_{ci} ($i = 1, 2$) is a clamping capacitor whose capacitance is large enough compared with that of the resonant capacitor. The odd- and even-numbered switches are complementarily operated with a duty ratio of 50%. In Fig. 1(a), when Q_1 and Q_3 are conducted, C_{r1} and C_{r2} are discharged, and when Q_2 and Q_4 are conducted, C_{r1} and C_{r2} are charged. On the basis of the circuit operation of the Dickson converter, the

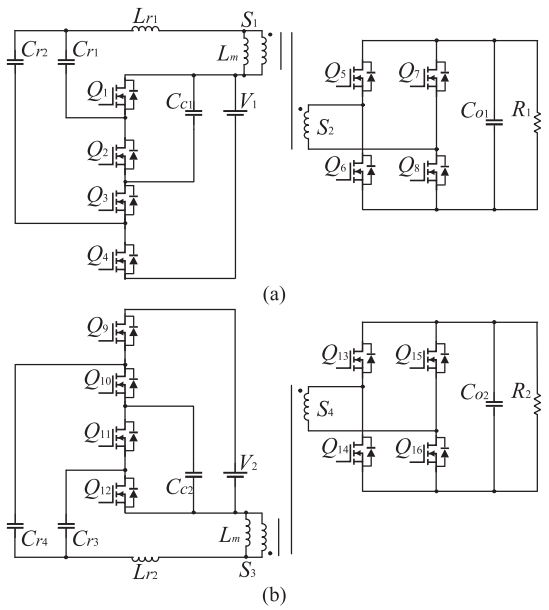

FIGURE 1. Circuit diagrams of (a) 4-to-1 step-down Dickson-type RSCC-based hybrid LLC converter and (b) its mirrored one.

average voltage stresses of each capacitor are represented as

$$V_{Cr1} = \frac{1}{4}V_1, \quad V_{Cc1} = \frac{1}{2}V_1, \quad V_{Cr2} = \frac{3}{4}V_1. \tag{1}$$

In the same manner, in Fig. 1(b), when Q_9 and Q_{11} are conducted, C_{r3} and C_{r4} are charged, and when Q_{10} and Q_{12} are conducted, C_{r3} and C_{r4} are discharged. The average voltage stresses of each capacitor are represented as

$$V_{Cr3} = \frac{1}{4}V_2, \quad V_{Cc2} = \frac{1}{2}V_2, \quad V_{Cr4} = \frac{3}{4}V_2. \tag{2}$$

Since the resonant capacitors are charged and discharged complementarily, and the average voltage stresses are symmetric, the proposed converter can be derived by combining the two circuits, as shown in Fig. 2(a). The four switches can be multiplexed since the gate driving signals of the corresponding switches are the same. The generalized M-level DRCLLC based on this circuit derivation is depicted in Fig. 2(b), and the modified generalized M-level DRCLLC by replacing parallel clamping capacitors with stacked clamping capacitors is depicted in Fig. 2(c).

IV. ANALYSIS OF PROPOSED CONVERTER

A. OPERATING PRINCIPLE

We utilize the 6-level DRCLLC shown in Fig. 3 to explain the operating principle. The proposed converter consists of three half-bridge pairs, Q_1–Q_2, Q_3–Q_4, and Q_5–Q_6, on the primary side, a full-bridge, Q_7–Q_{10}, on the secondary side, a transformer with a split primary winding, S_1, S_2, and S_3, a magnetizing inductance of the transformer, L_m, resonant inductors, L_{r1} and L_{r2}, resonant capacitors, C_{r1}–C_{r6}, clamping capacitors, C_{c1}–C_{c3}, and two DC-link capacitors, C_{in} and C_o. The odd- and even-numbered switches on the primary and secondary sides are complementarily operated with a duty

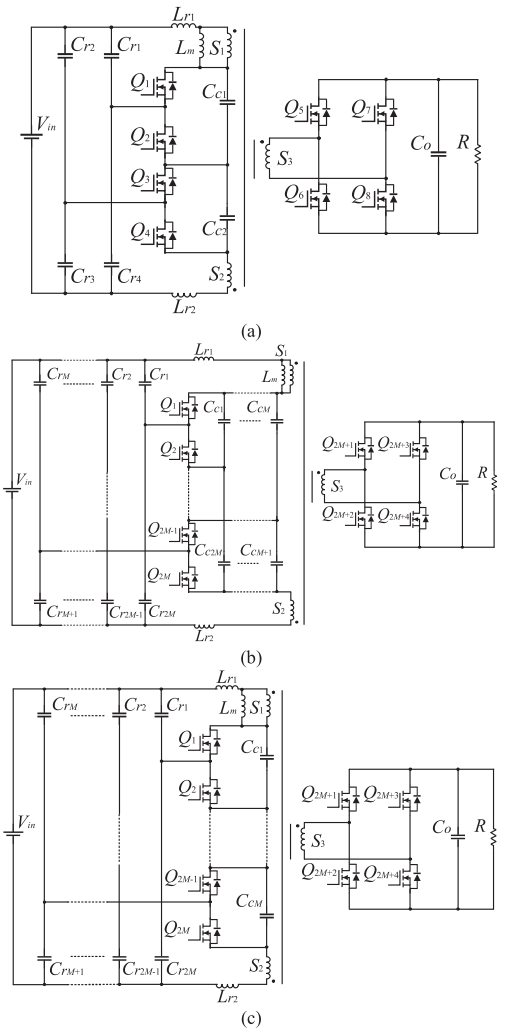

FIGURE 2. Circuit diagram of proposed converter with (a) 4-level configuration, (b) generalized M-level configuration, and (c) modified generalized M-level configuration.

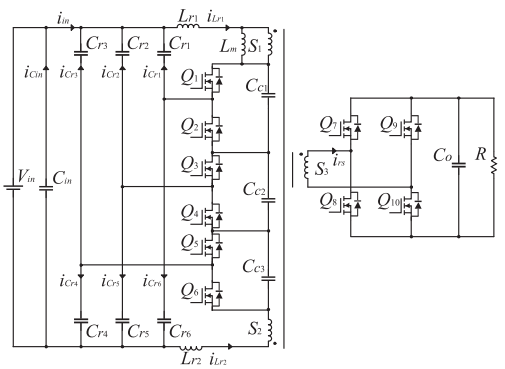

FIGURE 3. Circuit diagrams of 6-to-1 proposed converter.

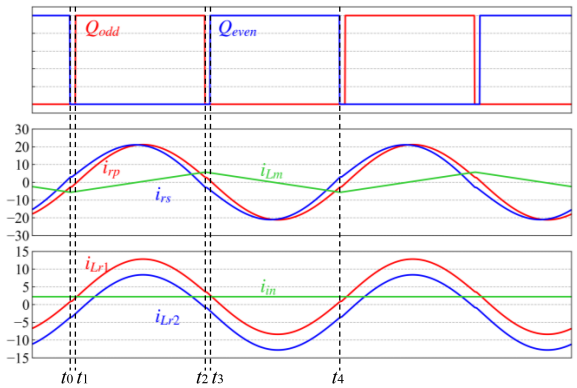

FIGURE 4. Key waveforms of proposed converter.

ratio of 50% and a small dead time T_d [8], [47]. The switching frequency, f_{sw}, is set to the resonant frequency, f_r. Fig. 4 shows the key waveforms of the proposed converter. There are four operating modes in one switching cycle. In the half-switching cycle, there are two modes for power transferring and zero-voltage-switching (ZVS) transition. In the ZVS transition, a split magnetizing current charges or discharges the output capacitors of the switches on both sides [47]. The ZVS analysis is described in subsection IV-B, here, the analysis of the power transfer is focused on.

To simplify the following time-domain analysis of the circuit operation, we assume that the resonant inductors have identical inductances L_r, the resonant capacitors have identical capacitances C_r, the clamping capacitors also have identical capacitances C_c, the clamping capacitors and DC-link capacitors are large enough and can be regarded as constant voltage sources, the turn ratio of the transformer is 1:1:1, the switching frequency is the same as the resonant frequency, and the dead time durations are ignored. During the positive half-cycle, KVL and KCL yield the following set of equations.

$$\begin{cases} L_r\frac{di_{Lr1}}{dt}+\frac{1}{C_r}\int i_{Cr1}dt = v_{Cr1}(t_0)-V_o \\ L_r\frac{di_{Lr1}}{dt}+\frac{1}{C_r}\int i_{Cr2}dt = v_{Cr2}(t_0)-V_o-V_{Cc1} \\ L_r\frac{di_{Lr1}}{dt}+\frac{1}{C_r}\int i_{Cr3}dt = v_{Cr3}(t_0)-V_o-V_{Cc1}-V_{Cc2} \\ L_r\frac{di_{Lr2}}{dt}+\frac{1}{C_r}\int i_{Cr4}dt = V_{Cc3}-V_o-v_{Cr4}(t_0) \\ L_r\frac{di_{Lr2}}{dt}+\frac{1}{C_r}\int i_{Cr5}dt = V_{Cc3}+V_{Cc2}-V_o-v_{Cr5}(t_0) \\ L_r\frac{di_{Lr2}}{dt}+\frac{1}{C_r}\int i_{Cr6}dt = V_{Cc3}+V_{Cc2}+V_{Cc1}-V_o-v_{Cr6}(t_0) \\ L_r\frac{di_{Lr1}}{dt}-L_r\frac{di_{Lr2}}{dt} = V_{in}-V_{Cc1}-V_{Cc2}-V_{Cc3}=0 \\ i_{rp}=i_{Lr1}+i_{Lr2}=i_{Cr1}+i_{Cr2}+i_{Cr3}+i_{Cr4}+i_{Cr5}+i_{Cr6} \end{cases} \tag{3}$$

On the basis of the circuit operation of the Dickson converter, the average voltage stresses of each capacitor are

$$V_{Cr1}=V_{Cr4}=\frac{1}{6}V_{in}, V_{Cr2}=V_{Cr5}=\frac{1}{2}V_{in},$$
$$V_{Cr3}=V_{Cr6}=\frac{5}{6}V_{in}, V_{Cc1}=V_{Cc2}=V_{Cc3}=\frac{1}{3}V_{in}. \tag{4}$$

Thus, the voltage stresses of the switches are automatically shared. As explained in Section III, the upper and lower sides

of the resonant capacitors are discharged and charged, respectively, in the positive half-cycle. Hence, the voltages across each resonant capacitor at t_0 are

$$v_{Cr1}(t_0) = \frac{1}{6}V_{in} + \Delta v_{Cr},\ v_{Cr2}(t_0) = \frac{1}{2}V_{in} + \Delta v_{Cr},$$
$$v_{Cr3}(t_0) = \frac{5}{6}V_{in} + \Delta v_{Cr},\ v_{Cr4}(t_0) = \frac{1}{6}V_{in} - \Delta v_{Cr},$$
$$v_{Cr5}(t_0) = \frac{1}{2}V_{in} - \Delta v_{Cr},\ v_{Cr6}(t_0) = \frac{5}{6}V_{in} - \Delta v_{Cr}, \quad (5)$$

where Δv_{cr} is a voltage ripple across the resonant capacitors. By substituting (4) and (5) into (3), the derivative equation of i_{rp} is

$$\frac{1}{2}L_r\frac{di_{rp}}{dt} + \frac{1}{6C_r}\int i_{rp}dt = \Delta v_{Cr}. \quad (6)$$

The solution for (6) is expressed

$$i_{rp}(t) = \sqrt{2}I_{rp}\sin(2\pi f_r t - \varphi),$$

where

$$f_r = \frac{1}{2\pi\sqrt{3L_rC_r}}. \quad (7)$$

Here, I_{rp} is the RMS value of i_{rp}. The average output current, I_o, can be calculated as

$$I_o = \frac{1}{2T_{sw}}\int_{t_0}^{t_o+T_{sw}/2} i_{rp}(t)\,dt = \frac{2}{\pi}\frac{\Delta v_{Cr}}{\sqrt{L_r/12C_r}}. \quad (8)$$

Thus, the voltage ripple across the resonant capacitors is represented as

$$\Delta v_{Cr} = \frac{\pi I_o}{2}\sqrt{\frac{L_r}{12C_r}} = \frac{\pi I_o}{12\omega_r C_r} = \frac{\pi P_o}{12\omega_r C_r V_o}. \quad (9)$$

Due to the symmetric circuit configuration, the current through each resonant capacitor is represented as

$$i_{Crm} = \frac{1}{6}i_{rp}(m = 1, 2, 3, 4, 5, 6). \quad (10)$$

Thus, the switch currents are automatically shared. By applying KCL, i_{Lr1} is derived as

$$i_{Lr1} = i_{Cr1} + i_{Cr2} + i_{Cr3} + i_{Cin} + I_{in} = \frac{1}{2}i_{rp} + i_{Cin} + I_{in}. \quad (11)$$

Note that (11) holds independently of the operating modes. The average currents of the capacitors are zero based on the charge balance of the capacitors in the steady state. Therefore, i_{Lr1} has a positive DC bias current whose amplitude is the same as I_{in}. Similarly, i_{Lr2} has a negative DC bias current. Here, the AC components of i_{Lr1} are i_{rp} and i_{Cin}. Referring to (3), the derivatives of i_{Lr1} and i_{Lr2} are the same, which yields the following equation:

$$\frac{d}{dt}(i_{Lr1} - i_{Lr2}) = 2\frac{d}{dt}(i_{Cin} + I_{in}) = 0. \quad (12)$$

Therefore, the input current ripple is canceled out in the proposed converter, as shown in Fig. 4. The component stress of the proposed converter as based on this analysis is summarized in Table 1.

TABLE 1 Component Stress of Proposed Converter

Component	Quantity
Pri. switch voltage stress	$\frac{V_{in}}{3}$
Sec. switch voltage stress	V_o
Pri. switch current stress	$\frac{\pi P_o}{6\sqrt{2}V_o}$ (when L_m is ignored.)
Sec. switch current stress	$\frac{\pi P_o}{2\sqrt{2}V_o}$ (when L_m is ignored.)
Inductor current stress	$\sqrt{I_{in}^2 + \left(\frac{\pi}{4\sqrt{2}}I_o\right)^2} = \frac{P_o}{V_o}\sqrt{\frac{8+9\pi^2}{288}}$ (when L_m is ignored.)
Clamping capacitor voltage stress	$\frac{V_{in}}{3}$
Resonant capacitor voltage stress	$v_{Cr1} = v_{Cr4} = \frac{1}{6}V_{in} + \frac{\pi P_o}{12\omega_r C_r V_o}$, $v_{Cr2} = v_{Cr5} = \frac{1}{2}V_{in} + \frac{\pi P_o}{12\omega_r C_r V_o}$, $v_{Cr3} = v_{Cr6} = \frac{5}{6}V_{in} + \frac{\pi P_o}{12\omega_r C_r V_o}$.

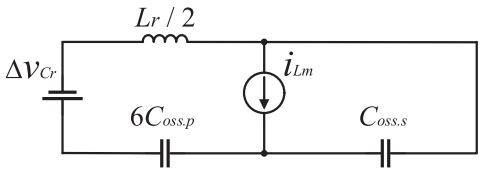

FIGURE 5. Equivalent circuit during ZVS transition.

B. ZVS ANALYSIS

In the proposed converter, the output capacitors of the primary-side switches are connected in parallel, and those of the secondary-side switches are connected in series-parallel during the ZVS transition. Fig. 5 shows the equivalent circuit of the proposed converter during the ZVS transition at t_0 in the forward power flow (cf. Fig. 4). In the equivalent circuit, the magnetizing inductance is assumed to be a constant current source, and voltage ripple by transferring power is assumed to be a constant voltage source. To achieve both-side ZVS, the charge delivered by magnetizing inductance should be greater than the total charge of the output capacitors of both side switches. Thus, the ZVS constraint in (13) can be derived:

$$L_m \le \frac{T_{ZVS}T_{sw}}{8\left(6C_{oss.p} + C_{oss.s}\right)}, \quad (13)$$

where $C_{oss.p}$ is the output capacitor of a switch on the primary side, $C_{oss.s}$ is that on the secondary side, and T_{ZVS} is the duration for ZVS transition. In addition to the constraint in (13), the resonant currents i_{rp} and i_{rs} should be greater and less than zero, respectively, during the ZVS transition, which

are represented as

$$\begin{cases} i_{rp} = -i_{rZVS} + \frac{C_{oss.eq}}{C_{oss.s}} i_{Lm} \geq 0 \\ i_{rs} = -i_{rZVS} - \frac{C_{oss.eq}}{6C_{oss.p}} i_{Lm} \leq 0 \end{cases},$$

where,

$$i_{rZVS} = \frac{\Delta v_{Cr}}{\sqrt{L_r / 2C_{oss.eq}}} \sin\left(\frac{t}{\sqrt{L_r C_{oss.eq}/2}}\right),$$

$$C_{oss.eq} = 6C_{oss.p} // C_{oss.s} = \frac{6C_{oss.p}C_{oss.s}}{6C_{oss.p} + C_{oss.s}}. \quad (14)$$

From (14), the constraint for i_{rp} is more critical for both-side ZVS. Thus, (15) should be satisfied for the charge or discharge output capacitors of the primary-side switches.

$$\int_0^{T_{ZVS}} \left(-i_{rZVS} + \frac{C_{oss.eq}}{C_{oss.s}} i_{Lm}\right) dt$$

$$\geq \int_0^{T_{ZVS}} \left(\frac{C_{oss.eq}}{C_{oss.s}} \frac{V_o T_{sw}}{4L_m} - \frac{\Delta v_{Cr}}{\sqrt{L_r / 2C_{oss.eq}}}\right) dt \geq 6C_{oss.p} \cdot 2V_o \quad (15)$$

By substituting (9) into (15), another constraint for ZVS can be derived:

$$L_m \leq \frac{T_{SW} T_{ZVS}}{8\left(6C_{oss.p} + C_{oss.s}\right) + \frac{2\pi^2 P_o f_r C_{oss.s} T_{ZVS}}{V_o^2} \sqrt{\frac{2L_r}{C_{oss.eq}}}}. \quad (16)$$

The constraint in (16) satisfies (13) and (14). Therefore, to achieve both-side ZVS, the constraint in (16) should be satisfied in the forward power flow. Similarly, the ZVS constraint for the backward power flow can be derived by replacing $C_{oss.s}$ with $6C_{oss.p}$ in (16). In summary, the ZVS constraint for both-side ZVS independent of power flow directions is derived as (17) shown at the bottom of this page.

C. DYNAMIC MODEL

Fast transient response and constant voltage gain characteristics are essential for the proposed converter to operate as a DCX. To evaluate these characteristics, the dynamic model of the proposed converter is necessary. Among the various available modeling methods, the equivalent circuit model is the most intuitive and easy to use in terms of extensibility [48], and so we derive it in this subsection. However, since the proposed converter is a hybrid converter composed of a ripple-cancel LLC and Dickson-type RSCCs, it is challenging to derive them simultaneously. Therefore, referring to [49], we derive a hybrid converter model by decomposing each circuit according to its functions, modeling them individually, and recombining them. Fig. 6 shows the decomposition of the proposed converter, which consists of an embedded filter block of a ripple-cancel LLC and three RSCC blocks. The DC

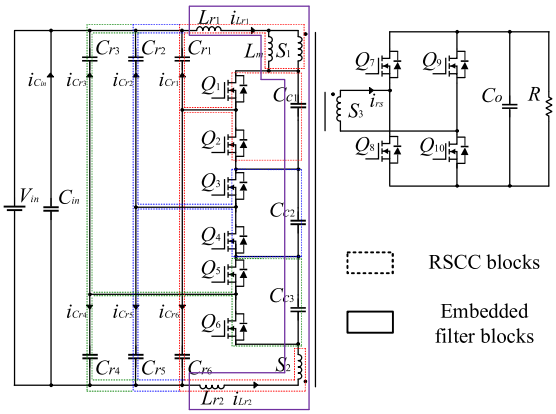

FIGURE 6. Decomposition of proposed converter in accordance with its functions.

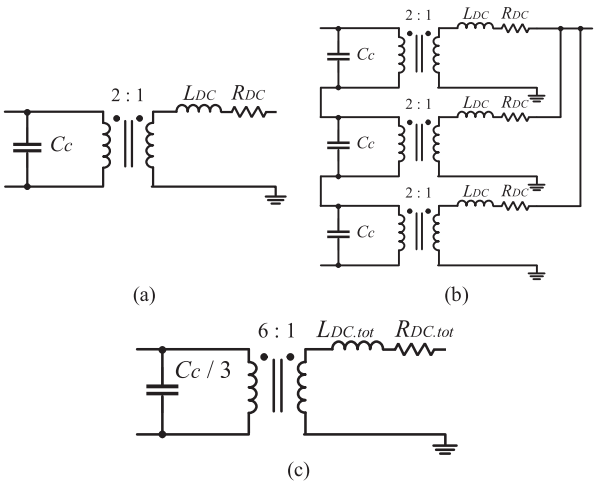

FIGURE 7. DC equivalent circuits of (a) RSCC block, (b) three RSCC blocks, and (c) three simplified RSCC blocks.

equivalent model of the ripple-cancel circuit has already been reported [34], so its derivation is not described in this paper.

The input terminals of each RSCC block are connected to each clamping capacitor, and the output terminals are connected to the output port through the transformer. Thus, the RSCC block can be modeled by the equivalent circuit consisting of an ideal transformer with a 2:1 turn ratio, DC equivalent resistor R_{DC}, and DC equivalent inductor L_{DC}, as shown in Fig. 7(a). Fig. 7(b) depicts the equivalent circuit of the three RSCC blocks [48], [49], with a simplified version shown in (c). The power flow through each RSCC block is associated with a dissipation loss and a certain amount of stored energy in the resonant tank. Therefore, the loss and stored energy should be equal to those in the DC equivalent circuit. R_{DC}

$$L_m \leq \frac{T_{SW} T_{ZVS}}{8\left(6C_{oss.p} + C_{oss.s}\right) + \frac{2\pi^2 P_o f_r T_{ZVS}}{V_o^2} \sqrt{\frac{2L_r}{C_{oss.eq}}} \cdot \max\left[6C_{oss.p}, C_{oss.s}\right]}. \quad (17)$$

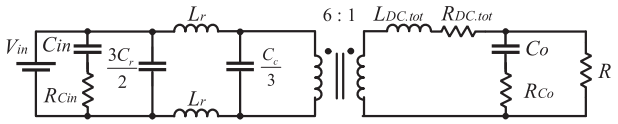

FIGURE 8. Dynamic model of proposed converter.

TABLE 2 Simulation Parameters

Parameters	Quantity
Input voltage V_i	900 V
Output voltage V_o	150 V
Turns ratio N	1:1:1
Switching frequency f_{sw}	130 kHz
Resonant inductor L_r	12 μH
Resonant capacitor C_r	41 nF
Clamping capacitor C_c	20 μF
On-resistance of pri. switch R_{on}	120 mΩ
Input capacitor C_{in}	50 μF
Output capacitor C_o	94 μF
Magnetizing inductance L_m	50 μH (ignored in the model)
Coefficient I_{rp} / I_o	$\pi/2\sqrt{2}$ (ignoring L_m in the model)

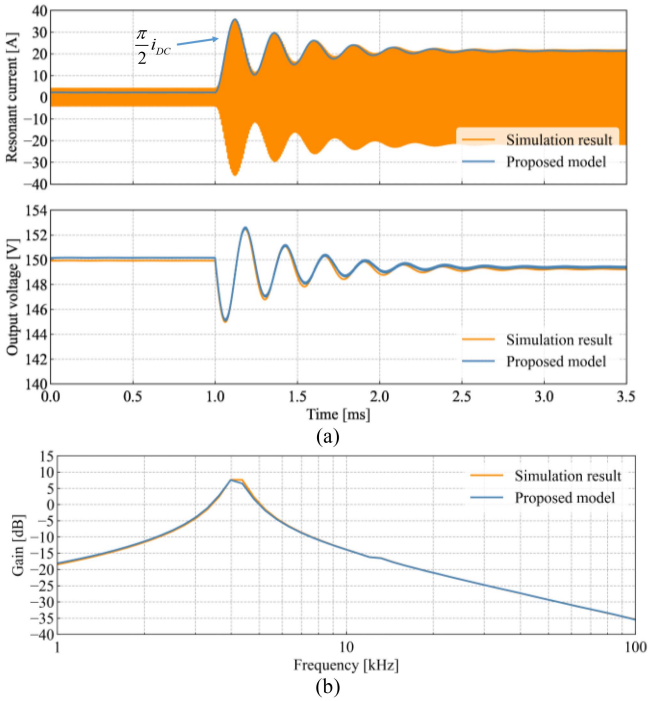

FIGURE 9. Comparison between simulation result and proposed dynamic model: (a) transient response, (b) output impedance.

is derived on the basis of the energy consumption of the on-resistance of the switch, R_{on}. From (10) and Fig. 7(b), R_{DC} is represented as

$$\left(\frac{1}{3}I_{rp}\right)^2 R_{on} = \left(\frac{1}{3}I_o\right)^2 R_{DC} \Leftrightarrow R_{DC} = \left(\frac{I_{rp}}{I_o}\right)^2 R_{on}. \quad (18)$$

L_{DC} is derived on the basis of the stored energy in the resonant tank (resonant capacitor). From (9) and Fig. 7(b), L_{DC} is represented as

$$\frac{1}{2}2C_r\Delta v_{Cr}^2 = \frac{1}{2}L_{DC}\left(\frac{1}{3}I_o\right)^2 \Leftrightarrow L_{DC} = \frac{3\pi^2}{8}L_r. \quad (19)$$

Due to the law of conservation of energy, $R_{DC.tot}$ and $L_{DC.tot}$ in Fig. 7(c) are represented as

$$R_{DC}\left(\frac{I_o}{3}\right)^2 \cdot 3 = R_{DC.tot}I_o^2 \Leftrightarrow R_{DC.tot} = \frac{R_{DC}}{3}, \quad (20)$$

$$\frac{1}{2}L_{DC}\left(\frac{I_o}{3}\right)^2 \cdot 3 = \frac{1}{2}L_{DC.tot}I_o^2 \Leftrightarrow L_{DC.tot} = \frac{L_{DC}}{3}. \quad (21)$$

By recombining the model of the ripple-cancel circuit in [34] and the model of RSCC in Fig. 7(c), the DC-equivalent circuit model of the proposed converter can be derived. Fig. 8 depicts the proposed converter with an embedded input filter consisting of resonant inductors and clamping capacitors. Transient response and output impedance simulations were conducted to verify the proposed model. Fig. 9(a) shows a comparison of transient response under the step load change from 110 Ω to 11 Ω with an input voltage of 900 V, and (b) shows a comparison of the output impedance. The parameters for this verification are summarized in Table 2. Based on the parameters, the $R_{DC.tot}$ and $L_{DC.tot}$ are 49.3 mΩ and 14.8 μH, respectively. As shown in the figure, the proposed model is in good agreement with the simulation results under both the time and frequency domains, which means it can be used to evaluate the fast response and constant voltage gain and even to design the converter parameters. When the clamping capacitors are large enough, the embedded input filter and RSCC blocks can be decoupled, and thus the embedded filter does not provide the output impedance with additional poles or zeros that could cause instability. The $L_{DC.tot}$ should be as small as possible to achieve a fast transient response. As for the corner frequency of the input filter, it is derived as

$$f_c = \frac{1}{2\pi}\sqrt{\frac{3}{2L_rC_c}}. \quad (22)$$

Note that the proposed converter will lose the input filter characteristics with a small L_r. Thus, there is a trade-off between fast transient response and input filter capability.

D. CONDITIONS FOR SOFT-CHARGING OPERATION

Although the proposed converter can operate with soft-charging under an ideal condition in which each resonant component is identical and clamping capacitors are assumed as the constant voltage sources, the exact condition for the soft-charging operation remains unknown. In this subsection, the exact condition for the soft-charging operation is clarified by performing the following procedure.

1) Determine the condition for the amount of voltage increase to prevent voltage mismatching.

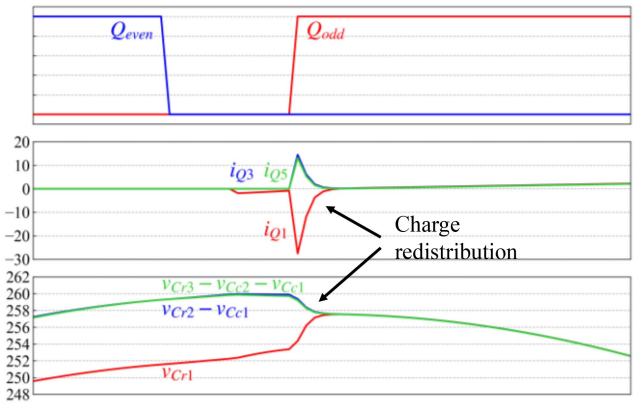

FIGURE 10. Waveforms of charge redistribution under insufficient capacitance of clamping capacitors.

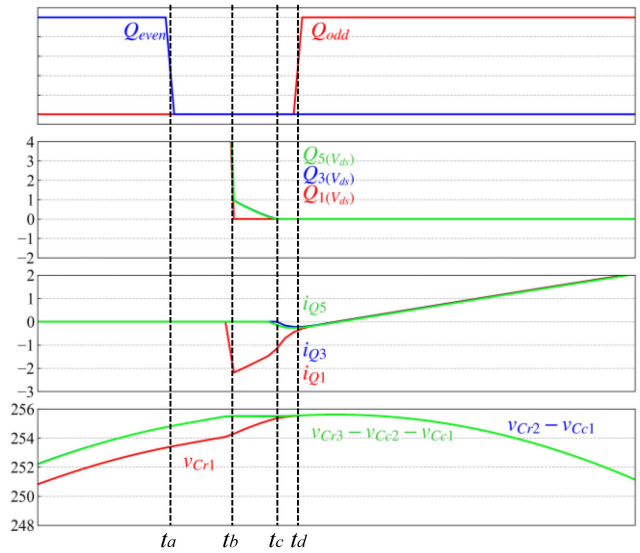

FIGURE 11. Passive compensation scheme for voltage mismatching.

2) Determine the charge through each flying capacitor by means of charge vector analysis.
3) From 1 and 2, determine the capacitor constraints for the soft-charging operation.

The constraints for the resonant and clamping capacitors are derived in (23) and (24), respectively. A detailed derivation is provided in Appendix A.

$$C_{r1} + C_{r6} = C_{r2} + C_{r5} = C_{r3} + C_{r4} = 2C_r. \quad (23)$$

$$C_{Cc1} = \infty, C_{Cc2} = \infty, C_{Cc3} = \infty \quad (24)$$

Eq. (23) indicates that although the total capacitance of the resonant capacitors in each leg should be the same, there are degrees of freedom in the design of the capacitance values in each leg. Thus, this analysis again confirms that the clamping capacitors should utilize sufficiently large capacitances and clarifies both the constraints and the design freedom of the resonant capacitors.

E. INCOMPLETE SOFT-CHARGING OPERATION AND COMPENSATION SCHEME FOR VOLTAGE MISMATCHING

Although the constraints for the capacitors to achieve soft-charging operation are developed as discussed in subsection IV-D, the constraints of (24) imply that the hard-charging operation may be possible as well. Thus, when the capacitances of the clamping capacitors are insufficient, the soft-charging operation is incomplete, and the inrush hard-charging current may occur in the internal flying capacitor network due to the capacitor voltage mismatching during the mode transition. Fig. 10 shows the voltage and current waveforms under the incomplete soft-charging operation. The parameter for the clamping capacitors C_c is set to 2.2 μF, and all other parameters are the same as those in Table 2. Although the capacitance of the clamping capacitors is more than 50 times greater than that of the resonant capacitors, voltage mismatching and the inrush hard-charging current occur (cf. Fig. 10), and the charge redistribution happens during the mode transition.

We propose a passive compensation scheme for voltage mismatching to avoid charge redistribution. The proposed scheme utilizes the dead time and magnetizing current effectively. For simplicity, resonant components are assumed to be identical in the following analysis. When the resonant components are the same, the amount of voltage increase of C_{c2}, Δv_{Cc2}, becomes zero (cf. Appendix A). As such, the charge redistribution can only happen by the voltage mismatching in the flying capacitor network of C_{r1}–C_{r2}–C_{C1} during the transition from the negative to the positive half-cycle and of C_{r2}–C_{r3}–C_{C3} during the opposite transition. Furthermore, since there is no voltage mismatching in the flying capacitor network of C_{r2}–C_{r3}–C_{C2} during the transition from the negative to the positive half-cycle and of C_{r1}–C_{r2}–C_{C2} during the opposite transition, v_{Cc2} and v_{Cc3} are the same during the transition from the negative to the positive half-cycle, and v_{Cc1} and v_{Cc2} are the same during the opposite transition. Consequently, v_{Cc1} is $|\Delta v_{Cc1}|$ smaller than v_{Cc2} and v_{Cc3} during the transition from the negative to the positive half-cycle, and v_{Cc3} is $|\Delta v_{Cc3}|$ smaller than v_{Cc1} and v_{Cc2}. Note that $|\Delta v_{Cc1}|$ is equal to $|\Delta v_{Cc3}|$. Under these conditions, the proposed scheme distinguishes three operating modes for dead time, as shown in Fig. 11. Due to the analogous operation, the transition from the negative to the positive half-cycle is explained.

Mode a [t_a – t_b]: Q_2, Q_4, and Q_6 are turned off at t_a. Since v_{Cc1} is slightly smaller than v_{Cc2} and v_{Cc3}, the drain-source voltage of Q_1 reaches zero faster than those of Q_3 and Q_5. This mode will end when the drain-source voltage of Q_1 reaches zero.

Mode b [t_b – t_c]: When the body diode of Q_1 is conducted at t_b, the drain-source voltages of Q_3 and Q_5 are not zero, and their amplitudes are $|\Delta v_{Cc1}|$. Since the body diode of Q_1 is conducted, the converter starts to transfer the power to the secondary side. During the operation of this mode, the resonant current flows through only the resonant capacitor leg

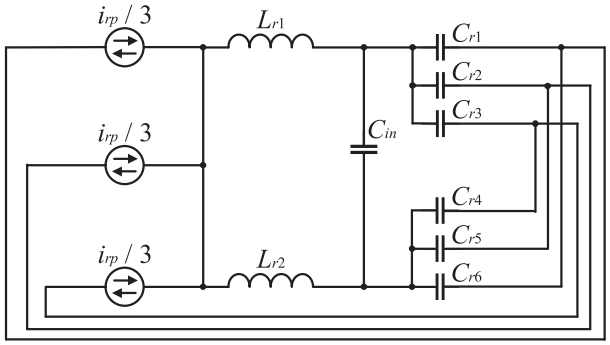

FIGURE 12. AC equivalent circuit of proposed converter.

consisting of C_{r1} and C_{r6}, so C_{r1} and C_{r6} are charged and discharged, respectively. Since the amplitude of voltage mismatching in the flying capacitor network of C_{r1}–C_{r2}–C_{C1} is $|\Delta v_{Cc1}|$, this mode continues until C_{r1} is charged for $|\Delta v_{Cc1}|$. After C_{r1} is charged, there is no longer voltage mismatching, and the drain-source voltages of Q_3 and Q_5 reach zero.

Mode c [t_c – t_d]: Since the drain-source voltages of Q_1, Q_3, and Q_5 are all zero, the body diodes of the switches are conducted. Q_1, Q_3, and Q_5 can be turned on with ZVS at t_d.

Similarly, the drain-source voltage of Q_6 reaches zero faster than those of Q_2 and Q_4 during the opposite transition. To eliminate the voltage mismatching in mode b, the charge delivered by the negative resonant current during dead time T_d should be larger than the charge required to charge C_{r1} and discharge C_{r6}, as represented in (25).

$$\left|\int_0^{T_d} i_{rp}(t)\,dt\right| \geq 2C_r\,|\Delta v_{Cc1}|$$
$$\Leftrightarrow \frac{\sqrt{2}I_{rp}}{2\pi}\left(\cos\left(\frac{2\pi T_d}{T_{sw}}-\varphi\right)-\cos\varphi\right) \geq \frac{2C_r}{C_c}I_{in} \quad (25)$$

F. RIPPLE-REDUCTION CAPABILITY UNDER THE NON-IDEAL CONDITION

In subsection IV-A, it is introduced that the proposed converter has a ripple-cancel capability under the ideal condition. However, resonant components have tolerance in practice. Although the component tolerance of a capacitor can be mitigated by applying class-I ceramic or film capacitors, that of an inductor is difficult to mitigate and generally has a ±10% tolerance. Thus, a ripple-reduction capability under the non-ideal condition is analyzed in this section. Based on the analysis in subsection IV-D, the total capacitance of the resonant capacitors in each leg is assumed to be the same, and the clamping capacitors are assumed to be sufficiently large. Since the total capacitance of the resonant capacitors in each leg is assumed to be the same, the impedance of each resonant capacitor leg is the same, and the i_{rp} is divided into three equal parts. Consequently, the AC equivalent circuit of the proposed converter can be constructed as represented in Fig. 12. In the equivalent circuit, the clamping capacitors are considered short circuits, and the switch-pairs are substituted by the sinusoidal AC current sources with the amplitude of i_{rp} / 3. As shown in Fig. 12, the equivalent circuit of the proposed converter can be represented as an aggregated Wheatstone bridge-like circuit. The current ripple through the input capacitor is represented as

$$i_{Cin} = \frac{L_{r1}(C_{r1}+C_{r2}+C_{r3}) - L_{r2}(C_{r4}+C_{r5}+C_{r6})}{6(L_{r1}+L_{r2})C_r} i_{rp}. \quad (26)$$

Therefore, when the relationship in (27) holds, the input current ripple will be canceled even under the non-ideal condition.

$$L_{r1}(C_{r1}+C_{r2}+C_{r3}) - L_{r2}(C_{r4}+C_{r5}+C_{r6}) = 0 \quad (27)$$

V. DESIGN EXAMPLE

To demonstrate the feasibility of the proposed converter and the validity of the analysis, we fabricated a prototype with the input and output voltages of 900 V and 150 V, respectively, the rated output power of 2 kW, and the switching and resonant frequencies of 130 kHz. In this section, the design methodology of the prototype as based on the analysis in Section IV is presented in this section. This section consists of five parts: the design of 1) the magnetizing inductance, 2) the dead time 3) the resonant inductor, 4) the resonant capacitor, and 5) the clamping capacitor.

A. DESIGN OF MAGNETIZING INDUCTANCE

To achieve both-side ZVS independent of the power flow direction, the constraint in (17) should be satisfied. In the proposed converter, $C_{oss.p}$ is 102 pF, and $C_{oss.s}$ is 400 pF. Thus, the constraint for backward power flow is more critical. The ZVS constraint for the prototype converter is

$$L_m \leq \frac{T_{SW}T_{ZVS}}{8\left(6C_{oss.p}+C_{oss.s}\right) + \frac{12\pi^2 P_o f_r C_{oss.p} T_{ZVS}}{V_o^2}\sqrt{\frac{2L_r}{C_{oss.eq}}}}$$
$$= 54.9\ \mu\text{H}. \quad (28)$$

Here, T_{ZVS} is assumed to be 80 ns, and L_r is assumed to be 12 μH. Based on (28), L_m was set to 50 μH in the prototype.

B. DESIGN OF DEAD TIME

Although dead time is required to achieve ZVS, an excessively lengthy dead time may possibly lead to the failure of ZVS. To prevent this, the switches should be turned on before the polarity of the resonant current become positive. Assuming that the ZVS transition T_{zvs} is much shorter than the switching period T_{sw} and can be ignored, and that the magnetizing current is split in accordance with the ratio of the output capacitors on the both-side capacitance ratio as in (14), the lagging phase φ in the forward power flow can be represented as

$$\varphi = \tan^{-1}\left(\left(\frac{C_{oss.eq}}{C_{oss.s}}\frac{V_o}{4L_m f_r}\right)\Big/\left(\frac{\pi I_o}{2}\right)\right). \quad (29)$$

Similarly, φ in the backward power flow can be derived by replacing $C_{oss.s}$ with $6C_{oss.p}$ in (29). Thus, the constraint of

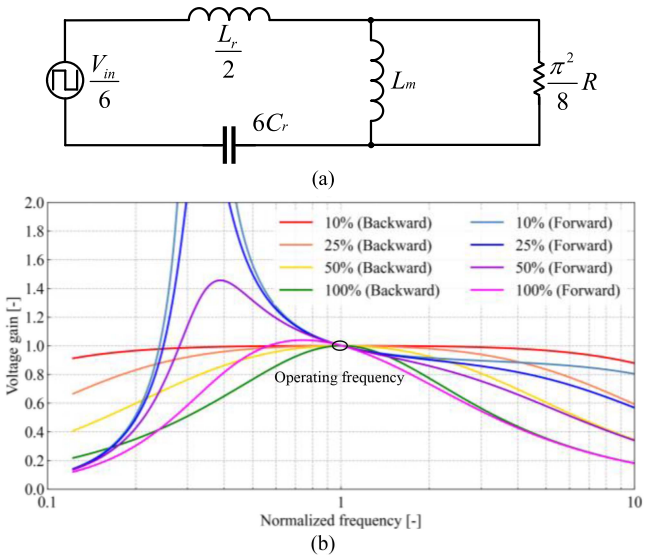

FIGURE 13. (a) FHA model of proposed converter and (b) voltage gains with inductance ratio L_m / L_r = 4.

dead time T_d is

$$T_{ZVS} = 80\text{ns} \le T_d \le T_{ZVS} + \frac{\varphi T_{sw}}{2\pi} = 212\text{ns},$$

where,

$$\varphi = \tan^{-1}\left(\left(\min\left[\frac{C_{oss.eq}}{C_{oss.s}}, \frac{C_{oss.eq}}{6C_{ossp}}\right]\frac{V_o}{4L_m f_r}\right)\Big/\left(\frac{\pi I_o}{2}\right)\right). \quad (30)$$

As discussed in subsection IV-E, the dead time needs to include a period of time to compensate for the voltage mismatching. On the other hand, an increase in dead time duration causes lower efficiency due to the long body diode conducting period. Thus, T_d was set to 200 ns in the prototype.

C. DESIGN OF RESONANT INDUCTOR

To operate the proposed converter as a DCX, the voltage gain should be constant near the resonant frequency. The fundamental harmonic approximation (FHA) model is applied to identify the voltage gain of the proposed converter. Fig. 13(a) shows the FHA model as derived from (6). The voltage gains with inductance ratio $L_m/L_r = 4$ are shown in Fig. 13(b), where the eight curves represent the voltage gains corresponding to the load factors of 10%, 25%, 50%, and 100% under bidirectional power flows. With the inductance ratio, the voltage gains are constant near the resonant frequency under a wide power range. Thus, the resonant inductor L_r was set to 12 μH in the prototype.

D. DESIGN OF RESONANT CAPACITOR

The parameter of the resonant capacitor can be designed on the basis of the resonant frequency and resonant inductor value, as

$$C_r = \frac{1}{12\pi^2 f_r^2 L_r} \Leftrightarrow 41.6\text{ nF}. \quad (31)$$

Since the total capacitance of the resonant capacitors in each leg should be the same as that shown in (23), the class-I C0G ceramic capacitors were applied to the prototype so as to mitigate the component tolerance. Further, the capacitance of the resonant capacitors in each leg can be arbitrarily divided because the constraints for the soft-charging and ripple-canceling operations depend on (23) and (27), respectively. To improve the power density, it is preferable to reduce the capacitance of C_{r3} and C_{r6}, whose rated voltages are large. Therefore, we made a prototype with different capacitance arrangements compared to the first proposed circuit. In the prototype, $C_{r1} = C_{r4} = 2C_r$, $C_{r2} = C_{r5} = C_r$, and C_{r3} and C_{r6} are open.

E. DESIGN OF CLAMPING CAPACITOR

The parameters of L_m, C_r, and T_d have already been designed in the previous subsections, so the parameter of the clamping capacitor can be calculated based on (25), as

$$C_c \ge \frac{2C_r I_{in}}{\frac{\sqrt{2}I_{rp}}{2\pi}\left(\cos\left(\frac{2\pi T_d}{T_{sw}} - \varphi\right) - \cos\varphi\right)} = 12.5\ \mu\text{F}. \quad (32)$$

On the other hand, C_c requires enough capacitance to satisfy the input filter characteristics. To prevent electromagnetic interference generated by the switching source from reaching the power line, the input filter should sufficiently attenuate the gain above the switching frequency, and the corner frequency of the input filter should be 1/10 of the switching frequency. The corner frequency of the input filter is described in (22). Thus, the other constraint can be derived as

$$C_c \ge \frac{3}{8\pi^2 L_r f_c^2} = 18.7\ \mu\text{F} \quad (33)$$

Considering these two constraints, the C_c was set to 20 μF in the prototype. Since C_c does not require a small tolerance, class-II ceramic capacitors with high permittivity were used. These capacitors suffer a capacitance degradation as the DC bias voltage increases, so the number of capacitors connected in parallel was designed to have the desired capacitance value at the rated voltage.

VI. EXPERIMENTAL RESULTS

We fabricated a prototype of the proposed converter and performed experiments to determine the validity of the comprehensive analysis and design theory. Fig. 14 shows a photograph of the prototype and Table 3 lists its specifications and circuit parameters. We used 650-V SiC MOSFETs, C3M0120065D, as the primary-side switches and 250-V OptiMOS^{TM}3 MOSFETs, IPP600N25N3G, as the secondary-side switches. Class-I C0G ceramic capacitors, CGA5L4C0G, were used as the resonant capacitors and class-II X7T ceramic capacitors, CGA9P4X7T, were used as the clamping capacitors. We connected 40 class-II ceramic capacitors in parallel to compensate for the capacitance degradation.

The steady-state measured waveforms of the main switches under 10% and full load conditions in the forward power flow are shown in Fig. 15 and those in the backward power flow

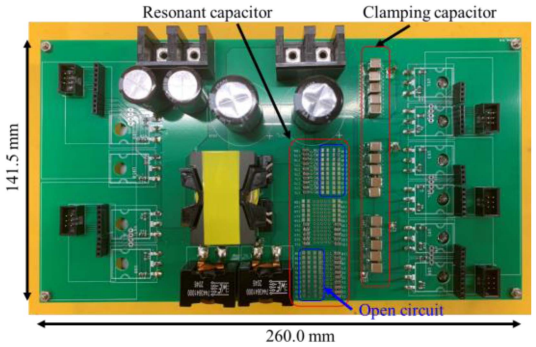

FIGURE 14. Prototype of proposed converter.

TABLE 3 Specifications and Electrical Parameters

Parameters	Quantity	
Rated power P	2 kW	
Input voltage V_i	900 V	
Output voltage V_o	150 V	
Switching frequency f_{sw}	132 kHz	
Resonant inductor L_{r1}, L_{r2}	10.8 µH, 10.8 µH (R_{Lr} = 103 mΩ (AC resistance))	
Resonant capacitor C_r	5 in parallel 8200 pF (CGA5L4C0G)	
Clamping capacitor C_c	40 in parallel 1.0 µF (CGA9P4X7T)	
Primary-side switch $Q_1 - Q_6$	SiC-MOSFET, C3M0120065D (V_{ds} = 650 V, $R_{ds(on)}$ = 120 mΩ, C_{oss} = 102 pF)	
Secondary-side switch $Q_7 - Q_{10}$	OptiMOS^{TM}3 MOSFET, IPP600N25N3G (V_{ds} = 250 V, $R_{ds(on)}$ = 60 mΩ, C_{oss} = 400 pF)	
Input capacitor C_{in}	2 in series 100 µF	
Output capacitor C_o	2 in parallel 47 µF (R_{Co} = 539 mΩ)	
Transformer 3C95 PQ 40/40	Turn number	7:7:7 (2 winding in parallel in sec. side)
	Magnetizing inductance L_m	48.5 µH
	Leakage inductance L_{k1}, L_{k2}, L_{k3}	1.35 µH, 1.07 µH, 0.167 µH
	Winding resistance R_{Tr1}, R_{Tr2}, R_{Tr3}	58 mΩ, 58 mΩ, 27 mΩ (AC resistance)

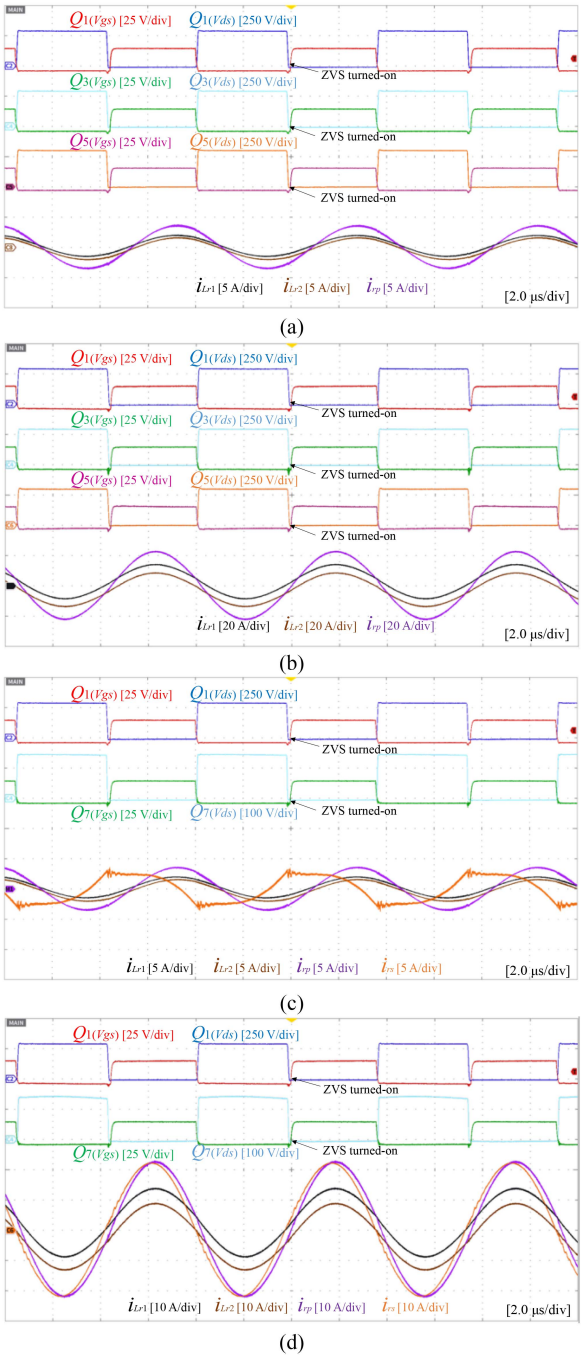

FIGURE 15. Steady-state measured waveforms of primary-side switches under (a) 10% load and (b) full-load conditions, and those of secondary-side switches under (c) 10% load and (d) full-load conditions in forward power flow.

in Fig. 16. The voltages through all the primary-side switches were clamped and each voltage stress was 300 V, which means automatic voltage sharing without additional circuits or controls could be achieved. In addition, all switches achieved ZVS operation independent of the load and power flow condition, thus demonstrating that load-independent soft-switching under bidirectional power flow could be achieved.

Fig. 17 shows the currents through the primary-side switches under the full load condition. As shown in the figure, the currents were well balanced not only in terms of RMS values but also instantaneous values. There was also no observation of inrush hard-charging current or ringing, which proves the validity of the design theory. These results demonstrate that the proposed converter can achieve automatic current sharing with the soft-charging operation.

Key waveforms of the ripple-canceling characteristics under the full load condition are shown in Fig. 18. As we can see here, the peak-to-peak current of i_{rp} was 43.4 $A_{p\text{-}p}$, and in contrast, that of the current through the input capacitor i_{Cin} was just 0.412 $A_{p\text{-}p}$. This indicates that the proposed converter significantly mitigated the input current ripple.

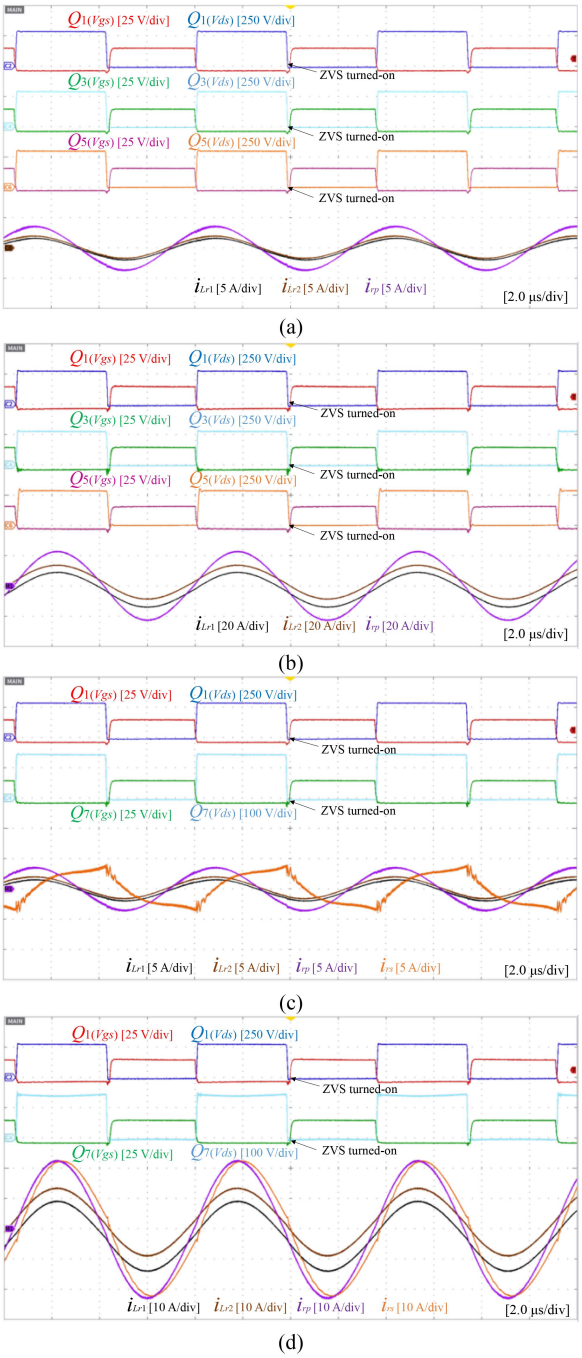

FIGURE 16. Steady-state measured waveforms of primary-side switches under (a) 10% load and (b) full-load conditions, and those of secondary-side switches under (c) 10% load and (d) full-load conditions in backward power flow.

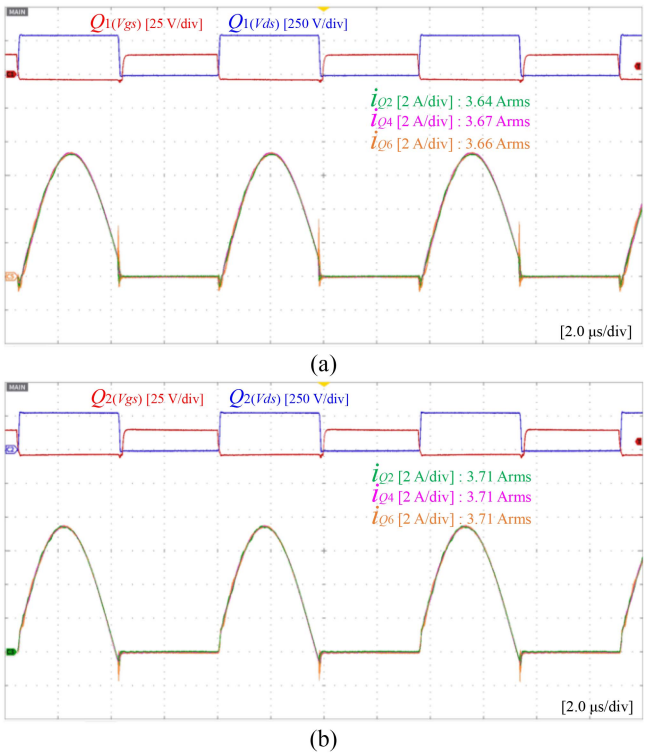

FIGURE 17. Currents through primary-side switches under full-load conditions in (a) forward power flow and (b) backward power flow.

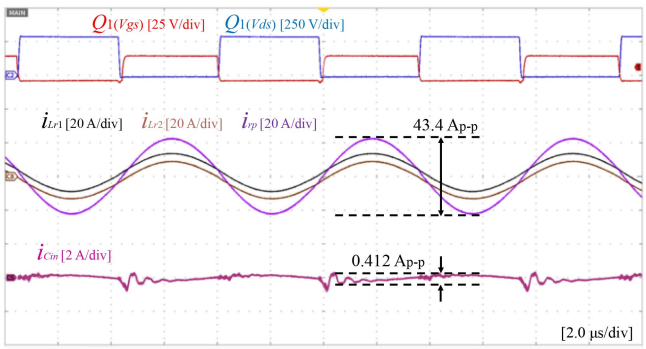

FIGURE 18. Key waveforms of ripple-canceling characteristics under full-load condition in forward power flow.

Fig. 19 shows a comparison of the transient response of the proposed converter with the proposed dynamic model, where the load step proceeds from 10% to full load. In subsection IV-C, we only considered the conduction loss on the primary side as dissipation loss for simplicity. However, total dissipation loss also includes the conduction loss on the secondary side, the copper loss of magnetic components, and the output capacitor DC-link equivalent series resistor (ESR) loss. Here, the input capacitor DC-link ESR loss can be ignored thanks to the ripple-cancel feature, so $R_{DC.tot}$ can be recalculated as

$$\begin{aligned} R_{DC.tot} &= \left(\frac{I_{rp}}{I_o}\right)^2 \cdot \left(\frac{R_{on.p}}{3} + 2R_{on.s} + \frac{R_{Lr} + R_{Tr.p}}{2} + R_{Tr.n}\right) \\ &\quad + \left(\left(\frac{I_{rp}}{I_o}\right)^2 - 1\right) R_{Co} \\ &= 393\text{m}\Omega \end{aligned} \tag{34}$$

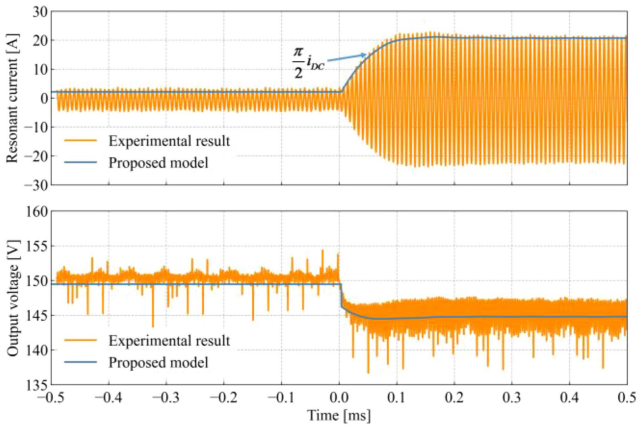

FIGURE 19. Transient response of proposed converter.

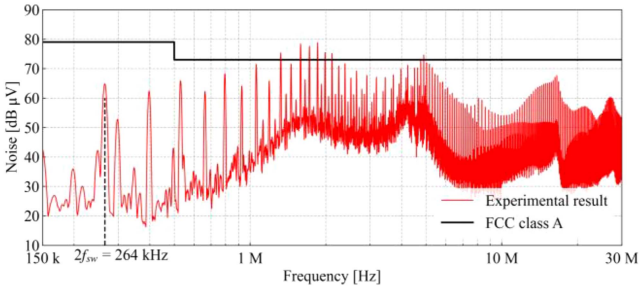

FIGURE 20. Conducted DM noise measurement result under full-load condition.

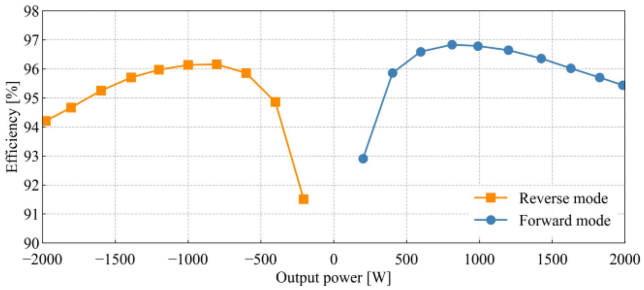

FIGURE 21. Measured efficiency of proposed converter.

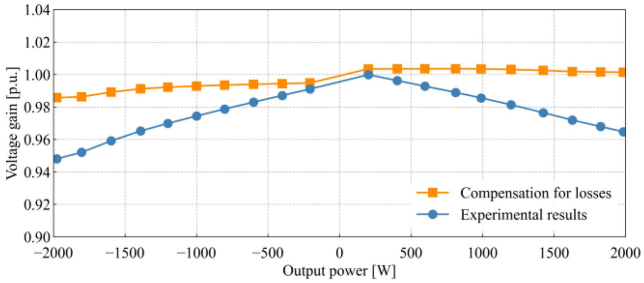

FIGURE 22. Voltage gains in accordance with output power.

where, $R_{on.p}$ and $R_{on.s}$ respectively denote the on-resistance of the primary-side switch and secondary-side switch, R_{Lr} is the ESR of the resonant inductor, and $R_{Tr.p}$ and $R_{Tr.n}$ respectively denote the winding resistance of the primary-side and secondary-side transformer winding. The $L_{DC.tot}$ can be calculated as 14.8 μH in accordance with the parameters listed in Table 3. As shown in the Fig. 19, the transient response of the proposed converter was good agreement with that of the proposed dynamic model under both steady and transient states, thus verifying the validity of the proposed dynamic model.

Fig. 20 shows the measured differential-mode (DM) noise spectrum of the proposed converter under full-load condition. Due to its configuration, the embedded filter is effective at suppressing DM noise but not at common-mode (CM) noise, so only the DM noise spectrum was measured. In the experimental system, a line impedance stabilization network was utilized to keep the line impedance constant at 50 Ω in the measured frequency band. To separate noise into DM and CM, power combiners, ZSCJ-2-2+ and ZAPDJ2-5W-521+, were used for measurements from 150 kHz to 5 MHz and from 5 MHz to 30 MHz, respectively. The output signals of the combiners had to be processed in the test receiver to produce the true DM voltage. First, the power combiners had specified insertion losses compensated in the receiver. Second, since the output signals of the combiners were twice as large as the true DM voltage in theory, the test receiver subtracted 6 dB μV from the received signals [50]. As shown in Fig. 20, the proposed converter met FCC class A regulations at twice the switching frequency with a margin of 14.2 dB μV. In addition, the proposed converter cleared the regulation in the frequency band up to the ninth harmonics. Although some frequency bands above the 10th harmonics exceeded the regulation, the DM filter can be downsized compared to the conventional converters because it satisfies the regulation at low harmonics where the DM noise is usually large. These results show that the embedded filter characteristics of the proposed converter have useful properties.

The measured efficiency of the proposed converter is shown in Fig. 21. The maximum efficiencies were 96.8% at 813 W and 96.2% at −802 W under the forward and backward power flows, respectively. Moreover, the proposed converter had an efficiency of over 90% under the whole load range in the bidirectional power flows since 1) it enables a wide-range both-side ZVS operation, as shown in Figs. 15 and 16, and 2) it achieves automatic current sharing, thus ensuring a good balance between the RMS currents of different switches and resulting in lower current stresses and conduction loss.

Fig. 22 shows the voltage gains corresponding to the output power, where we can see that these gains in the experiment were slightly smaller than the unity voltage gain. The difference between these two gains increased as the output power

TABLE 4 Topology Comparison

Topology		NPC three-level LLC [36]	SHB three-level LLC [38]	Ladder SCC hybrid LLC [39]	Ladder RSCC hybrid LLC [46]	Proposed converter
Input current ripple amplitude		Half of resonant current	Resonant current	Half of resonant current	Half of resonant current	Almost zero
Naturel voltage-sharing		No	No	Yes	Yes	Yes
Modulation complexity		Complex	Simple	Simple	Simple	Simple
Extensibility		Possible, but difficult	No	Possible, but no description	Yes	Yes
Suitability to high-power applications		Yes	Yes	No	Yes	Yes
Component counts (M : number of series half-bridge pairs ≥ 2)	Switch/diode	4/2	4	6	$2M$	$2M$
	*Inductor	L_r : 1	L_r : 1	L_r : 1	L_r : 1 L_{sc} : M-1	L_r : 2
	**Capacitor	C_r : 1 C_{DC} : 2	C_r : 1 C_{DC} : 2	C_r : 1 C_{DC} : 2 C_{sc} : 1	C_r : 1 C_{DC} : M C_{sc} : M-1	C_r : $2M$ C_{DC} : 1 C_{sc} : M
	Transformer	N : 1	N : 1	N : 1	N : 1	N : N : 1 : 1
Switch stress	Voltage stress	V_{in} / 2	V_{in} / 2	V_{in} / 2	V_{in} / M	V_{in} / M
	Current stress	I_{rp}	I_{rp}	***I_{rp}	I_{rp} / M	I_{rp} / M
Conversion gain		1 / 2N	1 / 2N	1 / 2N	1 / 2MN	1 / 2MN
Reported efficiency		94.7%	> 98%	97.3%	97%	96.7%
Output power		54 V/540 W	1050 V/15 kW	48 V/2 kW	48 V/1 kW	150 V/2 kW

* L_r is the resonant inductor and L_{sc} is the inductor in the switched capacitor network.
** C_r is the resonant capacitor, C_{DC} is the DC-link capacitor, and C_{sc} is the capacitor in the switched capacitor network.
*** The current stresses of the switches are different; here, the highest current stress is shown.

increased. Dissipation losses are mainly what caused this voltage drop. Using the dynamic model of the proposed converter, the DC output impedance can be calculated as $R_{DC.tot}$. The compensated voltage gains considering the dissipation losses are also plotted in Fig. 22. As shown in the figure, the voltage gains are almost constant and unity when ignoring dissipation losses under both power directions.

VII. TOPOLOGY COMPARISON

In this section, the proposed converter is compared with the conventional high-voltage LLCs from various aspects including ripple reduction, natural voltage-sharing, modulation complexity, extensibility, suitability to high-power applications, component counts, switch stresses, conversion gain, reported efficiency, and output power. The comparison is summarized in Table 4. The primary-side component counts and switch stress are targeted since the converters utilize general full-wave rectifiers on the secondary side.

As discussed in Section II, the proposed converter is superior to conventional topologies in terms of ripple reduction, automatic voltage-sharing, simple modulation, extensibility, and suitability to high-power applications. Further, it requires no additional inductors for the soft-charging operation even as the level increases, indicating greater robustness to the component tolerance compared to the ladder RSCC hybrid converter. Since all the compared converters have soft-switching capability, the conduction loss has a significant impact on the efficiency. Thus, the efficiency comparison was conducted in the same output current range for all converters and found that the proposed converter achieved the same level of high efficiency.

On the other hand, the proposed converter has the largest number of components among the converters when the same number of switches with the three-level converter is used. However, most of the components are resonant capacitors with a small capacitance, and the number of clamping capacitors is the same as that of the DC-link capacitor of the other three-level converters. Thus, the power density of the proposed converter as a PM will be about the same or slightly lower than those of the other three-level converters. In addition, as discussed in the Introduction, an increase in the number of modules significantly reduces the entire power density. To approximate this effect, we can use the modularization penalty, which is a highly simplified consideration [26]. From this, the entire power density of the SST consisting of the proposed 6-level converter can be higher than that of the three-level SHB converter unless the power density of the proposed converter is less than 1/1.4 of that of the SHB LLC converter, which has the fewest number of components. A detailed calculation is provided in Appendix B. In addition, the power density of the entire SST can be improved by further reducing the number of modules based on the extensibility of the proposed converter.

VIII. CONCLUSION

In this paper, we proposed a ripple-cancel multilevel converter to overcome the high current ripples and high voltage stress of PMs. In contrast to SCC-based hybrid converters, which generally have to deal with an inrush hard-charging current, the proposed converter achieves soft-charging operation without additional inductors. Further, since it consists of a ripple-cancel LLC and Dickson RSCCs, our proposed converter

inherits the advantageous characteristics of these converters, namely, load-independent soft switching, automatic voltage sharing, reduction of the current ripple, an embedded filter function, constant voltage gain, and flexible extensibility. The proposed converter also enables automatic current sharing due to the symmetric circuit configuration, which results in low current stress and conduction loss. We analyzed these characteristics and the conditions for the soft-charging operation in detail and presented a passive compensation scheme for the soft-charging operation and a design methodology on the basis of the analyses. Our experimental results demonstrate the validity of the proposed converter and show that it is an attractive candidate for use as the PM of SST.

APPENDIX

A. DERIVATION OF THE FLYING CAPACITORS' CONSTRAINTS

Capacitor voltage mismatch causes an inrush hard-charging current during operating mode transition, so there is a risk of this occurring in internal flying capacitor networks. The proposed converter features two such loops in each half-cycle. In the positive half-cycle, $C_{r1} - C_{r2} - C_{C1}$ and $C_{r2} - C_{r3} - C_{C2}$ constitute such loops, and in the negative half-cycle, $C_{r1} - C_{r2} - C_{C2}$ and $C_{r2} - C_{r3} - C_{C3}$ constitute such loops. Note that although other flying capacitor networks can be selected in both half-cycles, the same constraint is obtained from KVL (e.g., $C_{r5} - C_{r6} - C_{C1}$ in the positive half-cycle is the same constraint as $C_{r1} - C_{r2} - C_{C1}$). To prevent voltage mismatching, KVL in each cycle must hold continuously at the switching transition, i.e., KVL for the amount of voltage increase in each cycle must be satisfied simultaneously. Under the positive half-cycle with the soft-charging operation, KVL yields

$$\begin{cases} -v_{Cr1} + v_{Cr2} - v_{Cc1} = 0 \\ -v_{Cr2} + v_{Cr3} - v_{Cc2} = 0 \end{cases}. \tag{A.1}$$

Thus, a similar relationship holds for the amount of voltage increase within the positive half-cycle.

$$\begin{cases} -\Delta v_{Cr1.p} + \Delta v_{Cr2.p} - \Delta v_{Cc1.p} = 0 \\ -\Delta v_{Cr2.p} + \Delta v_{Cr3.p} - \Delta v_{Cc2.p} = 0 \end{cases} \tag{A.2}$$

Similarly, the relationship in the negative half-cycle can be represented as

$$\begin{cases} -\Delta v_{Cr1.n} + \Delta v_{Cr2.n} - \Delta v_{Cc2.n} = 0 \\ -\Delta v_{Cr2.n} + \Delta v_{Cr3.n} - \Delta v_{Cc3.n} = 0 \end{cases}. \tag{A.3}$$

Due to the charge balance of capacitors in the steady state,

$$\begin{cases} \Delta v_{Cri.p} + \Delta v_{Cri.n} = 0 \\ \Delta v_{Cci.p} + \Delta v_{Cci.n} = 0 \end{cases} (i = 1, 2, 3). \tag{A.4}$$

From (A.2) to (A.4), the constraints of the amount of voltage increase for the soft-charging operation are derived.

$$\begin{cases} \Delta v_{Cr1.p(n)} = \Delta v_{Cr2.p(n)} = \Delta v_{Cr3.p(n)} \\ \Delta v_{Cc1.p(n)} = \Delta v_{Cc2.p(n)} = \Delta v_{Cc3.p(n)} \end{cases}. \tag{A.5}$$

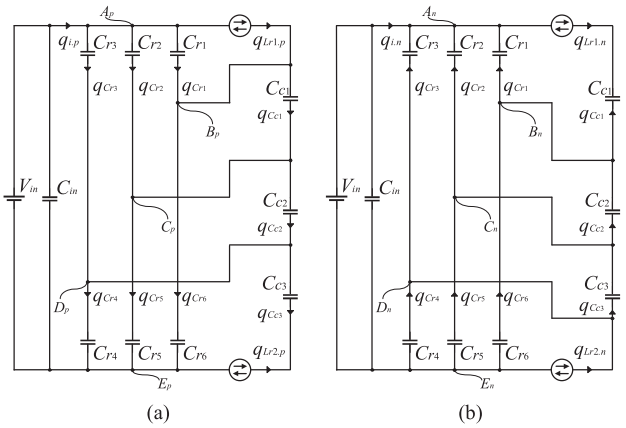

FIGURE 23. Charge flows of proposed converter with (a) odd-numbered and (b) even-numbered switches on.

Charge vector analysis is performed to identify the constraints of the capacitor. Fig. 23 shows the charge flow of the proposed converter, where the inductors and transformers are modeled as current sources. During the positive half-cycle (cf. Fig. 23(a)), KCLs at nodes $A_p - E_p$ yield the following set of equations:

$$\begin{cases} q_{i.p} - q_{Cr1} - q_{Cr2} - q_{Cr3} - q_{Lr1.p} = 0 \\ q_{Cr1} + q_{Lr1.p} - q_{Cc1} - q_{Cr6} = 0 \\ q_{Cc1} + q_{Cr2} - q_{Cc2} - q_{Cr5} = 0 \\ q_{Cc2} + q_{Cr3} - q_{Cc3} - q_{Cr4} = 0 \\ -q_{i.p} + q_{Cr4} + q_{Cr5} + q_{Cr6} - q_{Lr2.p} = 0 \end{cases}. \tag{A.6}$$

During the negative half-cycle (cf. Fig. 23(b)), KCLs at nodes $A_n - E_n$ yield the following set of equations:

$$\begin{cases} q_{i.n} + q_{Cr1} + q_{Cr2} + q_{Cr3} - q_{Lr1.n} = 0 \\ -q_{Cr1} - q_{Cc1} + q_{Cc2} + q_{Cr6} = 0 \\ -q_{Cr2} - q_{Cc2} + q_{Cc3} + q_{Cr5} = 0 \\ -q_{Cr3} - q_{Cc3} + q_{Cr4} + q_{Lr2.n} = 0 \\ -q_{i.n} - q_{Cr4} - q_{Cr5} - q_{Cr6} - q_{Lr2.n} = 0 \end{cases}. \tag{A.7}$$

The charges delivered from the input voltage and each resonant inductor are represented as

$$\begin{cases} q_{i.p} + q_{i.n} = I_{in} T_{sw} \\ q_{Lr1.p} = \frac{I_{in} T_{sw}}{2} + \frac{L_{r2}}{L_{r1}+L_{r2}} \frac{I_o T_{sw}}{2} = \frac{I_{in} T_{sw}}{2} \left(1 + \frac{6L_{r2}}{L_{r1}+L_{r2}}\right) \\ q_{Lr1.n} = \frac{I_{in} T_{sw}}{2} - \frac{L_{r2}}{L_{r1}+L_{r2}} \frac{I_o T_{sw}}{2} = \frac{I_{in} T_{sw}}{2} \left(1 - \frac{6L_{r2}}{L_{r1}+L_{r2}}\right) \\ q_{Lr2.p} = -\frac{I_{in} T_{sw}}{2} + \frac{L_{r1}}{L_{r1}+L_{r2}} \frac{I_o T_{sw}}{2} = \frac{I_{in} T_{sw}}{2} \left(-1 + \frac{6L_{r1}}{L_{r1}+L_{r2}}\right) \\ q_{Lr2.n} = -\frac{I_{in} T_{sw}}{2} - \frac{L_{r1}}{L_{r1}+L_{r2}} \frac{I_o T_{sw}}{2} = \frac{I_{in} T_{sw}}{2} \left(-1 + \frac{6L_{r1}}{L_{r1}+L_{r2}}\right) \end{cases}. \tag{A.8}$$

Here, the charge delivered from the resonant inductor consists of a DC bias current and resonant currents through each resonant inductor. Since the resonant current is distributed in accordance with the admittance of the resonant inductance,

the charge is also distributed corresponding to the admittance. From (A.6) to (A.8), the charges through the switches are derived as

$$q_{Q1} = q_{Q2} = q_{Q3} = q_{Q4} = q_{Q5} = q_{Q6} = I_{in}T_{sw}. \quad \text{(A.9)}$$

In other words, (A.9) indicates that the charge flowing through each resonant capacitor leg is the same. Hence, the constraints for the resonant capacitors are derived from (A.5) and (A.9) as follows.

$$C_{r1} + C_{r6} = C_{r2} + C_{r5} = C_{r3} + C_{r4} = 2C_r. \quad \text{(A.10)}$$

As for the charges through the clamping capacitors, they are derived from (A.6) to (A.8).

$$\begin{cases} q_{Cc1} = \frac{I_{in}T_{sw}}{2}\left(\frac{6L_{r2}}{L_{r1}+L_{r2}} - 1\right) \\ q_{Cc2} = \frac{I_{in}T_{sw}}{2}\left(\frac{6L_{r2}}{L_{r1}+L_{r2}} - 3\right) = q_{Cc1} - I_{in}T_{sw} \\ q_{Cc3} = \frac{I_{in}T_{sw}}{2}\left(\frac{6L_{r2}}{L_{r1}+L_{r2}} - 5\right) = q_{Cc2} - I_{in}T_{sw} \end{cases} \quad \text{(A.11)}$$
$$\Leftrightarrow q_{Cc1} \neq q_{Cc2} \neq q_{Cc3}$$

Therefore, the constraints for voltages across clamping capacitors in (A.5) cannot be satisfied. To mitigate the hard-charging inrush current, the constraints for the clamping capacitors are derived from (A.5) and (A.11).

$$C_{Cc1} = \infty, C_{Cc2} = \infty, C_{Cc3} = \infty \quad \text{(A.12)}$$

B. MODULARIZATION PENALTY

The modularization penalty is a concept indicating that modularization reduces the power density of the entire system below the module's power density due to additional isolations and overheads. For simplicity, the power P here is processed in a sphere with a radius R_0. The volume of the entire system can be denoted as follows with the number of modules X.

$$V(X) = \frac{4}{3}\pi\left(\frac{R_0}{X^{1/3}} + d_{iso}\right)^3 \cdot X \quad \text{(B.1)}$$

Here, d_{iso} refers to the additional isolations and overhead distance. As an example, the system in [27] consists of 27 modules composed of diode-clamped NPC AC-DC converters and SHB LLCs. In this case, the entire power density decreases by about 1/10 of the module's power density. Therefore, d_{iso} can be calculated as 1.37 R_0 in this case. By utilizing the proposed 6-level converter, the number of modules can be reduced to 2/3 according to the voltage stress of the switch in Table 4, and the power density reduction improves from about 1/10 to about 1/7. Although each module includes an AC-DC converter, it can be assumed to be negligible for simplicity because it consists of only switches and diodes. In such a case, the entire SST consisting of the proposed converters may have a higher power density than that consisting of the SHB LLCs unless the power density of the proposed converter is less than 1/1.4 of that of the SHB LLC. Note that although the proposed 6-level converter has 1.5 times as many components per module as the SHB LLC in terms of clamping capacitors and switches, the power density will not be significantly reduced compared to SHB LLC because the power rating is also 1.5 times higher due to the reduction of the number of modules.

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SHOTA OKUTANI (Graduate Student Member, IEEE) was born in Kyoto, Japan, in 1995. He received the B.S. and M.S. degrees in electrical engineering in 2018, and 2020, respectively, from the Kyoto Institute of Technology, Kyoto, Japan, where he is currently working toward the Ph.D. degree. His research interests include modeling and control of DC-DC converters, high-power-density DC-DC converters, switched-capacitor converters, and high voltage DC-DC converters.

RYO NISHIYAMA (Graduate Student Member, IEEE) was born in Osaka, Japan, in 1997. He received the B.S. degree in electrical engineering in 2021 from the Kyoto Institute of Technology, Kyoto, Japan, where he is currently working toward the M.S. degree. His research interests include resonant converters and high-power-density DC-DC converters.

PIN-YU HUANG (Member, IEEE) was born in Taipei, Taiwan, in 1985. He received the M.S. and Ph.D. degrees in electrical engineering from the National Taiwan University of Science and Technology, Taipei, Taiwan, in 2011 and 2015, respectively. In 2013, he was a Visiting Scholar with the Center for Power Electronics, Virginia Polytechnic Institute and State University, Blacksburg, VA, USA. From 2015 to 2018, he was a Postdoctoral Researcher with Power Electronic Laboratory, Tokyo Metropolitan University, Hachioji, Japan. Since 2018, he has been an Assistant Professor with the Kyoto Institute of Technology, Kyoto, Japan. His research interests include voltage multipliers, high-power-density DC-DC converter design, multi-level converters, measurement techniques for the passive component characteristics of capacitors and inductors, and 3-port power routers for the renewable energy DC microgrid.

YUICHI KADO (Member, IEEE) received the M.S. and Ph.D. degrees in electronics from Tohoku University, Miyagi, Japan, in 1983 and 1998, respectively. In 1983, he joined the Electrical Communication Laboratories, Nippon Telegraph and Telephone Public Corporation (now NTT), Tokyo, Japan, where he was engaged in research on SOI structure formation by hetero-epitaxial growth. From 1989 to 1998, he worked on the development of fully depleted CMOS/SIMOX LSIs and ultra-low-power CMOS circuits. From 1999, he was engaged in R&D on compact network appliances using ultra-low-power CMOS circuit technologies for ubiquitous communications. He led research and development projects on ultra-low-power network appliances, sub-terahertz-wave wireless communication, and intra-body communication as the Director of the Smart Devices Laboratory, NTT Microsystem Integration Laboratories during 2003–2010. In July 2010, he joined the Department of Electronics, Kyoto Institute of Technology, Kyoto, Japan. His research focuses on multi-port power routers to build energy interchanging systems.