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A High Current High Power Density Motor Drive for a 48-Volt Belt-Driven Starter Generator (BSG) System

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ABSTRACT A 48 V Belt-Driven Starter Generator (BSG) System is featured with high output current, high starting torque, and highly efficient thermal management. This paper firstly elaborates hardware design considerations of a high power density three-phase BSG inverter to address the challenges of even current distribution among paralleled MOSFETs, small drain-source voltage spike and good thermal dissipation. In order to satisfy the high-current requirement, a careful selection of MOSFET device with high-current rating and low on-resistance has been presented. In order to suppress circulating current among paralleled devices, individual gate resistors have been placed in the gate loop of each MOSFET. In order to provide good thermal dissipation, an Insulated Metal Substrate (IMS) board and single-layer layout technique have been implemented. Multiple low-profile electrolytic capacitors are used to increase the power density of the prototype. Moreover, the use of automotive gate driver IC TLE9180 and microcontroller TC1782 makes the prototype more readily accepted by industry. An improved Interior Permanent Magnet (IPM) motor control strategy and a pump-back system based on a virtual machine concept have been implemented to facilitate the validation of the prototype under rated condition without using a real motor. The control algorithm automatically adjusts the onset of field-weakening by using an additional inverter voltage loop and takes into account the nonlinearity of the stator flux linkage by using curve fitting technique, which makes the motor drive adaptive to machine parameter changes as well as DC bus voltage fluctuation. A three-phase BSG inverter prototype with a peak power of 12 kW has been built and tested. The prototype power density has reached 20.3 kW/L. Both PLECS simulations and hardware experiments show a continuous and stable operation with up to 200 A phase current and up to 600 Hz output frequency.

INDEX TERMS BSG inverter, high power density, current sharing, paralleled MOSFETs, IPM control strategy, pump-back system.

I. INTRODUCTION

The 48 V Belt-Driven Starter Generator (BSG) system has been developed for cost-efficient mass hybridization. Its capability of advanced stop-start, coasting and electric boost can help reduce CO_2 emission by up to 10%. For a mild-hybrid application, the 12 V alternator is replaced by the 48 V electric motor which is directly mounted to the engine via a belt [1]. Interior Permanent Magnet Synchronous Machines (IPMSMs) are commonly used in this BSG system due to their high efficiency, high power density, wide speed range operation, and maintenance-free characteristics [2] [3].

Inverter is an essential component which needs to be compactly integrated with the BSG motor. A typical topology of a 48 V BSG inverter is shown in Fig. 1. The power supply is 48 V DC. The peak power can go up to 12 kW and last for several seconds. The peak output current can be up to 300 A. The challenge on the hardware design is to achieve 3 key targets which are well-balanced current among paralleled MOSFETs,

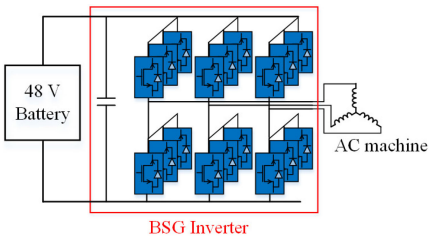

FIGURE 1. **Circuit configuration of a 48 V BSG inverter.**

low drain-source voltage (V_{ds}) spike during turn-off transient, and small thermal resistance of the heatsink system [4]. Most of the existing literature focus on the switching characteristics of the BSG power stage. [5] presents a design and measurement of an integrated H-bridge and a compact DC/DC converter for a commercial 48 V BSG system . [6] presents a BSG inverter prototype with 6 MOSFETs connected in parallel in each arm and [7] uses 8 devices instead. Individual gate resistor for each MOSFET is used in both papers to suppress circulating current among paralleled switches and to reduce the drain-source voltage overshoot in high-current operating conditions. Thermal behavior of the inverter is also included in [6] showing that individual gate resistor helps even current sharing. However, [6] and [7] only show switching waveforms of the MOSFETs, and no inverter operation waveforms are provided. [4] illustrates a design of 48 V BSG inverter using 4 MOSFETs in parallel in each inverter arm. Besides individual gate resistors, an Insulated Metal Substrate (IMS) board has been used to provide smaller temperature difference among paralleled devices compared with [6]. However, the power density of the prototype has been compromised due to the height of the DC link capacitors and no operational waveforms are provided.

In order to test the BSG inverter hardware, a simple and robust IPM control strategy should be implemented in the controller. The control algorithm should be able to achieve stable and robust field-weakening operation [8]–[10]. [11]–[13] adopts an additional DC/DC boost converter to raise the DC bus voltage so that the operating speed can be expanded. However, the additional switches and passive components lower down the power density of the inverter. In terms of current controllers, [14] directly uses equations to compute d-axis and q-axis current commands and [15] proposes to use one current regulator to decouple the two current components. [16]–[18] utilizes either phase current error or inverter voltage error to determine the amount of demagnetizing current in d-axis. However, the methods in [14]–[18] fails to take into account the nonlinearity of the stator flux linkage, which can lead to unstable operation of the controllers. The nonlinear effect can be accommodated by inserting look-up tables [19] and by using curve fitting equations based on Finite Element Analysis (FEA) results of a physical IPM machine [20]–[23]. However, these methods are not adaptive to machine parameter changes and DC bus voltage variation since the look-up tables and the curve fitting equations cannot be tuned online.

The research gaps have been identified and the main contributions of this paper are illustrated from the following aspects. Firstly, this paper provides the readers with not only a complete design guideline of a 48V BSG inverter but also an economical and feasible approach to test the designed prototype under rated operating conditions without using a real machine, which is missing in the existing literature. Secondly, improvements have been made in terms of both hardware design and IPM control strategy in order to make the prototype more reliable and robust so that it can be more readily accepted by industry. From hardware perspective, this paper elaborates the hardware design considerations of a low-voltage high-current high power density three-phase 48V BSG inverter to address the challenges of even current distribution among paralleled MOSFETs, small drain-source voltage spike and good thermal dissipation. Appropriate device selection in order to satisfy the high-current requirement in such applications is missing in the existing literature. As a result, an iterative method for selecting MOSFET with an ultra-low on-state resistance (R_{dson}) has been presented. The power density of the BSG inverters in the previous literature has been compromised due to the large size of the DC link capacitors. In the proposed design, multiple low-profile electrolytic capacitors have been used so that the power density of the prototype has been increased. Moreover, none of the previously published papers covers the topic of gate driver and microcontroller ICs which are compliant with automotive standard and specialized for electric vehicle applications. In the proposed prototype, the gate driver ICs TLE9180 and the microcontroller TC1782 which are specifically designed for electric vehicles have been implemented. From the aspect of IPM control strategy, an improved IPM control strategy and a pump-back system have been implemented, which facilitates the validation of the designed inverter hardware under rated conditions without using a real motor. The control algorithm automatically adjusts the onset of field-weakening by using an additional inverter voltage loop, which makes it adaptive to machine parameter changes and DC bus voltage fluctuation. At the same time, the nonlinearity of the stator flux linkage has been taken into consideration by using curve fitting equations so that the control accuracy is improved. In addition, the improved control scheme is suitable for both speed control and torque control. A three-phase BSG inverter prototype with a peak power of 12 kW has been built based on current industrial requirements, and the prototype power density has reached 20.3 kW/L.

The rest of the paper is organized as follows. A detailed hardware design procedure for a 48 V BSG inverter is firstly presented in Section II including device selection, device paralleling, DC link capacitor selection, IMS board and heatsink selection, and an introduction to automotive standard gate driver ICs and microcontrollers for this application. Section III shows a brief operation analysis of an IPM machine and an optimized operation curve which not only simplifies the control but also keeps a relatively large output torque. A constant current based control method is implemented in Section IV. In order to test the performance of the designed

TABLE I Key Parameters for a 48 V BSG System and the Final Prototype Design Specification

System requirements	
Structure	Integrated motor and inverter
Dimension	≤ D155 mm*L180 mm
Mass	≤ 10.5 kg
Continuous torque	10 Nm
Continuous power	5 kW
Peak torque	≥ 20 Nm, @0~1500 rpm, 2 s
Peak motor power	≥ 8 kW@48 V, lasting 10 s
Peak generator power	≥ 10 kW@48 V, lasting 10 s
Maximum mechanic speed	12000 rpm
Efficiency	≥ 83%, measured at 25 °C
Operation temperature	– 40 ~ 100 °C
Cooling	Air cooling
Specifications of the final design	
DC bus voltage	36 V ~ 52 V (rated @ 48 V)
Continuous phase current	200 A_{peak}
Peak phase current	300 A_{peak}
Switching frequency	12 kHz
dv/dt	< 1 V/ns
Efficiency of the inverter	98.5%
Power density of inverter	20.3 kW/L

inverter hardware and the improved control method, a pump-back test bench is introduced in Section V based on a virtual machine concept. PLECS simulations and hardware experiments are presented in Section VI and VII, respectively, to show not only the continuous operation of the prototype but also the robustness of the improved control technique under machine parameter changes and DC bus voltage variation.

II. HARDWARE DESIGN CONSIDERATIONS

The three challenges for the inverter hardware design are current sharing among paralleled devices, V_{ds} spike suppression at 300 A_{peak} current, and thermal management under 100 °C environment temperature. In addition, the high motor speed (600 Hz) at limited switching frequency (12 kHz) and high efficiency target also superimpose challenges to the inverter design. A three-phase motor drive inverter prototype with a peak power of 12 kW has been constructed in the lab for an industry-funded project. The system requirements and the specifications of the final design are presented in Table I.

A. POWER DEVICE SELECTION

The power device selection includes four aspects which are drain-source voltage rating, drain current rating, on-state resistance, and device package.

1) DEVICE VOLTAGE RATING SELECTION

The avalanche breakdown voltage of an Infineon OptiMOS transistor is slightly higher than its voltage rating due to a typical safety margin. The voltage rating is defined at room temperature. Breakdown voltage shows a strong positive temperature coefficient in Fig. 2(a). Breakdown voltage at typical operation temperature of 100 ~ 120 °C is approximately 7% higher than its rated voltage. Another criterion for selecting the voltage rating of a MOSFET is the voltage spike. During

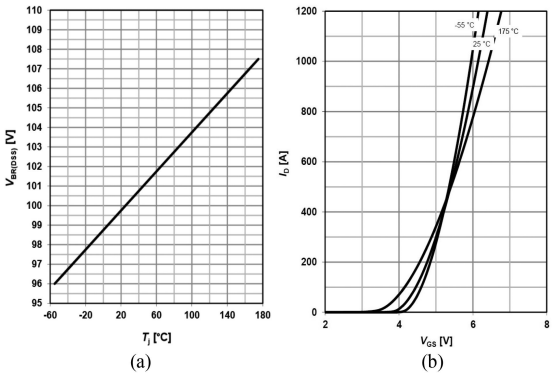

FIGURE 2. Characteristic curves of Infineon MOSFET IAUT300N10S5N015: (a) Breakdown voltage as a function of junction temperature: $V_{DS}=f(T_j)$ and (b) Drain current as a function of gate-source voltage under different temperatures: $I_D=f(V_{gs})$ [24].

turn-off transient, the voltage across drain and source can reach a much higher value than that in steady state due to parasitic inductance in the circuit. The maximum steady state voltage during turn-off should not exceed 70% to 90% of the rated voltage. In this project, a maximum junction temperature of 150 °C is considered for voltage rating deviation, and a 50% voltage spike is assumed based on possible *dv/dt*. Finally, a 100 V device is selected in this design.

2) OPERATING JUNCTION TEMPERATURE SELECTION

Similar reliability rules can be applied to the selection of operating junction temperature of the MOSFET. The operating junction temperature should not exceed the maximum value specified in the datasheet. Pushing the operating temperature to its maximum is not reasonable. In order to achieve high forecasted reliability, the operating temperature should be lower than the maximum value. For example, reducing the junction temperature by 30% will improve the Mean Time Between Failure of the OptiMOS by an order of magnitude. On the other hand, the R_{dson} increases with junction temperature. It leads to an increase in conduction power loss. For these reasons, a derating factor between 70% and 90% of the maximum junction temperature is used. In this design example, the maximum temperature of the device is 175 °C, and 85% of the maximum temperature, which is 150 °C, has been chosen as the operating temperature. The highest environment temperature is 100 °C, which means the maximum allowable device temperature rise is 50 °C. It is found in the experiments that the temperature rise is only around 20 °C. Therefore, the current and voltage rating selected based on 150 °C is enough for continuous operation of the inverter.

3) DEVICE CURRENT RATING SELECTION

In the high-current applications, the MOSFET is not being stressed up to its maximum current rating due to poor cooling conditions. Designer prefers to take advantage of low R_{dson} of the MOSFET in order to reduce power loss. Usually, a

MOSFET with selected low R_{dson} has a higher current rating than needed in the application. Nevertheless, it is useful to check the Safe Operating Area of the selected MOSFET. On the other hand, gate-source voltage (V_{gs}) should be high enough to completely turn on the MOSFET. The transistor should be able to carry the maximum pulse current in the converter under all conditions. Especially during start-up or short circuit, the supply voltage for the control IC can fall close to under voltage lockout limit. Some modern control ICs have an under voltage lock out of approximately 7 V. The gate-source voltage of MOSFET can be less than 5 V, if we consider the voltage drop on the output stage of the IC. MOSFET should be able to carry the required current without an increase of drain-source voltage at a given gate-source voltage. In this design, the transfer characteristic from the datasheet (Fig. 2(b)) can be used to verify device current capability when V_{gs} becomes low. If the MOSFET does not meet the requirements, another transistor with higher current rating should be selected.

4) R_{DSON} SELECTION

The most complicated task is to choose a device with the correct R_{dson}. The selection of R_{dson} is based on the maximum allowable power dissipation of a particular application and the maximum junction temperature of the MOSFET. Here it is assumed that the switching frequency is fixed and that the space for heat sink is known which means we can estimate the thermal resistance of the heat sink (R_{sink}).

Step 1: Calculate how much power loss is allowed for a given heat sink and a specific junction temperature based on the efficiency target.

Step 2: Calculate the required R_{dson} satisfying the maximum power loss from Step 1. At this point we already know the value of the maximum allowable power dissipation. We also know the circuit topology and the drain current waveform. Therefore, we can calculate the value of R_{dson} which satisfies the maximum power loss. For the first iteration we will consider only conduction loss because we do not know the MOSFET type yet. The switching loss strongly depends on the specific MOSFET device. For this reason, the switching loss will be skipped for now and be checked in the following steps.

Step 3: Select an OptiMOS with pre-calculated R_{dson} in Step 2. Note that instead of using room temperature, the junction temperature which is specific for a particular design (usually between 110 °C and 120 °C) should be used.

Step 4: Calculate the total power loss for the selected OptiMOS transistor in Step 3. Now we have enough information to calculate the total power loss for the selected OptiMOS transistor under particular operating condition. Since we know the exact transistor type, we will be able to calculate the switching loss for a given switching frequency.

Step 5: Recalculate the maximum power dissipation for the selected OptiMOS. With the junction to case thermal resistance of the selected OptiMOS device, it is possible to make the calculation of maximum allowable power dissipation more precisely. This step can help to skip one of the iterations that will be explained in Step 6.

Step 6: Compare the total power loss calculated in Step 4 for the selected OptiMOS with the maximum allowable power dissipation from Step 5. If the total power loss from Step 4 is lower than the maximum allowable power dissipation from Step 5, then the selected OptiMOS meets the requirements. In case that the total power loss from Step 4 is higher than the maximum allowable power dissipation from Step 5, select a new device from the OptiMOS family with a lower R_{dson}. Then repeat Steps 4, 5 and 6. Another possible approach would be to adjust the heat sink. To speed up the iteration process, the drain current versus the switching frequency chart, as well as output power versus the switching frequency chart can be used as a pre-selection of the MOSFET type.

Particularly in this project, for Step 1, the designed junction temperature is 150 °C, and the maximum environment temperature is 100 °C. Since the system efficiency target is 98.5% and the power under continuous operation is 5 kW, the allowable system power loss is around 75 W in the worst case. The heatsink needs to have a super low thermal resistance to dissipate this high amount of power loss. Therefore, an IMS board is used instead of a normal PCB board. For Step 2, when calculating the conduction loss, R_{dson} should be considered as a function of junction temperature. When calculating the switching loss, both E_{on} and E_{off} strongly depend on the value of the drain current. E_{on} is dominated by the commutated diode instead of the MOSFET. The relationship between E_{on}, E_{off}, and the drain current can be represented as a polynomial function using curve-fitting technique. The switching energy is also a function of gate resistor. The recharging speed of OptiMOS capacitance can be controlled by a gate resistor. It influences the switching time and correspondingly the switching loss. The E_{on}/E_{off} versus gate resistor curves are almost linear. Therefore, if the gate resistor used in the hardware is different from the value on the datasheet where E_{on} and E_{off} are claimed, a bias plus a corrective factor needs to be applied. The drain-source voltage also has an effect on the device switching behavior. The dependence of switching loss on the drain-source voltage is almost linear. In our case, when the DC link voltage varies, a bias plus a corrective factor needs to be applied to E_{on} and E_{off}.

After the six-step iteration, the Infineon Automotive OptiMOS transistor IAUT300N10S5N015 has been selected as shown in Table II. Three devices are connected in parallel to undertake a continuous current of 200 A and a peak current of 300 A at the designed junction temperature of 150 °C. This device is featured with ultra-low R_{dson}, which is good

TABLE II Infineon Automotive OptiMOS Transistors

Device Part NO.	V_{DS}	$R_{dson,MAX}$	$I_{D,nom}$	Operating Temp
IAUT240N08S5N019	80 V	1.9 mΩ	240 A	-55 ~ 175 °C
IAUT300N08S5N014	80 V	1.4 mΩ	300 A	-55 ~ 175 °C
IAUT300N08S5N012	80 V	1.2 mΩ	300 A	-55 ~ 175 °C
IAUT165N10S5N035	100 V	3.5 mΩ	165 A	-55 ~ 175 °C
IAUT300N10S5N015	***100 V***	***1.5 mΩ***	***300 A***	***-55 ~ 175 °C***

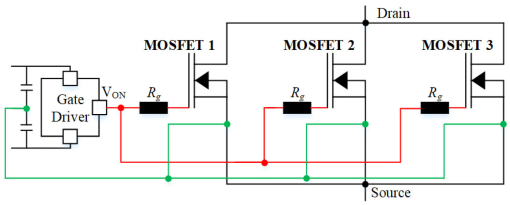

FIGURE 3. Gate driver output circuitry for three paralleled MOSFETs in the same arm.

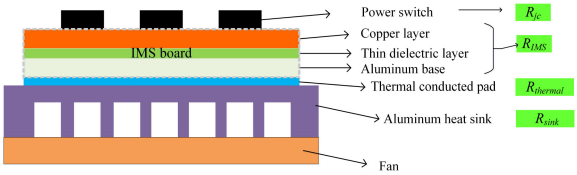

FIGURE 4. Structure of the proposed IMS board.

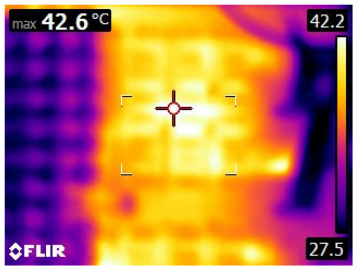

FIGURE 5. Thermal image of the MOSFETs in continuous operation.

TABLE III Comparison Between Panasonic and Chemi-Con Electrolytic Capacitors

Manufacturer	Panasonic	Chemi-Con
Product	EEHZC1K470P	EGPD101E621MM30H
Capacitance	47 μF	620 μF
RMS current of the cap	1.3 A	3.2 A
Number of caps needed	55	23
Volume of each cap	0.8 cm^3	7.63 cm^3
Total volume of capacitor	44 cm^3	175.5 cm^3
Footprint of capacitors	43.2 cm^2	46.2 cm^2

TABLE IV Comparison Between IMS Board and Standard FR4 PCB

	IMS board	Standard PCB
Thermal conductivity	4.1 W/mk	0.35 W/mk
Dielectric strength	80 kV/mm	20 kV/mm

for lowering the device loss in high-current condition, and at the same time, reducing the temperature rise. The maximum operating voltage for this BSG application is 52 V. But twice the voltage has been selected for the device to overcome the high frequency resonance ripple on V_{ds} caused by *dv/dt* and large current. A gate driver voltage of 12 V is selected.

B. PARALLELING OPTIMOS TRANSISTORS

The major challenge for paralleling OptiMOS transistors is the static and dynamic unbalance in current sharing. The second challenge is the destructive high-frequency oscillation. The first problem is due to the asymmetry of R_{dson} or the difference in the gate voltages. The second problem is due to slight imbalance in gate thresholds or circuit parasitic [25]. Because the parasitic determines the high frequency current flow. For static and dynamic current sharing, matched R_{dson}, perfectly symmetrical circuit layout, and matched gate thresholds are essential. In addition, some strategies can be applied to mitigate the unbalance or oscillation effect.

Fig. 3 shows the gate driver output circuitry for paralleled OptiMOSs in each arm. All the gates of the paralleled devices are driven by a single gate driver IC, and each OptiMOS has its own gate resistor. Large gate resistors are chosen to suppress potential circulating current in different gate loops. The gate resistor selection is also constrained by the required *dv/dt* and the maximum switching loss. Fortunately, the requirement of *dv/dt* in this application is below 1 V/ns. And the switching loss is low as well due to the low DC voltage. Thus, a 15 Ω gate resistor can be selected. As shown in Fig. 5, the currents are well balanced so that the temperature difference among the paralleled devices is within 2 °C.

C. DC LINK CAPACITOR SELECTION

55 Aluminum Electrolytic Capacitors manufactured by Panasonic (Part No. EEHZC1K470P) are connected in parallel to construct the entire DC bus. Each capacitor is 47 μF and rated at 80 V. The power density of the prototype has been greatly improved compared with [4] which uses Chemi-Con capacitors for the DC bus. Table III shows the comparison between the two types of electrolytic capacitors. The footprint taken by Panasonic capacitors is almost the same as that when Chemi-Con capacitors are used. However, the total volume has a 75% reduction when Panasonic capacitors are used, which leads to a much higher power density. Unlike the prototypes in existing literature, the height of the DC link capacitors is no longer a bottleneck of the box volume of our prototype.

D. IMS BOARD AND HEATSINK SELECTION

Fig. 4 shows the cooling structure of the power stage. The MOSFETs are soldered on an IMS board. The IMS board has a copper layer, a dielectric layer and an aluminum layer. The IMS board has a much better thermal conductivity compared with a standard FR4 PCB board as shown in Table IV. The detailed parameters of the selected IMS board can be found in Table V. The IMS board was mounted on a forced air cooled heatsink with a thermal pad. In the design phase, the temperature rise during steady state operation could be estimated

TABLE V Parameters of the Selected IMS Board

IMS board design parameters		Reason for the design
Board type	Thermal Clad HT04503	
Copper thickness	3 oz(105 μm)	Handle 500 A_{RMS}/10mm width
Aluminum carrier thickness	2 mm	Handle dynamic thermal of 500 A_{RMS} for 300ms
Insulator layer thickness	76 μm	6.8 kV insulation with 80V/ μm dielectric strength
R_{IMS}	0.11 K/W	For the conductive layer

TABLE VI Simulation Parameters

Parameters	Values
DC bus voltage	48 V
Output frequency range	0 ~ 600 Hz
Load torque	2 Nm
Switching frequency	12 kHz
Deadtime	1 us

from power loss multiplying the total thermal resistance. The junction to case thermal resistance, R_{jc}, is 0.4 K/W. The thermal resistance of the selected IMS board, R_{IMS}, is 0.11 K/W. The total thermal resistance of the thermal pad, $R_{thermal}$, and the heat sink, R_{sink}, is 0.22 K/W. The total thermal resistance, R_{th_total}, is estimated to be 0.73 K/W. The device power loss under continuous operation has been estimated by PLECS simulation, and the value is 25 W. As a result, the temperature rise of the MOSFETs at steady state could be estimated as

$$\Delta T = P_{loss} \cdot R_{th\_total} = 25 \cdot 0.73 = 18.54^{\circ}\mathrm{C} \qquad (1)$$

The measured temperature rise shown in Fig. 5 is around 14.7 °C, which matches with the calculation pretty well. In addition, the maximum allowable device temperature rise is 50 °C in the worst case where the environment temperature is 100 °C and the maximum device junction temperature is 150 °C. Therefore, the heatsink design meets the requirement.

E. AUTOMOTIVE STANDARD GATE DRIVER INFINEON TLE9180D-31QK

One important contribution of this work is that the gate driver IC and microcontroller used in the prototype are compliant with automotive standards, which makes the prototype more readily accepted by industry. The TLE9180D-31QK is an advanced gate driver IC which is dedicated to control 6 external N-channel MOSFETs of an inverter for high-current three-phase motor drive applications in the automotive sector [26]. A sophisticated high-voltage technology allows the TLE9180D-31QK to support applications for single and mixed battery systems with battery voltages of 12 V, 24 V and 48 V even in tough automotive environments. Therefore, the pins that are related to inverter bridges, motor, and power supply can withstand voltages of up to 90 V. Motor related pins can even withstand negative voltage transients down to–15 V without damage. All low- and high-side output stages

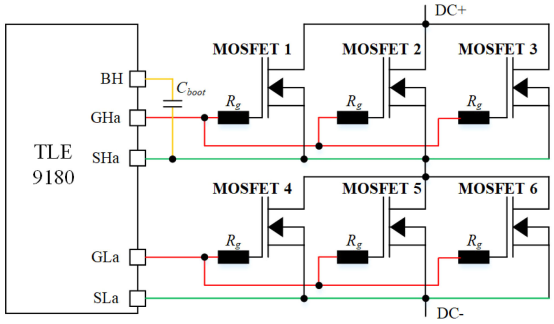

FIGURE 6. Schematic of gate driver TLE9810D-31QK output section for phase A. Each arm consists of three paralleled MOSFETs. C_{boot} is the bootstrap capacitor which is connected to BH and R_g is the gate driver for each switch. GHa and SHa represent the high-side gate output and source output pins of the gate driver IC, respectively. GLa and SLa represent the low-side gate output and source output pins of the gate driver IC, respectively.

are based on a floating concept, and the driver strength of the IC is enough to drive MOSFETs with the lowest R_{dson} on the market. The suggested schematic is shown in Fig. 6 and external circuitry parameters can be found in [26].

An integrated SPI interface is used to configure the TLE9180D-31QK. After successful power-up, parameters can be adjusted by SPI. Monitoring data, configuration and error registers can be read by external controllers. Cyclic-Redundancy-Check (CRC) over data and address bits ensures safe communication and data integrity. Specifically, CRC8 has been implemented in this IC. Bridge currents can be measured by the 3 integrated current sense amplifiers. The output of the current sense amplifiers is compatible with 5 V Analog-to-Digital (AD) converters, and the robust inputs can withstand negative transients down to–10 V without damage. The proportional gain and zero current offset can be adjusted by SPI, and the offset can be calibrated as well. Diagnostic coverage and redundancy have increased steadily in recent years in automotive applications. The TLE9180D-31QK also offers a wide range of diagnostic features, like monitoring of power supply voltage as well as system parameters. A testability of safety relevant supervision functions has been integrated. Failure behavior, threshold voltages and filter time constants of the supervisions of the device are adjustable via SPI. The TLE9180D-31QK is integrated in a LQFP64 package with an exposed pad, which provides an excellent thermal characteristic.

F. AUTOMOTIVE STANDARD MCU INFINEON TC1782

The TC1782 is a high-performance microcontroller which includes a TriCore CPU, program and data memories, buses, bus arbitration, an interrupt controller, a peripheral control processor, a Direct Memory Access (DMA) controller, and several on-chip peripherals. The TC1782 is designed to meet the needs of the most demanding embedded control system applications where the competing issues of price/performance, real-time responsiveness, computational power, data bandwidth, and power consumption are key design elements. The

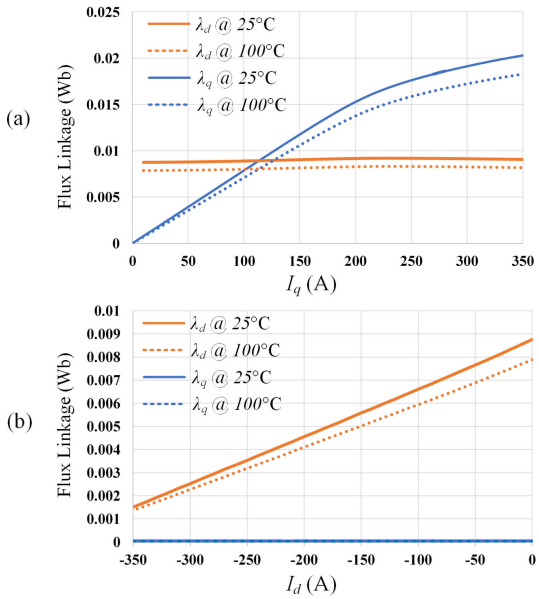

FIGURE 7. FEA results showing the relationship between stator flux linkages and winding currents under different room temperatures: (a) Stator flux linkage curves with different *q*-axis current and (b) Stator flux linkage curves with different *d*-axis current.

TC1782 offers several versatile on-chip peripheral units such as serial controllers, timer units, and AD converters. Within the TC1782, all these peripheral units are connected to the TriCore CPU/system via the Flexible Peripheral Interconnect (FPI) Bus and the Local Memory Bus (LMB) [27].

III. IPM MACHINE OPERATION AND OPTIMIZATION

This section includes a brief analysis of an IPM machine and proposes an optimized operation curve which not only simplifies the control strategy but also keeps a relatively large output torque. The operation of an IPM machine can be described using a series of equations and constraints which will be presented in the following subsections.

A. EQUATIONS

An FEA simulation has been performed on a physical 6-pole IPM machine. Based on Fig. 7 and curve fitting technique, the equations of stator flux linkage at 25 °C have been generated as a function of stator winding current.

$$\lambda_d = f_1(I_d) = 6.457 \times 10^{-14} \cdot I_d^4 + 5.751 \times 10^{-11} \cdot I_d^3 + 1.855 \times 10^{-8} \cdot I_d^2 + 2.293 \times 10^{-5} \cdot I_d + 8.760 \times 10^{-3} \tag{2}$$

$$\lambda_q = f_2(I_q) = 1.119 \times 10^{-14} \cdot |I_q|^5 - 8.327 \times 10^{-12} \cdot |I_q|^4 + 1.714 \times 10^{-9} \cdot |I_q|^3 - 1.255 \times 10^{-7} \cdot |I_q|^2 + 8.142 \times 10^{-5} \cdot |I_q| - 3.125 \times 10^{-6} \tag{3}$$

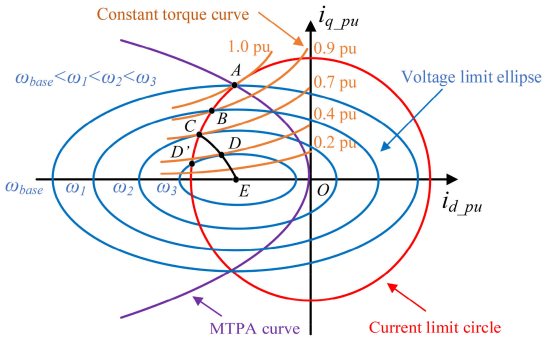

FIGURE 8. IPM operation curves in I_d–I_q plane.

where λ_d and λ_q are stator flux linkages in *d*-axis and *q*-axis, respectively. I_d and I_q are *d*-axis and *q*-axis stator current, respectively.

Output Electromagnetic (EM) torque is a function of stator flux linkage and winding currents as well as number of pole-pairs of the machine. It can be expressed as

$$T_e = \frac{3}{2} p \left(\lambda_d I_q - \lambda_q I_d\right) \tag{4}$$

where T_e is the output EM torque, and p is the number of pole-pairs.

Stator terminal voltages in the rotating reference frame can be expressed as

$$V_d = r_s I_d - \omega_e \lambda_q + \frac{d\lambda_d}{dt} \tag{5}$$

$$V_q = r_s I_q + \omega_e \lambda_d + \frac{d\lambda_q}{dt} \tag{6}$$

where V_d and V_q represent *d*-axis and *q*-axis stator terminal voltages, respectively. r_s is the stator winding resistance. ω_m and ω_e are rotor mechanical speed and electrical speed, respectively. The stator terminal phase voltage, V_t, can be expressed as

$$V_t^2 = V_d^2 + V_q^2 \tag{7}$$

B. CONSTRAINTS

The voltage constraint is imposed by the finite DC bus voltage of the three-phase inverter and can be expressed by

$$V_d^2 + V_q^2 \le V_{\max}^2 \tag{8}$$

where $V_{\max}$ represents the maximum available stator terminal voltage. The current constraint can be expressed as

$$I_d^2 + I_q^2 \le I_{\max}^2 \tag{9}$$

where $I_{\max}$ represents the maximum allowable current and is determined by inverter device current rating and stator winding current rating.

C. IPM OPERATION CURVES

The IPM operation and constraint curves are plotted in Fig. 8. The voltage constraint depicts an ellipse under a certain motor speed, and the ellipse shrinks as the speed increases. Fig. 8

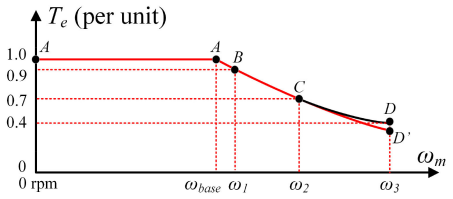

FIGURE 9. Maximum output EM torque versus mechanical speed.

shows four blue ellipses under four different electrical speeds. With fixed maximum winding current and device current rating, the current constraint can be simply represented by a circle which does not change with machine speed. Fig. 8 also shows a series of constant EM torque curves corresponding to different torque values varying from 0.2 to 1.0 per unit. On each torque curve, there is always an (I_d, I_q) pair yielding minimum winding current. Connecting all these (I_d, I_q) pairs from different EM torque curves produces a Maximum Torque Per Amp (MTPA) curve which is shown as the purple curve in Fig. 8.

D. IPM OPERATION OPTIMIZATION

Fig. 9 shows maximum output EM torque versus mechanical speed of the IPM machine used in the experiment. ω_{base} is the critical point between constant torque and field-weakening region. It can be seen that the maximum EM torque is constant when the speed is below ω_{base}. The machine enters field-weakening when its speed goes beyond ω_{base}, and the maximum output EM torque starts to decrease. The optimization target before field-weakening is to achieve MTPA which ensures maximum acceleration and minimum winding current that produces minimum conduction loss in the inverter devices and minimum iron loss in the machine windings. Therefore, the operating point in this region is Point A. In order to calculate the value of I_d and I_q at Point A, curve fitting method is used instead of deriving the analytical expressions since the stator flux linkages are also data driven. The flow chart of the curve fitting equation generation is illustrated in Fig. 10. The generated equations are expressed as follows,

$$I_q = f_3(T_e) = -4.494 \times 10^{-4} \cdot |T_e|^4 + 3.803 \times 10^{-2} \cdot |T_e|^3 - 1.237 \cdot |T_e|^2 + 2.446 \times 10^{1} \cdot |T_e| + 1.098 \quad (10)$$

$$I_d = f_4(I_q) = -1.663 \times 10^{-8} \cdot I_q^4 + 3.350 \times 10^{-6} \cdot I_q^3 - 2.841 \times 10^{-3} \cdot I_q^2 - 2.277 \times 10^{-1} \cdot I_q + 1.777 \quad (11)$$

In this way, the minimum current can be calculated using the above equations given by any torque command.

When IPM machine speed is higher than ω_{base}, the optimization target is to keep EM torque as large as possible so that the machine can reach its targeted speed as quickly as possible. From Fig. 8 and 9, operating at maximum available torque can be separated into two segments. The operating point should firstly follow along the red curve ABC when the speed is between ω_{base} and ω_2. On this curve, the output EM torque is always at its maximum. After the speed goes higher than ω_2, the operating point should follow the black curve CD. This is because the point producing maximum torque is no longer on the red circle. The equation of this black curve can be acquired using curve fitting technique that ensures MTPA from zero speed to infinity. However, these equations are not adaptive to DC bus fluctuation and other machine parameter changes. Instead, the proposed control strategy here chooses to regulate the current vector to continue following the red curve CD' (current limit curve) instead of the black curve CD. Even though the resulting EM torque is around 10% smaller, the control strategy is much easier to be implemented. The additional voltage loop which is used to modify d-axis current reference makes the algorithm more adaptive, and the voltage limit can be fulfilled during the whole operating range.

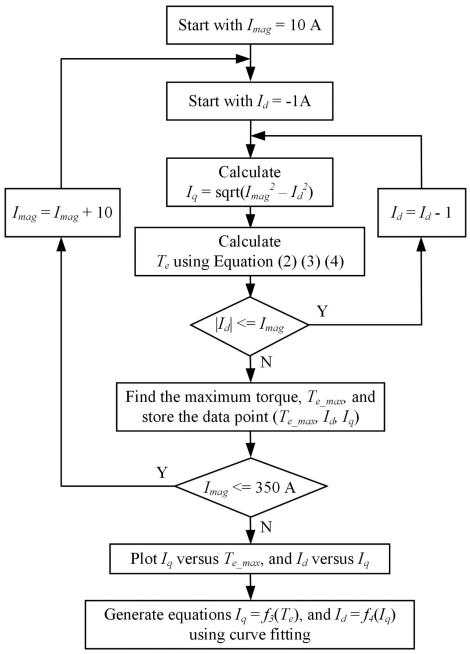

FIGURE 10. Flow chart of equation generation of MPTA using curve fitting where I_{mag} represents the winding current magnitude.

IV. PROPOSED CONSTANT CURRENT CONTROL STRATEGY

Based on the analysis in Section III, an improved IPM control strategy is illustrated in Fig. 11. V_{DC} represents the DC bus voltage. i_A, i_B, i_C represent the three-phase line current feedbacks. θ_m is the rotor mechanical angle while θ_e is the corresponding electrical angle. ω_m^* represents the mechanical speed command. ω_{fbk} is the motor mechanical speed feedback. T_e^* is the EM torque command. I_d^* and I_q^* are current references on d-axis and q-axis, respectively. V_d^* and V_q^* are voltage references generated from the current regulators on d-axis and q-axis, respectively. The proposed constant current control consists of the following three parts.

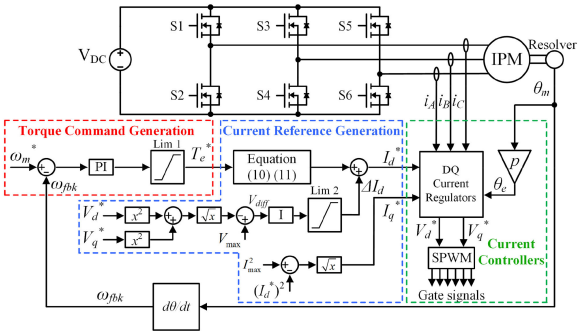

FIGURE 11. Proposed IPM motor drive control block diagram.

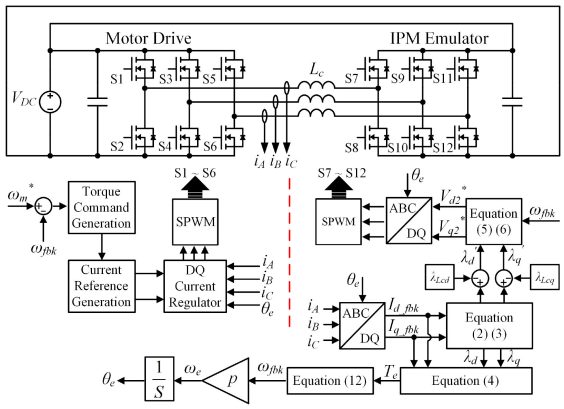

FIGURE 12. Control block diagram of the proposed pump-back system.

A. TORQUE COMMAND GENERATION

The EM torque command is generated by a speed loop followed by an output limiter. The controller is designed such that the output will be clamped at its maximum limit when the motor speed is low compared with the pre-set reference. During this period, the PI controller is saturated, and the output torque command is 10 Nm. When the speed feedback is very close to its command, the PI controller will exit saturation region. In torque control mode, a direct torque command is used to calculate corresponding current commands based on Equation (10) and (11).

B. CURRENT REFERENCE GENERATION

The control loop enclosed by the blue dashed line represents the inverter current reference generation. Based on the analysis in Section III, the control strategy is separated into two cases.

In order to determine whether the motor enters field-weakening region, the inverter output voltage magnitude will be computed using the two outputs of the current regulators, V_d^* and V_q^*. Since the inverter output voltage cannot exceed its maximum value $V_{\max}$ (half of V_{DC} in this case), the difference between inverter output voltage magnitude and $V_{\max}$ is used to determine motor operation region, and this voltage difference is represented by V_{diff} as shown in Fig. 11. If the inverter voltage is smaller than its maximum value, the current reference will follow the MTPA equations (10) and (11). When the inverter voltage is higher than its maximum value, the voltage loop will generate a negative ΔI_d to modify the original I_d^*. The I_q^* is then calculated such that the winding current magnitude is kept constant. Therefore, the operating point will drift from the purple MTPA curve in Fig. 8, but it still fulfills the voltage and current constraints. In this way, field-weakening happens automatically, and the controller is capable of adjusting the starting point of field-weakening when DC bus voltage fluctuates and other machine parameter changes since $V_{\max}$ will change when DC bus voltage varies.

C. DQ-FRAME CURRENT CONTROLLERS

As shown in Fig. 11, two simple PI controllers are used to generate inverter output voltage reference and traditional SPWM technique is used to generate device gate signals.

D. ADVANTAGES OF THE PROPOSED CONTROL STRATEGY

The proposed IPM drive control strategy has the following advantages over the existing solutions. Firstly, no look-up tables are involved in the control loops, which saves memory of the digital controller. Secondly, the proposed control strategy is adaptive to machine parameter changes caused by temperature and other operating conditions as well as DC bus voltage fluctuation, since an online regulation is implemented by the voltage integrator. Thirdly, no piecewise functions are involved in generating torque command and current references compared with [21]. In addition, Lim 2 ensures smooth change of d-axis current reference when the machine enters field-weakening. Therefore, a seamless transition can be realized from non-field-weakening to field-weakening operation. Two improvements have been made compared with [18]. Firstly, the nonlinearity of stator flux linkage has been taken into consideration, and the self-inductance is not assumed to be constant. Secondly, the proposed control scheme is suitable for not only speed control but also torque control.

V. PUMP-BACK TEST BENCH DEVELOPMENT

The designed power stage and the proposed IPM motor drive control strategy can be tested and verified using a pump-back system which does not need a real machine and has been implemented in literature [21], [28]–[31] as well.

A pump-back system contains two identical three-phase inverters. One inverter serves as the Motor Drive while another is controlled to mimic the operation of an IPM machine (called IPM Emulator). This "virtual machine" concept was proposed in [29] and the machine emulators in [29]–[31] also show excellent reaction to the motor drive under test.

The control block diagram of the proposed pump-back system is shown in Fig. 12. The AC terminals of the two inverters are connected through three inductors due to the PWM voltages at inverter output. The DC terminals of the two inverters are directly connected to the same DC power supply. As a result, the real power circulates between the two converters and the DC power supply only provides loss of the system. In Fig. 12, L_c represents the inductors linking the two inverters.

I_{d_fbk} and I_{q_fbk} are current feedbacks on d-axis and q-axis, respectively. V_{d2}^* and V_{q2}^* are calculated terminal output voltages of the virtual IPM machine on d-axis and q-axis, respectively. $\lambda_d^{'}$ and $\lambda_q^{'}$ are flux linkages seen from the IPM Emulator AC terminals on d-axis and q-axis, respectively. T_e is the calculated EM torque. λ_{Lcq} and λ_{Lcq} represent the flux linkages generated in L_c on d-axis and q-axis, respectively. The control diagram on the left-hand side of the red dashed line represents the improved IPM control strategy presented in Section IV. The control of the second inverter (IPM Emulator) is shown on the right-hand side. Since the motor drive controls AC side current, open-loop voltage control is implemented in the IPM Emulator. Stator flux linkages on both d-axis and q-axis are firstly calculated using Equation (2) and (3) subtracted by the flux produced in L_c. Along with the mechanical speed of the motor, the machine terminal voltage can be computed using Equation (5) and (6).

In order to get the information of the rotor speed and position without having a real machine and a resolver, the following equation is used.

$$\omega_{fbk} = \int \frac{1}{J}\left(T_e - T_{Load}\right) dt \tag{12}$$

In Equation (12), ω_{fbk} is the mechanical speed of the machine. J is the moment of inertia of the IPM machine and can be acquired from the nameplate. The output EM torque, T_e can be calculated using Equation (4). T_{load} is the load torque and can be set as a constant in the experiment. As a result, the electrical speed is just p (number of pole-pairs) times of the mechanical speed, and the rotor electrical angle is the integral of the electrical speed. This rotor angle will be shared between the two inverters. The second issue is how to design the value of L_c. All components outside of the motor drive should be regarded as the virtual IPM machine. Therefore, the flux produced by the AC inductors is also a part of the flux produced in the virtual machine. This is the reason why λ_{Lcd} and λ_{Lcq} should be subtracted from the calculated stator flux linkage. The inductor L_c should be designed such that the generated flux is smaller than the total flux calculated from Equation (2) and (3). In this case, L_c is designed as 20 uH.

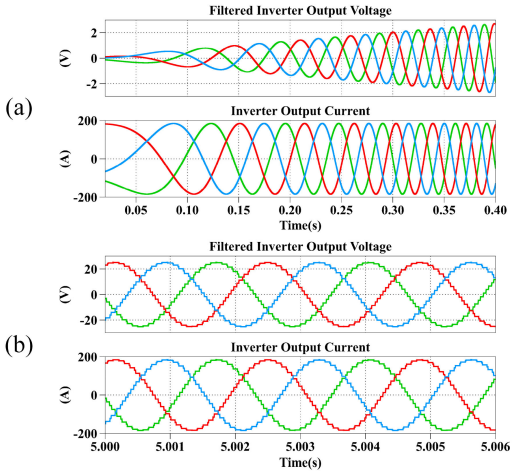

FIGURE 13. PLECS simulation results of filtered inverter output voltage and current (a) before entering field-weakening operation and (b) after entering field-weakening operation.

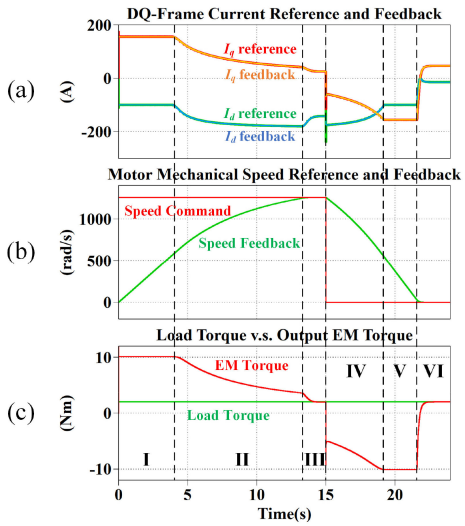

FIGURE 14. PLECS simulation results: (a) Stator current reference and feedback in dq-frame; (b) Mechanical speed reference and feedback; and (c) Load torque and output EM torque.

VI. SIMULATION RESULTS

PLECS simulations have been performed to verify the effectiveness of our proposed constant current based IPM motor drive control technique, and to prove the correctness of our proposed pump-back system control algorithm. Some of the simulation parameters are listed in the following table.

The first simulation was conducted using an IPM machine model provided by PLECS with a load torque of 2 Nm which has an opposite direction as the rotation. The machine parameters can be directly typed into the model or inserted as look-up tables. Fig. 13(a) shows the inverter output current and filtered terminal voltage before the machine enters field-weakening region (corresponding to Point A in Fig. 8). The current waveform indicates a constant current magnitude when the motor speed increases. However, the output terminal voltage amplitude increases with motor speed. Fig. 13(b) shows the inverter current and filtered output voltage after the motor enters field-weakening region. It is obvious that the current magnitude is still kept constant. The output terminal voltage is also limited at a constant level due to the voltage integrator.

In the simulation, the IPM machine operates as a motor in the first 15 seconds and changes to generator operation after 15 seconds. The results of the entire process are shown in Fig. 14. Region I to III are motor operation (acceleration) while Region IV to VI represent generator operation (deceleration) of the IPM machine. Fig. 14(a) shows that the current feedback perfectly tracks its reference, which validates the effectiveness of the designed current controllers. Since the speed error is very large in Region I, the speed regulator is saturated and the output has been clamped to 10 Nm. Since

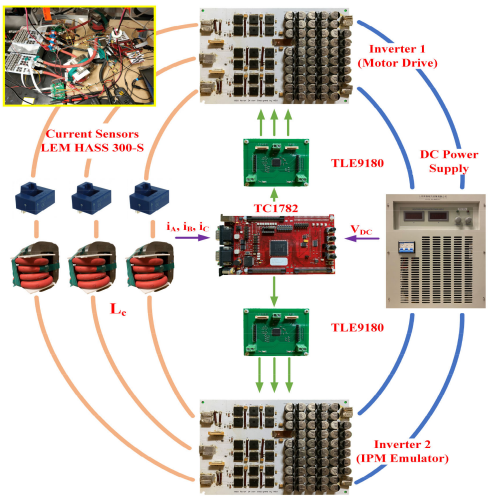

FIGURE 15. Experimental setup using Infineon technologies TC1782 micro-controller and TLE9180 gate driver IC.

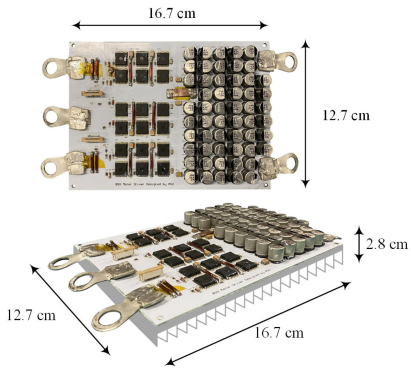

FIGURE 16. Dimension of the designed power board.

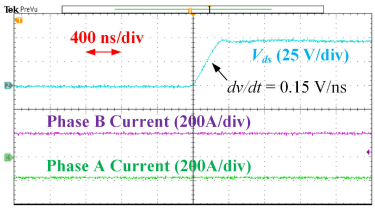

FIGURE 17. Drain-source voltage (V_{ds}) of the device and *dv/dt* measurement.

the EM torque is the largest in this region, the slope of the mechanical speed, which represents the acceleration, is also the largest. Region II represents the field-weakening region of the motor. In this region, the inverter terminal voltage loop starts to play a role in *d*-axis current reference generation, and I_d^* becomes more negative due to a negative ΔI_d. I_q^* also decreases in order to keep the phase current magnitude constant. At the same time, the speed acceleration decreases due to smaller output EM torque. When the motor speed is close to its command, the machine enters Region III where the speed regulator retreats from saturation, and the output torque is trying match the load torque. The speed command changes from 12000 rpm to 0 at t = 15 s and the machine starts to decelerate. In Region IV, since the speed is still high, the machine operates in the field-weakening region. However, the output EM torque becomes negative and I_q changes its polarity from positive to negative. As the speed becomes even lower, the machine leaves field-weakening and enters constant torque operation. As shown in Region V, the output EM torque becomes -10 Nm. Finally, when the speed becomes very low, the output EM torque is trying to balance the load torque, and the speed loop exits the saturation region. The results show that the proposed control strategy works for both motor and generator operations.

A pump-back system simulation has also been conducted to verify the proposed control strategy. The motor drive shows the same behavior as that in the previous simulation with an IPM machine model. This also proves the equivalence between a real machine and an emulator.

VII. EXPERIMENTAL RESULTS

The constructed pump-back test bench is shown in Fig. 15. Top view of each component including power board, controller board, gate driver board, AC inductors, current sensors, and DC power supply have been provided. The actual hardware setup is shown on top left corner of Fig. 15. The dimension of the power stage is shown in Fig. 16. The designed prototype reaches a power density of 20.3 kW/L.

A. DEVICE DV/DT REGULATION

Since the ratio of switching loss over conduction loss is very small, the major limitation of the *dv/dt* is on the motor side. High *dv/dt* of the machine terminal voltage can lead to high EMI noise and, most importantly, can create stresses that cause motor insulation to deteriorate and to fail [32]. Unlike traditional AC motor drives where mitigation of high *dv/dt* usually occurs at the motor end due to the long cable connection between AC drives and machines, the inverter and the motor are compactly integrated in this 48V BSG system. As a result, reducing *dv/dt* at the inverter output has been implemented by adding large gate resistors so that the gate-to-source current of the Si MOSFETs during turn-on and turn-off transients can be effectively limited. The final *dv/dt* is around 0.15 V/ns, as shown in Fig. 17.

B. EXPERIMENTS OF CLOSED-LOOP CURRENT CONTROL WITH RL LOAD

The first experiment is to achieve closed-loop current control of the inverter by using a three-phase RL load which consists of a 90 mΩ resistor and a 20 μH inductor in each phase. The closed-loop current control can be easily verified by changing the DC bus voltage. The experimental waveforms are shown in Fig. 18. The magnitude of the phase current has been well regulated at 186 A under different DC bus voltages.

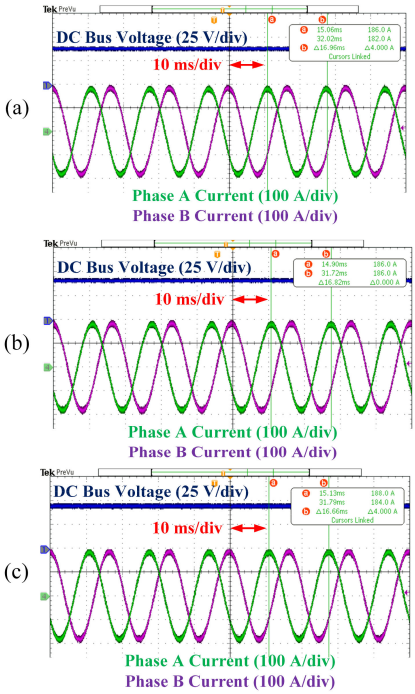

FIGURE 18. Closed-loop current control experimental results under the DC voltage of (a) 39 V, (b) 42 V, and (c) 46 V.

C. EXPERIMENTS OF THE PROPOSED PUMP-BACK SYSTEM

The control strategy of the proposed pump-back system has been verified using the constructed test bench. Fig. 19 shows the current waveforms under four different frequencies which are 60 Hz, 200 Hz, 400 Hz, and 600 Hz. Each waveform corresponds to a point on the Torque-Speed curve shown in Fig. 20. The test waveforms show the proposed constant current control and pump-back system control are effective. Note that the current magnitude in the 400 Hz and 600 Hz case is smaller than 186 A. The reason is that there is a large voltage drop across the inductor L_c between two inverters, and this voltage drop increases with higher current magnitude and electrical frequency. The terminal voltage of the IPM Emulator inverter can become much larger than that of the Motor Drive inverter. In order to avoid over modulation of the Emulator inverter under the same DC bus voltage, the current magnitude is intentionally decreased. As a result, the corresponding output EM torque is also below the green curve.

D. PUMP-BACK EXPERIMENTS UNDER MACHINE PARAMETER CHANGE CAUSED BY TEMPERATURE

We have conducted pump-back experiments considering stator flux linkage change caused by temperature variation. In the experiments, all the equations on the Motor Drive side remain unchanged since all the equations from curve fitting can only be tuned offline. However, the flux linkage equations will be updated using the FEA data acquired at 100 °C on the IPM Emulator side, which represents machine parameter changes caused by temperature variation. The experimental results are shown in Fig. 21 and Fig. 22.

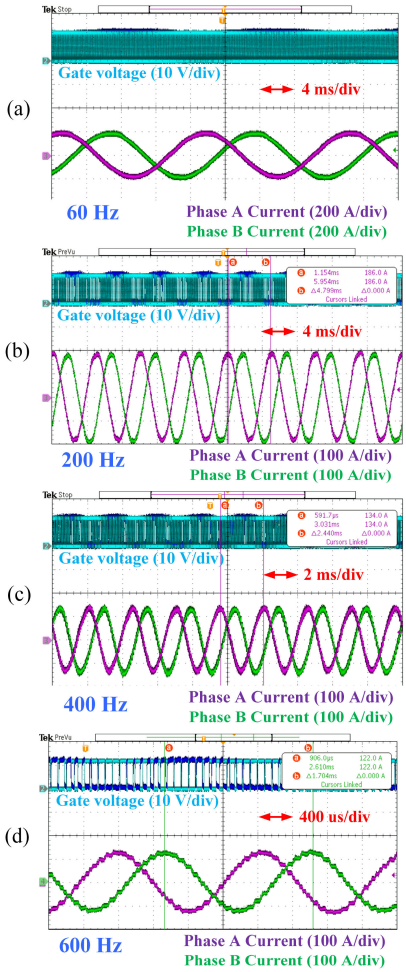

FIGURE 19. Pump-back system experimental results of phase A and B currents with an output frequency of (a) 60 Hz; (b) 200 Hz; (c) 400 Hz; and (d) 600 Hz.

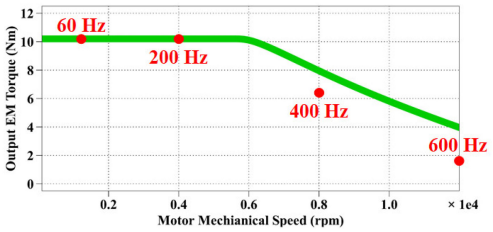

FIGURE 20. Output EM torque versus motor mechanical speed.

Fig. 21 shows the d-axis and q-axis current feedbacks as well as output EM torque, and Fig. 22 shows the measured motor mechanical speed at two different temperatures. From Fig. 21(a) and (b), it is obvious that the onset of field-weakening happens early at 25 °C compared with the case at 100 °C. The EM torque at 100 °C is 5% smaller than that at 25 °C in constant torque region. Due to the difference in EM torque in two cases, the speed curves shown in Fig. 22 are also different. Larger torque leads to larger acceleration. As a result, the mechanical speed at 100 °C experiences a slightly

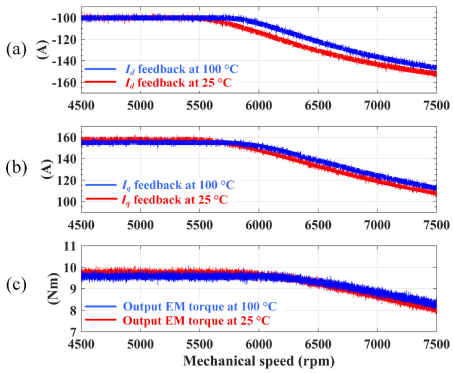

FIGURE 21. Experimental results using data at 25 °C and 100 °C: (a) *d*-axis current feedback; (b) *q*-axis current feedback; and (c) output EM torque.

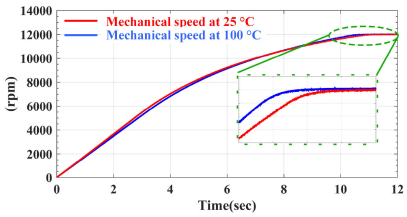

FIGURE 22. Motor mechanical speed measurement at 25 °C and 100 °C.

slower increase at the beginning. During field-weakening region, the motor acceleration at 100 °C increases and finally becomes larger than that at 25 °C.

The reasons for these difference can be analyzed as follows. Due to the difference in flux linkage equations at 25 °C and 100 °C, the voltage constraints become different. Since higher temperature leads to smaller flux linkage, the frequency of the onset point of field-weakening operation becomes higher. This explains a late change in *d*-axis and *q*-axis current feedbacks at 100 °C. The output EM torque is calculated using the updated flux linkage equations and winding current feedbacks, as shown in Fig. 21(c). These machine parameter changes do not affect the field-weakening control algorithm due to the inverter voltage loop which is not dependent on any machine parameters. As long as the inverter terminal voltage tries to exceed its limit, a negative ΔI_d will be added to *d*-axis current command in order to keep inverter voltage under limit. This machine parameter variation does not influence the speed loop as well. In the pump-back experiment, the motor mechanical speed is calculated on the IPM Emulator side with updated flux linkage equations. Therefore, the mechanical speed feedback has already taken into account the parameter changes, and the speed regulator can successfully make the motor speed equal to its reference. As shown in Fig. 22, both the red and blue speed curves reach 12000 rpm during steady state with small time difference. Therefore, the proposed field-weakening control is highly robust.

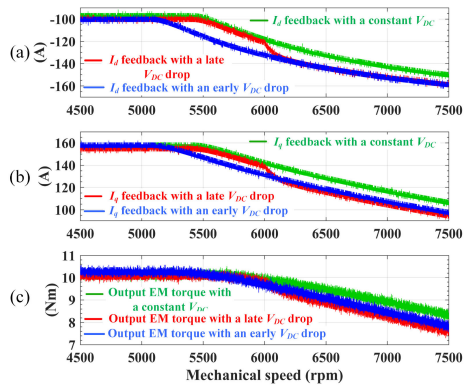

FIGURE 23. Experimental results with a DC bus voltage drop: (a) *d*-axis current feedbacks; (b) *q*-axis current feedbacks; and (c) output EM torque.

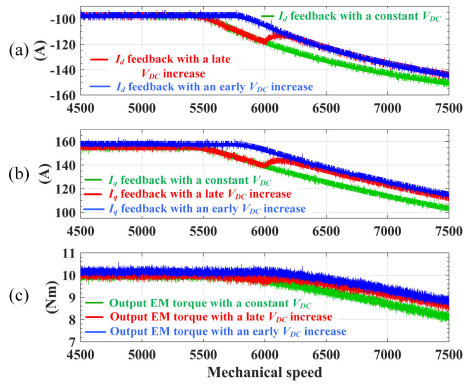

FIGURE 24. Experimental results with a DC bus voltage increase: (a) *d*-axis current feedbacks; (b) *q*-axis current feedbacks; and (c) output EM torque.

E. PUMP-BACK EXPERIMENTS UNDER DC BUS VARIATION

Another advantage of the proposed method is the adaptation to different DC bus voltages, and it has been validated by pump-back experiments as well. The experiments are classified into two categories which are "V_{DC} decreasing (Category I)" and "V_{DC} increasing (Category II)". The nominal DC bus voltage in a BSG system is 48 V. In Category I experiments, the DC bus voltage will decrease to 45 V while in Category II case, the DC link will rise to 51 V. In each category, we have conducted experiments in three cases. The DC bus voltage change will be controlled to occur before field-weakening as well as during field-weakening. The case with unchanged DC bus voltage will also be performed for comparison purpose. The results are presented in Fig. 23 and Fig. 24.

From Fig. 23(a) and (b), an early DC bus drop leads to early onset of field-weakening operation comparing the green curve with the blue curve. If the V_{DC} drop happens during field-weakening, there will be a negative step change in *d*-axis and *q*-axis current feedbacks as shown by the red curve, and finally the red curve will coincide with the blue curve. The same phenomenon can be observed in output EM torque as shown in Fig. 23(c). From Fig. 24(a) and (b), an early DC bus rise leads to a late starting point of field-weakening operation comparing the green curve with the blue curve. If the V_{DC} rise

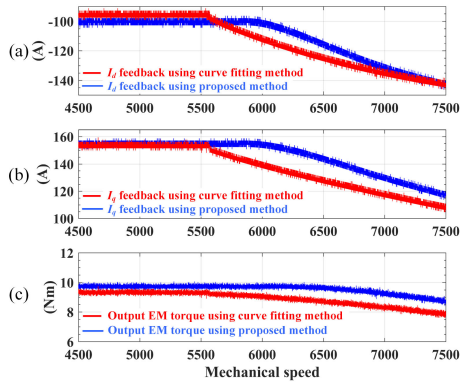

FIGURE 25. Experimental results comparison between proposed constant current based method and original curve fitting based method using stator flux linkage data at 100 °C.

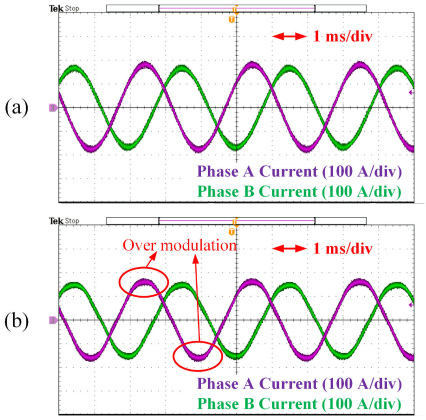

FIGURE 26. Experimental results of inverter output current using proposed constant current based method (plot (a)) and original curve fitting based method (plot (b)) with a DC bus drop from 48 V to 45 V.

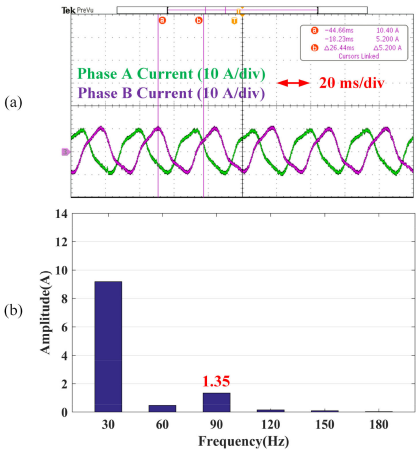

FIGURE 27. Pump-back system experimental results using TC1782 and TLE9180 without 3rd harmonic suppression: (a) Phase A and phase B current with a fundamental frequency of 30 Hz and (b) FFT analysis of Phase A current.

happens during field-weakening, there will be a positive step change in d-axis and q-axis current feedbacks as shown by the red curve, and finally the red curve will coincide with the blue curve. The same phenomenon can be observed in output EM torque as illustrated in Fig. 24(c).

The reasons can be analyzed as follows. In Category I experiments, smaller DC bus voltage means smaller $V_{\max}$. If the DC bus drop happens in constant torque region, the onset of field-weakening occurs at lower electrical frequency. If V_{DC} drops in field-weakening region, a more negative d-axis current is needed to reduce the terminal voltage magnitude so that no over modulation will occur. Therefore, a negative step change in d-axis and q-axis current feedbacks is expected. The output EM torque starts to decrease at lower frequency if V_{DC} drops in constant torque region since field-weakening will start at lower frequency. However, the torque experiences a negative step change when V_{DC} decreases during field-weakening because of a deeper field-weakening is expected. The same analysis applies to Category II results. Thanks to the additional voltage loop, the proposed IPM motor drive strategy is adaptive to all V_{DC} changes.

F. COMPARISON BETWEEN THE PROPOSED METHOD AND CURVE FITTING METHOD

We have conducted additional pump-back experiments using the curve fitting based method introduced in [21] for comparison purpose. We firstly compared the performance of the two methods when machine parameter changes. Fig. 25 shows the inverter output current with two methods using stator flux linkage data at 100 °C. As discussed in the previous section, smaller flux linkage leads to a late onset of field-weakening operation using the proposed method so that the DC bus voltage can be fully utilized. However, due to fixed curve fitting equations, the flux-weakening has not been delayed in the curve fitting method. In Fig. 25(a) and (b), I_d and I_q feedbacks in the curve fitting method starts to change around the same frequency as that at 25 °C. The proposed method generates a maximum torque of 10 Nm for longer time as shown by the blue curve in Fig. 25(c). Therefore, the machine will experience a longer and larger acceleration. The comparison of the two methods with DC bus fluctuation has also been performed. Fig. 26 shows the inverter output current using two different methods with a DC bus voltage drop from 48 V to 45 V. Due to the voltage integrator in the proposed method, it automatically adapts to the lower DC bus voltage and regulates the inverter output voltage to be within limit. However, the curve fitting based method uses fixed equations to generate current reference during the entire operation. Therefore, the controller still assumes a 48 V DC bus voltage, which leads to over modulation and current distortion.

Therefore, the proposed method can automatically adjust the onset of the field-weakening operation when machine parameter varies or DC bus voltage changes compared with the curve fitting method in [21].

G. COMMON-MODE CURRENT SUPPRESSION

As shown in Fig. 27, the current waveforms are distorted and contain 3rd order harmonics in the pump-back system. Since

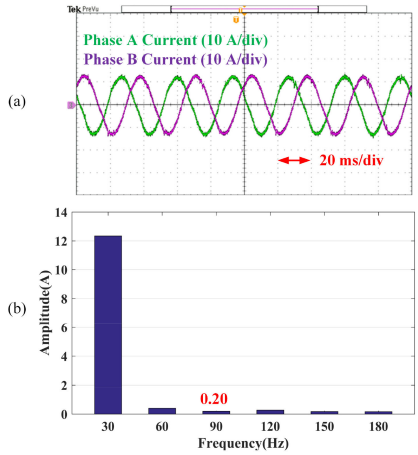

FIGURE 28. Pump-back system experimental results using TC1782 and TLE9180 with 3rd harmonic suppression: (a) Phase A and phase B current with a fundamental frequency of 30 Hz and (b) FFT analysis of Phase A current.

the DC bus of the two inverters are directly connected, the DC link capacitors of both inverters serve as a low-impedance path for the 3rd order harmonic current. A simple solution is to use a 3rd PR controller to suppress the circulating current. The result is shown in Fig. 28 where the 3rd harmonic component reduces from 1.35 A to 0.2 A. Fortunately, this common-mode current only exists in the pump-back system. When the inverter is directly connected to an IPMSM, the common-mode current will be eliminated since it has no path.

VIII. CONCLUSION

This paper firstly elaborates hardware design considerations for a low-voltage high-current high power density three-phase motor drive inverter to address the challenges of even current distribution among paralleled MOSFETs, small drain-source voltage spike and good thermal dissipation. In order to satisfy the high-current requirement in such applications, a careful selection of MOSFET device with high-current rating and low on-resistance has been presented. In order to suppress circulating current among paralleled devices, individual gate resistors have been placed in the gate loop of each MOSFET. In order to provide good thermal dissipation, an IMS board and single-layer layout technique have been implemented. Multiple low-profile electrolytic capacitors are used so that the power density of the prototype has been increased. Moreover, the gate driver IC TLE9180 and microcontroller TC1782 used in the prototype are compliant with automotive standard, which makes the prototype more readily accepted by industry. An improved IPM control strategy and a pump-back system based on a virtual machine concept have been implemented, which facilitates the validation of the designed inverter hardware under rated condition without using a real motor. The control algorithm automatically adjusts the onset of field-weakening by using an additional inverter voltage loop and takes into account the nonlinearity of the stator flux linkage, which makes the motor drive adaptive to machine parameter changes as well as DC bus voltage fluctuation. A 12 kW three-phase BSG inverter prototype has been built and tested. The prototype power density has reached 20.3 kW/L. The experimental results show a continuous and stable operation with up to 200 A phase current and up to 600 Hz output frequency.

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