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A High Efficiency and Low Cost ANPC Inverter Using Hybrid Si/SiC Switches

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ABSTRACT This paper presents a performance investigation and design optimization of a high efficiency three-level Active Neutral Point Clamped (ANPC) inverter topology using hybrid Si/SiC switches. It uses a modulation strategy that produces a cluster of low frequency switches commutating at fundamental line frequency (realized with Si IGBTs) and high frequency switches commutating at carrier frequency (realized with hybrid Si/SiC switches) to facilitate a tradeoff between the inverter efficiency and cost. A generalized Si/SiC current rating ratio optimization algorithm is presented for the hybrid Si/SiC switches based on the power loss profile of ANPC inverter. This algorithm determines the optimal current rating ratio between the Si IGBT and SiC MOSFET for the hybrid Si/SiC switches based on the inverter operating specification and Si/SiC gate control technique to achieve the best tradeoff between cost, loss and reliability. The performance of the proposed ANPC inverter system is investigated and compared with other similar ANPC inverter systems. The proposed ANPC inverter system achieves higher efficiency compared to an all Si IGBT based ANPC inverter system, all SiC MOSFET based ANPC inverter system, and other ANPC inverter systems consisting mixed Si IGBT and SiC MOSFET devices. On the other hand, the semiconductor device cost of the proposed ANPC inverter system is much lower than an all SiC MOSFET based ANPC inverter system and the mixed Si IGBT and SiC MOSFET based ANPC inverter systems while it is on par with an all Si IGBT based ANPC inverter system.

INDEX TERMS ANPC inverter, hybrid Si/SiC switches, Si/SiC current ratio optimization, efficiency improvement, cost reduction.

I. INTRODUCTION

The renewable energy market based on photovoltaic (PV) energy is rapidly growing [1], [2] and PV generation plants with MW-scale power capability are becoming common nowadays. However, as generation capacity is increasing, energy conversion efficiency continues to be a critical design element. When the converter power level increases, converter losses will also increase, hence it requires an advanced thermal management system to quickly dissipate the heat generated by the semiconductor devices and passive components. This will increase cost, size, and complexity of the energy conversion system. Due to this, improving efficiency and power density of energy conversion systems become the focus of current and future power electronics research efforts.

Three-level inverter topologies gained increased attention for high power energy conversion applications due to their benefits compared to two-level inverter topologies. Typical benefits of three-level inverter topologies over two-level inverter topologies are lower harmonic content in the output current waveform (requiring smaller filter components), reduced switching loss and reduced electromagnetic interference [3], [4]. The three-level T-type inverter topology is typically preferred for lower voltage applications because of its higher power conversion efficiency compared to other three-level inverter topologies, especially for low switching frequencies [5]. However, this topology is less economically attractive for high voltage applications

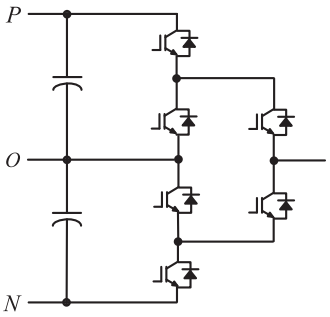

FIGURE 1. Phase leg of a three-level ANPC inverter topology.

since it requires higher blocking voltage rated semiconductor devices [6]. In addition, the T-type topology suffers from imbalanced loss distribution among the semiconductor devices due to the unequal voltage stress on the semiconductor devices [7]. The clamping leg devices have lower voltage stress hence lower loss than the main leg devices.

For high power applications, the three-level neutral point clamped (NPC) inverter topology is attractive due to its capability to handle higher voltage levels with lower voltage rated semiconductor devices [8], [9]. In this inverter topology, the semiconductor devices need to be rated for half of the input dc bus voltage. However, like the T-type inverter topology, it suffers from imbalanced loss distribution among its semiconductor devices [10], [11]. Depending on the load power factor, two kinds of switching loops exist in this inverter topology that results in imbalanced loss distribution among the semiconductor devices. When the load voltage and load current have the same polarity (rectifier operating mode), short commutation loop involving two switching devices exist. On the other hand, when the load voltage and load current have opposite polarity (inverter operating mode), long commutation loop involving four switching devices exist. These commutation loops result in different stray inductances hence different stress and loss for the semiconductor devices.

Conversely, the Active Neutral Point Clamped (ANPC) inverter topology eliminates the problem of imbalanced semiconductor loss distribution that its counterparts have. This topology has two redundant neutral current paths that can be flexibly configured to balance semiconductor device losses irrespective of the load power factor [12], [13]. In addition, like the three-level neutral-point clamped inverter topology, it requires low voltage rated semiconductor devices for high voltage applications. Therefore, it is very attractive solution for high power energy conversion applications.

Several modulation techniques and switching device configurations are proposed in the literature to improve the efficiency of an ANPC inverter. In [14], the topology shown in Fig. 6(a) is proposed. It uses the modulation strategy proposed in [15] where the inner switching devices (S_1–S_4) are commutating at the carrier frequency and the outer switching devices (S_5–S_6) are commutating at the fundamental line frequency. In [16], the topology shown in Fig. 6(b) is proposed

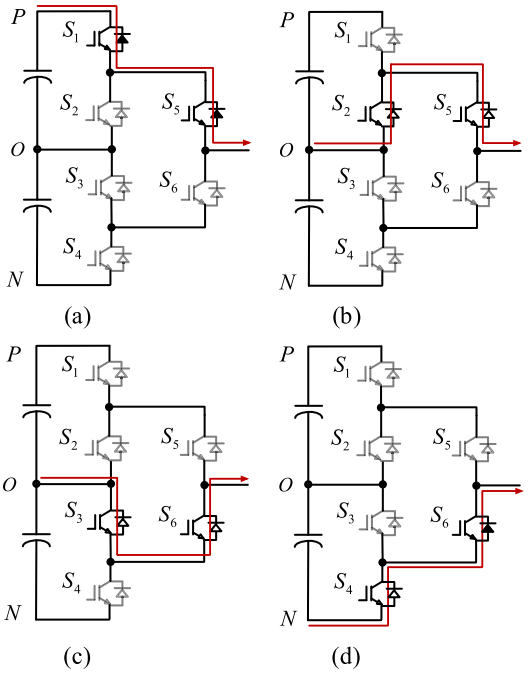

FIGURE 2. Switching diagram for modulation type I: (a) P state, (b) O^+ state, (c) O^- state, and (d) N state.

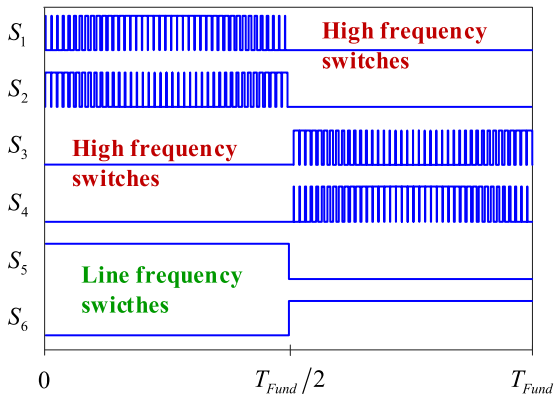

FIGURE 3. Gate signals for modulation type I.

along with the modulation strategy presented in [17], [34]. In this modulation strategy, the inner switching devices (S_1–S_4) are commutating at the fundamental line frequency while the outer switching devices (S_5–S_6) are commutating at the carrier frequency. These modulation techniques basically produce a cluster of low frequency switching devices switching at the fundamental line frequency and high frequency switching devices switching at the carrier frequency. By using Si IGBTs for the low frequency switching devices and SiC MOSFETs for the high frequency switching devices, these two topologies improved the efficiency of an ANPC inverter significantly. However, the cost of the inverter is increased compared to their silicon counterpart due to the high cost of SiC MOSFET devices.

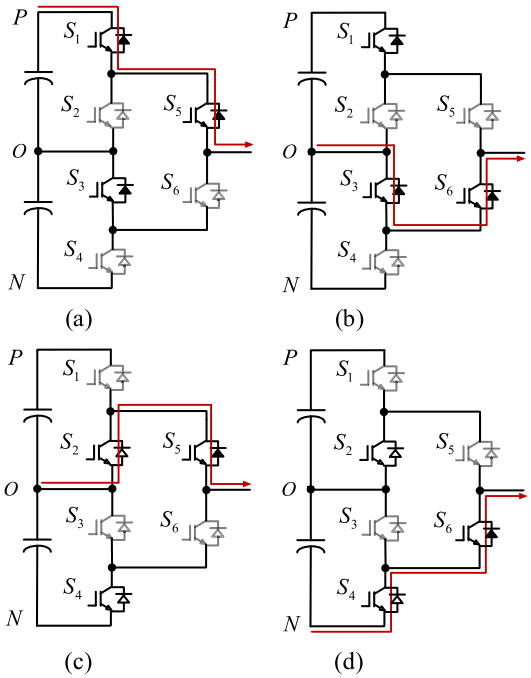

FIGURE 4. Switching diagram for modulation type II: (a) P state, (b) O^+ state, (c) O^- state, and (d) N state.

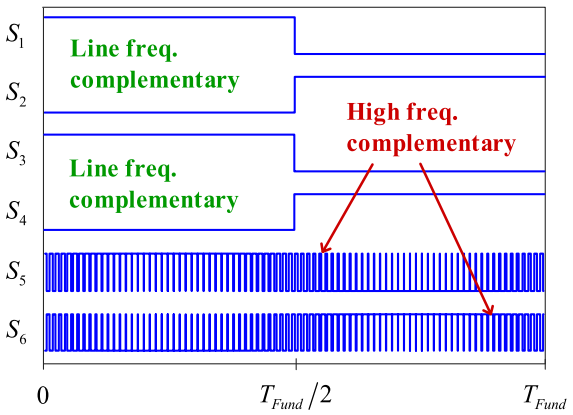

FIGURE 5. Gate signals for modulation type II.

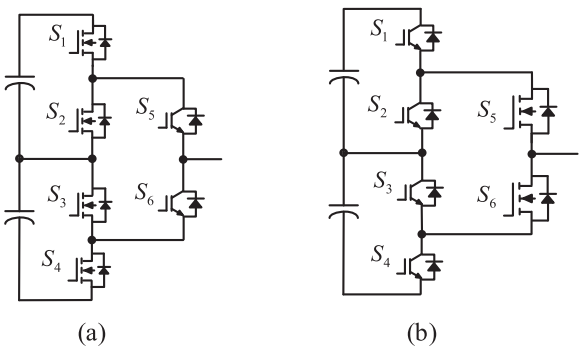

FIGURE 6. Mixed Si IGBT and SiC MOSFET ANPC inverter topologies: (a) topology proposed in [14] and (b) topology proposed in [16].

The efficiency of an ANPC inverter can be improved without significantly increasing the overall cost of the inverter by using hybrid Si/SiC switching devices for the high frequency switches. In [18]–[20], it is shown that the loss and cost of high frequency switches can be reduced by using hybrid Si/SiC switching devices compared to using a single SiC MOSFET. By using a higher current rated Si IGBT and a lower current rated SiC MOSFET, the static current sharing hence the cost and conduction loss of the SiC MOSFET can be reduced. On the other hand, using appropriate gate sequence control, the turn-on and turn-off sequence of the Si IGBT and the SiC MOSFET can be regulated to optimize the switching loss of the Si IGBT.

This paper presents an efficiency improvement for a three-level Active Neutral Point Clamped inverter using hybrid Si/SiC switches for the high frequency switching devices and Si IGBTs for the low frequency switching devices [21]. It achieves higher efficiency compared to other ANPC inverter systems such as an all Si IGBT based ANPC inverter system, an all SiC MOSFET based ANPC inverter system, and other ANPC inverter systems consisting mixed Si IGBT and SiC MOSFET devices. Another benefit of the proposed ANPC inverter system is its cost reduction; the semiconductor device cost of the proposed ANPC inverter system is much lower than an all SiC MOSFET based ANPC inverter system and the mixed Si IGBT and SiC MOSFET based ANPC inverter systems while it is almost comparable with the cost of an all Si IGBT based ANPC inverter system.

II. MODULATION AND SEMICONDUCTOR DEVICE CONFIGURATION FOR ANPC INVERTER

The three-level ANPC inverter topology shown in Fig. 1 contains four switching states: positive state (P), negative state (N) and two redundant neutral (O) states. The redundant neutral switching states increase the modulation freedom for this inverter topology since they can be flexibly configured to achieve different control objectives. Using this modulation flexibility, two major types of modulation strategies have been developed for ANPC inverter to optimize its switching performance and semiconductor device power losses. These modulation strategies differ from each other based on the neutral current path they are using during the positive and negative half cycle of the output voltage. However, these two neutral current paths result in different stress and loss for the semiconductor devices due to the difference in their switching loop stray inductances.

The first modulation type (modulation type I) [15] uses the top neutral current path (S_2 and S_5) during the positive half cycle of the output voltage and the bottom neutral current path (S_3 and S_6) during the negative half cycle of the output voltage as shown in Fig. 2. The switching states and corresponding gate signals for this modulation strategy are shown in Table I and Fig. 3, respectively. The O^+ and O^- states in the switching table represent the O states during the positive and negative half cycle of the output voltage. In this modulation strategy,

TABLE I Switching Table for Modulation Type I

State	Output	S_1	S_2	S_3	S_4	S_5	S_6
P	$0.5V_{dc}$	1	0	0	0	1	0
O^+	0	0	1	0	0	1	0
O^-	0	0	0	1	0	0	1
N	$-0.5V_{dc}$	0	0	0	1	0	1

TABLE II SWITCHING TABLE FOR MODULATION TYPE II

State	Output	S_1	S_2	S_3	S_4	S_5	S_6
P	$0.5V_{dc}$	1	0	1	0	1	0
O^+	0	1	0	1	0	0	1
O^-	0	0	1	0	1	1	0
N	$-0.5V_{dc}$	0	1	0	1	0	1

the switches (S_1–S_4) commutate at carrier frequency while the switches (S_5–S_6) commutate at fundamental line frequency. Therefore, it only involves short commutation loops consisting of two switching devices in all four operation quadrants. Hence it reduces the stress and loss of the semiconductor devices. The topology shown in Fig. 6(a) is proposed in [14] based on this modulation strategy. Using Si IGBTs for the low frequency switches and SiC MOSFETs for the high frequency switches, this topology provides an optimized ANPC inverter solution in terms of cost and efficiency.

The second modulation type (modulation type II) [17] uses the lower neutral current path (S_3 and S_6) during the positive half cycle of the output voltage and the upper neutral current path (S_2 and S_5) during the negative half cycle of the output voltage as shown in Fig. 4. The switching states and corresponding gate signals for this modulation strategy are shown in Table II and Fig. 5, respectively. In this modulation strategy, the switches (S_1 - S_4) are commutating at fundamental line frequency while the switches (S_5 - S_6) are commutating at carrier frequency. The topology proposed in [16], shown in Fig. 6(b), uses this modulation strategy. Similar to the topology in [14], it uses Si IGBTs for the low frequency switching devices and SiC MOSFETs for the high frequency switching devices to facilitate the tradeoff between semiconductor devices cost and power loss. However, the number of high frequency switches in this topology is reduced by half. Therefore, the cost of the semiconductor devices for this topology is lower than that of the former topology. This modulation strategy but results in long commutation loops consisting of four switching devices in all operation quadrants. Therefore, it increases the parasitic inductance of the switching loops which in turn increases the voltage overshoot and energy loss of the switching devices during switching. To mitigate this problem, switching loop parasitic inductance reduction is proposed in [22] by using a decoupling capacitor between the high frequency switching stage and the low frequency switching stage. The decoupling capacitor splits the large commutation loop that this modulation strategy creates into two smaller commutation loops hence it reduces the stress and loss of the high frequency switches.

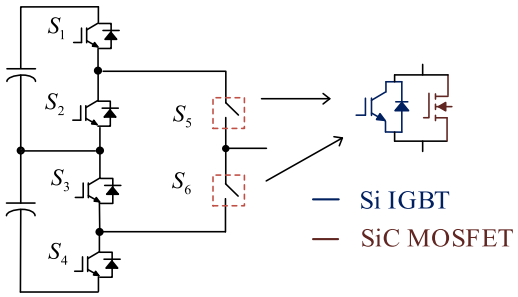

FIGURE 7. Hybrid Si/SiC switches based ANPC inverter topology proposed in this paper.

The topology proposed in this paper is shown in Fig. 7. It uses modulation type II because of its lower number of high frequency switches. It uses Si IGBTs for the low frequency switches in order to achieve low cost and low conduction loss, but it replaces the SiC MOSFETs with hybrid Si/SiC switching devices for the high frequency switches. A high current rated Si IGBT and a low current rated SiC MOSFET are used for the hybrid Si/SiC switches to reduce the static current sharing hence the cost and conduction loss of the SiC MOSFETs. Using appropriate gate sequence control for the hybrid Si/SiC switches (reviewed in Section III), the switching loss of the Si IGBT in the hybrid Si/SiC switches is minimized. Therefore, the proposed semiconductor device configuration provides higher efficiency compared to other ANPC inverter systems such as an all Si IGBT based ANPC inverter system, an all SiC MOSFET based ANPC inverter and mixed Si IGBT and SiC MOSFET based ANPC inverter systems. Regarding cost, the proposed ANPC inverter system has lower semiconductor device cost compared to an all SiC MOSFET based ANPC inverter system and the mixed Si IGBT and SiC MOSFET based ANPC inverter systems while it has almost comparable cost with an all Si IGBT ANPC inverter system.

In general, the novelties of this paper are:

- The use of hybrid Si/SiC switches for the high frequency switches in order to facilitate the tradeoff between efficiency and cost of ANPC inverter.
- The development of a generalized current ratio optimization algorithm for hybrid Si/SiC switches for ANPC inverter to facilitate the tradeoff between efficiency, cost and reliability.
- The design and validation of an ANPC inverter employing hybrid Si/SiC switches.

III. POWER LOSS AND THERMAL MODELING

In order to demonstrate the efficiency improvement of the proposed hybrid Si/SiC switch based ANPC inverter compared to other similar ANPC inverter configurations such as the all Si IGBT ANPC inverter, the all SiC MOSFET ANPC inverter

and the mixed Si IGBT and SiC MOSFET based ANPC inverters, the theoretical power losses of the different ANPC inverter systems are investigated. The conduction power losses of the semiconductor devices for the different ANPC inverter systems are modeled using the well-known piecewise linear model shown in (1) [23]–[26].

$$P_{\text{cond}} = V_0 I_{\text{avg}} + r I_{\text{rms}}^2 \tag{1}$$

where V_0 is the on-state voltage drop of the device, I_{avg} is the average current through the device, r is the equivalent on-state resistance of the device and I_{rms} is the root-mean-square (*rms*) value of the current through the device. The on-state forward voltage (V_0) and the on-state resistance (r) for the semiconductor devices are extracted from their respective datasheet using piecewise linear approximation.

The turn-on energy loss (E_{on}) and the turn-off energy loss (E_{off}) of the semiconductor devices are also extracted from their datasheets. The reverse recovery energy loss of the diodes are already included into the turn-on energy loss (E_{on}) as described in the datasheet. Since the switching loss data provided in the devices datasheet is at a test condition that is different from the circuit operating condition, the turn-on and turn-off energy losses provided in the devices datasheet are scaled according to (2)–(3) using the voltage and current values of the datasheet test condition and the actual circuit operating conditions. To simplify the switching loss modeling, switching losses are considered to be linear with the dc-link voltage [23]. The switching voltage of three-level ANPC inverter is half of the dc-link voltage ($0.5U_{\text{dc}}$). The relationship between switching loss and the device current is derived by using curve-fitting tools. The total switching power loss of the semiconductor devices is then determined by integrating the total switching energy loss of one switching cycle over the full output fundamental cycle.

$$E_{\text{on}} = \frac{0.5U_{\text{dc}}E_{\text{on, test}}}{U_{\text{test}}} \cdot \frac{k_{2\text{on}}I_0^2 + k_{1\text{on}}I_0 + k_{0\text{on}}}{k_{2\text{on}}I_{\text{test}}^2 + k_{1\text{on}}I_{\text{test}} + k_{0\text{on}}} \tag{2}$$

$$E_{\text{off}} = \frac{0.5U_{\text{dc}}E_{\text{off, test}}}{U_{\text{test}}} \cdot \frac{k_{2\text{off}}I_0^2 + k_{1\text{off}}I_0 + k_{0\text{off}}}{k_{2\text{off}}I_{\text{test}}^2 + k_{1\text{off}}I_{\text{test}} + k_{0\text{off}}} \tag{3}$$

where $E_{\text{on,test}}$ and $E_{\text{off,test}}$ are the datasheet turn-on and turn-off energy losses, U_{test} and U_{dc} are the dc-link voltages of the datasheet test condition and the actual circuit operating condition, I_0 and I_{test} are the actual current going through the device and the datasheet test current, and k_{ion} and k_{ioff} ($i = 0$, 1, 2) are the turn-on and turn-off fit coefficients.

The conduction behavior of the hybrid Si/SiC switches depend on the current sharing between the two devices and the polarity of the load voltage. During the positive half cycle of the load voltage, the Si IGBT and the SiC MOSFET conduct the load current. Therefore, the two devices share the load current according to their on-state resistance as shown in (4) and (5).

$$I_{\text{MOSFET}} = \frac{r_{\text{ce,IGBT}}}{r_{\text{ce,IGBT}} + r_{\text{ds,MOSFET}}} I_{\text{load}} \tag{4}$$

TABLE III CONVERTER SPECIFICATION

Rated output power, P_{rated}	20 kW
Dc-link voltage, U_{dc}	800 V
Output voltage, V_{out}	480 V
Dc-link capacitor	720 μF
Switching frequency	50 kHz

$$I_{\text{IGBT}} = \frac{r_{\text{ds,MOSFET}}}{r_{\text{ce,IGBT}} + r_{\text{ds,MOSFET}}} I_{\text{load}} \tag{5}$$

During the negative half cycle of the load voltage, the SiC MOSFET and the body diode of the Si IGBT conduct the load current. The body diode of the SiC MOSFET has high conduction loss due to its high forward voltage drop. Therefore, synchronous rectification is used for the SiC MOSFET. The current sharing between the SiC MOSFET and the body diode of the Si IGBT is given by (6) and (7).

$$I_{\text{MOSFET}} = \frac{r_{\text{bd,IGBT}}}{r_{\text{bd,IGBT}} + r_{\text{ds,MOSFET}}} I_{\text{load}} \tag{6}$$

$$I_{\text{bd,IGBT}} = \frac{r_{\text{ds,MOSFET}}}{r_{\text{bd,IGBT}} + r_{\text{ds,MOSFET}}} I_{\text{load}} \tag{7}$$

The energy loss of the hybrid Si/SiC switches for the proposed ANPC inverter is also dependent on the Si/SiC gate control strategy (presented in the next section). When the Si IGBT and the SiC MOSFET turn on simultaneously as in the case of Option I and Option II, the turn-on loss of the Si IGBT can be ignored and the SiC MOSFET can be assumed to turn-on at the rated load current. This is because the turn on speed of the SiC MOSFET is much higher than the Si IGBT so the SiC MOSFET turns on very quickly. The Si IGBT undergoes zero voltage switching for the most part. During turn off, both devices will experience turn-off energy loss proportional to their device current. On the other hand, when a delay time between the two gate signals is used as in the case of Option II–IV, the device which turns on or turns off first handles the full load current and the device which turns on or turns off later handles zero voltage or zero current during switching.

The accuracy of the switching loss model is first verified using measured switching loss data. The test is conducted at room temperature ($T_{\text{j}} = 25$ °C) but it will not lose too much accuracy for elevated temperatures since the switching energy losses are hardly dependent on temperature [26]. Table III shows the specifications of the converter for this test. An Infineon 650 V, 70 A Si IGBT (IRGP4069DPBF) and a ROHM 650 V, 70 A SiC MOSFET (SCT3030ALGC11) are used for the switches. The theoretically estimated and the measured switching energy losses of these switches are shown in Fig. 8. As can be seen from the figure, the estimated switching energy losses are very close to the measured energy losses and hence the switching loss model is acceptable. This switching energy loss model has also been proved acceptable in [27] and [28].

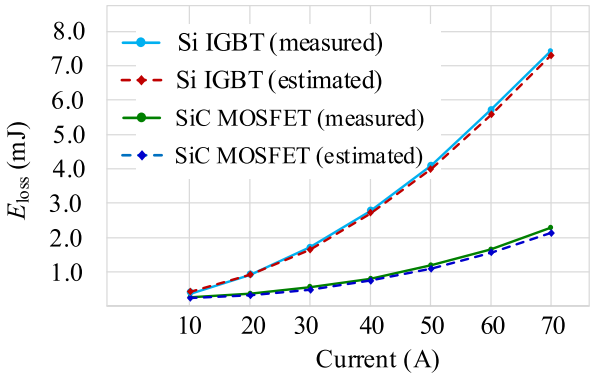

FIGURE 8. Estimated and measured switching energy losses of the Si IGBT and the SiC MOSFET ($T_j = 25\ ^\circ$C, $V_{GE} = 15$ V, $R_{G,\,IGBT} = 10\ \Omega$, $V_{GS} = 18\ \Omega$, $R_{G,\,MOSFET} = 0\ \Omega$).

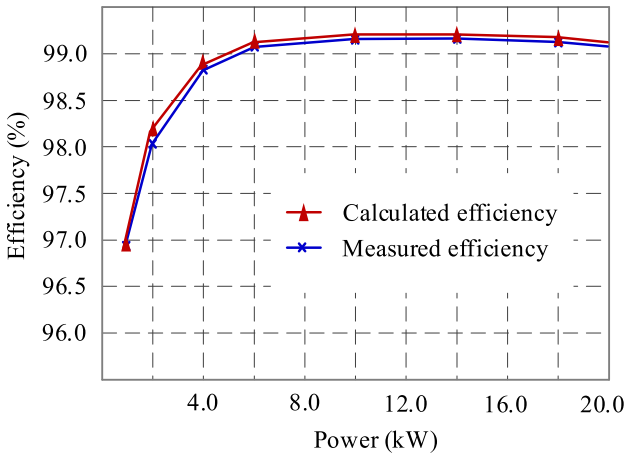

FIGURE 9. Comparison of measured and calculated efficiency for the proposed ANPC inverter for different power levels.

The overall power loss model is then verified using experimental efficiency data. The theoretical power stage efficiency of the proposed inverter is calculated for different load conditions and is compared with the measured power stage efficiency values. For the hybrid Si/SiC switches, the full current rated Si IGBT (IRGP4069DPBF) and the full current rated SiC MOSFET (SCT3030ALGC11) are initially used for the power loss model validation. The optimal current rating ratio between the Si IGBT and SiC MOSFET for the hybrid Si/SiC switches is later determined in Section IV based on the power loss model and the Si/SiC current ratio optimization algorithm. The theoretical switching power loss of the devices is calculated from their energy losses provided in their datasheet at room temperature. Switching energy losses hardly depends on junction temperature [26] so this will not compromise the accuracy of the switching power loss calculation for other junction temperature values.

Conduction power loss is however dependent on the junction temperature of the devices. Therefore, the conduction power loss and junction temperature of the devices are calculated iteratively. First, the conduction power losses of the devices is calculated using (1) from the datasheet parameters at room temperature ($T_j = 25\ ^\circ$C) and the total power losses of the switches is then calculated from their switching and conduction power losses. The junction temperature of the devices is then calculated from the total power loss, junction to case thermal impedance ($Z_{th,(j\text{-}c)}$) and case temperature (T_c) using the thermal model in (8). The case temperature of the devices is measured using thermal image camera for the power loss model validation but for the performance comparison between the different inverters, a reasonable case temperature value can be assumed since this is dependent on the cooling approach. Using the newly calculated junction temperature value, the devices on-state resistance (r) and on-state voltage (V_0) are then calculated as in (9)–(12) assuming linear relationship between these parameters and junction temperature.

$$T_j = (P_{cond} + P_{sw}) \cdot Z_{th,(j-c)} + T_c \tag{8}$$

$$r(T_j) = r(T_1) + \sigma_r(T_j - T_1) \tag{9}$$

$$V_0(T_j) = V_0(T_1) + \sigma_v(T_j - T_1) \tag{10}$$

$$\sigma_r = \frac{r(T_2) - r(T_1)}{T_2 - T_1} \tag{11}$$

$$\sigma_v = \frac{V_0(T_2) - V_0(T_1)}{T_2 - T_1} \tag{12}$$

where, T_j is the junction temperature of the current iteration, σ_r and σ_v are on-state resistance and on-state voltage temperature dependency coefficients, and T_1 and T_2 are the junction temperatures used for test in the device datasheet (usually 25 °C and 125 °C or 150 °C).

Then, using the newly calculated on-state resistance and on-state voltage values, the new conduction power loss is calculated using (1) again and the whole process is repeated until the junction temperatures of two consecutive iterations are sufficiently close to each other. After the conduction power loss and junction temperature calculation iteration is completed, the power stage efficiency is then calculated from the total conduction and switching power losses. Fig. 9 shows the measured and calculated efficiencies of the proposed ANPC inverter system. A resistive load bank (SIMPLEX ELECTRA-700) is used as a load while HIOKI power analyzer (PW6001) is used for the power stage efficiency measurement. The slight difference between the measured and estimated power stage efficiency of the proposed ANPC inverter is due to losses in PCB parasitic elements and connection wires which are not accounted in the inverter theoretical loss estimation. However, these power losses are very small and will not significantly compromise the accuracy of the theoretical power loss model.

IV. HYBRID Si/SiC SWITCH DESIGN

A. GATE CONTROL TECHNIQUES REVIEW

Four gate control options are proposed for hybrid Si/SiC switches in [29]–[31]. These option differ from each other in the relative switching on and switching off timing of the Si

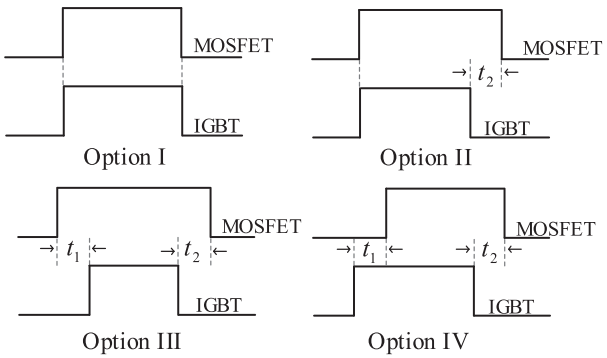

FIGURE 10. Gate control options for hybrid Si/SiC switches.

IGBT and the SiC MOSFET. Fig. 10 shows these gate control options. In the first option (Option I), both the Si IGBT and the SiC MOSFET switch on and switch off simultaneously. This option does not provide significant switching loss reduction since the Si IGBT will still have substantial turn-off energy loss due to its tail current. In the second gate control option (Option II), both devices turn on at the same time, but the Si IGBT turns off before the SiC MOSFET. This option eliminates the turn-off energy loss of the Si IGBT since it is switching off at zero voltage. In the third gate control option (Option III), the Si IGBT turns on after the SiC MOSFET completely turns on and it turns off before the SiC MOSFET turns off. In this gate control option, the SiC MOSFET handles the switching dynamics alone (the Si IGBT switches on and off at zero voltage). Therefore, the switching loss of the Si IGBT is eliminated. In the fourth gate control option (Option IV), the Si IGBT turns on and turns off before the SiC MOSFET. This gate control option eliminates the turn-off energy loss of the Si IGBT, but its turn-on energy loss still exists.

In order to ensure the switching loss reduction benefits of hybrid Si/SiC switches, the gate delay between the Si IGBT and SiC MOSFET (t_1) and (t_2) must be greater than the turn on and turn off times of these devices. The turn on and turn off times also depend on the parasitic elements present in the switching loop. Therefore, it requires careful tuning of the above time difference values to ensure soft switching for the Si IGBT.

B. Si/SiC CURRENT RATING RATIO OPTIMIZATION

Using a low current rated SiC MOSFET and a high current rated Si IGBT for the hybrid Si/SiC switches reduces the cost and conduction loss of the SiC MOSFET. However, smaller current rating means smaller die area (higher thermal resistance). Therefore, a transient temperature peak that could exceed the maximum permissible temperature of the SiC MOSFET will occur during switching if a very small current rated SiC MOSFET is used. If the junction temperature of the SiC MOSFET repeatedly exceeds its maximum permissible value, its material layer will degrade leading to total device failure. This will lead to a subsequent failure of the Si IGBT since it will be subjected to excessive switching loss at high switching

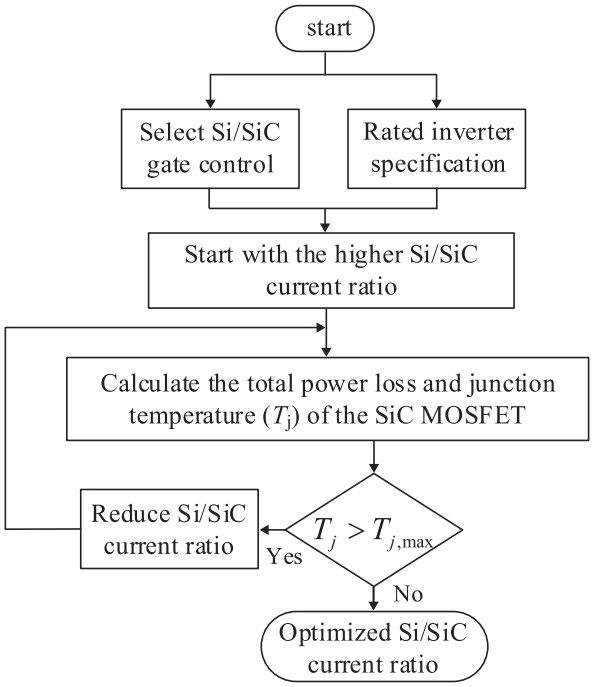

FIGURE 11. Si/SiC current rating ratio optimization algorithm.

frequency when the SiC MOSFET fails. Therefore, the minimum current rating for the SiC MOSFET that ensures a safe operation without its transient peak temperature exceeding its maximum permissible value must be determined to achieve the best tradeoff between cost, loss and reliability.

The optimal Si/SiC current rating ratio that achieves minimum cost and loss with safe operation is determined using the optimization algorithm shown in Fig. 11 which was first proposed in [20] for dc/dc converters. The algorithm determines the maximum junction temperature of the SiC MOSFET from its junction-to-case thermal impedance and total power losses for different Si/SiC current ratios and gate control options for a given inverter operation conditions. The algorithm begins with a higher Si/SiC current ratio value (smaller SiC MOSFET current rating) and reduces the current ratio until the maximum junction temperature of the SiC MOSFET is below its maximum permissible value. The switching power loss of the SiC MOSFET is calculated from its energy losses extracted from its datasheet at room temperature while the conduction and junction temperature of the SiC MOSFET are calculated iteratively as described in Section III. The optimization algorithm ends when the estimated junction temperature of the SiC MOSFET is lower than its maximum permissible value which is typically 175 °C [32].

When gate control option III is used, the SiC MOSFET carries the full load current during the time durations t_1 and t_2. Therefore, it will be periodically stressed with pulsed currents having a peak value over its rating. The current optimization algorithm uses this gate control option as a worst-case scenario to determine the minimum Si/SiC current ratio since it

FIGURE 12. Experimental prototype picture of a 20-kW hybrid Si/SiC switch based ANPC inverter.

TABLE IV Devices Selected For Current Ratio Optimization

ratio	Si IGBT	SiC MOSFET
85:15	IXGR24N60CD1 (600 V, 42.5 A)	SCT2450KEC (650 V, 7.5 A)
80:20	HGTG20N60B3 (600 V, 40 A)	SCT2280KEC (650 V, 10 A)
70:30	RGCL80TK60DGC11 (600 V, 35 A)	SCT3120ALHRC11 (650 V, 15 A)
60:40	IRGPC40S (600 V, 30 A)	SCT3080ALHRC11 (650 V, 20 A)

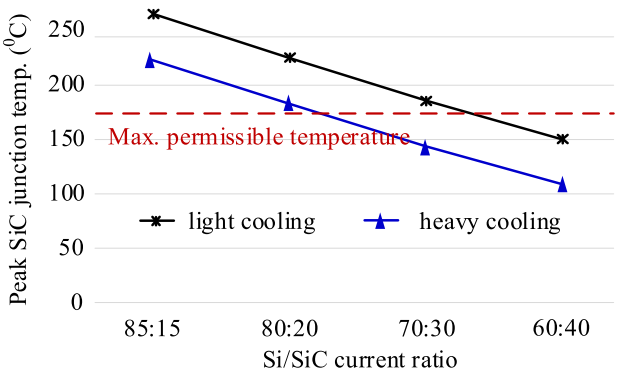

FIGURE 13. Peak junction temperature of the SiC MOSFET for different Si/SiC current ratios.

produces the highest junction temperature for the SiC MOSFET. Having known the gate control option for the hybrid Si/SiC switches, the second set of data required for the current optimization algorithm is the inverter rated specification. To demonstrate the current optimization algorithm, a 20 kW 480 V (*rms*) inverter system shown in Fig. 12 is developed. Table IV shows four different sets of Si/SiC switch combinations that can be used for the hybrid switches for this inverter system. These devices are selected solely based their current rating to demonstrate the current ratio optimization algorithm. In practice, several device figure of merits such as cost, power loss and availability should be considered when selecting devices.

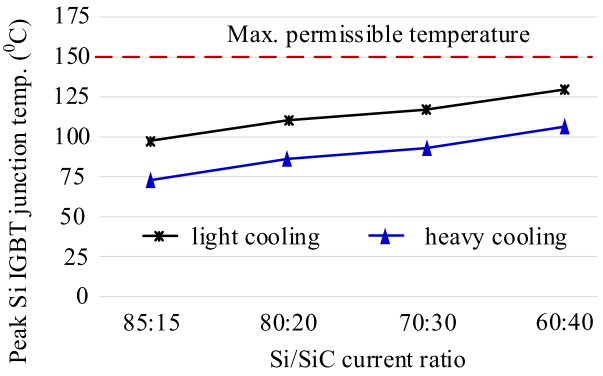

FIGURE 14. Peak junction temperature of the Si IGBT for different Si/SiC current ratios.

Fig. 13 shows the estimated peak junction temperature of the SiC MOSFET for different Si/SiC current ratios and different cooling approaches. For light cooling (for example natural air cooling), the 60:40 Si/SiC current ratio is the optimal choice whereas the 70:30 Si/SiC current ratio is the optimal choice for heavy cooling (for example liquid cooling), to attain the best tradeoff between cost, loss and safe operation. The transient peak junction temperature of the Si IGBT can also be determined using the above optimization algorithm. For the Si IGBT, the highest stress occurs when the first gate control option is used. When this gate control option is used, the Si IGBT experiences hard switching under high switching frequency. Therefore, it will face higher stress compared to other gate control options. Fig. 14 shows the estimated peak junction temperature of the Si IGBT for different Si/SiC current ratios and different cooling methods. The peak junction temperature of the Si IGBT is lower than the typical maximum permissible value for all Si/SiC current ratios and cooling media. Therefore, the SiC MOSFET is the critical component determining the Si/SiC current ratio. Light cooling (air cooled heatsink) is considered for this design, so the 60:40 Si/SiC current ratio is chosen.

V. PERFORMANCE COMPARISON

The performance of the proposed ANPC inverter system is compared with other similar ANPC inverter systems: (a) an all Si IGBT ANPC inverter system, (b) a mixed Si IGBT and SiC MOSFET ANPC inverter system shown in Fig. 6(a), (c) a mixed Si IGBT and SiC MOSFET ANPC inverter system shown in Fig. 6(b), and (d) an all SiC MOSFET ANPC inverter system in terms of inverter efficiency and cost. The inverter system specifications for the performance comparison are shown in Table V. The semiconductor device power loss for the different ANPC inverter systems is compared for different power factor and modulation index values. The cost of the semiconductor devices and the associated gate driving circuitry is also compared for the different ANPC inverter systems to assess the efficiency and cost benefit of the proposed ANPC inverter compared to other ANPC inverter

TABLE V Converter Specification for Performance Comparison

Parameter	Value	Cost
Rated power	20 kW	
Dc-link voltage	800 V	
Output voltage	480 V (*rms*)	
Switching frequency	50 kHz	
Full current Si IGBT	IRGP4069DPBF	$7.02
Full current SiC MOSFET	SCT3030ALGC11	$26.23
Hybrid Si/SiC switches	Si IGBT: IRGPC40S	$5.23
	SiC MOSFET: SCT3080ALHRC	$16.73

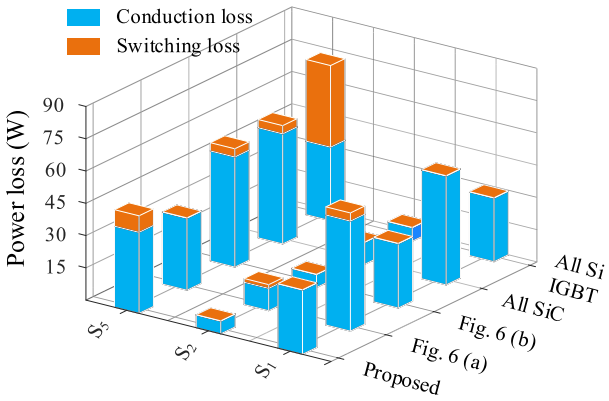

FIGURE 15. Power loss distribution for the different ANPC inverter topologies under unity power factor.

systems. Only the cost of the power stage is considered for the cost comparison in order to have a universal cost comparison for different applications such as motor drives and renewable energy conversion applications.

A. POWER LOSS AND EFFICIENCY COMPARISON

With the data derived from the device datasheet and the help of the power loss model, the power loss of the different ANPC inverter systems is investigated for different operating conditions. In order to have fair comparison with the proposed ANPC inverter, similar modulation strategy (modulation type II) is used for the other ANPC inverter systems except for the ANPC inverter in Fig. 6(a). The semiconductor device configuration for this topology is based on modulation type I hence its efficiency-cost benefits will be discarded if modulation type II is applied.

The power loss distribution of the semiconductor devices for the different ANPC inverters is investigated under different operating conditions. Since the power loss of an ANPC inverter is symmetrical, only the power loss of the upper half devices (S_1, S_2 and S_5) are shown. Fig. 15 shows the power loss distributions for the different ANPC inverter systems under unity power factor. As can be seen from the figure, the

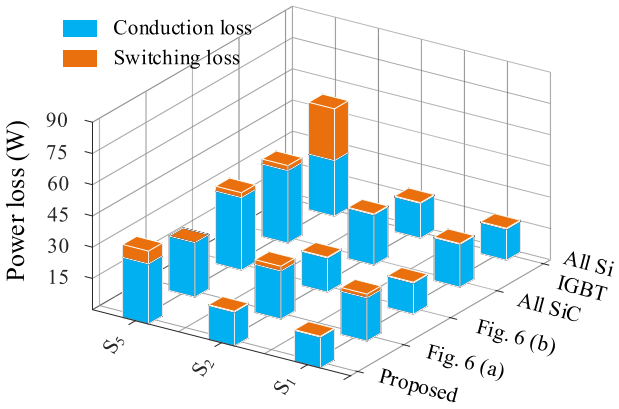

FIGURE 16. Power loss distribution for the different ANPC inverter topologies for low power factor (pf = 0.6).

low frequency switches (S_5 for the topology in Fig. 6(a), and S_1 and S_2 for the other topologies) have negligible switching loss since they commutate at fundamental line frequency. Conduction loss is the dominant one for these devices hence using Si IGBTs for these switches provides lower conduction loss compared to SiC MOSFETs since Si IGBTs have lower conduction loss compared to SiC MOSFET for high output current [23], [25]. For the high frequency switches (S_1 and S_2 for the topology in Fig. 6(a), and S_5 for the other topologies), SiC MOSFETs provide much lower switching loss at the expense of higher conduction loss as can be seen from the power loss of S_5 for the all-Si IGBT, all-SiC MOSFET topologies and the topology in Fig. 6(b). In the proposed ANPC inverter, hybrid Si/SiC switches are used for the high frequency switches. Therefore, it combines the benefits of both Si IGBT (lower conduction loss) and SiC MOSFET (lower switching loss). This is evident from the power loss of S_5; it has lower overall loss compared to the topologies using SiC MOSFET for this switching position.

Fig. 16 shows the power loss distributions for the different ANPC inverter systems for low power factor values. When the power factor is reduced, the inner switches (S_2 and S_3) will have higher power loss due to their higher switching current stress than that for higher power factor values. The phase leg power loss of the inverter shifts more to the inner switches with decreasing power factor value (this topic is investigated in detail in [33]). But this does not affect the overall power loss of the proposed ANPC inverter. The proposed ANPC inverter system still has lower power loss (hence higher efficiency) compared to the other ANPC inverters. The switching loss of the inner switches with Si IGBTs would have increased for low power factor values if they were commutating at carrier frequency. But since they are commutating at fundamental line frequency, their switching loss is negligible.

Fig. 17 shows the power loss distribution of the different ANPC inverter topologies for low modulation indices. The power loss of the different ANPC inverter systems is investigated for a modulation index of 0.4 as an example to

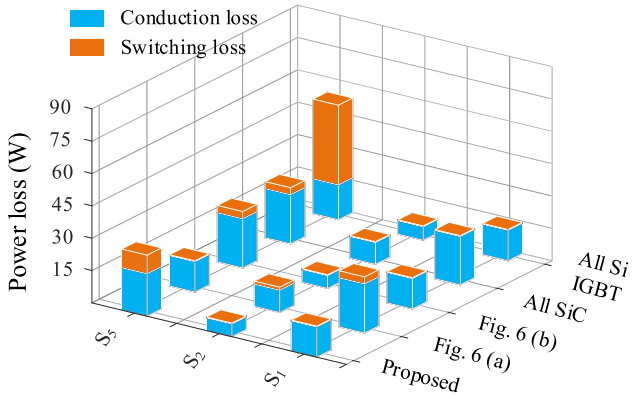

FIGURE 17. Power loss distribution for the different ANPC inverter topologies for low modulation index ($m_a = 0.4$).

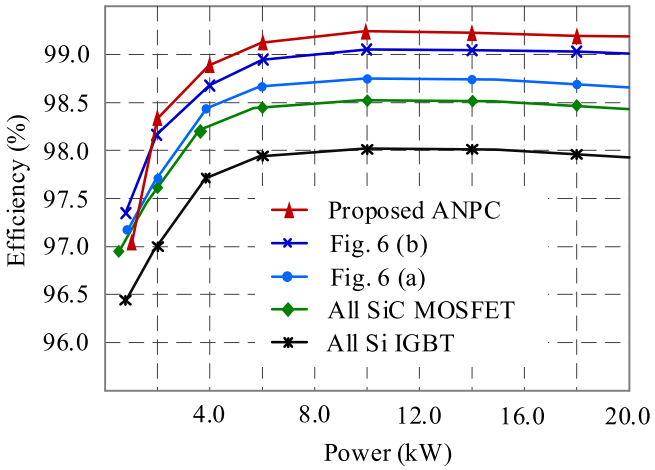

FIGURE 18. Efficiency comparison between the proposed ANPC inverter and other ANPC inverters for inverter operation.

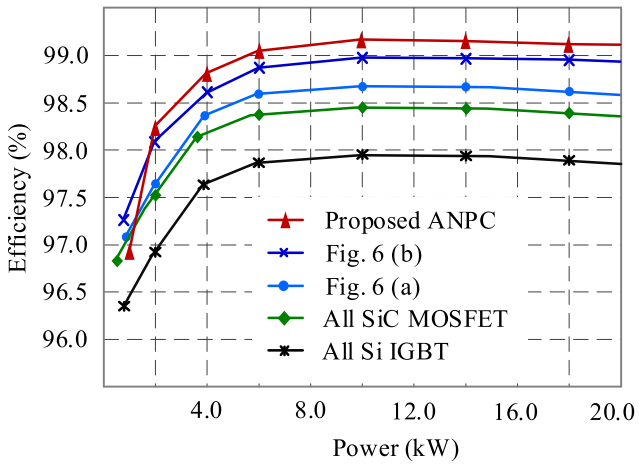

FIGURE 19. Efficiency comparison between the proposed ANPC inverter and other ANPC inverters for rectifier operation.

demonstrate the power losses of the different ANPC inverter systems for low modulation indices. When the modulation index is reduced, the output voltage and current of the inverter reduces hence the output power and the power loss of the semiconductor devices reduces too. But, as can be seen from the figure, the proposed ANPC inverter system still has lower overall power loss (hence higher efficiency) compared to the other ANPC inverters for this modulation index value. But the power loss reduction benefit of the proposed inverter system is lower for lower modulation indices compared to that for higher modulation indices. This is because the conduction loss benefits of Si IGBTs compared to SiC MOSFET reduces with lower current and for very low output current Si IGBTs actually have higher conduction loss than SiC MOSFETs [23], [25].

Therefore, the proposed ANPC inverter system will have slightly higher power loss (lower efficiency) than the all-SiC MOSFET topology and the topology in Fig. 6(a) for very small modulation indices. However, power converters commonly operate at high modulation index, so this is not necessarily a drawback for the proposed ANPC inverter.

The efficiency of the different ANPC inverter systems is shown in Fig. 18 and Fig. 19 for different power levels for both inverter and rectifier operation. As can be seen from these figures, the proposed ANPC inverter system achieves higher efficiency compared to the all Si IGBT based ANPC inverter system, the all SiC MOSFET based ANPC inverter system and the mixed Si IGBT and SiC MOSFET based ANPC inverter systems for different power levels. As it is evident from the above power loss analysis, the proposed ANPC inverter system also has higher efficiency compared to the other ANPC inverter systems for low power factor and modulation index values.

B. COST COMPARISON

The inverter cost for the different semiconductor device configurations is estimated using off-the-shelf component prices as shown in Table V obtained from digikey website. The cost of the inverter PCB, housing and cooling system is generally fixed and accounts for approximately 50 percent of the total inverter cost [35]. Therefore, the cost of these components is not considered for the cost comparison between the different ANPC inverter systems; only the semiconductor devices and their associated gate driving circuitry cost are considered. Fig. 20 shows the estimated semiconductor device and gate driver costs for the different ANPC inverter systems. The figure shows the proposed ANPC inverter system has a comparable semiconductor device cost with an all Si IGBT based ANPC inverter system and lower semiconductor device cost compared to the mixed Si IGBT and SiC MOSFET ANPC inverter systems and the all SiC MOSFET ANPC inverter system. The proposed ANPC inverter system however has a slightly higher gate driving circuit cost. This is because the hybrid Si/SiC switches are currently individually driven by a separate gate driver. However, research is underway to reduce the cost and complexity of gate driver for hybrid Si/SiC switches. In [36], a single gate driver for the hybrid Si/SiC

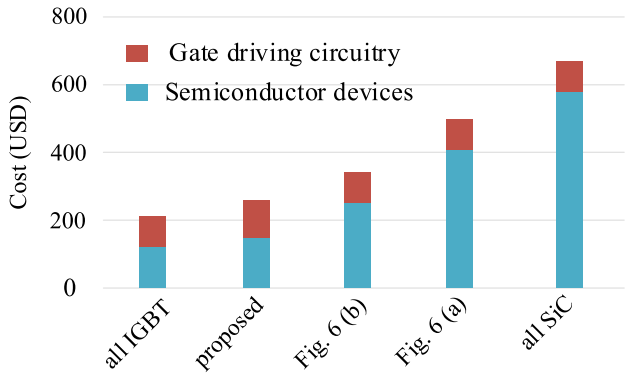

FIGURE 20. Variable inverter cost comparison for different ANPC inverter configurations.

switches is designed and experimentally validated. It features lower cost and lower complexity compared to the conventional gate driving approach for hybrid Si/SiC switches. Therefore, the slightly higher gate driving circuit cost of the proposed ANPC inverter at the moment will not be necessarily a drawback in the future.

VI. EXPERIMENTAL RESULTS

The operation of the proposed ANPC inverter is validated by experimental test. A double-pulse test (DPT) experiment is first conducted on the actual inverter phase leg to validate the switching characteristics and current sharing of the hybrid Si/SiC switches. The device current for the Si IGBT and SiC MOSFET are measured using Tektronix Ultra Mini Rogowski current probe (TRCP0300). This current measurement technique is suitable for TO-247 packaged devices since it can easily clamp around the device legs. The forward voltage is measured using active differential voltage probe (THDP0200). It should be noted that this voltage measurement technique is not the best choice since it introduces additional loop inductance and hence pronounces the measured voltage overshoot. It is used for this test due to its simplicity and availability.

Gate control option III is used for the hybrid Si/SiC switches to enable soft switching for the Si IGBT. In this gate control strategy, the Si IGBT is turned on after the SiC MOSFET is fully turned on and the SiC MOSFET is turned off after the Si IGBT is fully turned off as shown in Fig. 23 to achieve zero voltage switching (ZVS) for the Si IGBT. However, in order to guarantee ZVS for the Si IGBT, the gate turn on delay time ($T_{\text{on\_delay}}$) between the Si IGBT and the SiC MOSFET gate signals must be greater than the turn on time (t_{on}) of the SiC MOSFET and the gate turn off delay time ($T_{\text{off\_delay}}$) between the Si IGBT and the SiC MOSFET gate signals must be greater than the turn off time (t_{off}) of the Si IGBT. The turn on and turn off times of the SiC MOSFET and the Si IGBT can be extracted from their datasheet by applying current and voltage scaling factor as shown (13) and (14).

$$t_{\text{on}} = t_{\text{d(on)}} + \left(\frac{I_{\text{L}}}{I_0}\right) t_{\text{ri}} + \left(\frac{V_{\text{L}}}{V_0}\right) t_{\text{fv}} \tag{13}$$

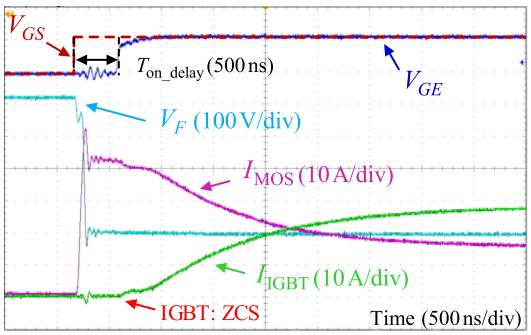

FIGURE 21. Turn on characteristics of the hybrid Si/SiC switches.

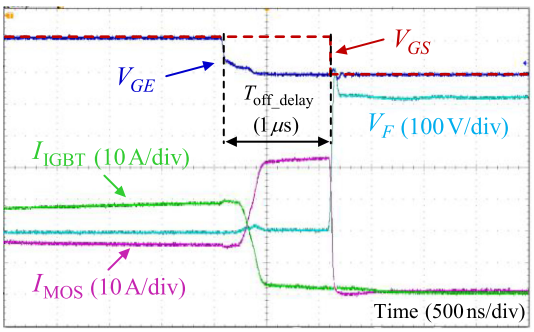

FIGURE 22. Turn off characteristics of the hybrid Si/SiC switches.

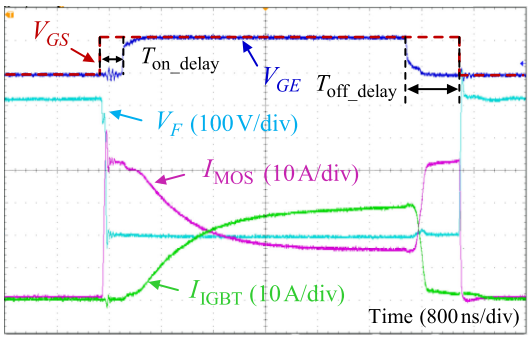

FIGURE 23. Switching and conduction characteristics of the hybrid Si/SiC switches.

$$t_{\text{off}} = t_{\text{d(off)}} + \left(\frac{I_{\text{L}}}{I_0}\right) t_{\text{fi}} + \left(\frac{V_{\text{L}}}{V_0}\right) t_{\text{rv}} \tag{14}$$

where $t_{\text{d(on)}}$ and $t_{\text{d(off)}}$ are the turn on and turn off delay time of the SiC MOSFET and the Si IGBT, I_{L} and V_{L} are the load current and load voltage of the specific application, I_0 and V_0 are the test current and test voltage of the datasheet, t_{ri} and t_{rv} are the current and voltage rise times, t_{fi} and t_{fv} are the current and voltage fall times.

However, the actual turn on and turn off times of the Si IGBT and SiC MOSFET depend on the parasitic inductance of the converter circuit. Large parasitic inductance decreases the switching speed of the devices hence the required turn on and turn off delay time would be greater than the turn on and turn off times of the SiC MOSFET and Si IGBT calculated from their datasheet. Therefore, the actual turn on time of the SiC

MOSFET and turn off time of the Si IGBT are experimentally measured using double-pulse test to determine the optimum turn on and turn off delay times between the Si IGBT and the SiC MOSFET gate signals required for this specific application. Based on the measured turn on time of the SiC MOSFET and turn off time of the Si IGBT, a turn on delay time of 500 ns and a turn off delay time of 1 μs are used. The turn on delay time is smaller than the turn off delay time since the former depends on the turn on speed of the SiC MOSFET and the later depends on the turn off speed of the Si IGBT.

Fig. 21 shows the turn on characteristics of the hybrid Si/SiC switches. During the turn on transient of the SiC MOSFET, the gate voltage (V_{GE}) of the Si IGBT should be zero. However, there will be a small oscillatory voltage as shown in the figure induced in the gate voltage of the Si IGBT due to the parasitic crosstalk effect of the SiC MOSFET and the Si IGBT. The fast changing SiC MOSFET gate current induces ringing voltage on the Si IGBT gate voltage. In order to make sure this phenomenon does not cause false triggering for the Si IGBT, a negative gate driving voltage (−4 V) is used. The value of the negative gate driving voltage depends on the magnitude of the ringing voltage (which in turn depends on the parasitic inductance of the converter circuit) and the threshold voltage of the Si IGBT. Larger negative gate driving voltage provides higher noise immunity, but it increases the switching energy loss of the Si IGBT since it increases the gate driver swing voltage. Fig. 22 shows the turn off characteristics of the hybrid Si/SiC switches.

Fig. 23 shows the conduction (static) characteristics of the hybrid Si/SiC switches. When gate control Option III is used, the SiC MOSFET carries the full forward current during the turn on and turn off process, but during conduction, the forward current is shared between the two devices according to their current rating. Based on the Si/SiC current rating optimization algorithm, the Si IGBT is designed to conduct 60 percent of the forward current and the SiC MOSFET is designed to conduct 40 percent of the forward current for the application considered in this paper. For other power levels and operating conditions, the optimal current sharing between the Si IGBT and the SiC MOSFET should be determined using the Si/SiC current ratio optimization algorithm.

In order to verify the thermal performance of the hybrid Si/SiC switches, the case temperature of the hybrid Si IGBT and SiC MOSFET devices is measured using infrared thermal image camera (FLIR C2) because of the difficulty of measuring the junction temperature of discrete power devices. The respective junction temperature value of the Si IGBT and SiC MOSFET is then estimated from the measured case temperature value using the device power loss and thermal model. Fig. 24 shows the measured case temperature and the estimated junction temperature of the hybrid Si IGBT and SiC MOSFET switches for different power levels. The figure shows the junction temperature of the hybrid Si/SiC switches is below their respective maximum permissible values for the different power levels. Therefore, the hybrid Si/SiC switches design is reliable.

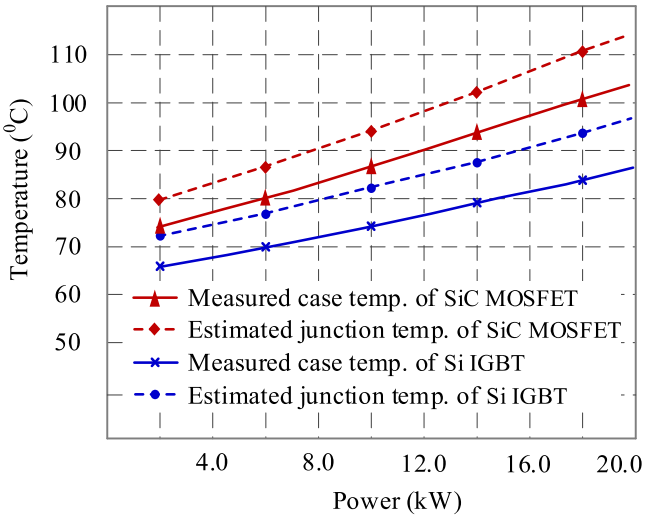

FIGURE 24. Measured case temperature and estimated junction temperature for the hybrid Si/SiC switches for different power levels.

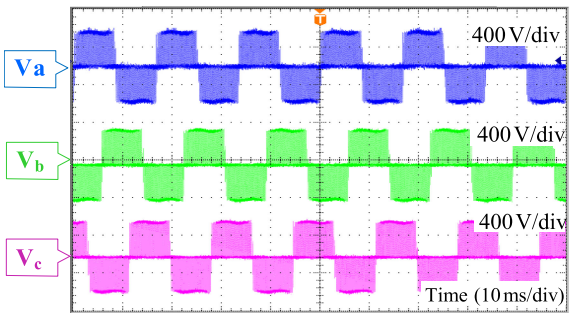

FIGURE 25. Inverter phase output voltage waveforms.

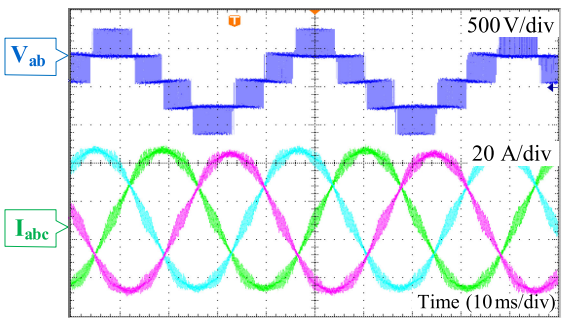

FIGURE 26. Inverter output line-to-line voltage and three-phase to output current waveforms.

The overall operation of the inverter is also tested. In terms of the overall operation of the inverter, using hybrid Si/SiC switches will not affect the operation of the inverter with respect to the output voltages and currents of the inverter since the operation of power converters fundamentally depends on the modulation (control) strategy and the output filter of the converter. Fig. 25 shows the three-phase output voltages of the inverter and Fig. 26 shows the line-to-line output voltage

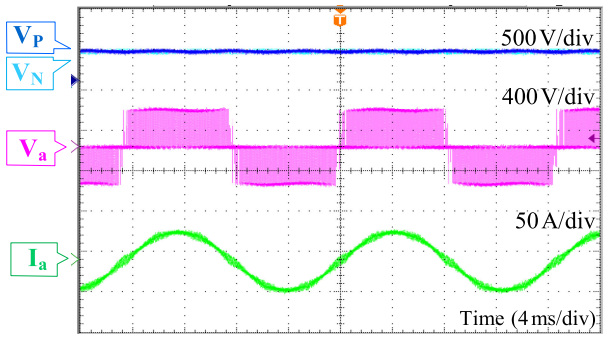

FIGURE 27. Dc-link capacitor voltages, output voltage and output current waveforms.

and three phase output currents of the inverter. The slightly higher ripples in the output current waveform are due to the output filter. Only one three phase reactor of 170 μH is used for the test just to verify the output waveforms of the inverter. In practice, a load side inductor and parallel capacitor would be required to eliminate these high frequency ripples. Fig. 27 shows the dc-link capacitor voltage waveforms along with the inverter phase voltage and current waveforms. The carrier-based dc-link capacitor voltage balancing strategy presented in [37] is used to achieve dc-link capacitor voltage balancing.

VII. CONCLUSION

This paper presented the design and validation of a high efficiency and low cost three-level Active Neutral Point Clamped (ANPC) inverter employing hybrid Si/SiC switches. It uses a modulation strategy that creates a group of low frequency switches commutating at fundamental line frequency and high frequency switches commutating at carrier frequency to enable the use of hybrid Si/SiC switches. Si IGBTs are used for the low frequency switches while hybrid Si/SiC switches are used for the high frequency switches to reduce the cost and power loss of the inverter. In order to fully leverage the benefits of hybrid Si/SiC switches while guaranteeing safe operation, an Si/SiC current ratio optimization algorithm is presented. The optimization algorithm determines the minimum Si/SiC current rating ratio that provides low cost, low loss and safe operation based on the inverter specifications and Si/SiC gate control strategy.

The proposed ANPC inverter system provides higher efficiency compared to an Si IGBT based ANPC inverter system, an SiC MOSFET based ANPC inverter system and mixed Si IGBT and SiC MOSFET based ANPC inverter systems for different power levels and operation modes. On the other hand, the semiconductor device cost of the proposed ANPC inverter system is comparable with an ANPC inverter system containing only Si IGBTs and much lower than an ANPC inverter system consisting only SiC MOSFETs or mixed Si IGBT and SiC MOSFETs. The gate driver cost for the proposed ANPC inverter system is currently slightly higher. But research is underway to reduce the cost and complexity of gate driver for hybrid Si/SiC switches and there are positive results in literature already. Therefore, this is not necessarily a drawback in the future.

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