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Topology, Design, and Characteristics of a Modular, Dynamic 100 kA Surge Current Source With Adjustable Current Shape

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ABSTRACT To guarantee sufficient surge current fault protection for power electronic converters, power semiconductors have to be tested under appropriate surge current conditions. Standard maximum surge current values include the permissible fault current amplitude, or the I^2t-value; however, they might not be sufficient to describe a power semiconductor's performance under all potential fault conditions. Surge current sources based on passive components are state-of-the-art, but are limited to usually only one specific current waveform. This article describes the topology and the design of a new modular and highly dynamic surge current source for power semiconductor tests with adjustable current waveforms. The new modular converter concept is introduced, with two potential operation modes: High current mode (HCM) and dynamic current mode (DCM). The requirements for the surge current tester are defined, and the electrical and mechanical design are described, including the modulation scheme and control. Experimental investigations prove the function of the current source with peak currents up to 100 kA (HCM) and the realization of highly dynamic load current trajectories with peak currents up to 50 kA (DCM). The output current ripple is exceptionally small with a theoretical value of below 1%.

INDEX TERMS Circuit testing, power electronics, pulse power systems, power semiconductor devices, power semiconductor switches, semiconductor device testing, test equipment.

I. INTRODUCTION

A. MOTIVATION

Power semiconductors are the key components of power electronics. They determine topology, design, and characteristics of converters and applications. For high power applications, diodes and thyristors are particularly important. Diodes play an important role in rectifiers and, as inverse diodes, also in voltage source converters (VSC) with IGBTs, IGCTs, or, e.g., SiC-MOSFETs. Thyristors are applied in high power converters such as high-voltage direct-current, medium voltage drives (e.g., LCI, cycloconverters), or high current rectifiers (e.g., electrolysis) and as protective devices (e.g., crowbar, bypass switch) in medium voltage converters, modular multilevel converters or doubly-fed induction machines (e.g., [1] and [2]).

One important device characteristic of power semiconductors is the overcurrent capability, which plays a major role in the design of a converter regarding fault events. The overcurrent ratings of diodes and thyristors are quantified using two values: the maximum surge current I_{TSM} and the I^2t-value. If the device surge currents do not exceed these values, the device manufacturer guarantees that the power semiconductors are not destroyed.

Both the maximum surge current I_{TSM} and the I^2t-value are defined for a half-sinusoidal current pulse with a pulse duration $T_{\mathrm{P}} = 10$ ms [3]. These parameters are related to each

other for a given sinusoidal current waveform as shown in the following equation [4]:

$$I^2t := \int_0^{T_\mathrm{p}} I_\mathrm{TSM}^2 \cdot \sin^2(\omega t)\,\mathrm{d}t = \frac{1}{2} I_\mathrm{TSM}^2 T_\mathrm{p}. \tag{1}$$

While these specifications are suitable for power semiconductors in line-commutated converters, the current stress of diodes in VSC or thyristors as protective device (e.g., in crowbars in the rotor of doubly fed induction machines [5]) differ significantly from a half-sine current shape with a pulse duration $T_\mathrm{P} = 10$ ms.

For press-pack thyristors or diodes, a typical immediate failure mechanism associated with destructive surge currents is the melting of the silicon structure itself. This is triggered by current filamentation at localized hot spots caused by a thermal runaway effect based on the high intrinsic conductivity of silicon at high temperatures: the device becomes thermally unstable [6], [7], [8].

Surge current failures of diodes or thyristors in modules are typically caused by the electro-thermal stress of the module structure or relatively small chip areas. Depending on the location of the heat generation and the local conditions for heat dissipation, damage occurs at different points. It is known that for very short pulses with large amplitudes, the heat generated in the semiconductor cannot be dissipated and the semiconducting material melts. For pulses with longer duration and lower amplitude, the device failure typically occurs at the connection between chip and aluminum wire [9].

These different failure mechanisms imply that both the duration and the shape of the current pulse play a role in the overload capability of power semiconductors. A characterization with a half-sinusoidal current pulse with fixed pulse duration T_P of 10 ms is a good indicator, but not sufficient for many applications. For this reason, many devices are tested in specific circuit configurations where the surge current's shape, amplitude, and duration are tailored to the application. The development, design, and realization of such test configurations is time consuming and expensive. To reduce this high expense for special circuit configurations, a pulse current source with adjustable current shape is required that can realize application-specific surge current waveforms.

B. REQUIREMENTS

Surge current capability is interesting for conventional power electronic devices like diodes and thyristors made from silicon, as well as, for example, IGBTs for automotive applications [10]. It is also an important parameter for emerging semiconductor technologies, such as SiC-MOSFETs and SiC-diodes. The nominal maximum peak current of thyristors reaches into the range above 90 kA (see, e.g., [11], [12], and [13]), while the peak currents of, e.g., the body diode of a SiC-MOSFET is significantly smaller (e.g., 4.7 kA for a 2200 V, 750 A SiC-MOSFET [14]). Therefore, it is necessary to control the output current over a wide amplitude range.

As discussed, the current waveform heavily depends on the application and the operating conditions. In order to cover a wide range of applications, the current source must be able to realize the desired current waveform with high accuracy. This means fast current changes and a low current ripple through the device under test (DUT) are required. Thus, an accurate and fast control scheme for the adjustable current is necessary.

C. STATE-OF-THE-ART

The standard solutions for generating high-amplitude pulse currents are based on the usage of passive components, either as a resonant circuit or via capacitor discharge into a resistive load. Currents up to the MA-range are achievable, for example, in applications for lightning simulation [15] or railgun applications [16]. This concept can be extended to repetitive pulse current sources based on recuperation of the residual energy left after each current pulse, e.g., [17] and [18]. However, these solutions can only generate fixed current waveforms with specific frequencies and time constants.

As an alternative, Verevkin et al. [19] present a current source that can be programmed in terms of the output current waveform. The authors of [19] propose a massive parallelization of 9360 MOSFET power amplifiers. This analog approach leads to very high power losses in its power transistors (6.14 MW average during a 120 kA half-sine current pulse), which greatly limits the pulse duration (10 ms) and repetition rate (one pulse per minute). The maximum current amplitude is also highly dependent on the chosen waveform (120 kA for half-sine wave, 16 kA for trapezoidal wave).

D. CONTRIBUTIONS OF THIS ARTICLE

As discussed earlier, state-of-the-art surge current sources are limited in either current amplitude or flexibility of the desired waveform. Therefore, the authors aim to develop a surge current source that overcomes these drawbacks. The current source should meet the target parameters as listed in Table 1.

In order to meet all requirements, the authors developed a surge current source with two modes of operation. The high current mode (HCM) focuses on achieving a maximum output current of 100 kA through parallel connection of 32 half-bridges (HBs). In the increasing current slope, this approach maximizes the $\mathrm{d}i_\mathrm{DUT}/\mathrm{d}t$, however, during decreasing current slopes, the $\mathrm{d}i_\mathrm{DUT}/\mathrm{d}t$ becomes dependent on the specific characteristics of the DUT.

To control the current during negative current slopes, the authors propose a parallel connection of 16 full bridges, which is called the dynamic current mode (DCM). This limits the maximum peak current to 50 kA. The absolute value for $\mathrm{d}i_\mathrm{DUT}/\mathrm{d}t$ is lower, but it is fully controlled during the entire current pulse. See also Table 2, Figs. 1 and 2.

The rest of this article is organized as follows. Section II presents the chosen topology as well as the electrical and mechanical design rules. The design for control hardware and software is given in Section III. Section IV presents the experimental verification of the correct operation of the apparatus.

TABLE 1. Surge Current Source Target Parameters

Parameter	Range	Notes
Maximum dc-link voltage $V_{C,x}$	1200 V	Low voltage, i.e., below 1500 V dc, for safety reasons
Maximum IGBT voltage V_{CES}	1700 V	Usage of low voltage IGBTs
Maximum stored energy ΣW_C	104 kJ	To guarantee specified pulse properties
Maximum current I_{pk}	100 kA	–
Maximum current ripple $I_{ripple,DUT}$	60 A	Equals 0.6 ‰ at 100 kA; see Fig. 14
Minimum current rise time t_r	380 µs	Controller-limit, see Table V
Maximum di_{DUT}/dt	768 A/µs	Hardware-limit, see Table II
	263 A/µs	Resulting from t_r and assuming 100 kA
Maximum pulse width T_p	≈ 1 ms … ≈ 100 ms	Min/max width, dependent on waveform and peak current
Freely programmable current waveform	–	within Surge Current Source's limits, common examples: see Fig. 6
Pulse trains with multiple consecutive current pulses	–	Maximum number dependent on waveform and peak current

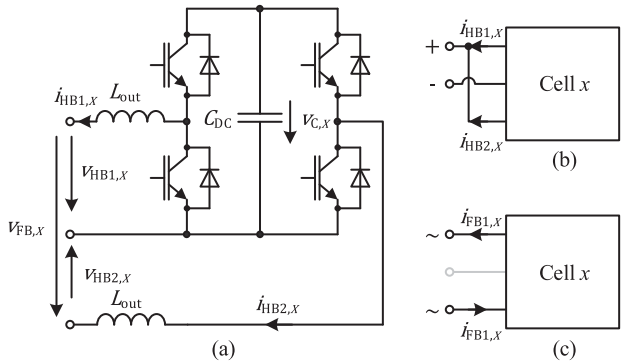


FIGURE 1. Electrical schematic of a cell. (a) Connections of semiconductors, dc-link, and output inductances within a cell. (b) Connection of the outputs for HCM. (c) Connection of the outputs for DCM.

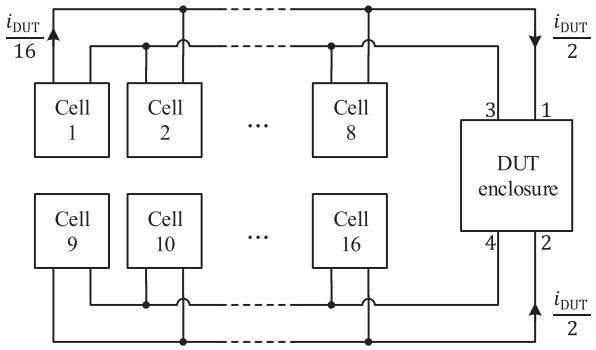


FIGURE 2. Block diagram showing the modular concept of the surge current source. The four connection points into the DUT enclosure are denoted as 1–4.

TABLE 2. Maximum and Minimum Current Slope di_{DUT}/dt in HCM and DCM

	$\frac{di_{DUT}}{dt} > 0$	$\frac{di_{DUT}}{dt} < 0$
HCM	Max. 768 A/µs	Min. n/a
DCM	Max. 192 A/µs	Min. −192 A/µs

Note: The falling di_{DUT}/dt is not intrinsically determined in HCM, since it depends on the load parameters.

II. DESIGN OF THE CURRENT SOURCE

A. MODULAR CONCEPT

Adjustable current waveforms with amplitudes up to 100 kA, an extraordinarily low current ripple (e.g., $I_{ripple,DUT} < 1\%$) and low losses encourage a modular topology of parallel connected cells with staggered switching.

Figs. 1 and 2 show the chosen topology for one cell and a block diagram of the modular converter. Each cell consists of a dc-link capacitor C_{DC} and two HBs with an output inductor L_{out} each. For reasons of safety, a dc-link voltage in the low voltage domain (below 1500 V dc) is required. An advisable selection for power semiconductors should focus on 1.7 kV IGBTs. Based on availability and price, the high power (1700 V, 1800 A) HB IGBT-modules *FF1800R17IP5* from *Infineon* are chosen as power semiconductors (datasheet: [20]). HB modules have the added benefit of a physically small circuit and thus potentially low stray inductance. It should be noted that other types of IGBT switches could also be a viable alternative.

The cells can be configured to operate as two separate HBs or one full bridge. The current source consists of 16 cells. Eight cells, connected to each other by mutual copper bars, are arranged on each side (Fig. 2). Both halves are connected close to the DUT. This structure is very advantageous for mechanical reasons, mainly to reduce the occurring magnetic forces.

Fig. 3 shows an equivalent circuit model of the output circuit, including the DUT. The output circuit is characterized by the pulsed output voltage v_{out} provided by the parallel connected cells, the inductance L_{eff}, and the equivalent circuit of the DUT.

If the cells are connected in HB configuration, the HBs of each cell work independently from each other with equal or different duty cycles $d_{y,x}$. This operation mode is referred to as

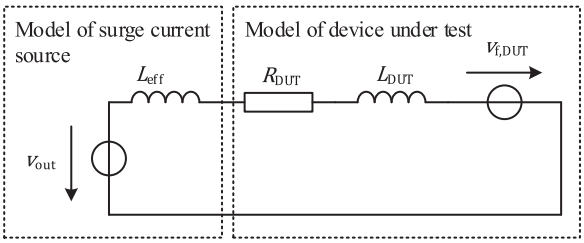


FIGURE 3. Simplified equivalent circuit for surge current source and DUT.

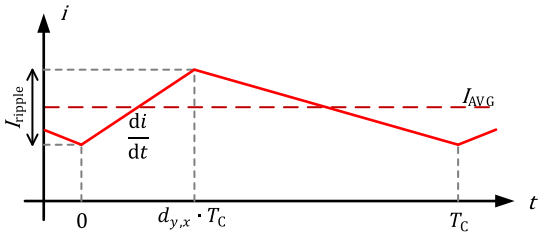


FIGURE 4. Definition of parameter I_{ripple} in comparison to the average current I_{AVG}. Display of one period $T_{\mathrm{C}} = 1/f_{\mathrm{C}}$ with duty cycle $d_{y,x} \cdot T_{\mathrm{C}}$ being highlighted as well as the slope $\mathrm{d}i/\mathrm{d}t$ of the rising current.

HCM. The maximum output current amplitude is given by the parallel connection of 32 HB modules. The HB output voltage $v_{\mathrm{HB},y,x}$ (with $x, y \in \mathbb{N}$ and $x = [1, N_{\mathrm{C}}]$, $y = [1, 2]$) is either zero or corresponds to the dc-link voltage $v_{\mathrm{C},x}$: $v_{\mathrm{HB},y,x} = \{0, v_{\mathrm{C},x}\}$. Thus, a rising or constant output current $i_{\mathrm{DUT}} = f(t)$ can be adjusted and controlled. However, the minimum output voltage of $v_{\mathrm{out}} = 0$ is the reason that a falling output current $i_{\mathrm{DUT}} = f(t)$ is determined by the inductance of the output circuit and the DUT characteristics (resistance, voltage drop).

If the cells are configured as full bridges the cell output voltage features three levels $v_{\mathrm{FB},x} = \{-v_{\mathrm{C},x}, 0, v_{\mathrm{C},x}\}$. The option of positive and negative output voltages enables a control of rising, constant, or falling output currents $i_{\mathrm{DUT}} = f(t)$. Therefore, this configuration is called DCM. The maximum output current amplitude in DCM is given by the parallel connection of 16 full bridge cells and corresponds to half that of the HCM.

B. ELECTRICAL DESIGN CONSIDERATIONS

The electrical design considerations include the dimensioning of the dc-link capacitance C_{DC} per cell and the cell output inductance L_{out} per HB, as well as the switching frequency f_{C}, while taking into consideration the properties of chosen semiconductor switches. As a result, the electrical behavior and limits of the surge current source can be defined.

The required output inductance is estimated based on the switching frequency and maximum permissible switch current (including ripple). A low switching frequency would be beneficial in terms of switching losses, however, a high switching frequency leads to a lower current ripple and/or a lower inductance L_{out}. As a compromise, a switching frequency of $f_{\mathrm{C}} = 3$ kHz per HB is chosen. Interleaved switching results in an effective switching frequency of $f_{\mathrm{S}} = 96$ kHz. For N_{C} cells in HCM ($2 \cdot N_{\mathrm{C}}$ HBs, respectively) the permissible ripple current per HB, $I_{\mathrm{ripple,max}}$, depends on the maximum peak output current $I_{\mathrm{pk}} := \max(i_{\mathrm{DUT}})$, and the maximum permissible repetitive switching current I_{CRM} per switch

$$I_{\mathrm{ripple,max}} = 2\left(I_{\mathrm{CRM}} - \frac{I_{\mathrm{pk}}}{2 \cdot N_{\mathrm{C}}}\right). \tag{2}$$

The ripple current I_{ripple} is defined as shown in Fig. 4. As can be seen from (2) both ripple and DUT-current contribute to the IGBT current. In order to maximize peak pulse current I_{pk}, the ripple current has to be kept at a minimum (within the constraints set by other parameters). The actual ripple current in HCM for the HB y,x can be calculated by the voltage across the corresponding inductor L_{out} during the time interval $0 \leq t \leq d_{x,y}T_{\mathrm{C}}$, with

$$I_{\mathrm{ripple}} = \int_0^{d_{x,y}T_{\mathrm{C}}} \frac{v_{\mathrm{C},x}(t) - v_{\mathrm{HB},y,x}(t)}{L_{\mathrm{out}}} \tag{3}$$

being derived from Figs. 1 and 4. Approximating both $v_{\mathrm{C},x}$ and $v_{\mathrm{HB},y,x}$ to be constant during one period T_{C}, the numerator in (3) can be simplified to $(1 - d_{y,x})v_{\mathrm{C},x}$. The integral can also be simplified as a multiplication. This leads to (4). The ripple current in HCM for HB y,x

$$I_{\mathrm{ripple}} = \frac{(1 - d_{y,x}) \cdot d_{y,x} \cdot v_{\mathrm{C},x}}{L_{\mathrm{out}} \cdot f_{\mathrm{C}}} \tag{4}$$

is dependent on various factors, including the capacitor voltage $v_{\mathrm{C},x}$, the duty cycle of the HB $d_{y,x}$, the switching frequency f_{C}, and the output inductance L_{out}.

To limit the ripple current, the following considerations are made. The switching frequency is limited by the thermal dimensioning of the IGBT. Both duty cycle $d_{y,x}(t)$ and capacitor voltage $v_{\mathrm{C},x}(t)$ are dependent on the DUT. The remaining way to limit ripple current, and thus increase the maximum DUT-current is by increasing the inductance L_{out}. However, this presents a trade-off, as increasing the output inductance results in a decrease in the maximum $\mathrm{d}i/\mathrm{d}t$ and therefore limits the dynamic performance of the surge current source, while also increasing the mechanical dimensions. The current $\mathrm{d}i/\mathrm{d}t$-limits imposed by the hardware – depending on dc-link voltage $v_{\mathrm{C},x}$ and output inductance L_{out} – are listed in Table 2.

Fig. 5 depicts the maximum permissible current $I_{\mathrm{pk,max}}$ versus duty cycle and capacitor voltage for a chosen output inductance of 50 μH. It also highlights the permissible curve for a 100 kA pulse. The 50 μH inductance does not permit every potential operation point. To protect the HB IGBTs, the test setup's controller does not permit operation outside of the depicted safe operating area (SOA).

Power semiconductor devices (such as diodes or thyristors) with a maximum surge current in the region around 100 kA usually have a forward threshold voltage of approximately $V_{\mathrm{f,DUT}} \approx 1$ V or lower and an on-state resistance significantly lower than $r_{\mathrm{DUT}} \approx 1$ mΩ, as shown in, e.g., [21], [22], and [23].

In the following analysis, a forward threshold voltage of 1 V and a worst-case resistance of the entire system (DUT + test

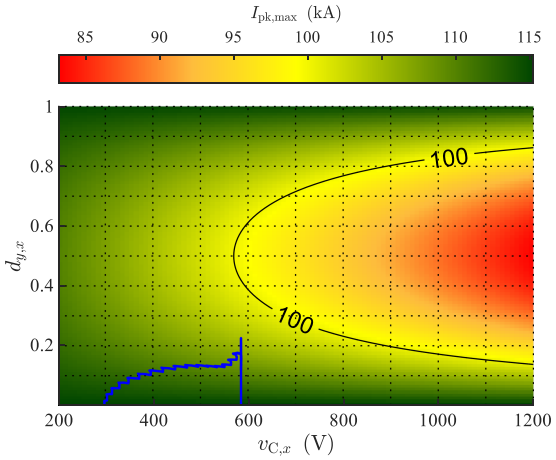


FIGURE 5. Maximum DUT-current as a function of capacitor voltage and duty cycle considering the current limit of 3.6 kA per IGBT in HCM. As an example, the blue line depicts the measured capacitor voltage versus duty cycle trajectory for a 100 kA, 10 ms half-sine current pulse with a short-circuit load.

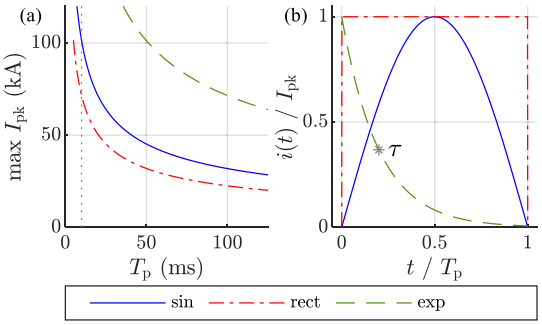


FIGURE 6. (a) Possible peak currents I_{pk} versus pulse duration T_p for sinusoidal (sin), rectangular (rect), and capacitor discharge (exp) current waveforms; single pulse. (b) Definition of specified current waveforms.

setup) of $ESR_0 \approx 2$ mΩ, as well as a capacitor charging voltage of 1.2 kV (charging prior to the current pulse) are assumed.

Under those conditions the curves for maximum peak currents I_{pk} versus pulse duration T_p (single pulse) for a sinusoidal, a rectangular, and a capacitor discharge current waveform are shown in Fig. 6. Alternatively, a pulse train of multiple current pulses is possible, albeit with a lower peak current per pulse, depending on the desired number of consecutive current pulses.

Under the assumptions made earlier, the amount of energy required for one 100 kA, 10 ms sinusoidal current pulse is approximately 100 kJ. For 16 cells, this results in a required cell capacitance of $C_C = 9$ mF. The amount of stored energy is therefore $\Sigma W_C \approx 104$ kJ. In practice, the capacitance per cell can also be a trade-off between stored energy and, e.g., physical size of the type of capacitor that is used.

C. MECHANICAL DESIGN CONSIDERATIONS

One main factor to consider for the mechanical design is the forces acting upon the conductors caused by the high peak

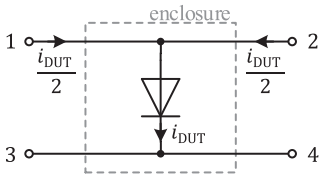


FIGURE 7. DUT (example: Diode) with two currents forming the total current I_{DUT}. Note: The currents flow into the enclosure on opposite sides.

current. Emphasis should be put on reducing occurring forces first, and reinforcing mechanical elements second.

Ampère's Force Law

$$\frac{F_m}{l} = \frac{\mu_0}{2\pi} \cdot \frac{i_1 \cdot i_2}{r} \tag{5}$$

describes the dependence of the magnetic force F_m between two thin, parallel conductors on their currents i_1 and i_2, their distance r and the permeability μ_0 (with $\mu_r \approx 1$ in air), per length l of the conductors. Three relevant conclusions can be drawn from (5):

1) The length l of conductors running high currents parallel to each other should be kept as short as possible.
2) The distance r between said conductors can be increased to decrease the force.
3) The absolute values of i_1 and i_2 being equal, the force is proportional to the peak current squared.

The other extreme case would be conductors with no parallel current paths with a resulting mutual force of zero. This principle is adopted in the connection of the DUT to the copper bars connecting all cells. Fig. 7 shows a sketch of the DUT connection inside its enclosure. The current is fed into the DUT from two sides, each connection conducting half of the current amplitude. This way the full current I_{DUT} is only present in the DUT itself. By halving the current, the force acting on each connection is divided by four.

The copper bars are mounted on two opposing sides of the test setup. One side can be seen in Fig. 9. The forces between both sides can be neglected due to their large distance apart. The forces between the two connections to the DUT enclosure can also be neglected, as they do not share a parallel current path.

As a result, only the forces within each of the copper bar connections are of interest. These should not be reduced by an increased distance between the conductors, since this would increase stray inductance and thus have a negative impact on the system's dynamics. Fig. 8 shows a schematic representation of the copper bars. The sketch displays the dimensions and spacing of the copper bar, as well as the direction of the forces in both HCM and DCM.

It should be noted that for DCM only two of four copper bars are conducting the current pulse. However, since the maximum current in DCM is half the maximum current in HCM this results in the same maximum current per copper bar independent from the operation mode used.

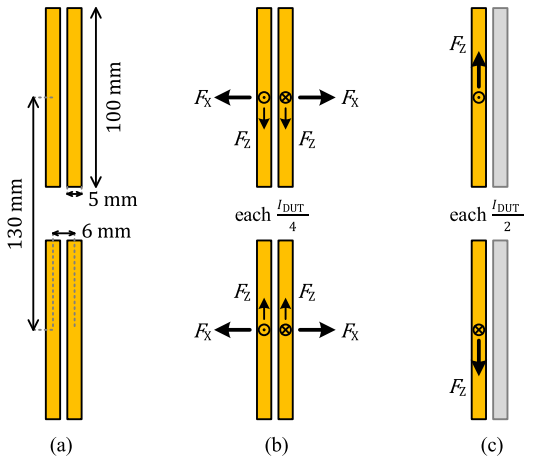


FIGURE 8. (a) Mechanical arrangement of the copper bars connecting the cells together and to the DUT (cross-section view, not to scale). (b) Qualitative display of the resulting forces in HCM. (c) Qualitative display of the resulting forces in DCM.

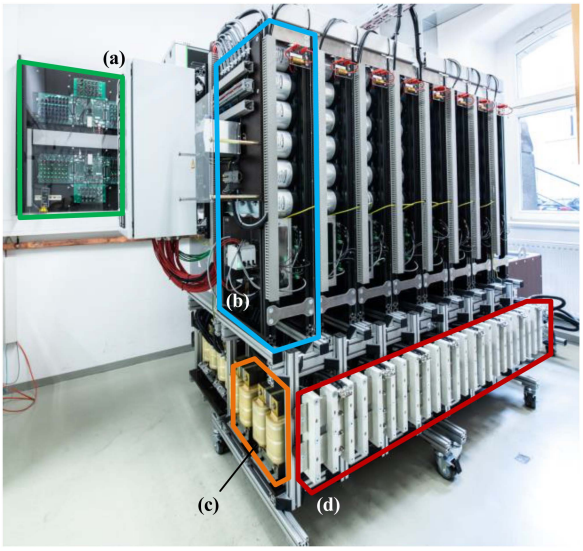
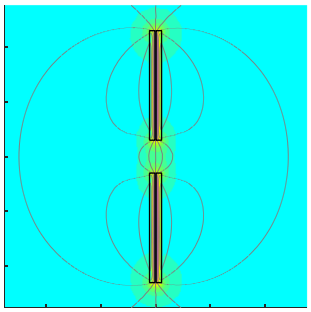
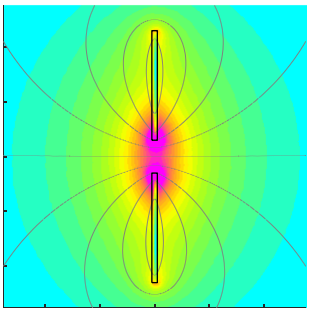


FIGURE 9. Photograph of the complete test setup. Highlighted parts: (a) Control platform, (b) one of the 16 cells, (c) two inductors belonging to one cell, and (d) copper bars and insulating clamps on one side of the setup.

The forces on the copper bars are simulated for both the entire length of the conductors of 1855 mm and for the maximum distance of 80 mm between the insulating clamps holding the conductors in place, as shown in Fig. 9. For these simulations, the free program FEMM is used, see [24]. Relevant simulation results are also listed in Table 3.

The force on the entire copper bar is relevant for the insulating clamps, as they hold the copper bar construction together. In addition, the forces on the 24 clamps have been estimated using the German standard *DIN EN 60865-1* [25]. This results in a force of under 600 N per pair of copper bars and clamp. Since each clamp holds two pairs of copper bars, as seen in Fig. 8(b), the resulting force is less than 1.2 kN per clamp. Each clamp is held together by three M10 screws with a

TABLE 3. Simulation Results Obtained by FEMM Simulation

HCM	DCM
B (T): 0.05 0.1 0.15 0.2 ≥0.25	
	
Magnetic flux density and field lines	Magnetic flux density and field lines
$F_{X1} = 6.36$ kN $F_{X2} = 274$ N	$F_{X1} \approx 0$ N $F_{X2} \approx 0$ N
$F_{Z1} = 9.6$ N $F_{Z2} \approx 0$ N	$F_{Z1} = 2.4$ kN $F_{Z2} = 104$ N

Displayed square section edge length: 276 mm. Index "1": conductor length of 1855 mm, index "2": conductor length of 80 mm.

property class 8.8 – resulting in a nominal pretension force of (24.7...31) kN, depending on coefficient of friction [26]. It is therefore at least an order of magnitude higher than the magnetic forces caused by the current pulse.

Fig. 9 shows a photograph of the complete surge current source. On the left side of the picture, the control platform (CP) can be seen attached to the wall, denoted as (a). On the bottom right (d), the (nickel-plated) copper bars are visible as well as the (white) clamps responsible for holding the conductors in place during the current pulses. Behind the copper bars the inductors (c) can be seen in the undercarriage of the setup. The cells (b) are sitting above.

As a final remark, the potential for a catastrophic DUT-failure has to be considered. To protect the system against heat, pressure, and UV radiation created by arcing and to ensure a fast turn-OFF of the entire current source in case of a DUT explosion, multiple safety features are implemented. These include a shrapnel-proof barrier around the DUT as well as a sound and shrapnel proof wall between the occupied control room and the unoccupied laboratory room (containing the apparatus), an overpressure vent, an active ventilation system, and an arc detection that triggers an emergency turn-OFF of the apparatus within one microsecond.

III. CONTROL DESIGN

A. CP DESIGN

The control of the surge current source is orchestrated with a rapid prototyping CP based on a Xilinx Zynq 7015 System on a chip that was developed in-house. This chip features an

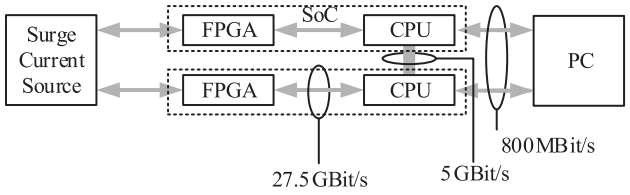


FIGURE 10. Structure of the distributed CP for the surge current source.

Artix-7 FPGA and two ARM Cortex A9 processors with a clock frequency of 766 MHz [27].

The system utilizes one CPU core as a deterministic real-time core, running the FreeRTOS operating system, while the other CPU core is utilized for asynchronous processes running Linux. Both cores operate in an asymmetric multiprocessing system, communicating via RAM-based first-in, first-out (FIFO) buffers. The platform also includes an open-source data modification and visualization tool called LabAnalyser [28]. The real-time core data tracer can transfer up to 400 Mbit/s of data to LabAnalyser via Linux. All the data can be displayed in real-time.

This control hardware and software framework are the basis of the control hardware for the surge current source.

B. IO REQUIREMENTS

As previously mentioned, the current source consists of 32 HBs that are used to control the current conducted through the DUT. Pairs of two HBs share the same dc-link. The necessary amount of sensor values as well as control signals is:

- Sensor Values
  - 32 x Currents
  - 16 x dc-link voltages
- Control Signals
  - 32 x Enable
  - 32 x PWM –Signals
  - 32 x Gate Unit Feedback
- Auxiliary Signals
  - 2 x Arc Detection
  - 4 x Contactor Control
  - 16 x Delta Sigma Clock

To accommodate the large number of necessary inputs and outputs (I/Os), a distributed control approach was implemented using two CP, such as to double the number of available I/Os and CPUs. A common clock is utilized to parallelize the CPs and to ensure a shared time base.

Fast communication between the platforms is achieved by two 5 Gbit/s SFP ports, which allow for writing to a FIFO memory on the on-chip memory of the other CP. This scheme enables rapid sharing of sensor values, with a latency of less than 1.5 μs. The complete distributed control architecture, including the corresponding bandwidth of each bus, is depicted in Fig. 10.

C. DATA PROCESSING

One of the main objectives was to evenly distribute the CPU and pin utilization between the two CPs. Thus, both

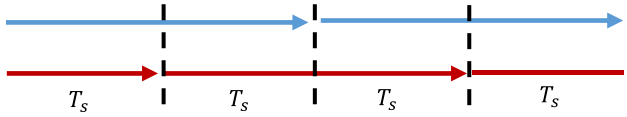


FIGURE 11. Phase shifted control cycles of the two CPs, the control task of the second (red) control cycle is delayed by T_s in comparison to the first control (blue).

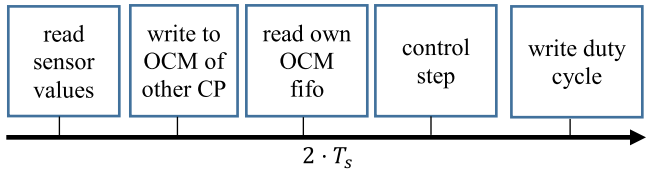


FIGURE 12. Timeline of one control cycle.

CPs feature an identical hardware and software layout. Each CP modulates 16 HBs and collects the corresponding sensor values. Based on 16 interleaved switched HBs per CP the resulting control cycle frequency is 3 kHz·16 (cells) = 48 kHz.

As all 32 HBs shall be switched interleaved, the control cycle of the second CP is shifted by half a control cycle (see Fig. 11).

To digitize the analog sensor values, Sigma/Delta ($\Sigma\Delta$) converters are used. The bit-stream of the converters is transferred via fiber-optics to the FPGSs of the CPs. In the FPGA, a SINC3/SINC1 filter-stage is used to decimate the bitstream. The modulation, a fast limit detection for the currents and voltages, the error handling and observing the CPU timing are implemented on the FPGA.

The timeline of one control cycle is depicted in Fig. 12 and is valid for both CPs. Each CP has a control cycle of $2 \cdot T_s$, but the combination of both allows for one control action every T_s.

D. MODULATION

Since the cells are operated in a buck converter mode, the modulation techniques known for this purpose can be used. One such technique is hysteresis control (HC), which involves constantly comparing the output current to upper and lower thresholds placed symmetrically around the desired current (see Fig. 13 top). This maximizes the dynamic range of the apparatus and results in a variable switching frequency. However, it requires a current measurement with a high bandwidth to accurately maintain the boundaries, and does not allow for phase shifting of the output currents to reduce the current ripple through the DUT.

Another technique, known as interleaved current mode control (CMC) [29], is similar to HC but results in a constant switching frequency. It reduces the output current if it reaches an upper threshold and increases it after a fixed time interval (see Fig. 13 middle). The switching times of the cells can be interleaved to greatly reduce ripple current through the DUT. However, this technique is only suitable for HCM.

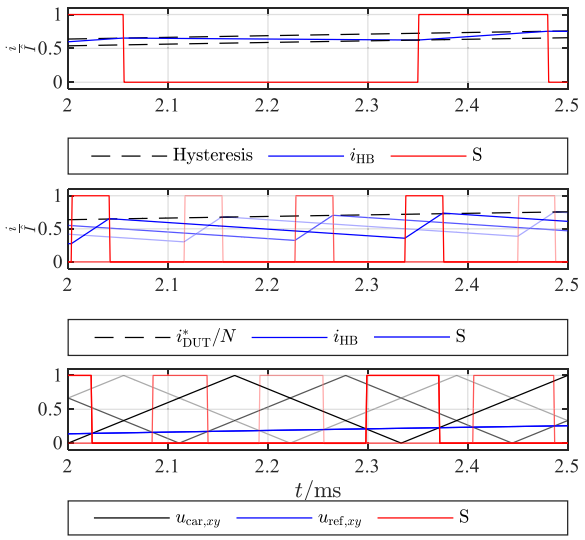


FIGURE 13. Modulation techniques for dc–dc-converters. Top: HC. Middle: Interleaved CMC for three cells. Bottom: Interleaved PWM with three cells.

TABLE 4. Comparison of Modulation Techniques for DC–DC-Converters

	HC	CMC	PWM
Dynamics	High	High	Dependent on overlaid control algorithm
Current measurement bandwidth	$x \cdot f_C$	$x \cdot f_C$	f_C
Overcurrent protection	Intrinsic	Intrinsic	Additional
DUT-current ripple	High	Low	Low
Switching frequency	Variable	Fixed	Fixed
Applicable for HB and FB	Yes	No	Yes
Flexibility when programming current trajectories	Complex	Complex	Easy

A third technique, interleaved Pulsewidth modulation (PWM), does not include current control or overcurrent protection as part of the modulation process. Instead, an overlaid digital current control and fast overcurrent protection are required. The output of the current control is a voltage, which then is synthesized by a pulse width modulator, using interleaved carrier signals in order to reduce current ripple through the DUT (see Fig. 13 bottom).

Table 4 summarizes the main characteristics of the modulation methods. Considering the requirements for flexibility regarding adjustable current trajectories, low current ripple, and suitability for both DCM and HCM, PWM was chosen as the most suitable modulation scheme. It offers the additional advantage of a fixed switching frequency, which simplifies the thermal design of the commutation cell.

Assuming PWM, the current ripple in the DUT $I_{\text{ripple,DUT}}$ depends on the circuit configuration (HCM: HB, DCM: full bridge), the duty cycle, and the capacitor voltage of the surge current source [30]. With the given output inductance of 50 µH and the switching frequency of 3 kHz per IGBT, the resulting current ripple is depicted in Fig. 14 for both operation

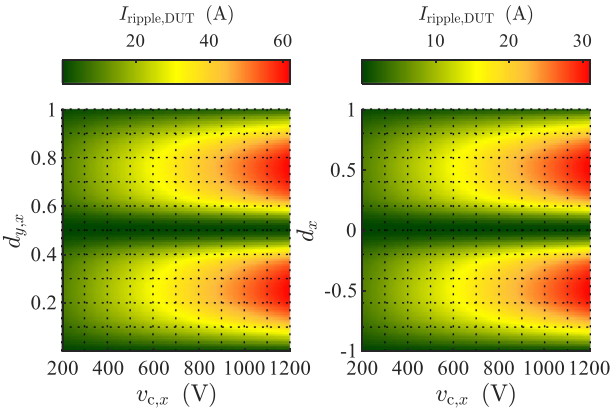


FIGURE 14. Current ripple through the DUT dependent on cell capacitor voltage and the duty cycle considering an equal duty cycle and capacitor voltage for all cells in HCM (left) and DCM (right).

modes. The maximum current ripple is about 60 A in HCM and 30 A for the DCM. This equals 0.6‰ of the respective maximum current.

E. CONTROL ALGORITHM

The PWM requires an overlaid control algorithm. The authors propose a highly dynamic control scheme consisting of a feedforward controller, a current controller for the DUT-current, and a balancing controller. Since an asymmetric interleaved PWM is used, the control algorithm has to be executed with a frequency of

$$f_S = \frac{1}{T_S} = 2 \cdot N_C \cdot f_C \tag{6}$$

in order to achieve the maximum dynamics of the apparatus.

1) BASIC STRUCTURE

The controller design allows for two different methods of controlling the current:

- Method I: Individual current control for each cell
- Method II: Control of the resulting DUT-current

Symmetrical cell currents are the essential advantage of the individual cell current control enabling a minimal DUT-current ripple and a similar thermal stress on the cells. However, this scheme has the disadvantage of a large time constant in the controlled system. To individually control each current, the mean value of each cell's output current must be measured and regulated. Assuming a switching frequency of the semiconductors of $f_C = 3$ kHz, the maximum current sampling frequency for asynchronous modulation is 6 kHz per HB.

The second method is controlling the DUT-current. This is based on two assumptions: First, the cell parameters are equal for all cells and second, transient cell current imbalances might appear if they do not significantly unbalance IGBT or diode junction temperatures.

The effective switching frequency of the DUT-current is 96 kHz, which is the same as the SINC decimation frequency

TABLE 5 Controller Design Parameters

Method	T_{dm}	T_{dc}	T_{df}	L_{eff} [μH]	R_{eff} [mΩ]	$v_{IGBT,eff}$ [V]	t_r [ms]	t_s [ms]
I DCM	16	32	32	100	75	2.4	0.55	1.8
I HCM	8	32	32	50	37.5	1.2	0.4	1.7
II DCM	4	2	1	6.25	4.69	2.4	0.38	0.8
II HCM	2	2	1	1.56	1.17	1.2	0.38	0.7

of the ΣΔ-converted sensor values. This means that the digitized DUT-current will not contain the switching ripple. One of the primary benefits of controlling the DUT-current using a system with a high sampling frequency of 96 kHz is the ability to determine control errors at a much faster rate than the previous method. However, this approach has the potential to result in unbalanced currents due to variance in cell inductors and different dissipative losses in steady state. To mitigate these issues, it is necessary to implement a balancing controller and to prevent current steps that could exceed the SOA of the used IGBTs.

Both methods were simulated using MATLAB, SIMULINK, and PLECS. To demonstrate the dynamic behavior, a simple PI-controller using the symmetrical optimum [31] is used.

The dead time effects of the current control arise due to three components: a conversion/filter time T_{df}, a calculation time T_{dc}, and a modulation time T_{dm}. Furthermore, the effective inductance for HCM and DCM L_{eff} as well as the effective resistive losses R_{eff} and the effective forward voltage of the IGBTs $v_{IGBT,eff}$ are defined.

The parameters used to calculate the controller gains are listed in Table 5. The table also shows the different rise t_r and settling times t_s. The rise time is defined as the time interval in which the sensor value reaches the target value for the first time. The settling time is the time interval in which the sensor value reaches a 5% band around the target value.

The different dynamic behavior is demonstrated by the step responses for Method I – DCM and II – DCM in Fig. 15. Fig. 16 shows the selected control structure with the best results, based on Method II.

2) FEED-FORWARD CONTROL

The output voltage v_{out} for both HB (HCM) and VB (DCM) can be described using the target DUT-current i^*_{DUT} by

$$v_{out} = i^*_{DUT} \cdot R_{eff} + \frac{di^*_{DUT}}{dt} \cdot L_{eff} + v_{IGBT} + i^*_{DUT} \cdot R_{DUT} + \frac{di^*_{DUT}}{dt} \cdot L_{DUT} + v_{f,DUT} \quad (7)$$

with the DUT resistance R_{DUT}, the DUT inductance L_{DUT}, and the threshold voltage drop across the DUT $v_{f,DUT}$. The

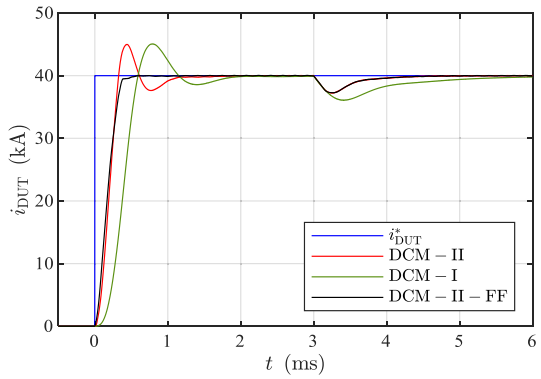


FIGURE 15. Simulated step response ($t = 0$ ms) and disturbance response ($t = 3$ ms) of the control for DUT-current control (green), separated control of all cell currents (red), and separated control of all cell currents with feed-forward control activated (black).

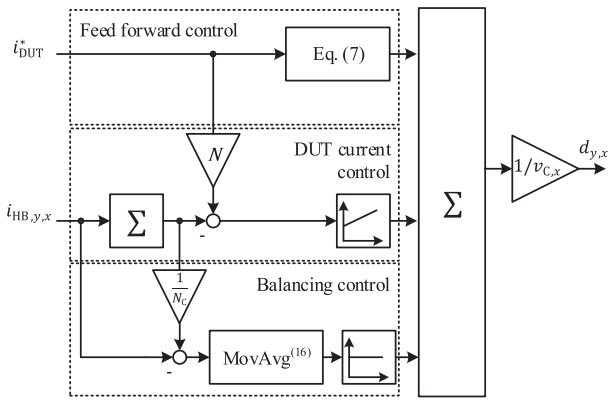


FIGURE 16. Control structure with feed-forward control, balancing control, and control of the DUT-current.

corresponding duty cycle can be calculated via

$$d_x = d_{y,x} = \frac{v_{out}}{v_{C,x}}. \quad (8)$$

Using the known parameters (Table 5) as well as the trajectory of the target DUT-current $i^*_{DUT}(t)$, (7) shall be evaluated in real-time. Therefore, it is necessary to filter the trajectory to comply with the following boundaries, where the Δi^*_{DUT} is the change of DUT-current during one sampling interval T_s. The first boundary

$$\Delta i^*_{DUT} \leq \frac{v_{C,x} - v_{out} \cdot z^{-1}}{L_{eff} + L_{DUT}} \cdot T_s \quad (9)$$

assures that the converter can provide enough voltage to follow the current rise of the trajectory.

Furthermore, the maximum peak current of every IGBT should not be exceeded.

$$-I_{pk,max} \leq i^*_{DUT} \leq I_{pk,max}. \quad (10)$$

As the currents of the IGBTs do not have to be equally balanced during transients it is further necessary to assure that the next switching IGBT can carry the current change in the

next time step.

$$-I_{\mathrm{AVG}} - i_{\mathrm{HB},y,\mathrm{x}} \leq \Delta i^*_{\mathrm{DUT}} \leq I_{\mathrm{AVG}} - i_{\mathrm{HB},y,x}. \tag{11}$$

Using these three equations to filter the target current trajectory, (7) can be used to forward the necessary voltage. To assure that the current including the ripple (4) does not exceed I_{CRM} the duty cycle is limited (12) in HCM and (13) in DCM if $b > 0$.

$$a = 8 \cdot L_{\mathrm{out}} \cdot f_{\mathrm{c}}$$

$$b = v_{\mathrm{C},x} \cdot \left(v_{\mathrm{C},x} + a \cdot \left(\left|\Delta i^*_{\mathrm{DUT}} + i_{\mathrm{HB},y,x}\right| - I_{\mathrm{CRM}}\right)\right.$$

$$d_{y,x} \leq 0.5 - \frac{\sqrt{b}}{2 \cdot v_{\mathrm{C},x}} \tag{12}$$

$$-\frac{\sqrt{b}}{2 \cdot v_{\mathrm{C},x}} \leq d_x \leq \frac{\sqrt{b}}{2 \cdot v_{\mathrm{C},x}}. \tag{13}$$

The step response using the presented feed-forward structure is shown in black in Fig. 15. It can be observed that the settling time corresponds to the rise time.

3) BALANCING CONTROL

In order to maintain a balanced load distribution, it is essential to implement a balancing controller. The use of a proportional controller, which sets the mean value of all currents as the target value for each individual cell, proves to be adequate for this purpose. However, the design of this controller involves trade-offs between its regulation dynamics and the ripple current of the DUT. As the sum of balancing currents is always zero, the balancing process will not adversely affect the DUT current. Furthermore, the presence of switching ripple in the cell currents at a frequency of f_{c} necessitates the implementation of a filter to calculate the ripple-free current value. A moving average (notch) filter with a window width of $N_{\mathrm{C}} = 16$ is an appropriate solution as it effectively eliminates the ripple. The delay introduced by this filter is acceptable as the dynamics of the imbalance occur at a slower rate than the required DUT current controller performance.

An active balancing of the capacitor voltages $v_{\mathrm{C},x}$, with $x = [1, 16]$, is not required for two major reasons. First, since the cells are of equal design and have equal parameters, and the currents are actively balanced, the resulting imbalance in the capacitor voltages is not significant; as shown in Section IV. Second, the dc links of the individual cells are connected for collective charging – however they are decoupled, each by resistors of 1 kΩ per connection. Therefore, the parasitic currents caused by voltage imbalances are limited to negligible amplitudes.

IV. EXPERIMENTAL TEST RESULTS

Experimental investigations of the adjustable current source were carried out for a short circuit load and a thyristor (SCR) as DUT in both DCM and HCM.

The first series of test pulses was performed with a short circuit load. This is a demanding circuit configuration for the controller, since there is minimal dampening in the circuit.

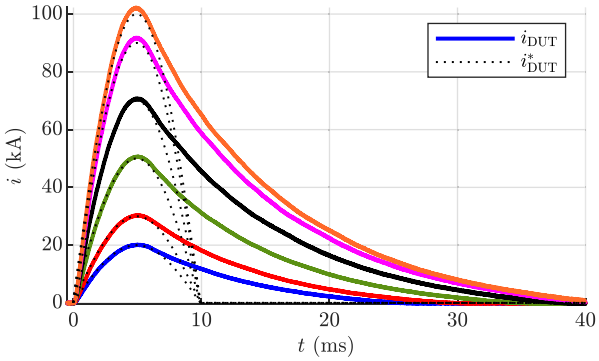


FIGURE 17. Comparison of current i_{DUT} measured via Rogowski coil and target current trajectory i^*_{DUT}. Half-sine waveform, short circuit load, HCM; $V_{\mathrm{C},x}(t = 0) \approx (300 \ldots 600)$ V, $I_{\mathrm{pk}} \approx (20 \ldots 100)$ kA.

The second series of test pulses was performed with a thyristor as a load, which is a realistic example for future operation of the surge current source.

A half-sine current waveform is used as a benchmark in the following section, since conventional pulse current testers for I^2t-tests on power semiconductors realize this current waveform. In addition, a current step waveform is used to show the high dynamics of the system. Subsequently, one example of a dynamic, freely configurable current waveform is presented to demonstrate the ability of the current source to realize arbitrary current trajectories.

The DUT current can be measured directly, e.g., with a Rogowski coil. However, the CP also calculates it as the sum of all cell currents according to (14) or (15), depending on the operation mode.

$$i_{\mathrm{DUT}} = \sum_{x=1}^{N_{\mathrm{C}}} \left(i_{\mathrm{HB1},x} + i_{\mathrm{HB2},x}\right) \tag{14}$$

$$i_{\mathrm{DUT}} = \sum_{x=1}^{N_{\mathrm{C}}} i_{\mathrm{FB},x}. \tag{15}$$

A. SHORT CIRCUIT LOAD

The short circuit load is especially important in HCM, as there is only little dampening in the circuit and the HCM cannot generate a negative output voltage. Fig. 17 displays multiple half-sine current pulses i_{DUT} with peak currents of 20 to 100 kA and the corresponding set current trajectory i^*_{DUT}. The waveforms show a high accuracy for the rising slopes of the current pulse. However, there is significant deviation between set and measured currents for the falling slope. The reason for this is that the minimum output voltage is approximately zero for $t > 6$ ms. Obviously, the fall of the currents is determined mainly by the load parameters like resistance and stray inductance. The set trajectories for the falling currents are physically not realistic for HCM.

The ripple current is an important characteristic of the current source. It can be obtained for the individual HBs from Fig. 18(a) which shows a zoom of the rising current slopes

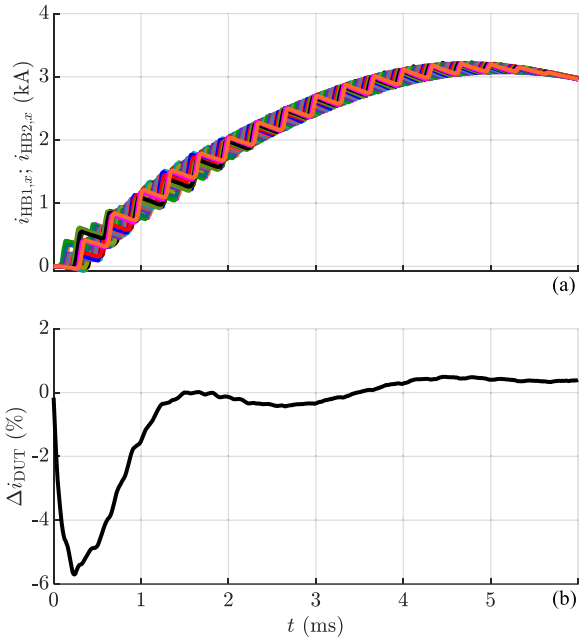


FIGURE 18. Cell currents and current ripple. (a) HB currents $i_{\mathrm{HB1},x}$, $i_{\mathrm{HB2},x}$. (b) Deviation Δi_{DUT} in percent. Half-sine waveform, short circuit load, HCM; $V_{\mathrm{C},x}(t=0) \approx 600$ V, $I_{\mathrm{pk}} \approx 100$ kA. $x = [1,16]$.

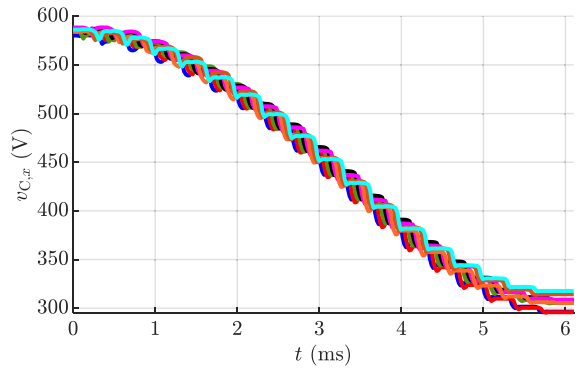


FIGURE 19. Cell capacitor voltages $v_{\mathrm{C},x}$ measured by the control system. Half-sine waveform, short circuit load, HCM; $V_{\mathrm{C},x}(t=0) \approx 600$ V, $I_{\mathrm{pk}} \approx 100$ kA. $x = [1,16]$.

of all HB currents. It can, however, not be measured directly. As seen in Fig. 14, the output current ripple is expected to be in the order of $< 1‰$ of the maximum load current. It is therefore not measurable by a Rogowski coil with a nominal current in the range of more than 100 kA.

Fig. 19 shows the capacitor voltages $v_{\mathrm{C},x}$ corresponding to the 100 kA pulse for the first 6 ms of the current pulse. A voltage ripple is clearly visible superimposed on the general discharge behavior during the current pulse. During the pulse, the capacitor voltages drift apart and show a maximum deviation of about 10% at $t = 6$ ms. This is considered irrelevant for the operation of the surge current source.

The ripple current can also not be calculated with sufficient accuracy from the cell currents because of bandwidth constraints in the signals measured by the CP. However, it is possible to calculate a deviation of the current i_{DUT} measured

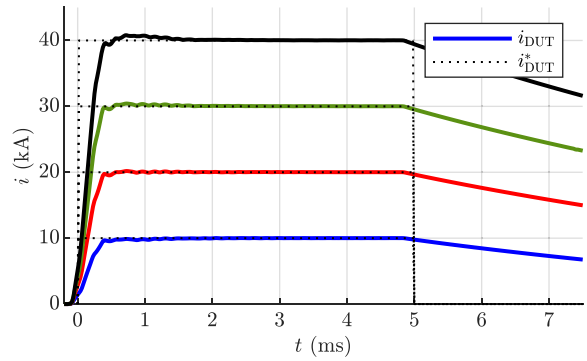


FIGURE 20. Comparison of current i_{DUT} measured by the control system and target current trajectory i^*_{DUT}. Current step waveform, short circuit load, HCM; $V_{\mathrm{C},x}(t=0) \approx 900$ V, $I_{\mathrm{pk}} \approx (10 \ldots 40)$ kA.

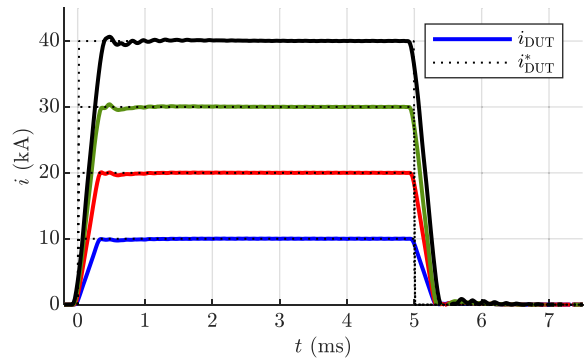


FIGURE 21. Comparison of current i_{DUT} measured by the control system and target current trajectory i^*_{DUT}. Current step waveform, short circuit load, DCM; $V_{\mathrm{C},x}(t=0) \approx 900$ V, $I_{\mathrm{pk}} \approx (10 \ldots 40)$ kA.

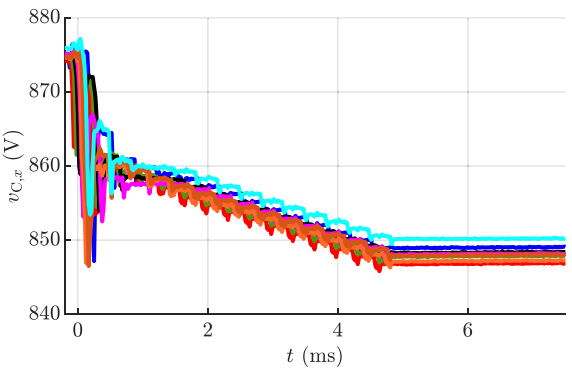


FIGURE 22. Cell capacitor voltages $v_{\mathrm{C},x}$ measured by the control system. Current step waveform, short circuit load, HCM; $V_{\mathrm{C},x}(t=0) \approx 900$ V, $I_{\mathrm{pk}} \approx 40$ kA. $x = [1,16]$.

by the CP from the set current i^*_{DUT} (16). The result is depicted in Fig. 18(b). The absolute value of the deviation increases at the start of the current pulse and decreases for $t > t_{\mathrm{r}}$, as is expected according to Table 5 and Fig. 15.

$$\Delta i_{\mathrm{DUT}} = \frac{i_{\mathrm{DUT}} - i^*_{\mathrm{DUT}}}{\max\left(i^*_{\mathrm{DUT}}\right)}. \tag{16}$$

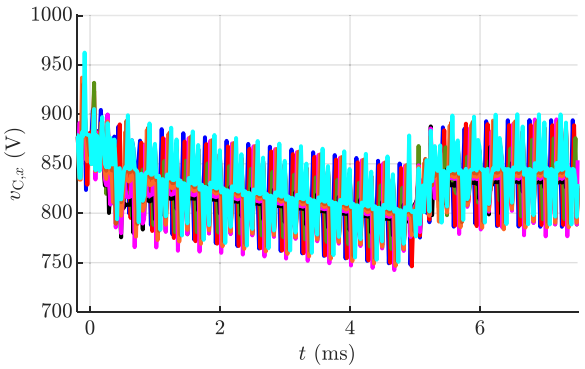


FIGURE 23. Cell capacitor voltages $v_{C,x}$ measured by the control system. Current step waveform, short circuit load, DCM; $V_{C,x}(t = 0) \approx 900$ V, $I_{pk} \approx 40$ kA. $x = [1, 16]$.

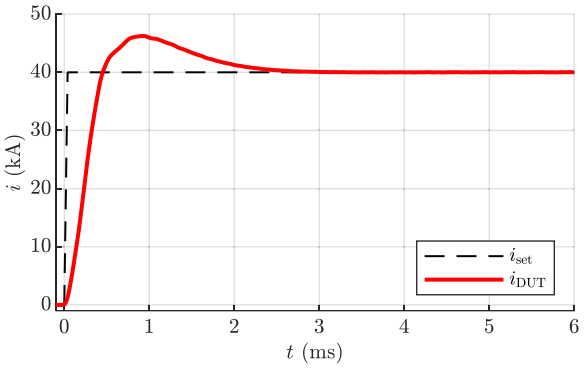


FIGURE 24. Comparison of current i_{DUT} measured by the control system and target current trajectory i^*_{DUT}. Current step waveform, short circuit load, DCM, feed-forward deactivated; $V_{C,x}(t = 0) \approx 900$ V, $I_{pk} \approx 40$ kA.

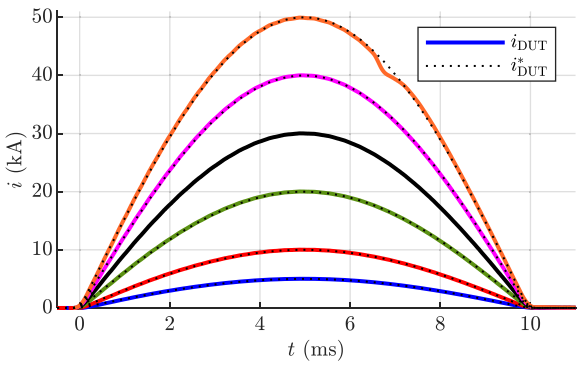


FIGURE 25. Comparison of current i_{DUT} measured by the control system and target current trajectory i^*_{DUT}. Half-sine waveform, thyristor as load, DCM; $V_{C,x}(t = 0) \approx (100 \ldots 600)$ V, $I_{pk} \approx (5 \ldots 50)$ kA.

Figs. 20 and 21 depict multiple current pulses with peak currents ranging from 10 kA to 40 kA for HCM and DCM, respectively. Both figures show rectangular current pulses with a duration of 5 ms, which test the apparatus' step response. In both Figs. 20 and 21, the rise time t_r of about 0.38 ms can be observed, as shown in Table 5. The current slope is, in these examples, not limited by the capacitor voltages $v_{C,x}$, with $x = [1, 16]$, and the output inductance L_{out} of the HBs, but by the controller. The falling current slope is limited by

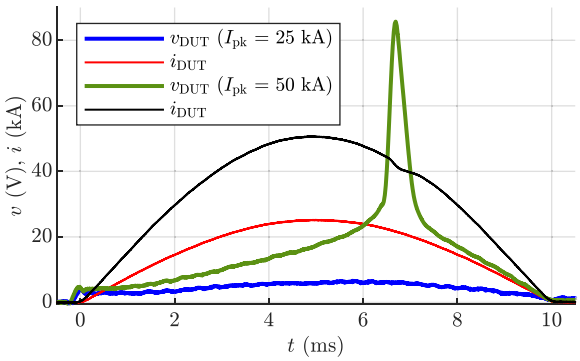


FIGURE 26. Comparison of current i_{DUT} measured by Rogowski coils and DUT on-state voltage v_{DUT} for two tests with different peak currents. Half-sine waveform, thyristor as load, DCM; $V_{C,x}(t = 0) \approx 600$ V, $I_{pk} \approx (25 \ldots 50)$ kA.

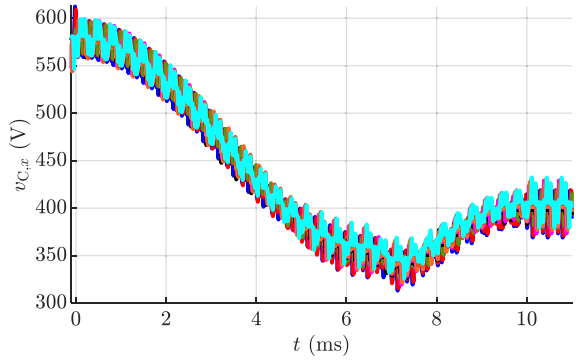


FIGURE 27. Cell capacitor voltages $v_{C,x}$ measured by the control system. Half-sine waveform, thyristor as load, HCM; $V_{C,x}(t = 0) \approx 600$ V, $I_{pk} \approx 50$ kA.

the same parameters in DCM. In HCM, it is limited by the load resistance (as well as the surge current source's parasitic resistance).

The maximum current amplitude is the same in HCM and DCM, enabling a side-by-side comparison between both modes. The maximum of 40 kA is chosen for the comparison with the simulation (Fig. 15) and measurement (Fig. 24) of the step response with feed-forward deactivated – the resulting current does not exceed the 50 kA maximum.

Figs. 22 and 23 show the corresponding cell capacitor voltages $v_{C,x}$ for the 40 kA pulse in both HCM and DCM. The comparison of both figures highlights the fact that in DCM a recuperation of residual energy is possible. Both capacitance and average current are approximately equal for the cells. Therefore, the capacitor voltages are indirectly balanced. Minor deviations are observable, but not significant.

Fig. 24 shows a current step response with feed-forward deactivated. This corresponds to DCM-II in Fig. 15. The measured value for rise time $t_r = 0.44$ ms matches the simulated value of $t_r = 0.38$ ms with adequate accuracy. The measured settling time $t_s = 1.79$ ms, however, deviates significantly from the simulated value of $t_s = 0.8$ ms.

This is caused by parasitic components, which are not perfectly emulated by the simulation. The observed differences

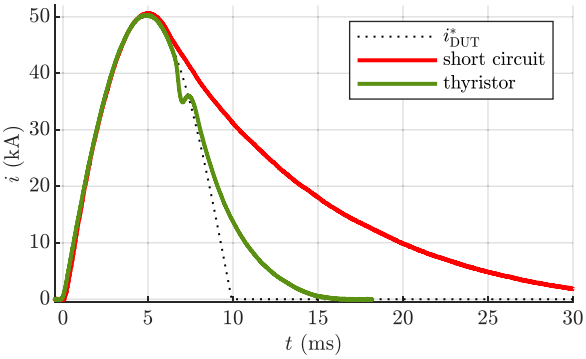


FIGURE 28. Comparison of target current trajectory i^*_{DUT} and DUT-current measured by Rogowski coils for a short circuit load and a thyristor as load, half-sine waveform, HCM; $V_{C,x}(t = 0) \approx (400 \ldots 600)$ V, $I_{pk} \approx 50$ kA.

are considered to have little relevance on the overall performance, especially since they do not appear with feed-forward control activated.

B. THYRISTOR LOAD

The second series of test pulses was performed with the (7500 V, 2100 A) SCR *T1901N* as a load [32]. During the measurements, the SCR was kept in an on-state with a continuous gate current of $I_G \approx 500$ mA. Measurements were performed both in DCM and HCM.

Fig. 25 displays several measurements of half-sine currents i_{DUT}, as measured by the CP, with amplitudes in the range of $I_{pk} \approx (5 \ldots 50)$ kA. The corresponding set current trajectories i^*_{DUT} are shown as well, but are barely visible due to being covered by the measured waveforms.

One noticeable exception is a current dip in the 50 kA curve at around 6.5 to 7 ms. This current dip is caused by a rapid increase of the DUT's on-state voltage v_{DUT}. Fig. 26 shows this behavior in more detail. The current dip corresponds to a voltage spike of the SCR which indicates an overheating event of the power semiconductor. Analysis and explanation of the on-state overvoltage of the SCR are out of the scope of this article. However, an overvoltage of the DUT during high current stress is not unusual. Thus, the behavior of the current source regarding the on-state overvoltage is important. Figs. 25, 26, and 28 show that a sudden increase of the load voltage causes a deviation between the set trajectory and the DUT-current. However, the current controller is able to limit the deviation and to prevent a lasting deviation. The cell capacitor voltages $v_{C,x}$ corresponding to the 50 kA current pulse are depicted in Fig. 27. They show no noteworthy peculiarities. The recuperation typical for DCM is clearly visible.

The comparison of the DUT current trajectory in HCM with short circuit and SCR load is depicted in Fig. 28. This figure illustrates the dependency of the falling load current on the load parameters in HCM. In contrast, DCM enables a freely adjustable falling current shape. Thus, DCM is preferable if the current drop must be faster than given by DUT parameters.

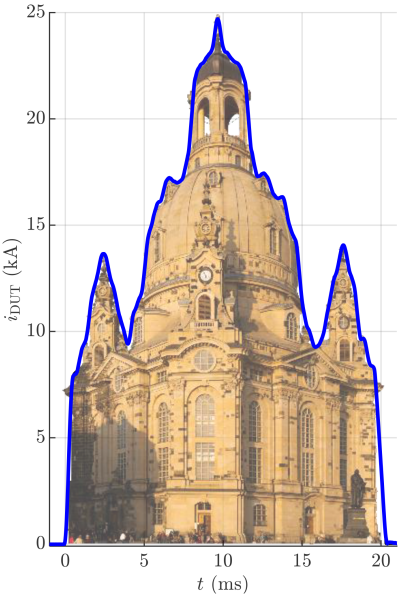


FIGURE 29. Example of a dynamic current waveform: DUT-current (measured by the control system) tracing a profile of the *Frauenkirche* in Dresden. Source of photograph [33]. Thyristor as load, DCM; $V_{C,x}(t = 0) \approx 300$ V, $I_{pk} \approx 25$ kA.

Fig. 29 shows an example of an arbitrary, dynamic current waveform. The current trajectory traces the profile line of the *Frauenkirche* in Dresden. The authors chose this to demonstrate the dynamic characteristics of the surge current source in DCM, since the waveform contains both regions of a current slope up to $\mathrm{d}i_{DUT}/\mathrm{d}t \approx 60\mathrm{A}/\mu\mathrm{s}$ including rapid sign changes, as well as short, sub-ms current spikes (e.g., at 9.6 ms).

V. CONCLUSION

This article presents the methodology for the design and construction of a 100 kA surge current source for power semiconductor surge current tests. The current source is able to generate user-specified current trajectories over a wide operating range. The details written about the design process encompass both the electrical and mechanical components, as well as the control hardware and software that enable precise control of the output current with minimal ripple (<1‰). Experimental results verify the correct functionality of the new pulsed current source and illustrate its superior characteristics compared with state-of-the-art current sources. Other potential use cases for the current source include testing on electromechanical switches, connectors, and cables; for example, in the fields of industrial or automotive (electric vehicles) applications.

APPENDIX

The measuring instruments used to gather data for the diagrams depicted in this document are listed in Table 6.

Table 7 lists controller and cell parameters defined for the experiments within this article. Table 8 lists experimentally estimated parasitic parameters of the test setup for different

TABLE 6. Measurement Devices Used in This Article

Parameter	Current probe	Nominal current	Notes
i_{DUT}	Rogowski-coil *CWT 1500*	300 kA	Short circuit load
$i_{\mathrm{DUT}}/2$	Rogowski-coil *CWT 600LF*	120 kA	Thyristor load
$i_{\mathrm{HB},y,x}$ $i_{\mathrm{FB},x}$	*LEM* current transducer *LF 2010-S*	4.25 kA	Cell currents

TABLE 7. Controller- and Cell Parameters

Parameter	Symbol	Value	Notes
IGBT threshold voltage	v_{IGBT}	1 V	
HB inductance	L_{out}	50 µH	
HB resistance	R_{out}	1.5 mΩ	Parasitic value
P current controller value	k_{p}	0.5	
I current controller value	k_{i}	628	
D current controller value	k_{d}	2.0	
P symmetrizing controller gain	k_{sym}	0.16	

TABLE 8. Experimentally Estimated Circuit Parameters for Different Configurations and Loads

Parameter	Symbol	Value	Notes
DUT threshold voltage	$v_{\mathrm{f,DUT}}$	0	Short circuit load, DCM
DUT inductance	L_{DUT}	0.8 µH	
DUT resistance	R_{DUT}	0.5 mΩ	
DUT threshold voltage	$v_{\mathrm{f,DUT}}$	0	Short circuit load, HCM
DUT inductance	L_{DUT}	0.35 µH	
DUT resistance	R_{DUT}	0.3 mΩ	
DUT threshold voltage	$v_{\mathrm{f,DUT}}$	1.2 V	Thyristor load
DUT inductance	L_{DUT}	1 µH	
DUT resistance	R_{DUT}	0.85 mΩ	

configurations and loads. It should be noted that these parameters can differ greatly between experiments as they are influenced by the load itself as well as the connection between test setup and load.

REFERENCES

[1] J. Morren and S. W. H. de Haan, "Short-circuit current of wind turbines with doubly fed induction generator," *IEEE Trans. Energy Convers.*, vol. 22, no. 1, pp. 174–180, Mar. 2007.

[2] X. Li, Q. Song, W. Liu, H. Rao, S. Xu, and L. Li, "Protection of nonpermanent faults on DC overhead lines in MMC-based HVDC systems," *IEEE Trans. Power Del.*, vol. 28, no. 1, pp. 483–490, Jan. 2013.

[3] Dynex Semiconductor, Ltd., "Case nun-rupture current ratings," Appl. Note AN5381-2, pp. 1–6.

[4] A. Wintrich, U. Nicolai, W. Tursky, and T. Reimann, *Application Manual Power Semiconductors*. Ilmenau, Germany: ISLE Verlag, 2015.

[5] M. Rodriquez, G. Abad, I. Sarasola, and A. Gilabert, "Crowbar control algorithms for doubly fed induction generator during voltage dips," in *Proc. Eur. Conf. Power Electron. Appl.*, 2005, pp. 1–10.

[6] D. Silber and M. J. Robertson, "Thermal effects on the forward characteristics of silicon pin diodes at high pulse currents," *Solid-State Electron.*, vol. 16, no. 12, pp. 1337–1346, 1973.

[7] Y. C. Kao and P. L. Hower, "The surge capability of high voltage rectifiers," in *Proc. Int. Electron Devices Meeting*, 1978, pp. 568–574.

[8] A. P. Silard, "High-temperature physical effects underlying the failure mechanism in thyristors under surge conditions," *IEEE Trans. Electron Devices*, vol. 31, no. 9, pp. 1334–1340, Sep. 1984.

[9] R. Wu, F. Blaabjerg, H. Wang, M. Liserre, and F. Iannuzzo, "Catastrophic failure and fault-tolerant design of IGBT power electronic converters—An overview," in *Proc. 39th Annu. Conf. IEEE Ind. Electron. Soc.*, 2013, pp. 507–513.

[10] Y. Hara, S. Yoshida, and D. Inoue, "Enhanced over-current capability of IGBT modules for xEVs," *Fuji Electric Rev.*, vol. 66, no. 4, pp. 198–200, 2020.

[11] Infineon Technologies Bipolar GmbH & Co. KG, "Technische information: T2563NH," T2563NH datasheet, May 2011.

[12] ABB, Ltd., "Phase control thyristor: 5STP 45Y8500," datasheet 5STP 45Y8500, Oct. 2016.

[13] ABB, Ltd., "Phase control thyristor: 5STP 48Y7200," datasheet 5STP 48Y7200, Oct. 2016.

[14] F. Carastro, J. Mari, T. Zoels, B. Rowden, P. Losee, and L. Stevanovic, "Investigation on diode surge forward current ruggedness of Si and SiC power modules," in *Proc. 18th Eur. Conf. Power Electron. Appl.*, 2016, pp. 1–10.

[15] J. Birkl and P. Zahlmann, "Extremely high lightning currents: A newly designed surge generator and some practical applications," in *Proc. Int. Conf. Lightning Protection*, 2014, pp. 1183–1188.

[16] O. Liebfried, "Review of inductive pulsed power generators for railguns," *IEEE Trans. Plasma Sci.*, vol. 45, no. 7, pp. 1108–1114, Jul. 2017.

[17] H. J. Boenig, C. H. Mielke, R. A. Robinson, J. B. Schillig, T. Painter, and Y. M. Eyssa, "Design of a 16 kV, 100 kA, 2 Hz power supply for high-field, repetitively pulsed, split-pair magnets," in *Proc. 12th IEEE Int. Pulsed Power Conf.*, 1999, vol. 1, pp. 532–535.

[18] S. Wettengel et al., "Novel thyristor-based pulsed current converter for a medical application—A conceptual introduction," in *Proc. Int. Exhib. Conf. Power Electron., Intell. Motion, Renewable Energy, Energy Manage.*, 2018, pp. 1–6.

[19] V. Verevkin, D. Ivanov, V. Kostusyak, A. Sytyi, P. Semenov, and D. Alymov, "A next-generation surge current tester," *Bodo's Power Syst.*, pp. 30–34, Aug. 2020.

[20] Infineon Technologies AG, "FF1800R17IP5," Datasheet FF1800R17IP5, Version 3.2, Mar. 2017.

[21] Infineon Technologies Bipolar GmbH & Co. KG, "Technical information: T4021N," datasheet T4021N, May 2011.

[22] Infineon Technologies Bipolar GmbH & Co. KG, "Technical information: D6001N," datasheet D6001N, Jun. 2014.

[23] ABB Power Grids Switzerland, Ltd., "Phase Control Thyristor: 5STP 52U5200," datasheet 5STP 52U5200, Apr. 2020.

[24] D. Meeker, "Finite element method magnetics: Home page," Accessed: Dec. 9, 2022. [Online]. Available: https://www.femm.info/wiki/HomePage

[25] *DIN EN 60865-1:1993, Kurzschlussströme - Berechnung und Wirkung - Teil 1: Begriffe und Berechnungsverfahren (IEC 865-1:1993): Deutsche Fassung EN 60865-1:1993*, Deutsches Institut für Normung e. V., , VDE Verlag GmbH, Berlin, 1994.

[26] Würth Industrie Service GmbH and Co. KG, "Dimensioning metric screw assemblies," Accessed: Jan. 5, 2023. [Online]. Available: https://www.wuerth-industrie.com/web/media/en/pictures/wuerthindustrie/technikportal/dinokapitel/Kapitel_06_DINO_techn_Teil.pdf

[27] J. Kienast, A. Hoffmann, M. Höer, and S. Bernet, "Novel distributed control platform and algorithm for a modular multilevel matrix converter," *IEEE Trans. Power Electron.*, vol. 38, no. 7, pp. 8089–8101, Jul. 2023.

[28] A. Hoffmann, "LabAnalyser," Jul. 2022. [Online]. Available: https://github.com/ConverterLabs/LabAnalyser/

[29] K. Suryanarayana, L. V. Prabhu, S. Anantha, and K. Vishwas, "Analysis and modeling of digital peak current mode control," in *Proc. IEEE Int. Conf. Power Electron., Drives, Energy Syst.*, 2012, pp. 1–6.

[30] X. Yang, S. Zong, and G. Fan, "Analysis and validation of the output current ripple in interleaved buck converter," in *Proc. 43rd Annu. Conf. IEEE Ind. Electron. Soc.*, 2017, pp. 846–851.

[31] C. Bajracharya, M. Molinas, and J. A. Suul, "Understanding of tuning techniques of converter controllers for VSC-HVDC," in *Proc. Nordic Workshop Power Ind. Electron.*, 2008, pp. 1–8.

[32] Infineon Technologies Bipolar GmbH & Co. KG, "Technical information: T1901N," datasheet T1901N, May 2011.

[33] J. Wellniak, "Dresden, frauenkirche, panorama.jpg." Sep. 2011. Accessed: Sep. 15, 2022. [Online]. Available: https://commons.wikimedia.org/w/index.php?title=File:Dresden,_Frauenkirche,_Panorama.jpg&oldid=461456248