IEEE Open Journal of
Industry Applications

Received 8 November 2022; revised 30 January 2023; accepted 23 February 2023. Date of publication 27 February 2023; date of current version 18 August 2023. The review of this article was arranged by Associate Editor Sudharshan Kaarthik.

Digital Object Identifier 10.1109/OJIA.2023.3250027

Three-Phase Four-Wire Inverter for Grid Emulator Under Wide Inductance Variation to Evaluate the Performance of Distributed Generator

TSAI-FU WU (Senior Member, IEEE), YUN-HSIANG CHANG, CHIEN-CHIH HUNG (Graduate Student Member, IEEE), AND JUI-YANG CHIU

National Tsing-Hua University Department of Electrical Engineering Hsinchu, Hsinchu 30013, Taiwan

CORRESPONDING AUTHOR: Tsai-Fu Wu. (e-mail: tfwu@ee.nthu.edu.tw)

ABSTRACT This article presents a three-phase four-wire inverter to generate voltage sources under wide filter inductance variation. The voltage sources with distortion and unbalance are to emulate grid voltages. The distortion includes voltage sags, voltage swells, and harmonic components, and the unbalance includes voltage and phase-angle differences. With a conventional PI control and direct digital control (DDC) only, the voltage distortion cannot fulfill precisely because of the improper controls. While with the proposed modified DDC (PDDC) and harmonic-angle adjustment algorithm, the soft core saturation can be taken into account and the harmonic voltage distortion can be accurately emulated, respectively. Moreover, the proposed control scheme can achieve a fast transient response. The control law is derived and the inverter with the control to generate grid voltage is described in detail. Simulated and experimental results from the 10-kW prototype have verified the analyses and discussions.

INDEX TERMS Direct digital control (DDC), grid voltage emulator, modified DDC, PI control, three-phase four-wire (3Φ4W) inverter.

I. INTRODUCTION

Renewable energy has been developed widely. For the test of renewable-energy equipment, grid emulators are indispensable. Power converters to emulate grid voltage have been studied intensively [1], [2], [3], [4], [5], [6], [7], [8], [9], [10], [11]. Most of them are focused on control [1], [2], [3], [4], [8], [9], [10], [11]. The converter uses a three-phase four-wire (3Φ4W) topology realized with insulated gate bipolar transistor (IGBT) and with disturbance generation algorithm to achieve grid emulator. However, the unbalanced mode has not been studied [1]. The one uses 3Φ3W topology, which can only generate a three-phase balanced disturbance applied to a three-phase balanced load, [4], resulting in quite limits of grid applications. The converter shown in [2], [11] can generate selective harmonics effectively with resonant controller and model predictive controller, while it requires *abc* to $\alpha\beta$ frame transformation, increasing computation burden. Narayanan and Umanand [3] employ virtual impedance to realize filters for grid emulator, which has special applications in testing distributed generation, requiring an estimator-based active damping and resulting in a slow transient response, around a one-line cycle to settle down. Liu et al. [8] have used parallel structure fractional repetitive control to realize a high-performance grid emulator, which can be a plug-in component. However, its control is too complicated, requiring individual harmonic controllers one by one. Kim et al. [9] have designed a grid simulator for transient analysis of grid-connected renewable energy system, having limited applications. Messo et al. [10] provide a voltage amplifier to emulate grid-following inverter for ac microgrid dynamics studies, resulting in low flexibility. Although all of these approaches can generate feasible grid emulators, they have some drawbacks and moreover, filter inductor with wide variation has not been addressed.

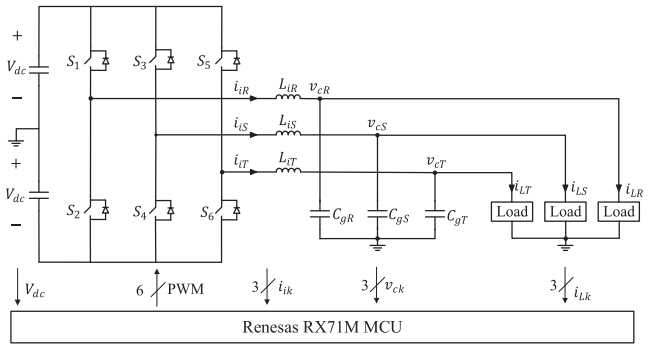

FIGURE 1. Circuit configuration of a 3-phase 4-wire inverter.

Repetitive control is a control scheme designed for tracking repetitive references, and has been intensively applied in industrial fields [12], [13], [14], [15], [16], [17], [18], [19]. It places infinite poles at the system fundamental and harmonic frequencies. Thus, they can achieve zero-error tracking performance. In addition, digital repetitive controllers have simple structures configured by N delay units, where N is the number of samples in one repetitive period, and can be applied to a plug-in type. Thus, a repetitive control is one of the most promising controls for grid simulators since repetitive ac voltages are required to be generated in these applications.

The repetitive control, however, has the limitations of transient response, selectivity, and flexibility issues. Moreover, it cannot cover the inductance variation. The inductor is usually constructed with powder core which has soft saturation and results in inductance variation with its bias current increase. The control [20] operating in *abc* nature frame can take into account the inductance variation. It uses only proportional (P) controller, which yields a significant steady-state error. For grid-current control, the steady-state error is not quite important since the current command is variable. However, for the grid-voltage control, the concern of steady-state error is very serious because of constant command. Thus, the modified direct digital control (MDDC) using PI controller is adopted for grid-emulator control, which can reduce the steady-state error significantly, yielding high-performance system output. Simulated and experimental results have verified the analyses and discussions.

The rest of this article is organized as follows. Section II addresses the inverter design and control algorithms, including conventional PI control, direct digital control (DDC), and MDDC. Simulated and experimental results are presented to verify the control in Section III. Finally, Section IV concludes this article.

II. GRID EMULATOR DESIGN AND CONTROL ALGORITHMS

A 3Φ4W inverter with LC filter to emulate grid voltage is shown in Fig. 1. Design of the filter of the grid emulator can be found in [21]. For the inductance, L, design, it is based on the current ripple attenuation criteria [21] to ensure the minimum current slew rate of the inverter, and it is 2 mH varying down to 0.8 mH. For the capacitance, C, design, it is based on voltage ripple analysis [20]. With linear loads, output voltage THDs mainly depend on the current ripple sharing between loads and filter capacitors. The worst case with the highest voltage THD is under no load condition in which the current ripple charges only the filter capacitors. Hence, to ensure that the voltage THD is within a given maximum THD_M, such as the suggested 8% in IEC 62040-3, the filter capacitance is designed with the voltage-ripple specification. It is around 15 μF.

The control algorithms are described as follows. With load current, capacitor voltage, inductor current and dc-voltage feedbacks, the *Renesas RX71M* microcontroller is following the control laws to determine PWM signals for generating the output voltages. There are three types of controls.

A. CONVENTIONAL PI CONTROL

A conventional PI control algorithm without considering inductance drop is shown as follows:

$$C(s) = k_p + \frac{K_i}{s} \tag{1}$$

where $k_p = 0.053$ and $k_i = 30$. The control block diagram is shown in Fig. 2, in which the inductor parameter is not included in the controller. The PI controller yields oscillating waveforms around the peak of the output voltage, because wide filter-inductance-drop is not taken into account and the control cannot cover so large variation. This will be verified with simulated and experimental results.

B. CONVENTIONAL DDC

The conventional DDC algorithm, which has been presented in [20], considers inductance-drop and can yield smooth output voltage waveforms, being reviewed here for reference. Its inner-current-loop control law through division-summation (D-Σ) process can be derived and shown as follows [20]:

$$d = \frac{1}{2} + \frac{\widetilde{L}_i \Delta i_i}{2V_{dc}T_s} + \frac{v_{ac}}{2V_{dc}} \tag{2}$$

where d is the duty ratio, V_{dc} is the dc-link voltage, T_s is the sampling period, v_{ac} is the output voltage and

$$\Delta i_i[n+1] = i_{Ck}[n+1] + i_{Lk}[n] - i_{ik}[n] \tag{3}$$

where

$$i_{Ck}[n+1] = C_{gk}\frac{V_{ref}[n+2] - v_f[n]}{2T_s}. \tag{4}$$

The argument in i_{Ck} is "n+1" since it uses the reference V_{ref} as the feedforward signal, while the arguments in i_{Lk} and i_{ik} are "n" because they are the feedback signals and the system is a causal system.

Combined with the outer voltage-loop, the overall control block diagram for each phase is shown in Fig. 3, in which $k_i = 0$ for DDC, C_{gk} is the filter capacitors, L_{ik} is the filter inductors where $k =$ R, S, and T, Z_o is the load, and G_d is the delay which is equal to e^{-sT_s}.

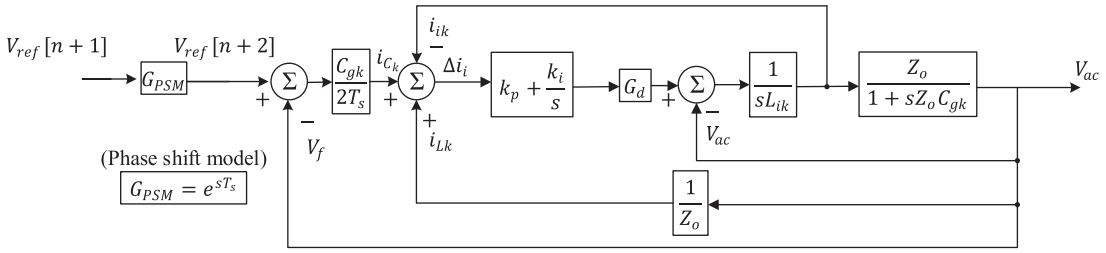

FIGURE 2. Overall control block diagram of the conventional PI control.

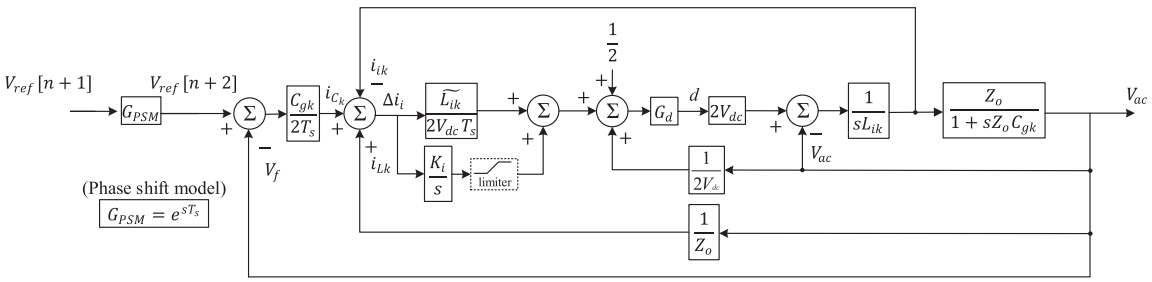

FIGURE 3. Overall control block diagram of the DDC ($k_i = 0$) and the modified direct digital control (MDDC) for each phase.

C. MODIFIED DDC

Since in conventional DDC, the inner-current loop is only with proportional control $\left(\frac{\tilde{L}_{ik}}{2V_{dc}T_s}\right)$, the steady-state error cannot be avoided. Thus, the inner-current loop is modified to the PI controller (MDDC), as follows:

$$d[n+1] = \frac{1}{2} + \frac{\tilde{L}_{ik}}{2V_{dc}T_s}\left(k_p\Delta i_i[n+1] + k_i\sum_{j=0}^{n}\Delta i_i[j]\right) + \frac{v_{ac}}{2V_{dc}} \tag{5}$$

where $k_p = 1$ and $k_i = 760$ are the proportional and integral gains, respectively. With the control law shown in (5) and with the control block diagram shown in Fig. 3, the output voltage can be controlled with reduced steady-state error and achieve fast transient response. Note that the limiter is used to limit the overshoot when there is a step-load change.

For harmonic-voltage control, we introduce the harmonic-angle adjustment algorithm. First, we make the bode plot of v_{ac}/V_{ref} from which the harmonic lagging angles are measured and then, the angles are compensated to generate accurately harmonic voltages. This is equivalent to a proportional-resonant control that can tune the harmonic frequency precisely.

III. SIMULATED AND EXPERIMENTAL RESULTS

The system is configured with six PWM switches and three sets of filter inductors and capacitors, and is operated in nature frame with SPWM control. The following shows the simulated and experimental results from a 10 kW inverter with the specifications shown in Table 1.

TABLE 1. Specifications and Design Parameters

	Symbol	Description	Value
Specifications	$3\phi 4W_{ups}$	Rated Power	10 kW
	V_{dc}	DC-bus voltage	±380 V
	v_C^*	Reference voltage (line-line)	311 V
	f_o	Output voltage frequency	60 Hz
	L_{derate}	Inductance drop	60%
Parameters	i_{ipp}	Maximum peak to peak current ripple	3.5 A
	v_{CTHD}	Output voltage THD (with linear load)	< 3%
	v_{Cerr}	Maximum voltage error	< 50%
	f_H	Switching frequency	20 kHz
	L_i	Inductance drop	2~0.8 mH
	C_g	AC filter capacitor	15 μF

A. SIMULATED RESULTS

The software package PLECS was used to simulate the performance of the grid emulator. The simulated results of an inverter with the conventional PI control algorithm and with the specifications shown in Table 1 are shown in Fig. 4(a). It can be observed that the output voltage waveforms present oscillation around peak, because the inductance-drop with bias current-increase has not been taken into account. While

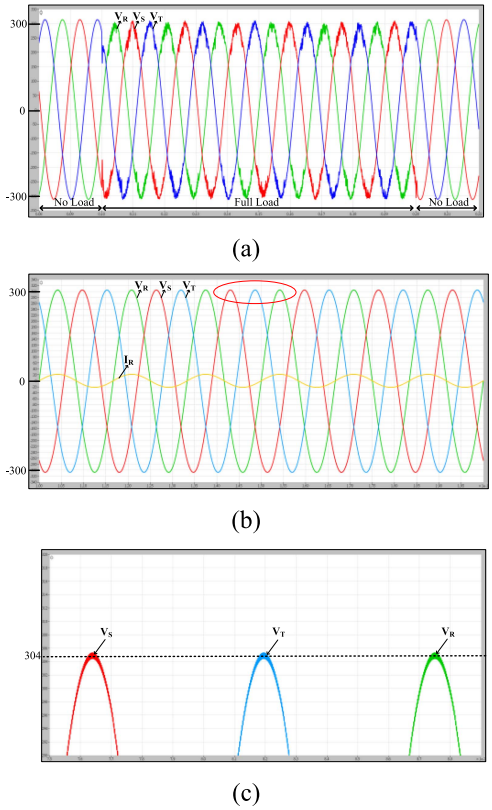

FIGURE 4. Simulated results of output voltage waveforms with (a) a conventional PI-controlled inverter, (b) the DDC, and (c) its zoom-in waveform.

with the DDC, taking into account inductance-drop, the output voltages are present stable waveforms as shown in Fig. 4(b) and their zoom-in waveforms are shown in Fig. 4(c).

However, the steady-state error is still too large (311–304 = 7 V). Thus, we add an integral compensator to the DDC, becoming MDDC, and the output voltages become the one shown in Fig. 5(a) in which the zoom-in waveforms are shown in Fig. 5(b). It can be observed that the steady-state value is around 311 V, improved by 2.25%, since we introduced a PI controller to the MDDC.

For the system with a full-load step change, the results are shown in Fig. 6, in which the black plot is the reference, the red plot is with a conventional PI control and considering inductance-drop (with simulation only), the green plot is the one with P control (DDC) and a limiter of 0.02, and the blue plot is the one with the MDDC and with a limiter of 0.02. It can be seen that the blue one is closely tracking the reference and has less steady-state error than the green one. Note that the limiter is no control at the undershoot since it lacks control efforts.

B. EXPERIMENTAL RESULTS

The hardware prototype of the grid emulator is shown in Fig. 7. The experimental results are shown in Fig. 8 in which Fig. 8(a) shows the results with the conventional PI controller

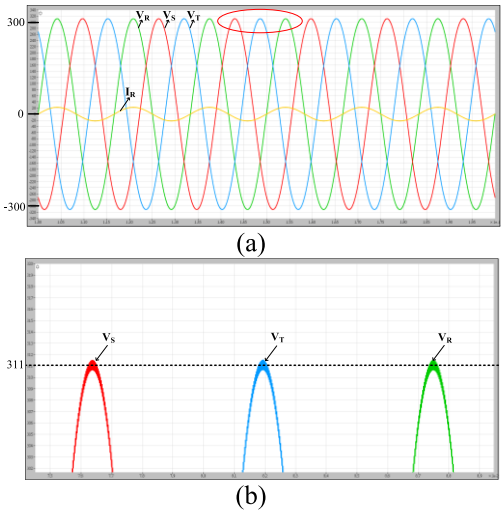

FIGURE 5. Simulated results of the inverter with (a) the MDDC and (b) its zoom-in waveform.

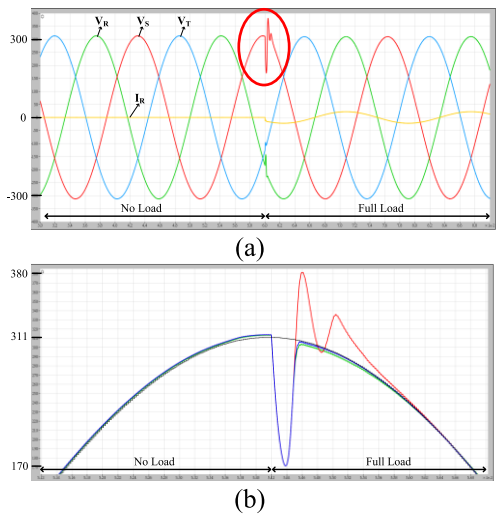

FIGURE 6. Simulated results of the inverter with step-load change. (a) Original, and (b) zoom in; the *black* with the reference, the *red* with conventional PI control. The *green* with DDC and the *blue* with MDDC.

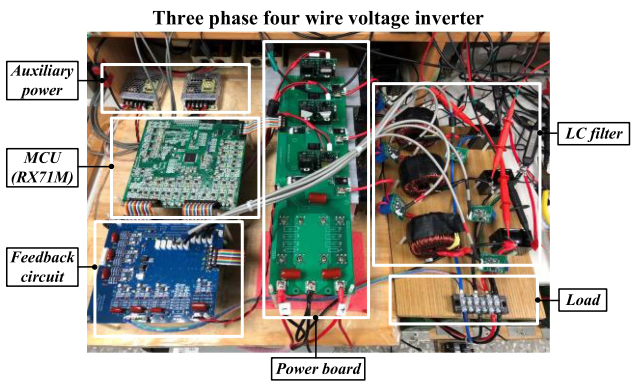

FIGURE 7. Photo of the prototype.

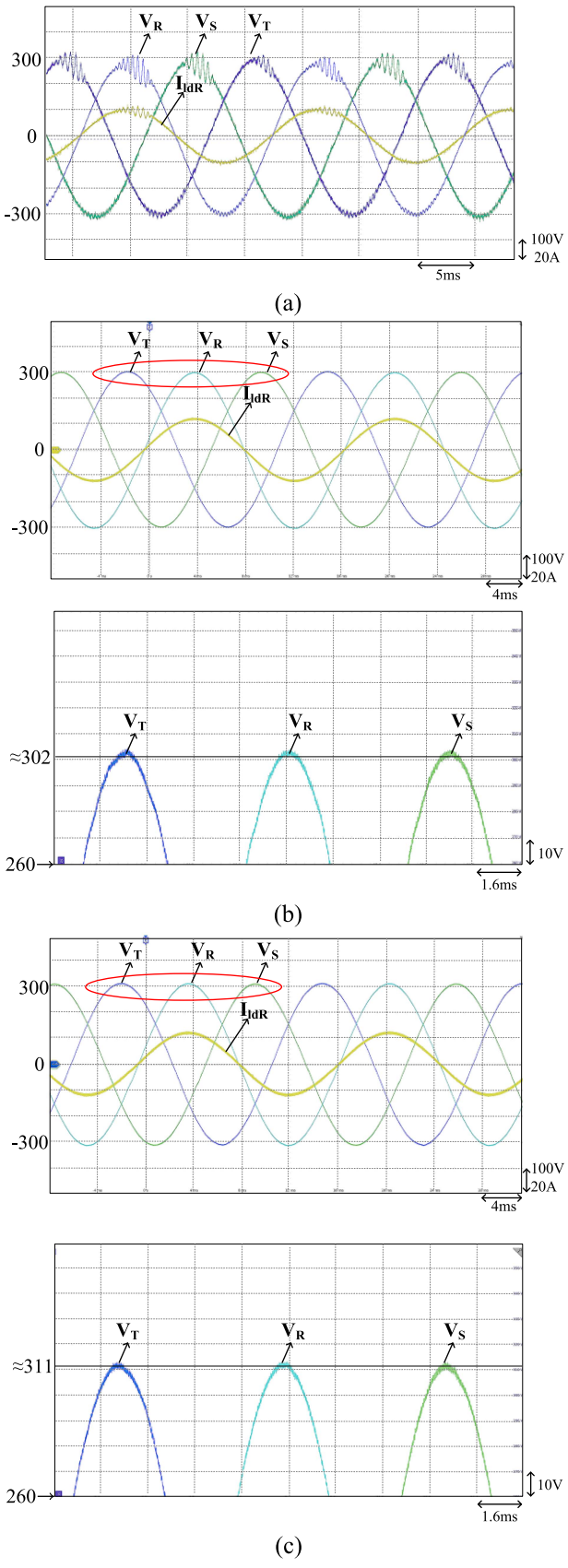

FIGURE 8. Experimental results. (a) With a conventional PI control, (b) with DDC, and (c) with MDDC.

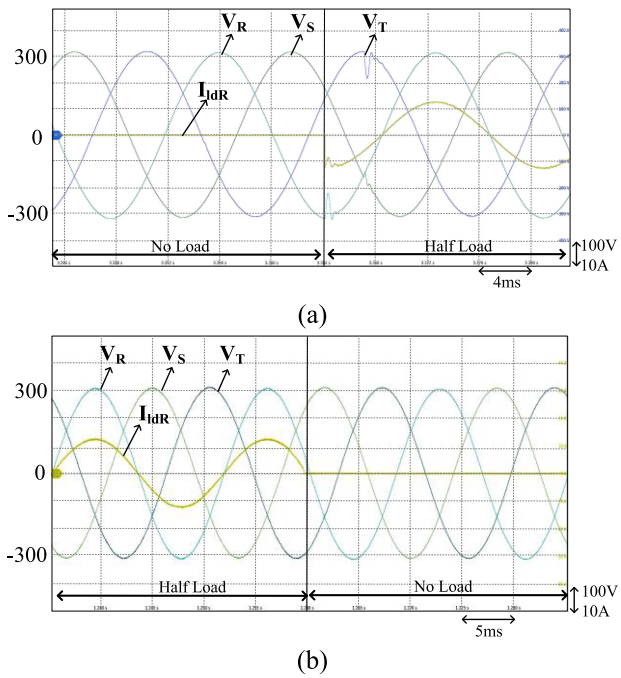

FIGURE 9. Experimental results under step-load change. (a) From no load to half-load, and (b) from half-load to no load.

but does not consider inductance-drop, Fig. 8(b) shows the one with DDC and the peak value = 302 V, and Fig. 8(c) shows the one with MDDC and the peak value is around 311 V, all under 10 kW. Fig. 8(a) shows the one with oscillation because the PI controller does not take into account inductance-drop. Fig. 8(b) shows the stable one but the steady-state error is significant. Fig. 8(c) shows the stable results and the steady-state error has been reduced a lot. It can prove that the proposed control scheme, MDDC, is stable and feasible.

With the step-load change, Fig. 9(a) shows the results from no load to half-load while Fig. 9(b) shows that from half-load to no load, both with the limiter of 0.02. Both Fig. 9(a) and (b) show the ones with less overshoot, proving that the MDDC and the limiter can achieve the desired outputs. The ones with MDDC and without/with limiter are shown in Fig. 10, in which Fig. 10(a) shows the one without limiter and Fig. 10(b) shows the one with limiter. The one with a limiter shows less overshoot.

With harmonics, the voltage source will be distorted and deviated from the nominal value without harmonic angle compensation. For the grid-connected inverter test, the power factor (PF) can be within 0.85 leading and 0.85 lagging, as suggested by IEEE-929 Std. PF = 0.85 leading is equivalent to an RC load, PF = 0.85 lagging is an RL load and PF = 1 is an R load. We make bode plots of the transfer function v_{ac}/V_{ref} under R, RC, and RL loads as shown in Fig. 11, and collect their lagging-phase angles of the fundamental and harmonics in Table 2.

For the loads, they are phase dependent and so are the parameters of the system. The lagging-phase angles can be

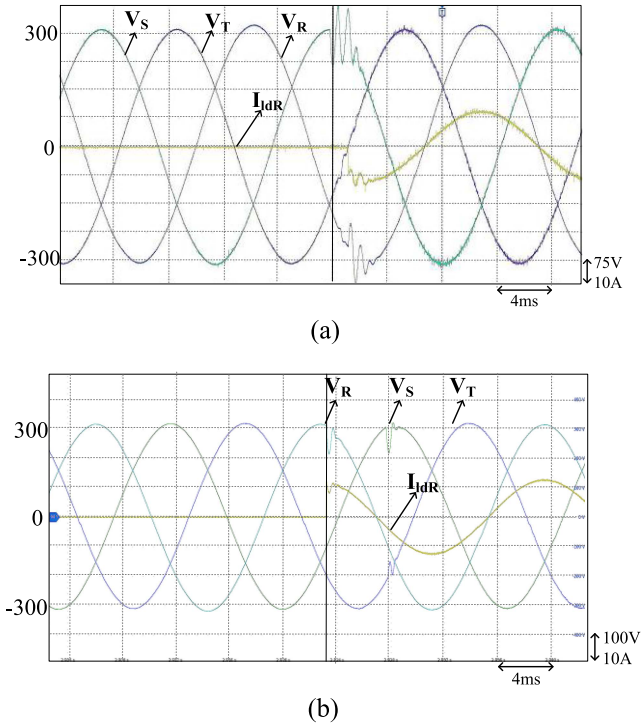

FIGURE 10. Experimental results with MDDC control. (a) Without limiter and (b) with limiter.

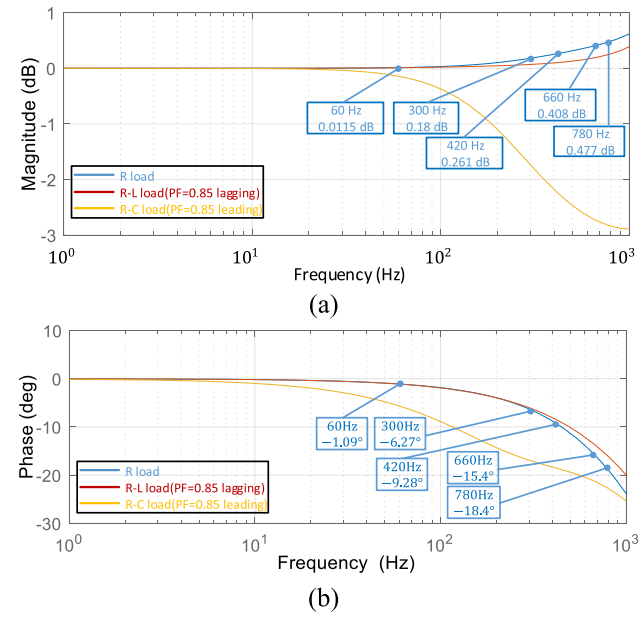

FIGURE 11. Bode plots of the input-to-output transfer function (v_{ac}/V_{ref}) shown in Fig. 3. (a) Magnitude plot. (b) Phase plot.

adjusted according to PFs, as collected in Table 2. For the magnitude, it is almost 0-dB from 10 Hz up to 1 kHz; thus, it is negligible and there is no compensation with the magnitude, except the RC load around 1 kHz.

TABLE 2. Lagging-Phase Angle of Fundamental and Harmonics Under Different PFs

	1st	5th	7th	11th	13th
PF = 1	−1.09°	−6.27°	−9.28°	−15.4°	−18.4°
PF = 0.85 (lagging)	−1.12°	−6.01°	−8.47°	−13.4°	−15.7°
PF = 0.85 (leading)	−5.67°	−16.9°	−18.6°	−21.1°	−22.5°

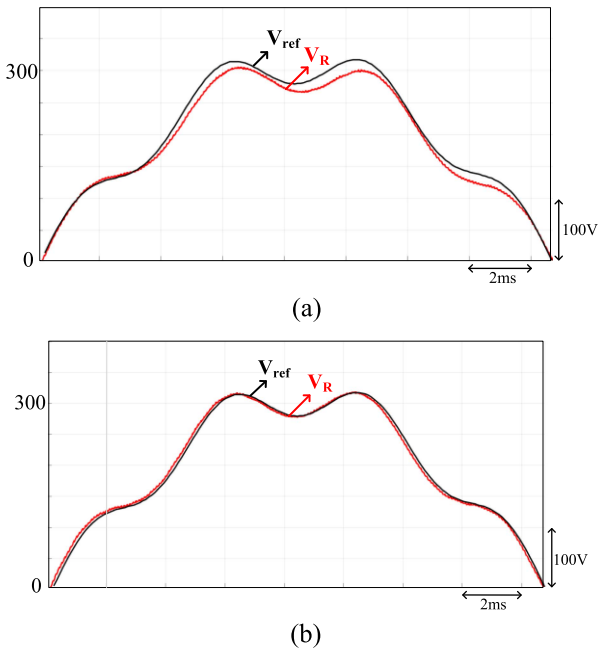

FIGURE 12. Experimental waveforms under 10%/7th harmonic: R load (a) without angle compensation, and (b) with angle compensation.

In the following, we use the 7th and 11th harmonic tests as examples. Fig. 12(a) shows the waveforms under 10%/7th harmonic and R load without angle compensation, while Fig. 12(b) shows that with the harmonic angle compensation. The compensated angle is obtained from the bode plots of the input-to-output voltage transfer function (v_{ac}/V_{ref}), where the 7th harmonic frequency = 420 Hz and lagging angle = 9.28°. The compensation angle is selected to be leading angle = 8.19° (=9.28°–1.09°) since the fundamental frequency = 60 Hz whose lagging angle is 1.09°. Following the same procedure, we can obtain the 10%/11th harmonic-angle compensation as 14.31°. Fig. 13(a) shows the waveforms without angle compensation, while Fig. 13(b) shows that with angle compensation. It can be seen that the compensated results are closely tracking the references. The angle compensation can

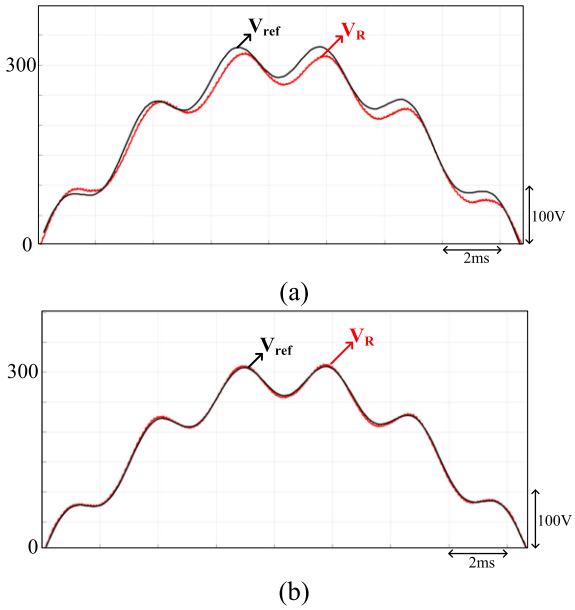

FIGURE 13. Experimental waveforms under 10%/11th harmonic: R load (a) without angle compensation, and (b) with angle compensation.

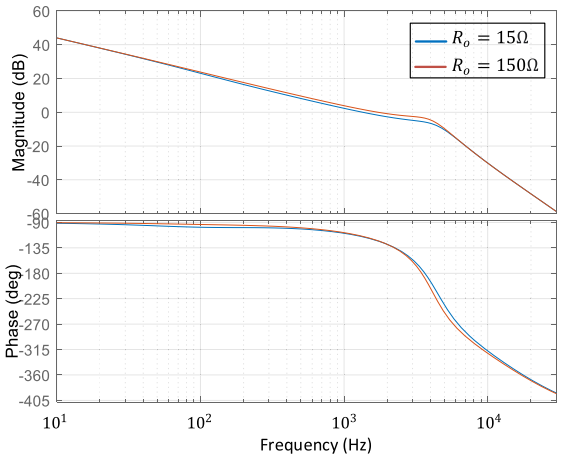

FIGURE 14. Bode plots of loop-gain.

help track the references precisely and therefore, the voltage waveforms can be generated accurately even under distortion and can emulate grid voltage accurately. The other harmonics can follow the same rule to adjust the compensated angles to achieve the accurate output waveforms.

System stability can be determined based on loop-gain plots. Fig. 14 shows the bode plots of the loop-gain of the control block diagram shown in Fig. 3, in which the phase margin is greater than 50°and the gain margin is 5 dB under light (150 Ω) and heavy (15 Ω) loads, proving the stability.

Fig. 15 shows the 10% voltage swell and 10% voltage sag. It can change the voltage abruptly, within 0.3 ms under half load. Furthermore, when voltage fault occurs, the voltage drops to zero and backs to normal. Fig. 16 shows the experimental waveforms whereas Fig. 16(b) shows their zoom-in

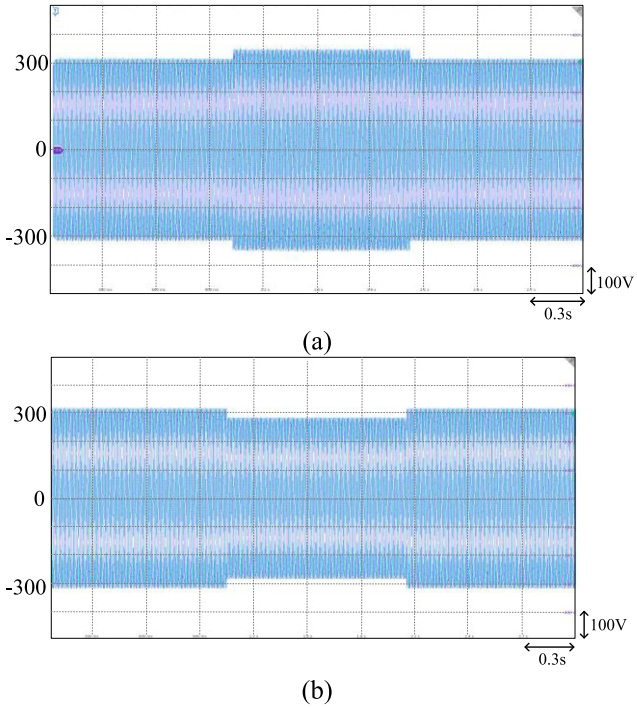

FIGURE 15. Experimental waveforms. (a) 10% voltage swell. (b) 10% voltage sag.

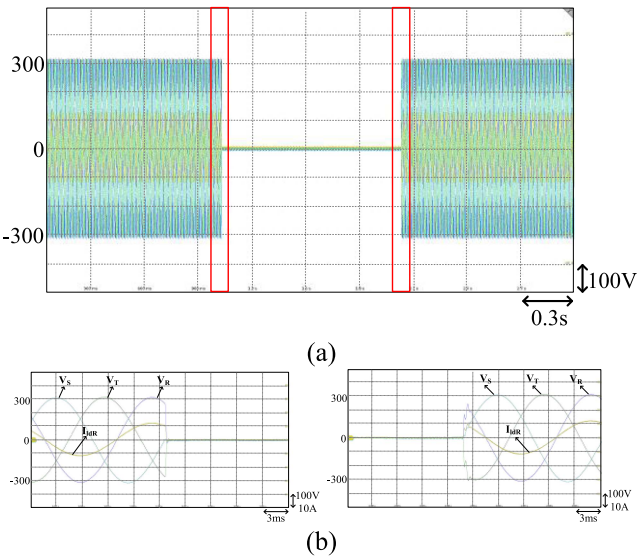

FIGURE 16. Experimental waveforms of three-phase voltage faults. (a) Original and (b) zoom-in, showing the fast response.

ones of the red-boxes shown in Fig. 16(a). With the proposed control MDDC, it can be seen that the response time is within 0.5 ms under half load and achieves a fast transient response.

The capability of the proposed grid emulator to test low-frequency oscillation in voltage amplitude is verified in Fig. 17, in which a $220V_{rms}$ 60Hz three-phase voltage with sinusoidal flicker is generated. The amplitude variation is 5% of the main voltage and the flicker-frequency is 4 Hz.

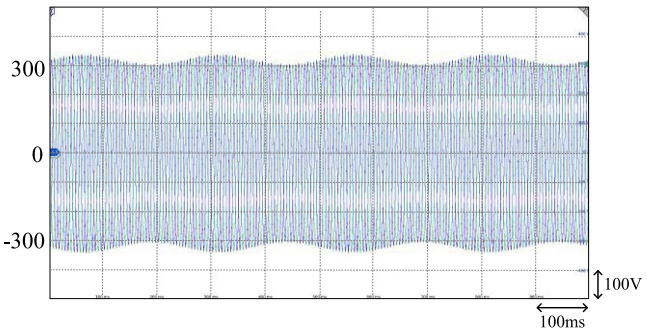

FIGURE 17. Voltage flicker.

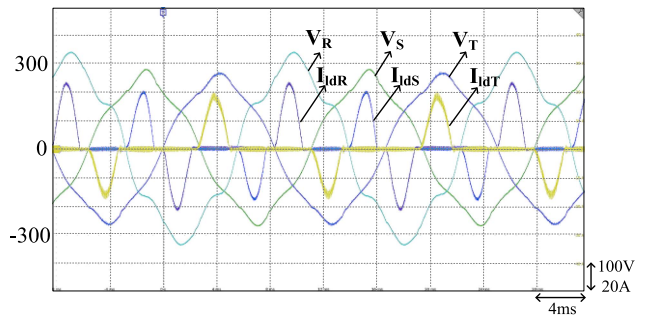

FIGURE 18. Hybrid disturbance.

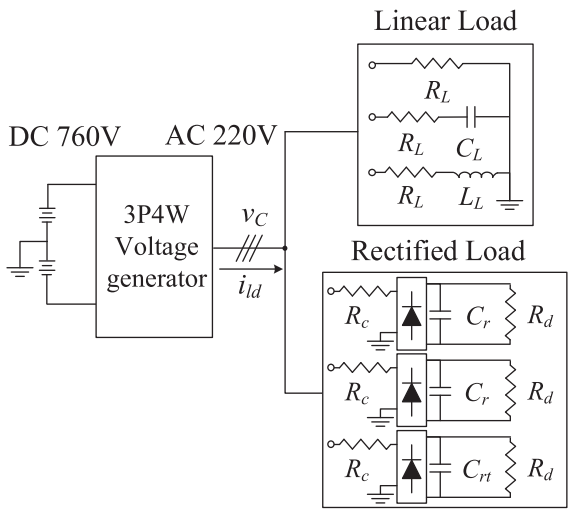

FIGURE 19. Rectified load and linear load.

The figure can verify the effectiveness of the proposed grid emulator.

Hybrid disturbance includes multiple types of disturbance to test the grid emulator. Both voltage dips and harmonic distortion are included in the main voltage. As shown in Fig. 18, V_R contains the 10%/5th-order harmonic and 5%/7th-order harmonic, V_S contains the 7%/5th-order harmonic and 10% voltage sag at the mains, and V_T contains 5%/5th-order harmonic and 10% voltage sag at the mains. The load type is a rectified load which is shown in Fig. 19. From the figure, it can be seen the effectiveness of the proposed grid emulator.

As compared with [3], the proposed MDDC can achieve fast transient response than that with active damping. As compared with [20] and [21], the proposed MDDC can achieve low steady-state error. As compared with [1], the unbalanced modes have been studied in this article. From the above discussions, the grid voltages can be emulated accurately and thus, it can be used to evaluate the performance of distributed generators.

IV. CONCLUSION

This article has presented the inverter with the proposed MDDC, which can achieve the desired outputs. With the MDDC, the inductance-drop with bias current increase has been taken into account; thus, it can avoid the oscillating waveforms and can reduce steady-state error. Moreover, it can reduce voltage overshoot with limiter while step-load changes. Particularly, with the harmonic-angle adjustment algorithm, it can compensate for lagging angle to precisely track the harmonic references, which can generate accurate distorted grid-voltages. The proposed control can achieve fast transient response while voltage faults. It is feasible to emulate grid voltage with the proposed MDDC.

REFERENCES

[1] B. A. Karuppaswamy, S. Gulur, and V. John, "A grid simulator to evaluate control performance of grid-connected inverters," in *IEEE Int. Conf. Power Electron., Drives Energy Syst.*, 2014, pp. 1–6.

[2] J. Eloy-Garcia, J. C. Vasquez, and J. M. Guerrero, "Grid simulator for power quality assessment of micro-grids," *Inst. Eng. Technol. Power Electron.*, vol. 6, no. 4, pp. 700–709, 2013.

[3] K. N. Narayanan and L. Umanand, "A virtual impedance based grid emulator for the performance analysis of distributed generations," in *Proc. IEEE Appl. Power Electron. Conf. Expo.*, 2019, pp. 3013–3018.

[4] G. Si and R. Kennel, "Comparative study of PI controller and quadratic optimal regulator applied for a converter based PHiL grid emulator," in *Proc. IEEE 8th Int. Power Electron. Motion Control Conf.*, 2016, pp. 768–775.

[5] Y. Hu, J. Cheng, Y. Zhou, and G. Chen, "Control strategy of a high power grid simulator for the test of renewable energy grid converter," in *Proc. IEEE 43rd Annu. Conf. Ind. Electron. Soc.*, 2017, pp. 7747–7752.

[6] E. Duymaz, S. Pourkeivannour, D. Ceylan, I. Şahin, and O. Keysan, "Design of a power plant emulator for the dynamic frequency stability studies," in *Proc. 13th Int. Conf. Elect. Mach.*, 2018, pp. 152–157.

[7] M. Jia, N. R. Averous, and R. W. D. Doncker, "Evaluation and comparison of different topologies for a grid emulator," in *Proc. IEEE 22nd Workshop Control Model. Power Electron.*, 2021, pp. 1–8.

[8] T. Liu, D. Wang, and K. Zhou, "High-performance grid simulator using parallel structure fractional repetitive control," *IEEE Trans. Power Electron.*, vol. 31, no. 3, pp. 2669–2679, Mar. 2016.

[9] N. Kim et al., "Design of a grid-simulator for a transient analysis of grid-connected renewable energy system," in *Proc. Int. Conf. Elect. Mach. Syst.*, 2010, pp. 633–637.

[10] T. Messo et al., "Using high-bandwidth voltage amplifier to emulate grid-following inverter for AC microgrid dynamics studies," *Energies*, vol. 12, no. 3, p. 379, Jan 2019, doi: 10.3390/en12030379.

[11] H. Rong, X. Qianming, C. Xu, D. Hongqi, and X. Qiaopo, "Model predictive control of modular multilevel grid simulator," in *Proc. IEEE PES Asia-Pacific Power Energy Eng. Conf.*, 2019, pp. 1–6.

[12] A. Garcia-Cerrada, O. Pinzon-Ardila, V. Feliu-Batlle, P. Roncero-Sanchez, and P. Garcia-Gonzalez, "Application of a repetitive controller for a three-phase active power filter," *IEEE Trans. Power Electron.*, vol. 22, no. 1, pp. 237–246, Jan. 2007.

[13] C. Rech, H. Pinheiro, H. A. Grundling, H. L. Hey, and J. R. Pinheiro, "Comparison of digital control techniques with repetitive integral action for low cost PWM inverters," *IEEE Trans. Power Electron.*, vol. 18, no. 1, pp. 401–410, Jan. 2003.

[14] Y.-Y. Tzou, S.-L. Jung, and H.-C. Yeh, "Adaptive repetitive control of PWM inverters for very low THD AC-voltage regulation with unknown loads," *IEEE Trans. Power Electron.*, vol. 14, no. 5, pp. 973–981, Sep. 1999.

[15] R. Cardenas, R. Pena, J. Clare, P. Wheeler, and P. Zanchetta, "A repetitive control system for four-leg matrix converters feeding non-linear loads," *Electric Power Syst. Res.*, vol. 104, pp. 18–27, 2013.

[16] B. Zhang, K. Zhou, and D. Wang, "Multi-rate repetitive control for PWM DC/AC converters," *IEEE Trans. Ind. Electron.*, vol. 61, no. 6, pp. 2883–2890, Jun. 2014.

[17] W. Lu, K. Zhou, D. Wang, and M. Cheng, "A generic digital $nk\pm m$-order harmonic repetitive control scheme for PWM converters," *IEEE Trans. Ind. Electron.*, vol. 61, no. 3, pp. 1516–1527, Mar. 2014.

[18] W. Lu, K. Zhou, D. Wang, and M. Cheng, "A general parallel structure repetitive control scheme for multiphase DC–AC PWM converters," *IEEE Trans. Power Electron.*, vol. 28, no. 8, pp. 3980–3987, Aug. 2013.

[19] G. Escobar, P. G. Hernandez-Briones, R. E. Torres-Olguin, A. A. Valdez, and M. Hernndez-Gomeza, "A repetitive-based controller for the compensation of 6l+/-1 harmonic components," *IEEE Trans. Ind. Electron.*, vol. 55, no. 8, pp. 3150–3158, Aug. 2008.

[20] T.-F. Wu, Y.-H. Huang, S. Temir, and C.-C. Chan, "3Φ4W hybrid frequency parallel uninterruptable power supply for reducing voltage distortion and improving dynamic response," *IEEE J. Emerg. Sel. Topics Power Electron.*, vol. 10, no. 1, pp. 906–918, Feb. 2022.

[21] T.-F. Wu, Y.-H. Huang, and Y.-T. Liu, "3ϕ4W grid-connected hybrid-frequency parallel inverter system with ripple compensation to achieve fast response and low current distortion," *IEEE Trans. Ind. Electron.*, vol. 68, no. 11, pp. 10890–10901, Nov. 2021.