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Review on Single-DC-Source Multilevel Inverters: Voltage Balancing and Control Techniques

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ABSTRACT Nowadays, single-dc-source multilevel inverter (SDCS-MLI) topologies are being considered as more suitable for many power system applications such as renewable energy conversion systems and electrified transportations compared to the multiple-dc-source MLIs. Voltage balancing of the auxiliary capacitors in those configurations is a major matter of concern. Different techniques have been developed to overcome this issue that can be mainly categorized as internal controller-based and external controller-based techniques. In the former techniques, the redundant switching states help balancing the capacitors voltages. On the other hand, the latter techniques involve external regulators to balance the capacitors' voltages. This article analyzes most of the existing techniques to control and balance the capacitors voltages in SDCS-MLIs, such as pulsewidth modulation, space vector modulation (SVM), hysteresis control, model predictive control, sliding mode, and artificial intelligence based control techniques. Furthermore, a comprehensive comparison is presented to illustrate the advantages/disadvantages of each technique. Finally, some industrial challenges and future works are projected.

INDEX TERMS Control techniques, modulation techniques, multilevel inverters, single dc-source, single-dc-source multilevel inverter (SDCS-MLI), voltage balancing.

I. INTRODUCTION

Multilevel inverters (MLIs) were initially proposed as an alternative to the 2-level inverters. Early research was focused on lowering the rated voltage of the employed switches for high power/medium voltage applications where the technology is market limited. Currently, MLIs are designed to have multiple output voltage levels to reduce the harmonic distortion and filtering size.

MLIs are basically built by combining switching devices and dc sources/capacitors to produce multiple voltage levels while drawing less voltage from each switch compared to the 2-level inverter case. The used switches are switched ON and OFF according to the selected switching pattern to generate different voltage levels at the output terminals yet at low switching frequencies, and thus improve voltage/current quality and reduce the size of the output filter.

The MLI technology was started in the late 1960s with the cascaded H-bridge (CHB) and flying capacitor inverter (FCI) topologies [1]. Later, the diode clamped converter was introduced for low power applications [2]. In the 1980s, neutral point clamped (NPCs) and CHBs were proposed for medium voltage applications [3], [4], while the FCI was employed in 1990 for the first time in the medium voltage and high power industries [5].

Multiple dc source MLI (MDCS-MLI) topologies are built using multiple isolated dc power sources [6], [7]. Such an isolated dc power source might be a PV module, a battery bank, or an ac power supply feeding a transformer and rectifier. However, the main disadvantage of MDCS-MLIs is the likelihood of unbalanced power sharing between feeders leading to power losses and system malfunction [8], [9].

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Therefore, the employment of MLI topologies where the multiple dc power supplies are replaced by auxiliary capacitors is commonly recommended. Such topologies, called Single dc source MLIs (SDCS-MLIs), are properly operating by controlling the voltage across the auxiliary capacitors by proper selection of switching states [10]. SDCS-MLIs have been aggressively replacing the 2-level inverters in power systems without the need of changes on the input side (dc), the output terminals (ac), and minor adjustments in the controller design (the capacitor voltage error will be used to generate the reference current). However, traditional modulation strategies should be replaced by multistage modulation techniques.

Typically, the control strategies applied to power electronic interfaces consist of cascaded current, voltage, or power loops (inner and outer loops). The inner current control is commonly used to ensure an accurate current tracking, sufficient control bandwidth, and fast transient operation [11]. In the outer loop, a voltage regulator is used to reduce the disturbance from both the input source and the network and ensure smooth power flow operation. In PV applications, voltage errors are additionally supplied to the current reference to control the dc link voltage. However, this is not enough to guarantee an appropriate share of active power between the dc-links to balance the capacitors' voltages. For example, an external regulator should be used to balance the voltage across the two dc capacitors of NPC and T3 (a modified version of the NPC inverter where the clamping diodes are replaced by bidirectional switches [12]) inverters in single-phase applications (three-phase applications can take advantage of the redundant switching patterns).

Therefore, the main challenge in a SDCS-MLI topology is to balance the voltage of the auxiliary capacitor while tracking the reference of the output current. Moreover, the state variables are interrelated in most of the SDCS-MLIs (FCI, CSC, MMC, etc.), which means that any change in one variable can affect the others. Thus, additional circuitry or external regulators are typically used to balance the voltage across the auxiliary capacitors, while this task is ensured by taking advantage of the switching patterns redundancy in some topologies. For example, Lim et al. [13] and Ghias et al. [14] proposed a strategy based on phase disposition pulsewidth modulation (PDPWM) to balance the capacitors' voltages of an FCI, while the same technique was applied in [15] to ensure the balancing of the capacitors' voltages of a 7-level 3x2 stacked multicell converter. In [16], an optimal switching-based voltage balancing technique was proposed for stacked multicell converter topologies. Additionally, several model predictive control (MPC)-based strategies (multiobjective control techniques) have been widely applied, as an alternative to the standard proportional integral (PI) controller, to FCIs [17], [18], [19], packed U cell (PUC) [20], [21], [22], [23], [24], [25], [26], [27], and MMCs [28], [29], [30].

Hence, the aim of this paper is as follows.

1) To review the control and voltage balancing techniques for SDCS-MLIs.
2) To discuss the merits and limitations of each technique.
3) To give recommendations for further research and development.

TABLE 1. All Possible Switching States of PUC5 Inverter

States	S_1	S_2	S_3	Output Voltage	V_{ab}	Effect on Auxiliary Capacitor
1	1	0	0	V_1	$+V_{dc}$	No Effect
2	1	0	1	V_1-V_2	$+V_{dc}/2$	Charging
3	1	1	0	V_2	$+V_{dc}/2$	Discharging
4	1	1	1	0	0	No Effect
5	0	0	0	0	0	No Effect
6	0	0	1	$-V_2$	$-V_{dc}/2$	Discharging
7	0	1	0	V_2-V_1	$-V_{dc}/2$	Charging
8	0	1	1	$-V_1$	$-V_{dc}$	No Effect

II. CONTROL TECHNIQUES

The most common control strategies applied to SDCS-MLIs are presented in Fig. 1.

A. PI-BASED TECHNIQUES

Usually, three stages could be identified in the operational structure of PI-based control techniques for SDCS-MLIs: current loop, modulator, and a mid-stage responsible for the capacitor voltage balancing. However, some PI-based techniques have been used to balance the capacitors voltages in SDCS-MLIs without the use of external regulators. In this regard, redundant switching states play a key role. Redundant states generate identical voltage level at the output of an inverter while using different current paths. Therefore, it can charge or discharge an auxiliary capacitor while generating same voltage amplitude at the output [10]. To clearly explain such techniques, a PUC5 inverter is shown in Fig. 2. It can generate 5-level voltage at the output [31], [32]. All switching states are shown in Table 1, where S_4, S_5, and S_6 are complementary to S_1, S_2, and S_3, respectively.

Afterward, to design a voltage balancing technique, all switching states should be analyzed to find their effect on the capacitor voltage. As seen in Table 1, some states charge the capacitor, and some other ones discharge it. The key point is that those redundant states generate same voltage level at the output. For instance, if one assumes that the capacitor voltage is $V_{dc}/2$, and the dc source voltage is V_{dc}, then states 2 and 3 produce the voltage level $V_{dc}/2$ at the output while closing the current path through different switches with different effect on the capacitor voltage. Therefore, an extra condition can be implemented in the modulation in which the voltage feedback from that capacitor is used. Whenever the modulation must generate $+V_{dc}/2$ or $-V_{dc}/2$ voltage level at the output, that feedback sends information regarding the capacitor voltage to the modulation to select between redundant states and sends the appropriate switching pulses to keep the capacitor voltage balanced. If the voltage is less than a threshold, the charging states will apply and vice versa. A sample result of voltage balancing in PUC5 inverter is shown in Fig. 3. The dc source voltage amplitude is changed rapidly to verify the voltage

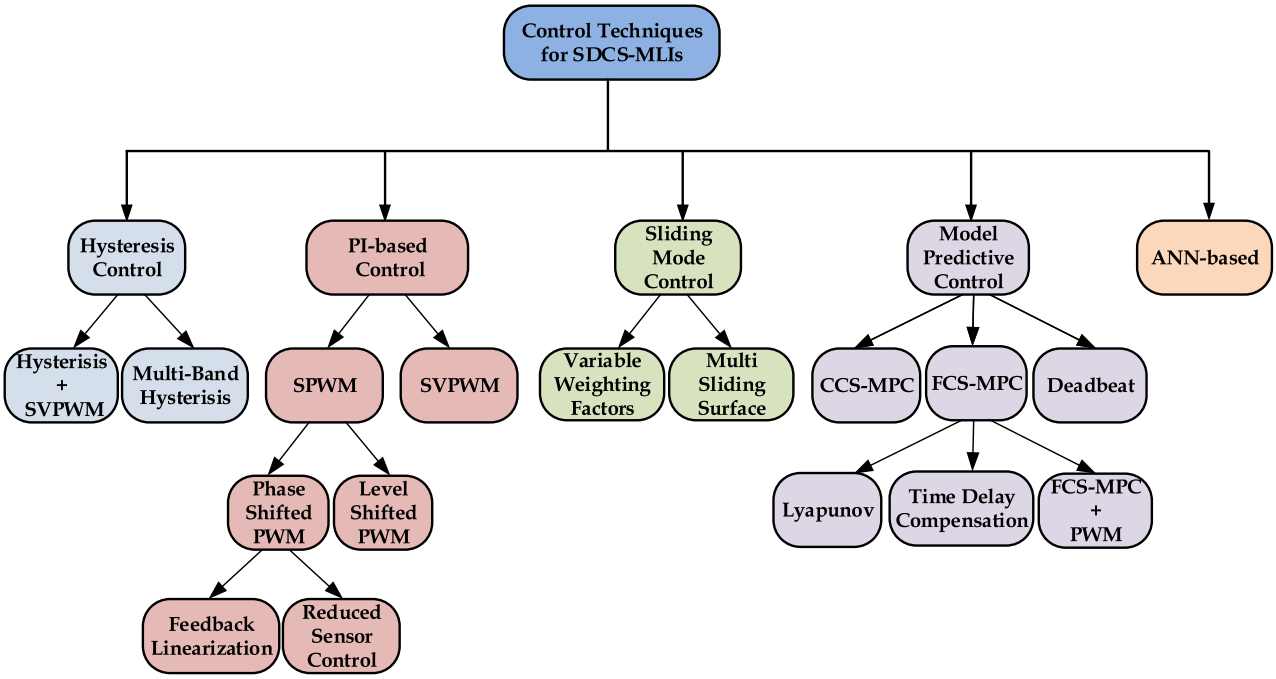

FIGURE 1. Common control techniques applied to SDCS-MLIs.

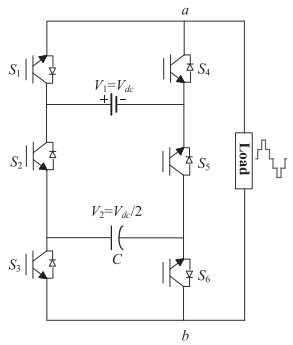

FIGURE 2. PUC5 inverter topology.

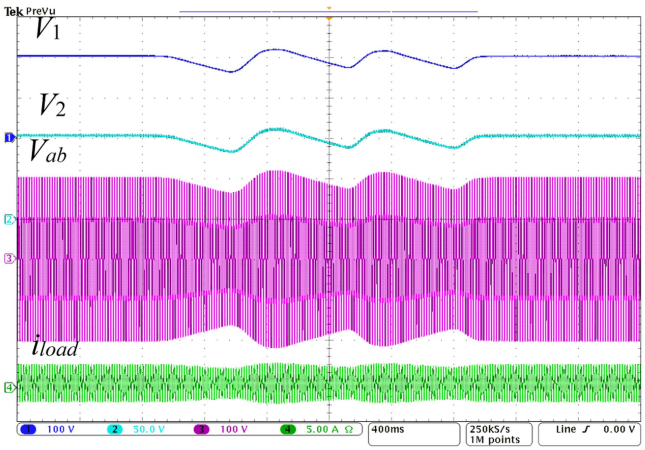

FIGURE 3. PUC5 inverter voltage balancing results.

balancing effectiveness. As it can be seen, capacitor voltage is tracking the dc source voltage precisely since the switching states are updated according to the real-time feedback of V_1.

Having switching redundancies is an asset for MLI configurations. It helps balancing the auxiliary capacitors voltages without using external regulators. Regarding PUC5 topology, various voltage balancing techniques have been developed in the literature. In [33], a sensorless method has been introduced where the capacitor voltage is controlled without feedback. Indeed, it has been proven that a symmetric reference waveform leads to a balanced capacitor voltage in the PUC5 topology due to the identical charging/discharging period of the auxiliary capacitor. Another work has been proposed in [34] to design a fast voltage balancing sensor-less technique, where the transition between redundant states occurs at the speed of switching frequency to reduce the voltage ripples.

Various modulation techniques have been elaborated to integrate the voltage balancing algorithms. For instance, multicarrier level-shift and phase-shift PWM techniques have been severally reported in the literature [35], [36], where they have been applied to different topologies such as CHB, NPC, and FC [37], [38], [39], [40], [41] As well, SVM and three nearest vector modulation have been designed for 3-phase 3-level NPC inverter (see Fig. 4) to balance the neutral point voltage [42]. It has been shown that in NPC inverter, the time of each voltage vector can be adjusted to control the current flowing into the dc link capacitors. Some voltage vectors charge the upper capacitor, while the others charge the lower one. Therefore, by controlling the space vector selection and their corresponding time, the neutral

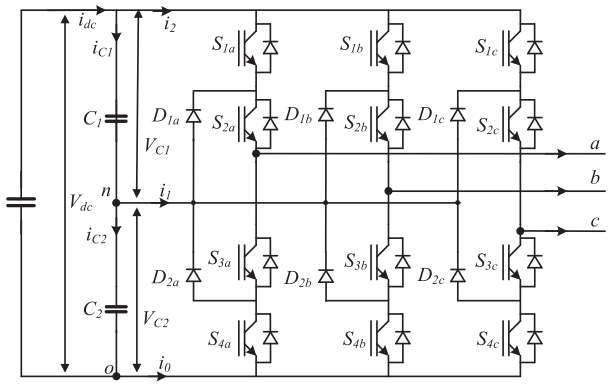

FIGURE 4. 3-phase 3-level NPC inverter.

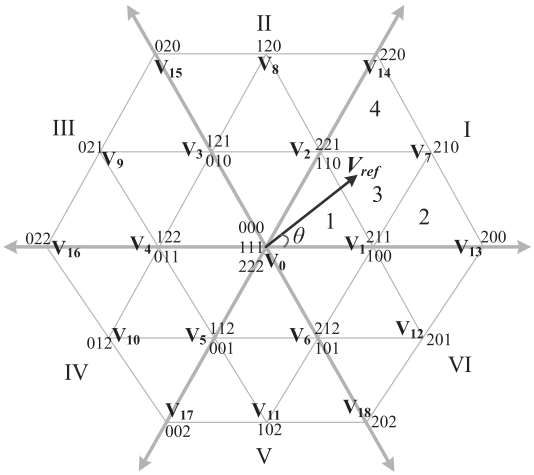

FIGURE 5. Three-level SVM hexagon including six sectors and four regions per sector.

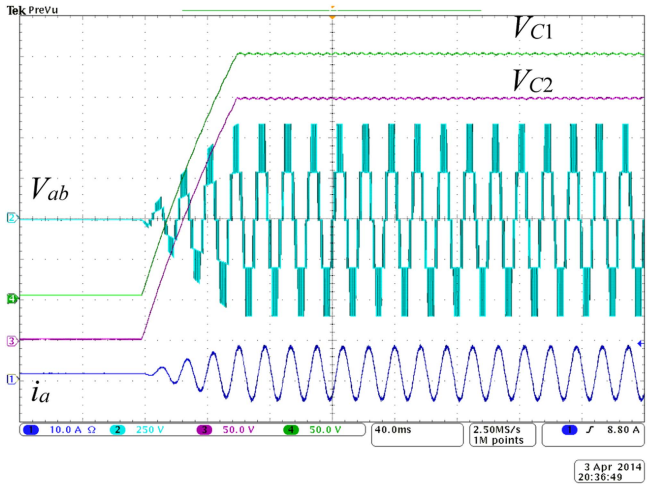

FIGURE 6. NPC Inverter voltage balancing of dc link capacitors.

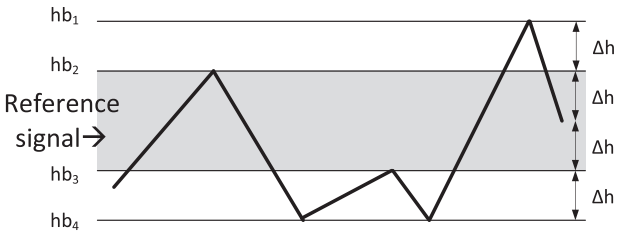

FIGURE 7. Typical multiband hysteresis control technique.

point voltage will be balanced to have identical voltages on dc link capacitors. A detailed design of SVM with integrated voltage balancing technique has been described in [43]. The hexagon of the SVM vectors is shown in Fig. 5. According to the location of the reference vector, three adjacent vectors are selected to produce it. Each vector corresponds to a switching state. Fig. 6 shows the results of voltage balancing using the SVM technique. It is seen that the dc link capacitors voltages track the changes in dc source voltage level accordingly.

B. HYSTERESIS BASED TECHNIQUES

In hysteresis-based techniques, a virtual band is defined based on the desired reference signal. The goal is to keep the real signal inside the reference hysteresis band. If the signal touches the upper limit, some switching pulses will be changed to reduce the signal amplitude. On the contrary, if the signal exceeds the lower limit, other switches will be turned ON to increase the signal and keep it among the upper and lower limits (band). The bandwidth is calculated based on system parameters and has direct effect on the control resolution and switching frequency. A narrow band results in high quality current waveform while increases the switching frequency undesirably. A typical idea of the hysteresis bands and reference signal in multilevel inverters is depicted in Fig. 7.

Hysteresis-based techniques are usually used as current controllers in which the reference current is selected as the converter reference signal. Then the actual current is controlled to remain in hysteresis bands by generating appropriate switching pulses. Hysteresis current control is also known as bang-bang control.

Some papers have derived an equation for the neutral point current of NPC inverter and then controlled it by hysteresis current control. Therefore, the dc link capacitors voltages became identical [44], [45].

In other works, authors have combined hysteresis current control with space vector modulation to control the converter output voltage/current while adjusting the time of switching intervals to balance the capacitor voltages [46], [47], [48].

Also, some papers defined multiband hysteresis current control. In this case, two different approaches have been used to balance the capacitors voltages. One solution is to control the capacitor voltage through an external PI control and then send the reference current into the hysteresis bands [49]. The multiband hysteresis current control is then responsible to generate the corresponding voltage levels at the output and shape a multilevel voltage waveform at the output of the inverter. The other solution has been introduced as a combination with the fact of using redundant switching states [50],

[51]. In this regard, the transitions between each band applies specific switching states that have preanalyzed effects on the capacitor charging or discharging procedure. Therefore, such predefined states help balancing the capacitor voltage through transition of the control signal between different bands.

C. MODEL PREDICTIVE CONTROL TECHNIQUES

In general, MPC techniques are based on predicting the values of the state variables over a prediction horizon using a discretized version of the system's model in the optimization of a designed cost function. MPC was widely proposed for SDCS-MLIs in different applications, where in most of the cases the capacitors' voltages and the output current are the variables to be controlled.

MPC is considered as a suitable controller for power converters owing to its numerous advantages. First, MPC combines the discrete nature of the control law with the continuous nature of the dynamic system. Also, it does not follow the cascaded controllers' structure as in linear control schemes, which results in a faster dynamic response [52]. Moreover, MPC maintains the nonlinearity of the system and waves the need of model linearization around a specific operating point. Its ability to include constraints and to control multiple state variables in one control law eases its implementation in systems with high number of state variables. Moreover, the flexibility in designing multiobjective cost functions makes it applicable for many systems with different natures.

On the other hand, the high computation burden of MPC techniques compared to classical control schemes is considered as the main drawback limiting its implementation. However, the improvement in the field-programmable gate arrays and digital signal processors can overcome this disadvantage. Since MPC is a model-based controller, the model's accuracy affects the control performance and errors. Moreover, the wide spectra resulting from the variable switching frequency of finite control set MPC (FCS-MPC) is a major limitation to its implementation. As it has been shown in the literature, these wide spectra can be kind of manipulated. Also, the delay effect of MPC is one of its performance concerns which pushed some researchers to propose delay compensation solutions.

1) FCS-MPC

FCS-MPC techniques were proposed for various SDC-MLI topologies in different applications, such as grid-connected PUC inverters with their 7L version [20], [21], [53], 9L [25], 15L [26], 23L [54], 7L-PUC rectifier [23], 5L-PUC dynamic voltage restorer [24], grid-connected 9L-CSC inverter [54], FCI with its 3L [56], 4L versions [29], [57], [58], [59], and 8L versions [60], NPC with its 3L [61], [62], 4L [63], and 5L versions [64], [65], 4-L Diode-Clamped Inverter [66], 3L-MMC [28], [29], [67], 5L [68], [69], [70], [71], 11L [72], [73], and 9-L PEC [74]. The main advantage of the FCS-MPC technique is the fact that it does not require the use of a modulation stage and consequently the control actions are applied directly to the system. An analysis of the factors that affect the performance of FCS-MPC showing guidelines for its design was proposed in [75].

The FCS-MPC algorithm is divided into three stages: finding the system's model, predicting the state variables' future values, calculating, and optimizing the cost function.

a) Modeling: The system's model is found offline during the design process. For most of the SDCS-MLIs, the state variables are the capacitors' voltages and the output current, while the system's output is represented by the inverter's output voltage. The values of the state variables and system depend on the switching state which varies the connections between the capacitors and the dc input voltage. Hence, the state space representation includes continuous variables (voltage and current) and discrete variables (switching states or energy modulators), which is considered as a hybrid model. Hybrid models can be obtained by using Bong Graph modeling that is based on the graphical representation of the power transfer [52], [76] or simply by using Kirchhoff's voltage and current laws.

The system's state space representation can be expressed as follows:

$$\begin{aligned} \dot{x}(t) &= Ax(t) + Bu(t) \\ y(t) &= Cx(t) + Du(t). \end{aligned} \tag{1}$$

It is worth noting that the system's matrix (A), the input matrix (B), the output matrix (C) and the feedforward matrix (D) are functions of the applied switching state (vary with time).

The switching configurations of the system are also added to the control algorithm during the design stage through finding all the combinations of the switches' states (ON and OFF) taking into consideration the switching constraints to avoid a short circuit of the dc source.

b) Prediction: The aim of the prediction stage is to find the expected future values of the state variables for a defined time horizon using actual measured values at previous time steps via a discretized version of the system's model. Most of the applied FCS-MPC used the simple Euler forward approximation method to find the discrete version of the state space equations for its simplicity and its low computation burden. Using fourth-order Runge–Kutta method enhances the control performance when it was applied on two levels inverter, however, it required more calculations [77]. The Euler's forward approximation can be written as follows:

$$\dot{x}(t) = \frac{x(k+1) - x(k)}{T_s} \tag{2}$$

where k represents the sampling instant and Ts is the sampling time. If the Euler approximation in (2) is applied to the system represented by (1), the discretized version of the state space representation is given by the following:

$$x(k+1) = x(k) + T_s(Ax(k) + Bu(k)) \tag{3}$$

where $x(k)$ and u(k) are the measured values of the state variables and system's input at instant (k).

The discretized model is used to predict the state variables for the time horizon using all possible switching configurations. The obtained values will be used to calculate the cost function in the following stage. In [60], to reduce the required calculations of predictions using all switching states, the method assumed that the 3-phase cells are isolated and there is no interconnection combination which reduces the prediction from 512 to 24 states. In [72], the prediction for an 11L-MMC is obtained only for a subset of switching configurations after sorting them based on the leg current polarity and capacitor voltage. A similar method was applied for MMC in [73] by using the desired output voltage as a reference to the used switching configuration sub-set for prediction.

To simplify the control algorithm and reduce the computational burden, most of the applied FCS-MPC used a one-step prediction horizon that is equal to the sampling time. This means that at each time step (k), the prediction of only one future time step (k+1) is found. According to [75], FCS-MPC applied to linear systems, with one-step/multistep prediction horizons and without constraints on the switching selection, can be interpreted as a quantized deadbeat control technique. In standard FCS-MPC, even if a multistep prediction horizon is adopted, only the first switching configuration will be applied which requires the same number of calculations to be repeated in the following time step to find its switching solution [52]. It is worth mentioning that using a long prediction horizon to solve an online constrained optimization problem increases the computation burden and the problem complexity [52]. To reduce the required calculations, Cortes et al. [78] showed that extending the predicted switching state for two predictions horizon is effective. However, extending this assumption to three prediction horizons led to an increased current THD. Long prediction horizon up to 100 time-steps was reached in [61] where MPC was applied on 3L-NPC feeding an induction motor.

c) Cost function: The predictions obtained from the previous stage are used to optimize a designed cost function. The switching configuration corresponding to the optimal solution will be applied to the inverter directly without modulation and it will be maintained during the sampling time. The design of the cost function highly depends on the control objective and the application. Overall, it is designed to minimize the deviation between the reference signals and the predicted signals combined in one function over the prediction horizon. Hence, the optimization problem (J) is to minimize the cost function over the prediction horizon as shown in the following:

$$J = \min g(k)$$
$$g(k) = \sum_{p=1}^{p=p_h} \sum_{n=1}^{N} \lambda_n \| x_n^*(k+p) - x_n(k+p) \|^2 \qquad (4)$$

where N is the total number of the objectives, p_h is the length of the prediction horizon, $x^*(k+p)$ is the desired value of the state variable at $(k+p)$instant and $x(k+p)$ is the predicted value obtained from the prediction stage. The weighting factor (λ_n) is added to prioritizes the objectives as it is shown later.

The reference signal $x^*(k+1)$ is not available at instant (k). It is an extrapolated value from reference values in previous instants. First-order and second-order Lagrange interpolations were used in [62], [79], and [80] as shown in the following equations:

$$x^*(k+1) = 2x^*(k) - x^*(k-1) \qquad (5)$$
$$x^*(k+1) = 3x^*(k) - 3x^*(k-1) + x^*(k-2). \qquad (6)$$

In most of the MPC related works in the literature, $x^*(k+1)$ is assumed to be equal to $x^*(k)$ for the sake of simplicity. This assumption reduces the required calculation and results in a good approximation, especially for a small sampling time.

The cost function g shown in (4) is using the squared norm ($\ell_2 -$ norm) for the tracking error, while some works simplified the cost function calculations by using a first-order norm ($\ell_1 -$ norm) that is a sum of the absolute errors. This simplification might lead to a decay in the overall performance and a closed-loop instability specifically for one-step predictive controllers [81]. More details about the impact of the choice of the norm in the cost function can be found in [81].

The main two objectives in the control of SDCS-MLIs are to regulate the capacitors' voltages around the reference values and to enforce the generated current to track its reference signal. Choosing the capacitors' voltage reference depends on the required number of levels at the inverter's output terminals. For example, maintaining the capacitor voltage at third the dc voltage ($V_{DC}/3$) in three cells PUC, generates seven levels [20], [53]. The same voltage reference was used to generate 9L for the CSC topology [54]. Four cells PUC can generate 9L and 15L when the reference values of the two capacitors' voltages are ($V_{DC}/2$, $V_{DC}/4$) and ($3V_{DC}/7$, $V_{DC}/7$), respectively [25], [26], [82]. In MMC topology, the capacitors' voltages are controlled to be maintained around (V_{DC}/N), where N is the number of submodules as in [28] and [70]. When the topology contains multiple cells with different switching frequency, more priority is given to the capacitor's voltage in the high frequency cell [54]. It is worth noting that the switching redundancy decreases when the number of levels increases which raise the effort on the controller function.

On the other hand, the current reference signal consists of three components as shown in (7): the current peak (I_p), the frequency (f), and the phase angle (θ)

$$I^* = I_p \sin(2\pi f + \theta). \qquad (7)$$

The values of the three components depend on the application and the required output power. In the case of stand-alone applications, the frequency term is obtained from an ideal sinusoidal wave and θ is set to zero to generate the maximum active power. For grid-tied PV systems, a phase-locked loop block is needed to guarantee that the generated current is in

phase with the grid voltage. However, a phase shift can be added to the reference signal if a reactive power generation is needed. The value of I_p varies with respect to the available irradiance and determined by a maximum power point tracker or the output of the converter's stage [25], [52]. If the objective is to control the active and reactive power in the system, then the current reference signal is obtained by the desired value of the power as in [74].

In addition, if the topology contains inner inductors such as MMC, eliminating the circulating current in the topology arms is important because of its effect on the rating values of the design components, voltage ripples, and inverter losses. Therefore, a term of the circulating current is added to the cost function [28], [68], [70].

Solving the optimization problem considering one sampling step and ignoring any penalty on the switching actions is a suboptimal solution of the problem [81]. Reducing the switching transitions impacts the conduction and switching losses of power electronics devices which are function of the switching frequency [83], [84]. In some designs, a term to reduce the switching transitions is added to the cost function as follows:

$$g = \lambda_{\text{sw}} \| S(k) - S(k+1) \|^2 + \sum_{n=1}^{N} \lambda_n \| x_n^*(k+1) - x_n(k+1) \|^2 \tag{8}$$

where $S(k)$ and $S(k+1)$ are the switching states at k and $k+1$ instants, respectively. The weighting factor λ_{sw} determines the priority of reducing the switching losses compared to the other errors. This objective was added in [62] and [68]. Another proposition to reduce the switching frequency is to penalize the deviation between the predicted switching frequency and the reference switching frequency over the prediction horizon and a filter can be used to capture the switching frequency [75], [85]. In [54], the total switching transitions was reduced by more than 9% for a one-second steady-state by taking benefits from the redundant states. The cost function is calculated without switching penalty. If the optimal solution is redundant, then all redundancies are compared to the current switching state to select the one with the least transitions. To reduce the switching losses and maintain the fast response of MPC, the design in [86] used a steady-state cost function that considers reducing the switching losses and a transient cost function that concentrates only on the current error.

The cost function was modified in [20], [21], [26], and [28] by normalizing the state variables to accommodate the ranges dissimilarity of the voltage and current variables, which leads to the enhancement of the tracking capability of the controller.

d) Weighting factors: Regarding the weighting factors, they are added to the cost function to sort the priority of the control objectives. Hence, if one variable is controlled, the weighting factor is neglected. To connect an inverter to the grid, the THD of the generated current should be less than 5% according to IEEE 929-2000 standard and IEEE 519 standard. Due to this condition, the current error is prioritized over the voltage error in grid connected systems [20], [54], [87]. Choosing the weighting factors is not straight forward and it has a crucial impact on the system's performance. Moreover, it is challenging in MLIs because of the codependency of the state variables. Therefore, tuning the weighting factors grasped the attention of researchers to propose practical guidelines. In practice, the weighting factors are optimized locally by defining a set of feasible values that are used to find a sub-optimal solution for a defined criterion [75], [88], [89].

Choosing the weighting factors based on branch and bound method for power converters was proposed in [90] by classifying the FCS-MPC cost function. The weighting factors were added as variables in the cost function proposed in [91] where the weighting factors are constrained to be in a trust region that satisfies a defined boundary conditions and the problem is solve repetitively. In [92], the weighting factors are autotuned online by selecting a suitable value from a finite set of weighting factors based on the predicted errors of the state variables. Two levels voltage source inverter was employed in induction motor system and the weighting factors were optimized at each time step using an analytical method [93]. Also, in [94] two levels inverter was used for uninterruptible power supply system, where artificial neural network (ANN) approach was used for weighting factors autotuning. The output of the ANN is the prediction of the system's performance indicators (voltage THD and switching frequency) given a set of possible weighting factors. These values are used to calculate a predesigned fitness function that determines the priority of each indicator. The optimal weighting factor minimizes the fitness function. That method was modified for grid tied 7L-PUC in [87] where the current reference signal was added as an input to the ANN and the performance indicators are the current THD and the error of the capacitor's voltage. By testing different reference current, the results showed that using ANN to autotune the weighting factors enhanced the output current THD. To simplify the autotuning process of multiple weighting factors in multiobjective cost function, some weighting factors can be fixed while autotuning the rest. At the end, the ratio of their respective priority is updated. In [52] and [57], a discrete filter function is used as frequency selective weighting function for the cost function. This proposition enhanced the spectrum of the voltage and current signals. Autotuning of an FCS-MPC applied to 7L-PUC based PV system using an online Sugeno-fuzzy algorithm was proposed in [94].

In [23], Makhamreh et al. proposed a Lyapunov-based MPC technique, where the cost function was designed from the stability point of view. The proposed technique offers no gains tuning requirement yet under various operating conditions and parameters deviation.

To avoid the complications of choosing proper weighting factors, Vyncke et al. [56] proposed a variable cost function that depends on the capacitor's voltage variation. The control technique divides the capacitor voltage range to three regions, namely the tolerance band, the safety voltage band, and the unsafe area. If the voltage deviation is within the tolerance band, the cost function consists only of the current error. If the

voltage deviation is in the safety voltage band, then the cost function combines the current error and the voltage deviation from the threshold of the tolerance band. The cost function is assumed to be infinity in the case of hitting the unsafe area.

In [97], the calculation burden was reduced by solving the dynamic equations just once in the control cycle to find the expected optimal vector and according to it, the nearest prediction is chosen. The proposed method was demonstrated on 3-phase 3-levels NPC. Cascaded FCS-MPC applied on 3-phase 4L-FCI was proposed in [98] to reduce the computational burden.

To manipulate the switching frequency, FCS-MPC were combined with PWM in [99], [100]. In [99], a switching method that combines FCS-MPC and PWM based techniques is proposed. The FCS-MPC is used in the transient response to drive the states near their reference values considering the system's nonlinear model. Then, the controller switches to the linear MPC to asymptotically reach the reference. The lookup table of the optimal explicit linear solutions of the locally linearized model are found offline, while the online algorithm focuses on determining the operating region. The method was proposed for a 4-level FCI, where the output current and the floating capacitors' voltages are controlled. In [100], FCS-MPC is followed by a demodulation stage (low-pass filter) to extract the fundamental and low-frequency components and pass them to a modulation stage to generate the converters gating signals based on the selected fixed frequency. To force the FCS-MPC to operate at a constant switching frequency, Tomlinson et al. [101] bounded the switching sequences to predetermined sequences obtained from PWM behavior. This method requires sampling frequency higher than the switching frequency. Virtual space vectors technique was used to generate fixed switching frequency in [102].

One of the concerns related to the digital implementation of MPC is the processing delay (calculations and samples measurements) which affects the system's performance negatively. Therefore, MPC with time delay compensation was proposed by [77], [103], [104], and [105]. The method solves the optimization problem for $(k+2)$ predictions using $(k+1)$ predictions and the measured values at (k). The predicted optimal solution for $(k+2)$ instant is applied at $(k+1)$ instant. In [106], three prediction steps were used for compensation. The results showed an enhancement in the current signal for different sampling frequency.

When SDC-MLIs are employed in power applications where the objective is to control the active and reactive power, the MLIs capacitors' voltages, the output current and the switching states are implicitly controlled through the power model prediction and the power cost function [66], [107], [108], [109].

It is worth mentioning that the parameters of the applied MPC, the cost function design and the prediction horizon affect the closed loop stability of the system [52], [75].

e) FCS-MPC applied to 3L-MMC: FCS-MPC is applied to the 3L-MMC inverter feeding an RL load (R_L, L_L) presented in Fig. 8. The topology consists of two arms (upper and lower) where each arm has two submodules. The submodule is formed by a capacitor (L) and two switches $(S_i, S_i^{'})$ which work in a complementary manner. All the valid switching states are shown in Table 2. The voltages of the capacitors should be maintained around $(V_{dc}/2)$ to have three voltage levels at the load. Six state variables are considered: the voltage of the four capacitors $(V_i,\ i = 1:4)$, the load current (I_{load}) and the circulating current (I_d). By using Kirchhoff's voltage and current laws, the state equations are obtained as shown in (11). The currents of the upper and lower arms are noted as I_{up} and I_{down}, respectively. These state equations are discretized using Euler's forward approximation which are used for model prediction over one step prediction horizon for all the switching states listed in Table 2.

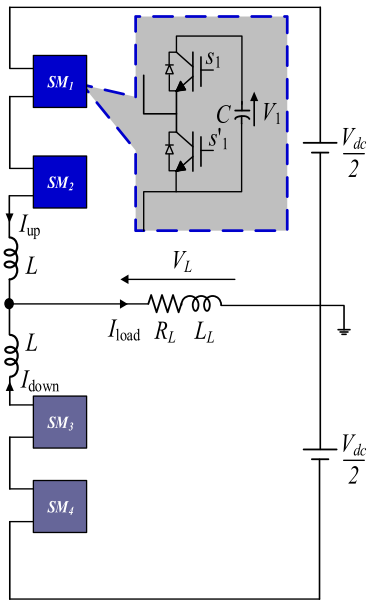

FIGURE 8. Standalone 3-level MMC.

TABLE 2. All Possible Switching States of MMC3 Inverter

States	S_1	S_2	S_3	S_4	Output Voltage
1	0	0	1	1	$V_{dc}/2$
2	1	1	0	0	$-V_{dc}/2$
3	1	0	1	0	0
4	1	0	0	0	
5	0	1	1	0	
6	0	1	0	0	

The obtained results from the prediction states are used to calculate the cost function. The objectives of MMC to eliminate the circulating current in the topology arms while regulating the capacitor voltages around their references and generating an output current that follows its reference signals. Thus, these objectives are combined in one normalized cost function (g) as follows:

$$g = \frac{\lambda_1 \|I_d^* - I_d\|^2}{\Delta I_d} + \frac{\lambda_2 \|I_{\text{load}}^* - I_{\text{load}}\|^2}{\Delta I_{\text{load}}} + \sum_{i=1}^{4} \frac{\|V_i^* - V_i\|^2}{\Delta V_i} \tag{9}$$

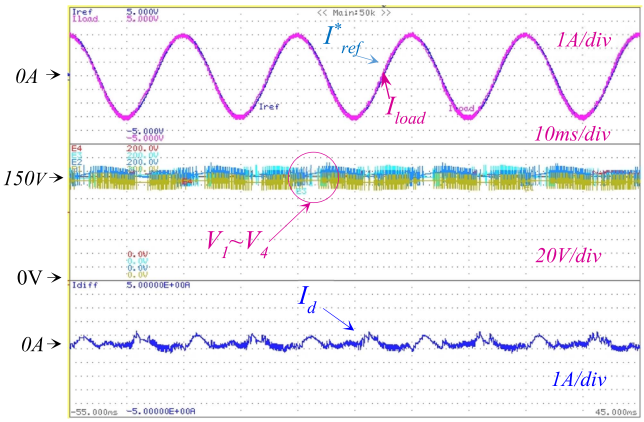

FIGURE 9. FCS-MPC steady-state performance with $\lambda_1 = 50$ and $\lambda_2 = 500$: upper load reference current and actual load current; middle capacitor voltages V_1–V_4; bottom circulating current.

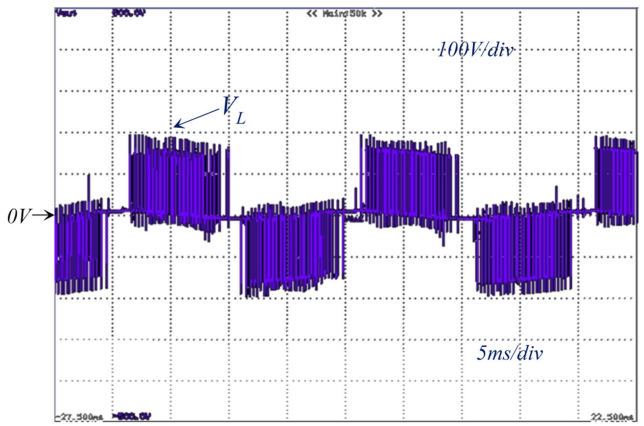

FIGURE 10. Experimental results of the 3-level output voltage waveforms.

$$\Delta x = |\max x\,(k+1) - \min x\,(k+1)| \tag{10}$$

where ΔI_d, ΔI_{load}, and ΔV_i are the normalization terms for the circulating current, the load current, and the capacitors' voltage, respectively. The normalization is based on finding the difference between the maximum and minimum values for the state variables at $(k+1)$ as shown in (10). For more details, refer to paper [28].

An FCS-MPC technique was applied in [28] to a standalone 3L-MMC, where the load is a series connection of an inductor $L_L = 50$ mH and $R_L = 19\ \Omega$, while the dc voltage source equals to 150 V. The inductor arm (L) is 1 mH and the submodules capacitors are 1000 μF. The overall system is operating at 50 Hz frequency, the sampling frequency is set to 10 kHz. The peak of I^*_{load} is set to 3 A. The weighting factors λ_1 and λ_2 are set to 50 and 500, respectively.

Figs. 9–10 show the experimental results of the FCS-MPC applied to a single-phase 3-level MMC. The upper part of Fig. 9 illustrates the load current tracking of the sinusoidal reference, while the middle and lower parts are showing the four capacitors voltages regulated around their reference value and the minimization of the circulating current I_d, respectively.

The generated 3 output voltage levels are depicted in Fig. 10.

$$\frac{V_{dc}}{2} = s_1V_1 + s_2V_2 + L\frac{dI_{\text{up}}}{dt} + RI_{\text{up}} + L_L\left(\frac{dI_L}{dt} + R_L\right)$$

$$\frac{V_{\text{dc}}}{2} = s_3V_3 + s_4V_4 - L\frac{dI_{\text{down}}}{dt} + RI_{\text{down}} - L_L\left(\frac{dI_L}{dt} - R_L\right)$$

$$V_{\text{dc}} = R\left(I_{\text{up}} - I_{\text{down}}\right) + L\left(\frac{dI_{\text{up}}}{dt} - \frac{dI_{\text{down}}}{dt}\right) + \sum_{i=1}^{4} s_iV_i$$

$$I_{\text{up}} = \frac{I_{\text{load}}}{2} + I_d \tag{11}$$

$$I_{\text{down}} = \frac{I_{\text{load}}}{2} - I_d$$

$$\frac{dI_d}{dt} = -\frac{R}{L}I_d + \frac{V_{\text{dc}}}{2L} + \sum_{i=1}^{4} -\frac{s_i}{2L}V_i$$

$$\frac{dV_i}{dt} = \frac{s_i}{C}\left(\frac{I_L}{2} + I_d\right),\ i = \{1, 2\}$$

$$\frac{dV_i}{dt} = \frac{s_i}{C}\left(-\frac{I_L}{2} + I_d\right),\ i = \{3, 4\}$$

$$\frac{dI_{\text{load}}}{dt} = -\frac{R + 2R_L}{2L_L + L}I_L + \sum_{i=1}^{2} -\frac{s_i}{2L_L + L}V_i + \sum_{i=3}^{4}\frac{s_i}{2L_L + L}V_i.$$

2) CCS-MPC

In FCS-MPC, only the real switching states that fulfill the switching constraints are considered as a solution to the optimization problem and the selected switching state is maintained fixed for the sampling time. In continuous MPC, virtual switching states, that form a linear synthesis of two real switching states or more, as shown in (12), are constituting a feasible solution for the optimization problem. Those real states are applied for a partial duration of the sampling time that at its end, the virtual switching state is reached. The complexity of the controller increases with the increase in the number of the virtual switching states [110]. Therefore, a modulator is added to the control scheme to provide the inverter with the switching state composite. This modulator can be PWM or vector-based modulator

$$S^{\text{virtual}} = \sum_{j=1}^{M} d_jT_sS_j^{\text{real}} \tag{12}$$

where $d_1 + \ldots + d_M = 1$, M is the total number of switching states or the candidate vectors $S^{\text{real}} \in$ real switching configurations, and d_j is the duty cycle.

This modulated MPC technique benefits from the advantages of the FCS-MPC and the modulation technique. Adding the modulation stage results in a fixed switching frequency which was one of the drawbacks of FCS-MPC. As a result, the spectrum dispersion of the generated signals is reduced. This leads to diminish the passive filter size [110]. In addition, considering the control region that is bounded by the real

switching states tends to reduce the steady-state error. Furthermore, lower current THD can be gained at low sampling frequency which reduces the control hardware requirements. On the other hand, the need for a modulation stage adds complexity to the MPC control scheme.

Discrete space vector modulation with FS-MPC was applied in [110]. The virtual states are assumed to be half distance from two real switching states. Hence, each real switching state is applied for half the sampling period. The same concept was applied in [111] with an interpolation stage to determine the real states components. Moreover, to reduce the switching losses, the order of the applied real states is decided by comparing the previously applied switching state to the two combination and start with the one with the lowest transitions. Although this method is applied on 2L inverter, it can be extended for MLIs. Instead of assuming a 50% duty cycle of each real switching state, the optimal duty cycles can be calculated based on minimizing the error signal. In [112], the virtual switching state is combined only from the two real configurations that lead to the least values of the cost function and result in non-monotonic states prediction. continuous control set MPC (CCS-MPC) was applied on 3L-FC boost converter [113], 4 leg inverter [114], 3L-NPC [115], 5L-H bridge [116].

In [117], two cascaded MPC technique with SVM was applied on 3L-T type inverter. The technique divides the control objectives into two separate MPC, one for the current and one for the voltage where the optimal solutions are independently determined. The control domain is divided into symmetrical sectors that at each time step, only subarea of the control domain is considered for the optimization problem based on the phase of inverter voltage vector or its magnitude.

Modulated MPC (M^2PC) is designed based on the deadbeat predictive control technique in which the cost function and the weighting factors tuning are eliminated from the control scheme [118]. The reference values are used in the prediction stage to decide the optimal switching state that is applied to the inverter through a modulation stage. In [118] and [119] the method was applied on MMC. For 3L-FCI, vector analysis based MPC was proposed in [120] with a variable switching patterns. The optimal switching state can be synthesized of three real switching states. This method can reach a deadbeat control with a slight increase in the computational burden compared to FCS-MPC.

D. SLIDING MODE CONTROL TECHNIQUES

The sliding mode control (SMC) is a quite interesting control technique [122], [123], [124] with the idea of carrying the system's representative point across a sliding surface, within a finite time, by the application of switching control elements regardless of the initial conditions. The sliding surface is usually defined by the system errors or as a linear combination of the system states, which makes the SMC method robust to parameters uncertainties.

In [122], an enhanced SMC based technique (with variable weighting factors in the sliding functions) was proposed to control the common and differential mode currents in single-phase and three-phase MMCs. The proposed SMC-based strategy provides similar steady-state performance and faster dynamic response compared to the conventional PI controller and less computational burden compared to the MPC-based techniques.

Sebaaly et al. [123] proposed a sliding mode current controller, based on Gao's reaching law to reduce the system chattering, to control the three-phase currents of a grid-connected 3-level NPC inverter.

However, the classical ways of designing SMC strategies are not appropriate for several SDCS-MLIs such as FCI and PUC topologies due to their hybrid nature (bilinear structure, where the control inputs are included in the control matrix) [126]. In such multiobjective control problems, the switching function could be defined as a combination of the error states (output current and capacitor voltage errors). Then, the control action is selected to drive the switching function to zero (zero steady-state error). A possible sliding function could be given by the following:

$$\sigma(x) = \alpha x_1 + x_2 \tag{13}$$

where the parameter α is a weighting gain and x represents the error vector. The system's representative point (state) moves from the initial state till the sliding mode occurs on the line $\sigma = 0$ (reaching mode). Then, the state "slides" on the sliding line till it reaches the steady-state (a zero error is maintained). To ensure the stability of the reaching mode, the condition $\sigma\dot{\sigma} < 0$ should be satisfied.

The controller design requires rules related to the switching function and the system parameters to achieve the achieved conditions. In traditional SMC designs, the dynamic equations of the system must be in such a form that x_2 is directly related to the time derivative of x_1. This allows the sliding mode to be designed to be stable with proper selection of parameter α. However, this is not the case for the PUC inverter. Thus, one of the main contributions of the work presented in [124] was to propose a new "multisliding surface" perception to facilitate the process of switching function selection for hybrid systems (PUC topology). The sliding function in (13) is then replaced by two separate switching functions for each state error. The switching functions were chosen as follows:

$$\begin{aligned} \sigma_1 &= x_1 \\ \sigma_2 &= x_2 \end{aligned} \tag{14}$$

Where the reaching conditions are given by the following:

$$\begin{aligned} \omega_1 &= \sigma_1 \dot{\sigma_1} < 0 \\ \omega_2 &= \sigma_2 \dot{\sigma_2} < 0. \end{aligned} \tag{15}$$

The flowchart of the proposed SMC algorithm, referred as finite control set SMC (FCS-SMC, is shown in Fig. 11. where

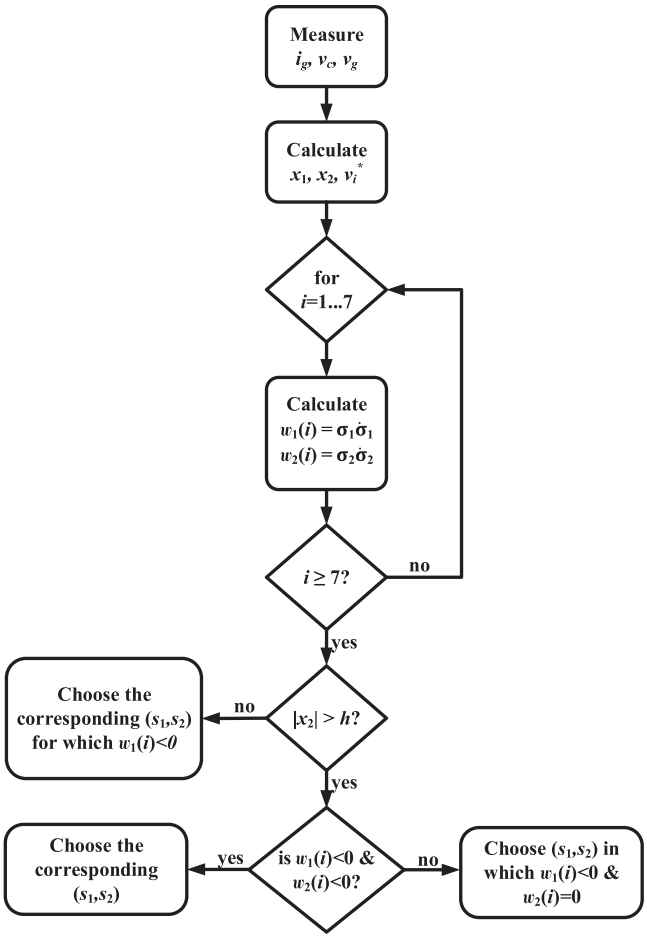

FIGURE 11. Flowchart of the FCS-SMC applied to a grid-connected PUC7 inverter [124].

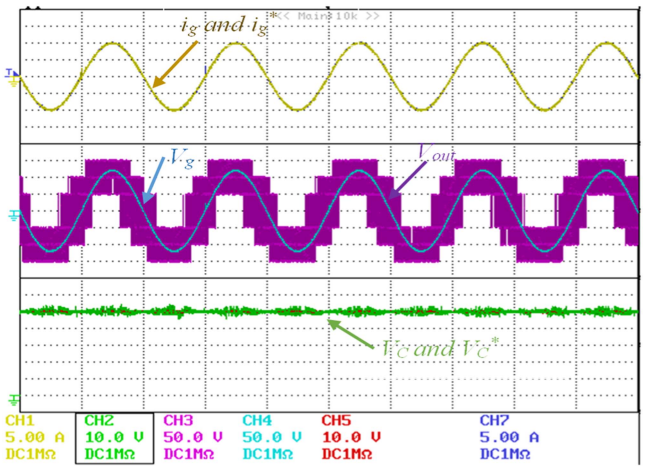

FIGURE 12. FCS-SMC steady-state performance with $h = 0$ V.

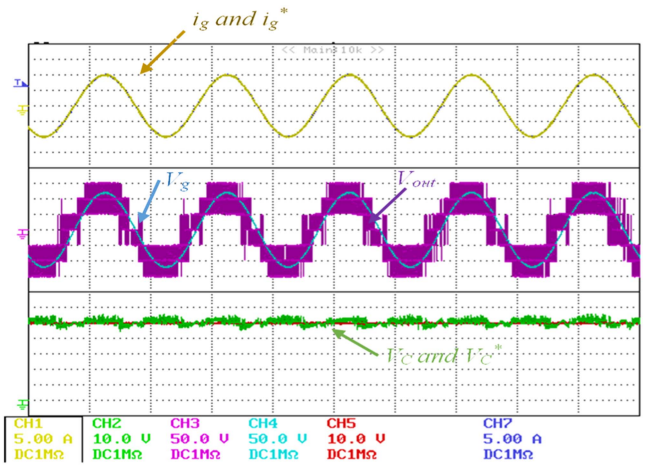

FIGURE 13 FCS-SMC steady-state performance with $h = 1$ V.

the parameter h refers to some hysteresis band of the capacitor voltage error (introduced to reduce the average switching frequency), while i is the index number ranging from $i = 1...7$ referring to the number of irredundant switching patterns (leading to the 7 distinct output voltage levels). The effect of the variation of the hysteresis band h on the average switching frequency could be seen in Figs. 12 and 13.

E. DEADBEAT CONTROL TECHNIQUES

Over the years, prediction-based control techniques and particularly the deadbeat control (DBC) strategies, referred as feedback compensation techniques too, have attracted an increasing research interest for discrete-time dynamic systems. Commonly, the DBC strategies make use of the discretized system model to calculate the control actions needed to achieve a finite settling time with zero steady-state error [128], [129], [130], [131], [132], [133], [134], [135], [136], [137], [138], [139], [140], [141], [142], [143], [144], [145], [146], [147], [148], [149], [150], [151], [152]. Thus, the DBC strategies have been always considered as the fastest (fast dynamic response) and most accurate (zero steady-state error) discrete-time control techniques offering robust time-delay compensation, while characterized by high sensitivity to parameters uncertainties.

The DBC techniques have been widely used in power electronic applications that require high dynamic performance so that the output can reach the reference within two sample periods. Most of these techniques are based on primary predictive control [129] and active filtering [130], [131] to control the output current of the voltage source inverter. However, other methods have been proposed for multiobjective control requirements [132], [137]. In addition, the DBC method is divided into two classes depending on the coordination strategy used (explicit and implicit integration functions). The first class consists of controllers with an explicit integral term in the transfer function (classic controller with deadbeat response and internal mode controller). This makes it possible to compensate for the controller's basic response delay in steady-state. In the second category, DBC responds with a double delay response to all frequency components of the setpoint. The tuning is based mainly on poles placement and differential equations. The latter consists of the direct development of a control algorithm in the form of a differential equation

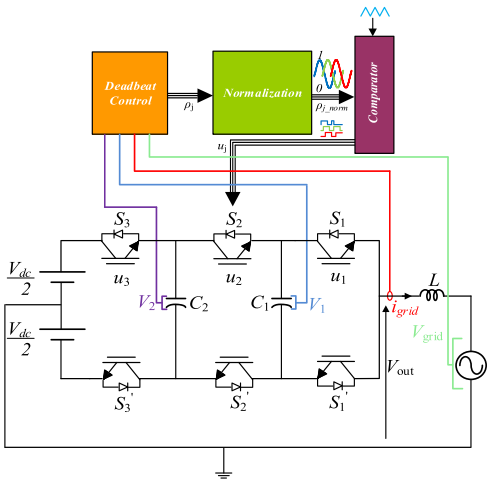

FIGURE 14. Normalized DBC technique for a grid-connected 4-level FCI.

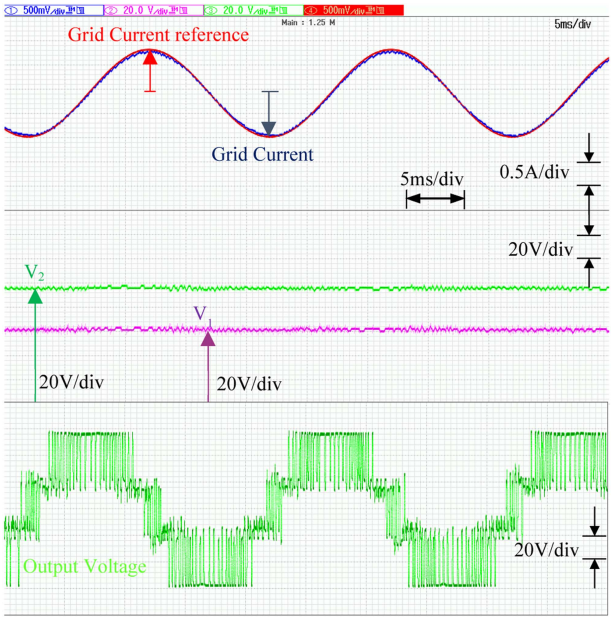

FIGURE 15. Performance of the proposed normalized DBC technique in controlling the grid current and capacitors voltages of a 4-level FCI.

(model inversion), which considers the external disturbances when adapting the controller actions, thus avoiding additional compensation.

In [132], a normalized DBC strategy has been proposed for a grid-tied 3-cell FCI (see Fig. 14) to control the two capacitors' voltages V_1 and V_2 around their reference values while injecting a sinusoidal current i_{grid} to the grid with unity power factor. In the proposed controller, when the desired state is out of reach within the sampling time, the generated duty cycles calculated by (16) are normalized to the common base ([0 1]):

$$D(k) = A_{X_k}^{-1}\left(\frac{1}{T_s}\left(X^*(k) - X(k)\right) - B\right) \tag{16}$$

where $D(k)$ is the control vector (regrouping the calculated duty cycles), A_{Xk} is a variable state matrix (expressed as a function of the grid current and capacitors' voltages state variables), and B is the input matrix.

The proposed overall control strategy is described in Fig. 14 while its performance in controlling the grid current and capacitors' voltages state variable is depicted in Fig. 15.

In [133], Pavan Kumar and Kim proposed a poles placement based modified deadbeat current controller for a hybrid multilevel switching converter. While controlling the output current, the proposed controller allows the voltage balancing among the input capacitors. The idea of the proposed technique is to track any random given reference (dc-biased sinusoidal and triangular reference signals), which is very promising for ring-magnet power supply applications.

In [134], an improved DBC strategy was proposed with considering the converter losses (by adding the voltage losses component to the computed voltage reference) for each switching cycle. The proposed technique has the aim of direct power control of a grid-connected switched capacitor-based PV MLI. In addition, the output voltage sensor was replaced by the prediction of the inverter voltage during the previous sample.

A similar objective (direct power control) was achieved by a deadbeat predictive controller applied for a 3L-NPC based active front end rectifier in [135]. The proposed controller calculates the α–β voltage references allowing the minimization of the active and reactive power tracking errors. The 2-phase voltage references are then converted to 3-phase references to be used along with a phase disposition PWM (PD-PWM) technique to generate the required gate pulses. The proposed controller is characterized by a constant switching frequency (due to the use of the PD-PWM strategy), unity power factor, in addition to a fast dynamic performance in the occurrence of disturbances (ac source frequency variation).

In [136], Chen et al. combined a nearest level modulation (NLM) strategy with DBC to eliminate the circulating harmonic currents in a single-phase MMC. The proposed controller is characterized by its high dynamic performance and capability of handling large steady-state circulating harmonic currents. Moreover, the coordination of the NLM and the DBC allowed the rejection of disturbances at the ac side whereas controlling the circulating current. Where Chen et al. [136] proposed a DBC technique for a single-objective control problem (control of the circulating current), another dual-objective deadbeat predictive current control strategy was presented in [137] to control the circulating and ac output currents in a single-phase MMC (taking advantage of the decoupling characteristic of the circulating and ac currents) by controlling the upper and lower arm voltages. A three-phase MMC was used in [138] to prove the effectiveness of a hierarchical direct power control based improved DBC strategy in balancing the energy of a tundish induction heating power supply system. Furthermore, in order to reduce the sensitivity of the proposed DBC to the plant parameters variation, an auto-correction

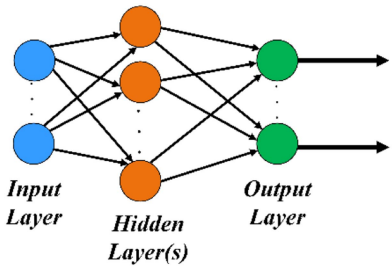

FIGURE 16. MLP-ANN architecture.

computation technique is adopted (estimation of the plant parameters' values).

F. ANN BASED TECHNIQUES

ANN is a simplified imitation for the human neurons that by using various learning techniques, a mapping algorithm between input and output values can be established. Generally, in SDCS-MLI applications, ANN is employed for two purposes: 1) to estimate parameters required in the applied control law, and 2) to replace the controller and generate the control decision. For both applications, multilayer perceptron (MLP) neural network topology is used. The MLP topology is structured of three layers: the input layer, the hidden layer, and the output layer (see Fig. 16) where each layer consists of several neurons. The input layer feeds the ANN with the required data to take the decision and the number of neurons in this layer is equal to the input parameters number. The neurons of the hidden layer are connected to each other based on the architecture design where each connection has a weighting factor, and each neuron has a biasing parameter. Those weighting factors and biasing are updated and determined by a training algorithm applied in the training phase. The hidden layer can be expanded to be multilayers based on the complexity of the problem.

However, Funahashi [139] proved that using one hidden layer with sigmoid functions approximates continuous mappings properly. The number of neurons in the output layer equals the number of estimated parameters by the ANN. The estimated output is mapped to the given input by a chosen output function given all the weighting factors, the biases parameters, and the active function of the hidden layers. This output is fed to the control algorithm or the system according to the application.

The implementation of ANN is mainly divided to three phases.

1) DATA COLLECTION

A set of inputs with their corresponding outputs for several operation conditions are required to train the ANN. This dataset is usually divided into three subsets: a training set, a validation set, and a testing set. The greatest portion is reserved for the training set that is used to update the weights throughout the iterations. The validation set is used to monitor the error of the network during the iterations. The testing set, which is not used during the training iterations, indicates the ANN estimations performance [140]. It is worth mentioning that if the available dataset is small, then all the available data can be devoted for model fitting [140].

2) TRAINING

Generally, this training phase is conducted offline. In this phase, the weighting factors and biases are updated by providing the three data subsets. The difference between the predicted output and the provided output is defined as the error signal. The error values of all predictions are designed into an optimization problem where the objective is to minimize this error given the input, output, and the previous set weighting factors. Different algorithms can be used to solve the optimization problem. The training phase ends when a satisfied performance is reached based on a predefined indicators that vary with the problem such as estimation error and predictive correlation coefficient.

The data collection phase and the training phase can be combined by adding the ANN block to the system and train it during the simulation run.

3) IMPLEMENTATION

After reaching a satisfied performance, the trained ANN is applied to the system. If ANN is used for control's parameters estimation, then the output of the ANN is an input to the control algorithm. When the designed ANN is control based, then it will replace the control block in the system.

As previously mentioned, ANN was used in [87] to estimate the optimal weighting factors of MPC applied on PUC7. The same concept was applied in [141] to autotune the positive power factors of the Lyapunov controller for a grid-tied single-phase 9-levels PEC inverter. Compared to using fixed parameters, autotuned controllers-based ANN showed an enhanced dynamic performance and lower current THD. The Bayesian regularized algorithm was used in [87] where the validation process is unnecessary, while artificial bee colony (ABC) algorithm was applied in [141] to obtain and accurate model in reduced training time. Moreover, the reference tracking was enhanced in [141] and [142] by adding the integral error as an input to ANN.

In [87], an ANN was implemented to autotune the weighting factors in a FCS-MPC applied for a grid connected PUC7 (see Fig. 2). The control objective is to minimize the capacitor's voltage and grid current errors. The designed cost function (g) is given by the following:

$$g = \frac{\lambda_i \left| I_g^* - I_g \right|}{\Delta I_g} + \frac{\lambda_v \left| V_c^* - V_c \right|}{\Delta V_c} \tag{17}$$

where I_g, $I_g{}^*$, V_c, and $V_c{}^*$ are the grid current, the current reference, the capacitor's voltage, and the capacitor's voltage reference, respectively. It is worth noting that ΔI_g an ΔV_c are computed as shown in (10).

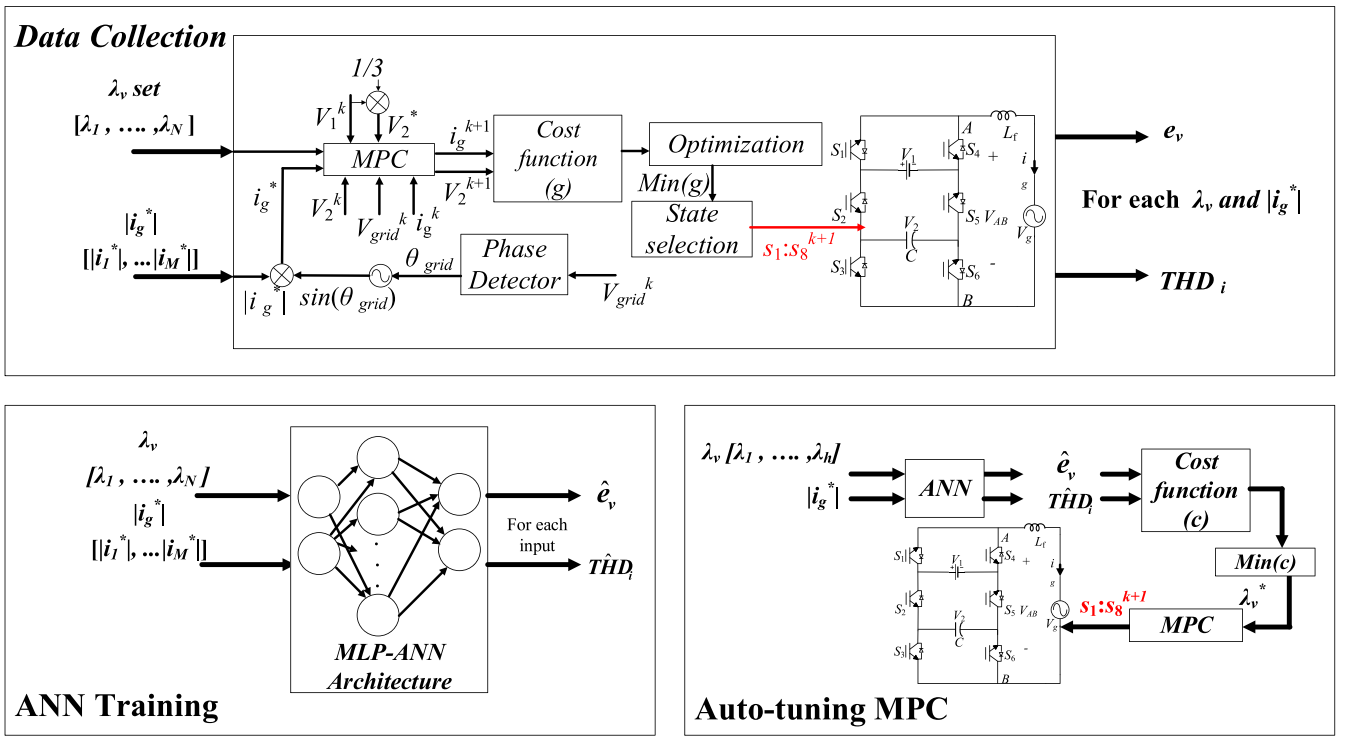

FIGURE 17. Synoptic of the proposed autotuning algorithm.

The ANN was designed to choose the optimal weighting factors (λ_i, λ_v) given the magnitude of the grid current reference $|I_g^*|$ and a set of possible weighting factors to choose from. For the sake of simplicity, λ_i was fixed to 1 while λ_v is dynamic. Since the system is connected to the grid, a higher priority is given to the current error. Hence, λ_v set is chosen to be in [0.01 0.5]. The three phases of the ANN implementation are shown in Fig. 17.

During the data collection phase, $|I_g^*|$ was ranging from 3 to 6 A with a set of λ_v (from 0.001 to 0.5 with 0.001 increment). For each simulated case, the error of the capacitor voltage (e_v), which is the difference between the measured voltage and the reference voltage and the grid current THD_i is computed. These collected data were used to train the ANN using Bayesian regularized algorithm to estimate e_v and THD_i for the input set ($|I_g^*|$, λ_v). The estimated error e_v and the estimated THD_i are $\hat{e}_v$ and $\hat{\text{THD}}_i$, respectively. After the training phase, the designed ANN is implemented in the system as a prior stage to the FCS-MPC. The peak of the reference current $|I_g^*|$ is fed during the system's operation to the ANN with the set of λ_v. The ANN output is ($\hat{e}_v$, $\hat{\text{THD}}_i$) for each ($|I_g^*|$, λ_v). All the obtained estimations are substituted in the cost function (c) shown in (18), where λ_v corresponding to the minimum c is considered as the optimal weighting factor (λ_v^*). The resulted λ_v^* is fed to the FCS-MPC algorithm to select the switching configuration of the PUC7 inverter

$$c = \alpha\ \hat{\text{THD}}_i + (1-\alpha)\,\hat{e}_v. \tag{18}$$

The cost function (c) is designed to reflect the system's priorities through assigning weights to the ANN estimations.

TABLE 3. Grid Current THD for Different $|I_g^*|$ Values and λ_v Tuning Methods

Reference Current $\lvert I_g^*\rvert$	Dynamic λ_v	THD% (Dynamic λ_v)	THD% (Fixed $\lambda_v = 0.2$)
3 A	0.11	2.5	3.1
4 A	0.13	2	2.6
5 A	0.14	1.6	2.2
6 A	0.16	1.3	1.6

Since PUC7 is connected to the grid, a higher priority is given to the current THD which according to international standards (e.g., IEEE 519-1992) must be under 5%. Therefore, α is chosen to be 90%.

To compare the system's performance with a fixed λ_v and a dynamic λ_v, the grid current THD was found for the two cases when $|I_g^*|$ equals to 3, 4, 5, and 6 A. The fixed λ_v is set to 0.2, while the dynamic λ_v is obtained from the trained ANN. The simulation results presented in Fig. 18 show that the use of the dynamic λ_v resulted in a lower THD_i for all current cases compared to a fixed λ_v. The peaks shown in Fig. 18 are due to the numerical calculations of the THD and it doesn't affect the generated grid current [87]. This is shown clearly in Fig. 19 where the generated grid current i_g has a smooth transient response as the reference current is changed. The obtained λ_v by the ANN stage are shown in Table 3 with the current THD in both studied cases.

On the other hand, ANN was used to generate the control decision in some applications to overcome the vulnerability

TABLE 4. Comparison of the Simulation Performances of 4 Common Control Techniques Applied to a Grid-Tied PUC Inverter

	PI	FCS-MPC	OFFLINE SMC	ONLINE SMC
CURRENT THD (%)	1.9	1.46	2.94	2.54
CAPACITOR VOLTAGE ERROR (V)	7.53	0.04	0.96	0.43
TOTAL NUMBER OF SWITCHING TRANSITIONS/CYCLE	728	1874	1257	2037

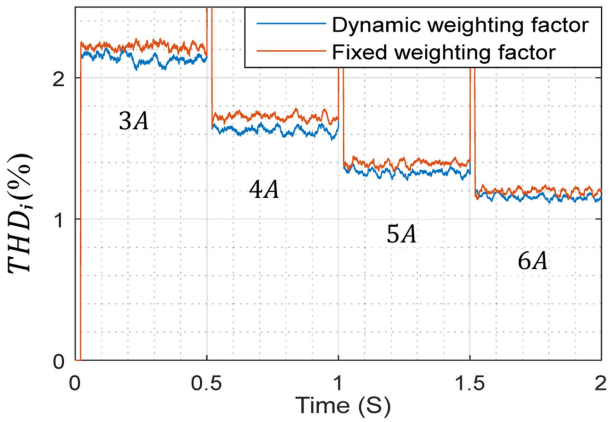

FIGURE 18. THD of the injected grid current for fixed and dynamic weighting factors for four different current magnitudes.

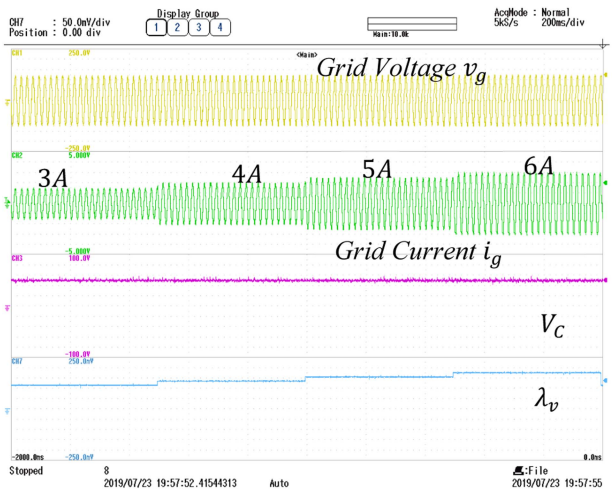

FIGURE 19. Experimental results under dynamic weighting factor.

to the system's parameters and the tuning difficulties of the conventional PI controllers [142], [143], [144]. In [143], an ANN based selective harmonic elimination technique was proposed for modified PUC5 for solar PV applications. The designed ANN was trained with the back-propagation technique based on genetic algorithm to estimate the optimal switching angles as the input dc voltage varies. The architecture consists of a single-hidden layer with 20 neurons and the activation function is chosen to be a binary threshold function that introduces a nonlinearity in the structure. The same approach was applied in [145] and [146]. The inverter in [145] consists of two cascaded modified PUC7 that generates 49-levels asymmetrical MLI where one hidden layer with 10 neurons was used to estimate 24 angles. In [146], ANN is implemented to reduce the required memory size and computing time in the selective harmonics' elimination technique for 9-levels NPC.

The output of the ANN might be followed by a modulation stage to choose the switching configuration of the inverter such as in [144] where ANN was designed for a grid-tied sensor-less PUC5 to regulate the grid line current. ANN based dynamic programming technique was proposed for grid connected rectifier/inverter and PV application to minimize the current tracking error [142], [147]. ANN based SVPWM to regulate the capacitors voltages of 5-levels three phase diode clamped inverter was proposed in [148]. The feed-forward tan-sigmoidal activation functions were selected because of their capability in approximating nonlinear function of arbitrary degree with the minimum number of neurons. ANN based radial-chordal decomposition control was proposed in [149] for a 9-levels PEC used in electrical spring application.

III. CONTROL TECHNIQUES COMPARISON

The simulation performances of four controllers applied to a grid-tied PUC5 inverter, namely FCS-MPC [20], PI-based controller [33], online SMC (calculates the control low at each time step for all the switching patterns and chooses the state that satisfies the sliding surface conditions) [124], and offline SMC (a lookup table is calculated offline by considering all possible switching patterns with the sliding surface conditions) [125], are investigated in section. The system's parameters were unified for all the simulation cases, where the grid voltage is set to be 120 Vrms with a fundamental frequency equal to 60 Hz, the filtering inductor is equal to 5 mH with a series resistor of 0.01 Ω, the size of the PUC5 capacitor is 1 mF, the peak current reference is set to 10 A, and the input dc source voltage is 200 V.

All controllers were designed to minimize the THD of the grid current and regulate the PUC5 capacitor voltage around its reference value, while working at unity power factor. Since FCS-MPC and SMC have variable switching frequency, their

TABLE 5. Comparison of the Most Common Control Techniques for SDCS-MLIs

Control Families	Control Technique	Advantages	Disadvantages
PI-based Techniques	PI + Conventional modulation techniques	• Easy implementation • Fixed switching frequency	• Cannot ensure a proper share of the active power among the DC links • External controllers/additional circuits should be employed to regulate the DC capacitors' voltages
	Modified LSPWM based technique [35]	• Use of the redundant switching states to balance the capacitors' voltages	• Higher complexity compared to conventional techniques
	Modified PSPWM based technique [36]		
	Modified SVM based techniques [37], [38], [39], [40], [41]		
Hysteresis-based Techniques	Hysteresis + SVPWM [46], [47], [48]	• Easy implementation • Fast dynamic performance • Good accuracy	• High switching frequency for a better accuracy • External controllers/additional circuits should be employed to regulate the DC capacitors' voltages
	Multi-band Hysteresis [49]		
MPC	FCS-MPC [20], [21], [22], [23] [24], [25], [26], [27], [28], [29]	• Fast dynamic response • Ability to include constraints with different natures • Multi-objective control • Doesn't require the use of a modulation stage	• Variable switching frequency • Complexity of weighting factors' tuning • Time delays
	FCS-MPC + PWM [99], [100], [101], [102]	• Fixed switching frequency	• The modulation stage adds complexity compared to the FCS-MPC • Time delays
	FCS-MPC with time delay compensation [77], [103], [104], [105]	• Time delay compensation • Improved system performance	• Increased complexity • Higher computation burden
	Lyapunov-based MPC [23]	• No gain tuning is required. • Easy implementation • Reduced number of sensors • Cost function derived from a stability point-of-view	• Variable switching frequency
	CCS-MPC [110], [111], [112], [113], [114], [115], [116], [117], [118], [119], [120],	• Fast dynamic response • Ability to include constraints with different natures • Multi-objective control • Fixed switching frequency • Reduced steady-state error	• Complexity increases with the increase in the number of the virtual switching states • The modulation stage adds complexity compared to the FCS-MPC • Increased computation burden compared to FCS-MPC
SMC	Variable weighting factors-SMC [122]	• Low computational complexity • Robustness (matched external disturbances, parameters variation...) •	• Chattering • Not appropriate for hybrid topologies
	Gao's reaching law-based SMC [123]		
	Multi-sliding surface [124]	• Easier switching function selection for hybrid systems • Low computational complexity • Needless of gain tuning	• Variable switching frequency
DBC	Normalized Deadbeat Control [132]	• Zero steady-state error • Fastest dynamic performance • Robust time-delay compensation	• High sensitivity to model parameters and measurement noise
	Poles placement based modified DBC [133]		
ANN-based Techniques	ANN based controllers [87], [141]	• Capture the non-linear relationship between the input parameters • Enhance the dynamic performance of the system	• Add efforts to the control design (data collection and training phases) • Accuracy depends on the size and operating condition of the collected data • Higher computation effort
	ANN controllers [143], [148]		

maximum switching frequency (25 KHz) is chosen to be the PWM switching frequency of the PI-based controller. The weighting factor of the FCS-MPC is set to 0.2, while the voltage hysteresis of the SMC is set to 1 V.

The simulation results are summarized in Table 4 where the capacitor voltage error is the mean of the absolute voltage error, and the total number of transitions/cycles measures the average of total switching events of the six switches per one fundamental cycle. The presented results show that, under the same simulation conditions, all controllers succeeded to track the sinusoidal current reference with a THD less than 5%, while FCS-MPC is offering the least current THD of 1.46% and capacitor voltage error (0.04 V). It is worth mentioning that severe reductions of the capacitor size by 95% (50 μF) and 99% (10 μF) have almost no effect on the quality of the grid current tracking (a current THD of 1.46% and 1.44% respectively) and a marginal effect on the capacitor voltage error (0.86 and 4.3 V, respectively) when applying FCS-MPC. However, the cost of the high performance of the FCS-MPC can be observed by the high total number of switching transitions per cycle which is more than the double of the computed one when applying PI controller and 50% more than the one corresponding to the application of the offline SMC.

Furthermore, Table 5 presents a summary of the advantages/disadvantages of the most applied control techniques.

IV. CHALLENGES AND FUTURE TRENDS

Nowadays, new MLI topologies are finding their way to industry where NPC and CHB are already used in high-power applications. Although SDCS-MLIs have the highest chance to get attracted by power electronics companies, the main reason which currently restricts their applications is the auxiliary capacitors and the associated voltage balancing issues as mentioned in the classification of control techniques presented in this article. Some topologies use large capacitors to reduce the voltage ripples. This results in a higher manufacturing cost and large size of the product. On the other hand, some voltage balancing techniques are characterized by high computation burden. As a remedy (low-complexity voltage balancing, design consideration …), 5-level SDCS-MLIs (such as 5-level ANPC and PUC5) are currently considered as mature technologies and widely used in many applications (EV chargers, PV inverters …). However, the higher the number of voltage levels, the more complicated voltage controllers. Thus, more research and development are needed to design new control techniques for SDCS-MLIs, which meet the requirements such as reducing voltage ripples, high dynamic performance, less sensitivity to parameters' changes, high steady-state performance, reduced computation burden and complexity (novel switching techniques with embedded voltage balancing approaches), easy implementation, and fault tolerance. The latter has been considered as the most challenging requirement for SDCS-MLIs. Usually, modifications are made on the SDCS-MLI topologies (replacing auxiliary capacitors by additional dc sources) to integrate fault tolerance [153]. Postfault strategies with no hardware alterations have been also introduced in the literature where the fault tolerance capability is ensured by the available redundant switching states and adjustments on the generated control signals. However, the main challenge has been the loss of the capacitors' voltage balancing in some faulty scenarios (yet the output voltage levels are fully generated) [154]. Therefore, some of the challenges regarding the control and voltage balancing of SDCS-MLIs can be listed as the following.

1) Reducing the auxiliary capacitors voltage ripples.
2) Reducing the high-frequency current in auxiliary capacitors.
3) Reducing common mode voltage.
4) Integrating voltage balancing techniques into switching patterns for MLIs with high number of voltage levels.
5) Designing fault tolerant controllers for SDCS-MLIs.
6) Reducing the complexity of voltage controllers on SDCS-MLIs with high number of output voltage levels.
7) Designing new switching algorithms with integrated voltage balancing techniques and harmonic suppression.

V. CONCLUSION

This article proposed an extensive review on voltage balancing and control techniques for SDCS-MLIs, while design illustrations have been shown for some topologies. The mostly applied methods, such as MPC-based, PI-based, SMC-based, and ANN-based control techniques have been reviewed and analyzed based on their structure, advantages/limitations, and industrial applications. The reviewed techniques have been categorized into two categories. The first one regroups the techniques using modulators integrated into the switching patterns and use redundant states to balance the capacitors' voltages. The second category regroups the controller-based techniques that use modeling, equations, or external regulators to control the capacitors voltages along with other control states in the inverter. While PI controllers combined with conventional modulations techniques could be seen as the most easily implemented solutions, they are strongly suffering from their incapability of proper sharing of the active power among the dc links, while external controllers/additional circuits should be employed to regulate the dc capacitors' voltages. From the other side, MPC-based techniques have been extensively considered as good alternatives to the former strategies owing to their high dynamic performances and ability to include constraints with different natures (multiobjective control). However, though some MPC-based techniques such as CCS-MPC solve the problem of variable switching frequency, the wide application of MPC in industrial applications is slowed down by the requirement of powerful processors to perform the needed real-time calculations (high computation burden). This is where SMC-based techniques have been gaining ground with offering easier switching function selection for hybrid systems, lower computational complexity, and needless of gain tuning. However, most of the latter techniques are affected by the chattering problem. Accordingly, the industrial challenges and future works have been discussed in

this article to give better and extended ideas, depending on the specific application, to the researchers in the field.

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