









# A Survey on FEC Techniques for Industrial Wireless Communications

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**ABSTRACT** Industry 4.0 aims to digitize industrial processes entirely, and wireless technologies represent one of the enablers for scalable and flexible communications. However, the current standards and proprietary solutions do not meet the industry's tight requirements in fundamental use cases such as factory automation (FA). One of the key research challenges toward replacing wired fieldbuses with wireless links is the design of techniques that enable real-time and deterministic behavior when transmitting short packets. Forward error correction (FEC) techniques are critical to this objective, and coding/decoding algorithms must comply with reliability and low latency specifications. This article surveys existing FEC techniques for short packet transmissions. Compared to other survey papers in the field, we propose several FEC candidate techniques specifically suitable for FA wireless systems. We explore four of these techniques, also examining hardware architecture proposals. This article proposes a methodology to evaluate their latency and reliability performance. We finally discuss the lessons learned and challenges for future research.

**INDEX TERMS** Complexity, factory automation (FA), forward error correction (FEC), industrial wireless communications, Industry 4.0, latency, PHY, reliability, short packet transmission, wireless communications.

## ABBREVIATIONS USED IN THIS ARTICLE

3GPP	3rd Generation Partnership Project.	BPSK	Binary phase-shift keying.
5G NR	5G New Radio.	B-DMC	Binary-input discrete memoryless channel.
AR3A	Accumulate-Repeat-3-Accumulate.	BER	Bit error rate.
AR4JA	Accumulate-Repeat-by4-Jagged-Accumulate.	BLER	Block error rate.
AWGN	Additive white Gaussian noise.	BCH	Bose–Chaudhuri–Hocquenghem.
ASIC	Application specific integrated circuit.	BPM	Burst position modulation.
ASIP	Application-specific instruction set processor.	CVA	Circular Viterbi algorithm.
ATSC	Advanced Television Systems Committee.	CCSDS	Consultative committee for space data systems.
ARQ	Automatic repeat request.	CC	Convolutional codes.
BM	Base matrix.	CA-Polar	CRC-aided polar.
BP	Belief propagation.	CRC	Cyclic redundancy check.

DVB-S2	Digital Video Broadcasting - Satellite - Second Generation.	TPC	Turbo product codes.
DVB-T2	Digital Video Broadcasting - Second Generation Terrestrial.	URLLC	Ultrareliable low latency communications.
DSSS	Direct sequence spread spectrum.	UWB	Ultrawideband.
E2E	End-to-end latency.	UMTS	Universal mobile telecommunications system.
FA	Factory automation.	USRP	Universal software radio peripherals.
FPGA	Field programmable gate arrays.	WirelessHP	Wireless high-performance.
FEC	Forward error correction.	WIA-FA	Wireless networks for industrial automation-factory automation.
GPU	Graphics processing unit.	WPAN	Wireless personal area network.
HART	Highway addressable remote transducer protocol.	WiMAX	Worldwide interoperability for microwave access.
HARQ	Hybrid automatic repeat request.	WAVA	Wrap-around Viterbi algorithm.
HAR2D-FI	Hybrid channel Access with redundancy for reliable and deterministic Wi-Fi.	ZTBCC	Zero tailbiting convolutional codes.
IEC	International Electrotechnical Commission.		
ISM	Industrial Medical Scientific Band.		
ISA	International Society of Automation.		
LDPC	Low density parity check.		
LLR	Logarithmic likelihood ratio.		
LTE	Long-term evolution.		
LT	Luby transform.		
MAP	Maximum <i>a posteriori</i> .		
MediaFLO	Media forward link only.		
MAC	Medium access control layer.		
MBMS	Multimedia broadcast multicast services.		
NASA	National Aeronautics and Space Administration.		
OMNET++	Objective Modular Network Testbed in C++.		
OSI	Open systems interconnection model.		
OSD	Ordered statistics decoding.		
OFDMA	Orthogonal frequency-division multiple access.		
OFDM	Orthogonal-frequency division multiplexing.		
PER	Packet error rate.		
PLR	Packet loss rate.		
PCCC	Parallel concatenated convolutional codes.		
H	Parity check matrix.		
PHY	Physical layer.		
PPDU	Physical layer protocol data unit.		
PAC	Polarization-adjusted convolutional codes.		
PEG	Power edge growth.		
PA	Process automation.		
QPSK	Quadrature phase-shift keying.		
QC	Quasi-cyclic.		
RAN	Radio access network.		
RS	Reed–Solomon.		
SCCC	Serial concatenated convolutional codes.		
SNR	Signal-to-noise ratio.		
SDR	Software-defined radio.		
SVC	Sparse vector code.		
SCF	Successive cancellation flip.		
SCL	Successive cancellation list.		
SHARP	Synchronous and hybrid architecture for real-time performance.		
TBCC	Tailbiting convolutional codes.		
TDMA	Time-division multiple access.		

## I. INTRODUCTION

The fourth industrial revolution, also referred to as Industry 4.0, is one of the most promising fields where research on information technologies is under development. Its principal goal is to digitalize the entire industrial process. The transition requires the inclusion of the latest communication technologies: wireless networks, tactile internet, Internet of Things, and in general, the optimization of the so-called cyber-physical systems. Wireless communications bring significant advantages to this scenario while posing relevant technological challenges [1].

Regarding the wireless transition, numerous actors from both the industrial world [2], [3], [4], [5], as well as from the standardization committees [6], [7], [8] have established several guidelines for successful wired to wireless transition in a variety of scenarios [4]. Indeed, the industrial world encompasses diverse environments, which differ in applications and environmental properties. Some examples are factory production processes or factory automation (FA), surveillance systems, electricity production assets, transport infrastructure, oil production, chemical material handling, etc. FA is among the most challenging use cases for *ad hoc* wireless system design and deployment. Contrary to the traditional requirements of generic wireless communications, which entail the transmission of large-size data, FA wireless communications involve the transmission of short data packets with high reliability and reduced latency.

### A. FIELDS OF APPLICATION FOR FA

FA comprises different fields of application that are necessary for the operations of monitoring and controlling in the industrial environment. These processes are distinguishable among critical and noncritical processes. Based on the criticality level of the processes, several layers of the Open Systems Interconnection model (OSI model) have to be adapted [9].

Numerous players from the industrial world [2], [3], [4], [5] and from standardization committees [6], [7], [8] have suggested their use case vision for FA, and defining the desired performance at the MAC layer. However, such guidelines are challenging to accomplish in the case of highly critical or safety communications. Few proposals offer partial solutions

**TABLE 1.** Proposed Fields of Application

Use case	Reliability [PER]	Latency [ $\mu$ s]	Payload [B]
Safety communications	$10^{-9}$	0.25-4	From 6 to 24
Critical communications	$10^{-9}$	0.5-20	From 8 to 1024
Noncritical communications	$10^{-7}$	Not relevant	Up to 33k

that, nevertheless, do not entirely fulfill the required performance range [10]. Table 1 presents a classification of the fields of application for the industrial wireless systems as a function of the link-level requirements. The definition of requirements follows the guidelines of [4], [7]. We have considered three key parameters: payload length, reliability, and latency. Reliability and latency are defined as packet error rate (PER) and end-to-end (E2E) latency. The PER evaluates the correct interpretation of the message, while the E2E latency estimates the time interval between the data generation and its future reception at the MAC layer.

Based on the presented parameters, three prominent fields of application are recognized: Non-critical communications, which include, for example, monitoring operations and involve less stringent requirements. Existing wireless technologies are currently applied in such scenarios. Critical communications demand communication systems designed to protect people, machines, and production processes. Such scenarios denote strict reliability and latency requirements. Finally, the case of safety communications covers all the risk reduction operations associated with personnel and equipment damage prevention and protection. In this case, the communications require extremely low latency data transfer.

## B. WHY FEC?

Optimizing all ISO/OSI layers towards real-time communications [9] is necessary for the demanded performance for FA fields of application. Focusing on the PHY layer, two strategies can be considered [11]. First, the automatic repeat request (ARQ) techniques introduce some check-bits in the transmitted packet for retransmitting the erroneous messages. However, on the other hand, retransmissions introduce undesirable delay during the packet transmission [12]. The other strategy is the FEC. These techniques include some redundancy bits within the packet during transmission. At the receiver, this redundancy allows the detection and error correction of the received message, avoiding the delay effect discussed in the previous case. Consequently, including FEC techniques within the industrial wireless systems has potential benefits for achieving the desired performance in terms of reliability and latency. The requirements have been briefly introduced in Section I-A.

## C. RELATED WORKS AND CONTRIBUTIONS

### 1) RELATED WORKS

Despite a large body of surveys on FEC for short packet transmissions, only [20] attempts to address some issues related to FA. The majority of the encountered surveys focus on URLLC, which requires different performances related to latency and reliability. However, their results are essential for the development of this topic.

Sybis et al. [13] compare different FEC candidates for 5G URLLC communications, previously identified by 3GPP. Analysis for both reliability and complexity are proposed, considering different decoding algorithms. Liva et al. [14] present a survey of modern codes for short packet transmission. Iscan et al. [15] compare different FEC schemes for 5G URLLC communications. Moreover, different decoding algorithms are included in the study. Wu et al. [27], for short packet communications made with SDR, analyzes different FEC candidates. Tzimpragos et al. [17] review different FEC schemes for 100-Gb/s optical networks. Also, an analysis of the published results is included. Shirvanimoghaddam et al. [18] review the state of the art of the FEC techniques for URLLC. Moreover, a comparison of reliability and decoding complexity analyzes different decoding algorithms. The results are obtained from MATLAB simulations. Qiao et al. [19] compare the performance of numerous FEC within a flexible ASIP decoder. Zhan et al. [20] analyzes FEC candidates for WirelessHP. This work also offers future directions for designing FEC schemes for industrial control applications. Hajiyat et al. [21] compare different candidates for 5G machine-type communications. Shao et al. [22] analyze the published results of the ASIC implementations of different 3GPP FEC techniques. Ahmed et al. [23] in their survey focused on addressing the design for future ARQ schemes, reviews suitable FEC techniques. In [24], Habib et al. study different decoding algorithms for LDPC un the context of Reinforce Learning. Lian et al. compare different decoding algorithms for TBCC and Polar in terms of reliability and complexity [25]. Ferraz et al. [26] analyze and compare numerous decoding algorithms for LDPC addressing issues associated with high-throughput and low energy consumption.

Table 2 outlines the existing survey articles and justifies how these publications differ from this survey article. Nowadays, no surveys in the literature simultaneously review numerous FEC techniques for short packet transmission and address the architectural and design problems of the FEC techniques for FA fields of Application.

### 2) CONTRIBUTIONS

The surveys available in the literature do not address the specific challenges of FA communications. An exception is given by [20], whose main contribution consists of surveying a set of candidate codes, and then, suggesting an *ad hoc* set of architectures. However, this work lacks the analysis of decoding algorithms. To the best of our knowledge, there is no comprehensive survey in the literature about FEC

**TABLE 2. Related Works**

Author	Year	Proposed scenario	FEC survey	Decoding survey	Hardware analysis	Reliability comparisons	Decoding latency comparisons	Future challenges for FEC	Future challenges for decoding	Ref
Sybis	2016	URLLC	Yes	Yes	No	Yes	No	No	No	[13]
Liva	2016	Theoretical	Yes	No	No	Yes	No	No	No	[14]
Iscan	2016	Theoretical	Yes	Yes	No	Yes	No	No	No	[15]
Wu	2016	High-Throughput Communications	Yes	Yes	Yes	Yes	No	No	No	[16]
Tzimpragos	2016	Optical Networks	Yes	No	No	Yes	No	Yes	No	[17]
Shirvani-moghaddam	2018	URLLC	Yes	Yes	No	No	No	Yes	Yes	[18]
Qiao	2018	High-Throughput Communications	Yes	Yes	Yes	Yes	No	No	No	[19]
Zhan	2018	High-Throughput Communications for FA	Yes	Yes	No	Yes	No	Yes	No	[20]
Hajyat	2019	Machine-type communications	Yes	Yes	No	Yes	No	No	No	[21]
Shao	2019	Broadband Communications	Yes	Yes	Yes	No	No	No	Yes	[22]
Ahmed	2021	URLLC	Yes	No	No	No	No	No	No	[23]
Habib	2021	Reinforce Learning	No	Yes	No	Yes	No	No	No	[24]
Lian	2021	Theoretical	No	Yes	No	Yes	No	No	No	[25]
Ferraz	2021	High-Throughput Communications	Yes	Yes	Yes	Yes	No	No	Yes	[26]
<b>This article</b>	<b>2022</b>	<b>FA</b>	<b>Yes</b>	<b>Yes</b>	<b>Yes</b>	<b>Yes</b>	<b>Yes</b>	<b>Yes</b>	<b>Yes</b>	

techniques for FA wireless systems that address at the same time reliability and latency aspect. Moreover, existing surveys neither consider theoretical nor hardware implementation results.

The main contributions of this article are summarized as follows.

- 1) A comprehensive taxonomy of several FEC techniques developed for short packet communications. These techniques are classified into block and memory codes, and their features are collected and compared in a table. The features are associated with the requirements of the FA use cases. The best-performing FEC techniques are considered as candidates.
- 2) For each candidate, several decoding architecture proposals are compiled and analyzed. The gathered results have been found from the information-theoretic and technique-oriented literature. Moreover, we compare those contributions by using reliability and latency metrics. Some examples are BLER and the number of required clock cycles.

- 3) As the results of the previous contributions, the authors provide some metrics for evaluating the FEC performance within FA wireless systems. Finally, the suggested metrics are used to benchmark the candidates.
- 4) Some lessons learned and future challenges are outlined.

#### D. ARTICLE OUTLINE

The rest of this article is organized as follows. Section II describes the research method adopted for the proposed literature review. Section III briefly describes FEC and defines the metrics analyzed in this survey. Section IV offers state-of-the-art of several FEC techniques suitable for short packet communications focusing on FA. Section V reviews the industrial wireless systems proposed, analyzing their FEC. This Section also includes the candidates detected by the authors in Section IV. Section VI collects the performance of several candidate hardware implementations and compares them. Section VII offers reliability and latency comparisons based

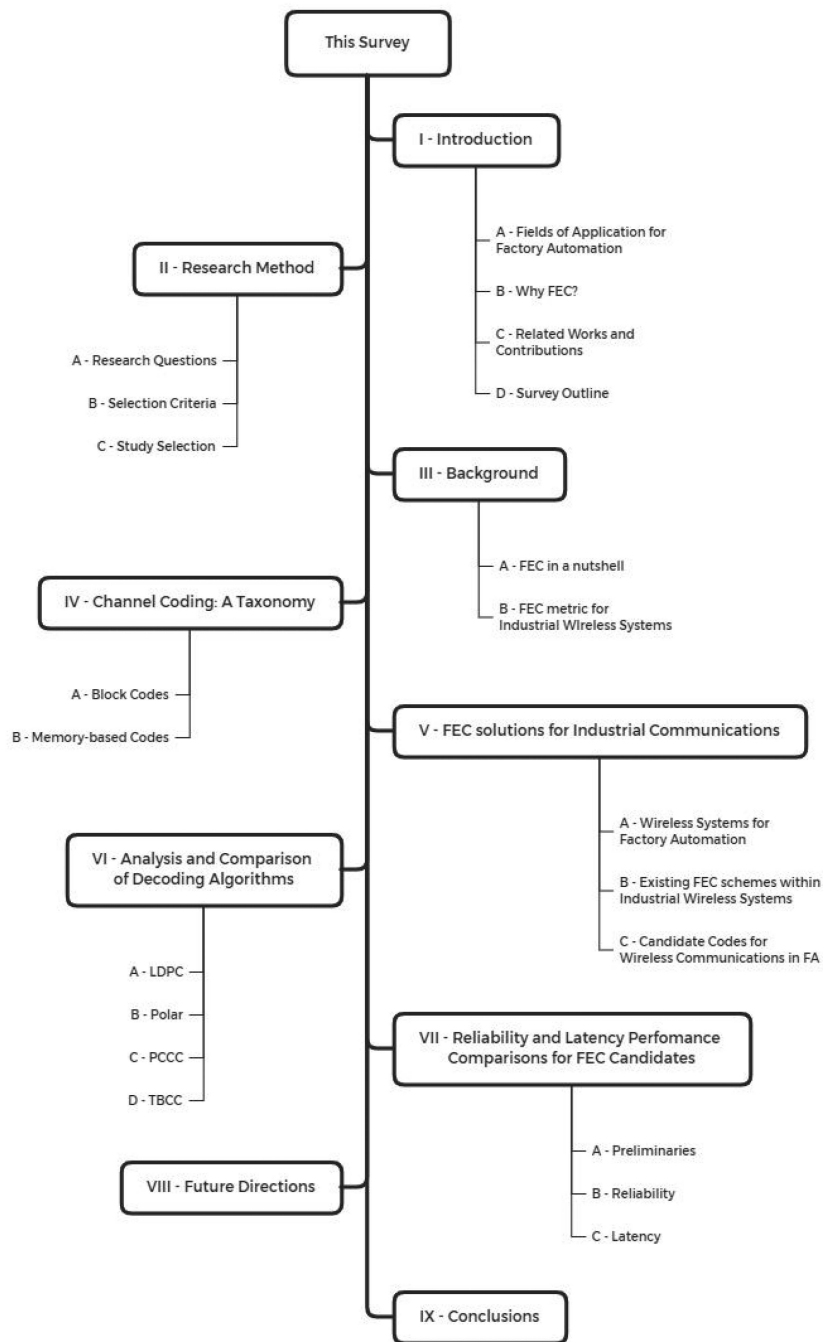


FIGURE 1. Survey structure.

on simulations and published results for the detected candidates. Section VIII contains the future challenges detected by this study. Finally, Section IX concludes this article. Fig. 1 offers an outline of the survey content.

**II. RESEARCH METHOD**

This study proposes a systematic literature review approach for reviewing the articles encountered in the considered databases. PRISMA is the guideline followed [28]. This

methodology comprises four main steps: issue detection and preliminary studies, collection of articles and reports, data extraction, and data inclusion. The first step aims to identify research questions, and therefore, the objectives. More in detail, this is the stage where the selection procedure of the article, keywords formulation for research and search queries, and the quality assessment criteria of extracted studies are defined. The subsequent step consists of using the keywords for the queries in the databases. The results are then collected



**TABLE 3. Research Question for This Survey**

#	Research Question
1	Which are the main goals in the design of wireless systems for FA?
2	Which are the traditional and modern FEC techniques for short packet communications proposed by the literature?
3	What are the application areas in wireless communications for short-packet communications?
4	What are the various metrics for evaluating the FEC for industrial communications, particularly for FA?
5	Which FEC techniques are commonly used in industrial communications?
6	Which decoding algorithms are to consider for fulfilling the FA requirements?

**TABLE 4. Selected Keywords for This Survey**

<b>Group 1:</b> FA-and URLLC related keywords	FA OR URLLC OR Reliability OR Latency OR Decoding Complexity OR Industry4.0 OR Industrial Communications
<b>Group 2:</b> FEC related keywords	Block Codes OR Convolutional Codes OR Non Linear Block Codes OR LDPC OR Polar OR Turbo OR Sparse Vector Codes OR TBCC OR QC LDPC
<b>Group 3:</b> Decoding algorithm related keywords	Belief Propagation OR Successive Cancellation List OR Viterbi OR Sphere OR OSD OR Full Parallelism OR Parallelism OR MINSUM OR FPGA OR ASIC
<b>Group 4:</b> Wireless Systems related keywords	IEEE 802.11 OR IEEE 802.15.4 OR 5G New Radio
<b>Search Query</b>	<b>(Group 1) AND (Group 2) AND (Group 3) OR (Group 1) AND (Group 2) OR (Group 1) AND (Group 4)</b>

in Zotero©, a software for managing bibliographic data and generally research materials encountered in databases or manually added.

### A. RESEARCH QUESTIONS

This study suggests FEC techniques for wireless systems for industrial environments like FA. Moreover, several guidelines are provided to the audience for designing *ad hoc* PHY layers for future industrial wireless systems proposals. For this aim, six research questions have been considered (see Table 3).

### B. SELECTION CRITERIA

After defining the objectives for this work, the databases are selected for the subsequent analysis. For this aim, the following databases have been considered IEEE Xplore, Google Scholar, and the 3gpp-database. This last collects many technical reports associated with FEC implementation for URLLC scenarios, which show similarities with FA.

Then, a list of keywords for the queries is generated as shown in Table 4. These are organized into four groups. The first contains the FA-related keywords, and the second includes FEC-related keywords. In contrast, the decoding algorithm-related keywords are grouped in the third group. Finally, Group 4 collects the keywords associated with industrial wireless systems.

Moreover, the articles selected are published in English and indicate a minimum of one citation. The result is a collection of documents published in English that covers more than 60 years of contributions associated with “FEC for short-packet communications.”

### C. STUDY SELECTION

Fig. 2 resumes the decision steps for including the articles in this work.

Initially, the research shows a total of 234 articles and technical reports to be analyzed. Among these, 18 were excluded as copies. Therefore, the amount passes to 216.

Then, the study passes to the screening phase, which consists of an initial examination of the title and abstract, followed by a full-text analysis. During the first step, the number of articles was reduced to 192, and subsequently, they passed to 184. The excluded manuscripts did not show any element for this scope. In this case, there are no explanations of the methodology proposed or the absence of comparable results. Consequently, this survey considers a total of 184 documents divided into academic articles and technical reports.

### III. BACKGROUND

This section presents a brief definition of FEC and the PHY-layer metrics proposed for analyzing the different FEC techniques presented in this work. According to the authors, this section aims to familiarize the general reader with the content proposed in this article.

#### A. FEC IN A NUTSHELL

In 1948, Shannon [29] proved that the error-free transmission of data is achievable in communication channels affected by noise. He demonstrated that the reliability is achievable in these scenarios by transmitting the data with a code rate  $R$  lower than the channel capacity, also known as Shannon limit.

The FEC techniques are one of the common approaches to this problem. It consists of applying some redundancy to the

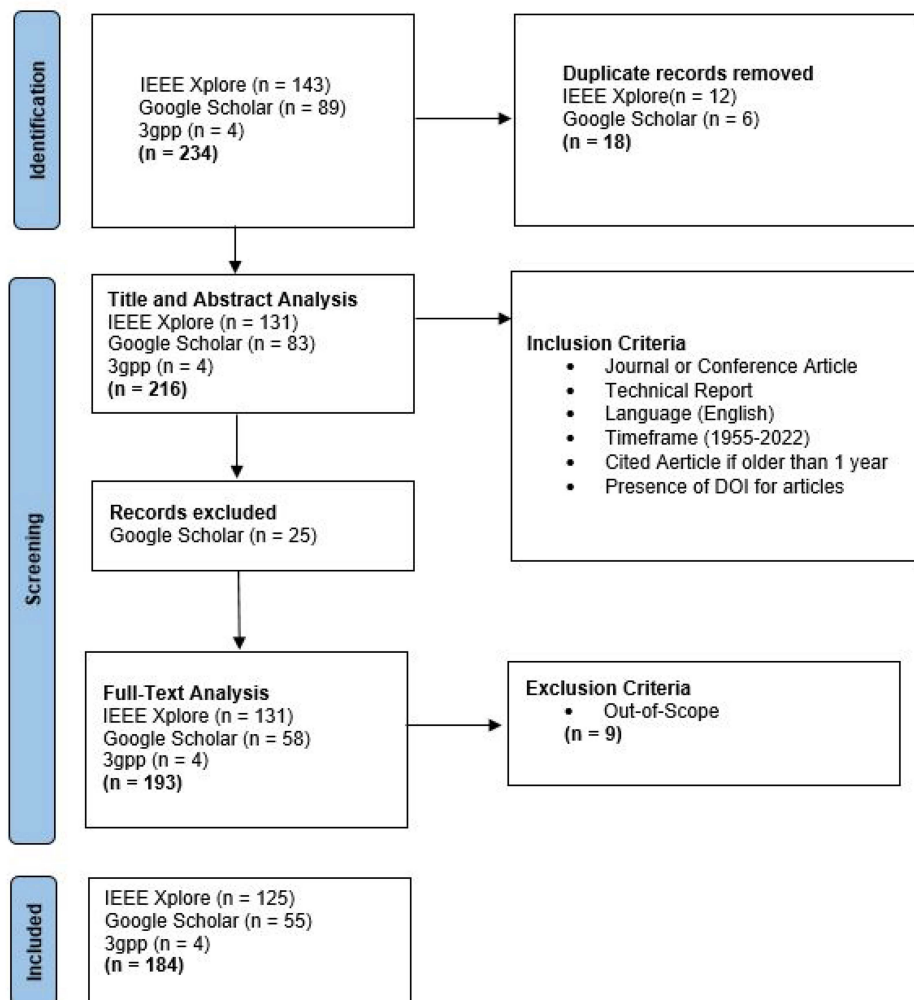


FIGURE 2. Selection criteria based on PRISMA.

data, which will be transmitted through the communication channel, with a determined code rate  $R$ .  $R$  is the ratio between the original data size of  $K$  bits and transmitted data of size  $N$ , where  $N > K$ . This redundancy helps the receiver detect and correct some corrupted bits within the transmitted data.

Ideally, the Shannon limit tends to infinity, and consequently, it is much easier to analyze the performance of FECs in the case of large packets [30]. Consequently, more assumptions are needed to evaluate FECs in short packet communications. In [31] a solid theoretical bound is proposed for the evaluation of FEC within short packet communications.

**B. FEC METRICS FOR INDUSTRIAL WIRELESS SYSTEMS**

**1) RELIABILITY**

Industrial wireless systems require high reliability during the transmission of short data. A transmission failure could affect critical aspects of the manufacturing processes associated with safety, equipment, and machinery integrity. The error rate is a metric strictly related to the probability of transmission failure. Its measurement in these particular environments is

defined at PHY or MAC layers and offers the rate of successfully delivered bits or packets.

The error rate metrics described in this section are used to evaluate the industrial wireless systems performance, where the desired performances are achievable using FEC and retransmission techniques. Some examples are bit error rate (BER), block error rate (BLER), packet error rate (PER), packet loss rate (PLR), and connection error rate (CER). The terms BLER, PER, and PLR are interchangeable in these scenarios. Commonly, BLER is associated with 5G NR, while PER for IEEE 802 standards for both PHY and MAC layer. PLR only refers to MAC-layer performances. CER evaluates the reliability performance in the presence of multiple connections among devices, and thus, is not included in this study.

Three main metrics have been detected and defined. BER is commonly used to evaluate the decoding performance at the PHY layer, indicating the probability of an erroneous bit transmission. BLER is defined exclusively at the PHY layer and represents the ratio between the erroneous packets received and the totality of transmitted packets. Finally, PLR considers

the erroneous transmission in the case of contiguous packets, evaluating the reliability at the MAC layer.

In [20], the authors compare the BER/BLER of different FEC candidates for high-throughput communications within factories, resulting from previous studies. While in [32], BER is used as a threshold for testing the WirelessHP PHY layer with different low-order modulations at different communications distances. A BLER threshold is defined in [33] to compare different FEC candidates' performance with the IEEE 802.11be PHY layer, assuming different industrial channel models. In [34], [35], and [36], BLER and PLR are an upper bound for testing the IEEE 802.11 PHY layer performance assuming deterministic protocols.

Generally, in industrial communications and FA, a system is considered reliable if it provides only one communication failure during thousand years [7]. This assumption is based on the recommendation IEC 61784, where the communication failure should compose at most 1% of the Mean time to failure, in this case of thousand years [37].

A communication failure is caused when the receiver lacks the correct packet reception, and this depends on one of the three following events.

- 1) The receiver does not receive the packet.
- 2) The received packet contains erroneous bits.
- 3) The packet is received outside the latency requirement.

Among the different metrics used for the reliability estimation, PER and BLER provide error rate values assuming the communication failure. Nevertheless, only BLER is focused on evaluating the performance at the PHY layer, and thus, is recommendable for evaluating the FEC techniques. For fair comparisons between different BLER results shown in different publications, additional elements such as SNR, channel typology, and channel properties must be included in the analysis.

## 2) LATENCY: DECODING LATENCY

In industrial communications, latency is generally expressed as cycle time [4], [7], [36]. This metric expresses the latency between the data transmission and its reception. Three main processes affect this metric. The first one is the transmitter latency, which expresses the time elapsed between the data available at the MAC layer and its subsequent transmission by the PHY layer. Coding and modulation processes are parts of this period. Second, propagation latency represents the associated delay of the channel. Finally, the receiver latency considers the required time for demodulation and decoding. Moreover, for the criticality of the processes involved within the industrial environment, cycle time is commonly bounded by a maximum value  $T_{\max}$ , which is half of the update rate period of the sensors and actuators included in the network [7].

An accurate estimation of the impact of the FEC on the latency performance of the wireless system is a complex measurement. Different and uncorrelated factors must be considered, such as the decoder architecture, the programming language, the interpretation of the algorithm's pseudocode,

and the hardware performance. In consequence, the comparison among different proposals is not straightforward.

FEC contributes notably to the receiver decoding latency [22]. In many works, it is described as the ratio between the clock cycles required by the decoding latency and the clock frequency of the hardware used for the implementation [33], [38], [39]

$$\text{Decoding Latency} = \frac{\text{Required Clock Cycles}}{\text{Decoder Clock Frequency}}. \quad (1)$$

## IV. CHANNEL CODING: A TAXONOMY

The literature includes many examples of FEC techniques suitable for short packet communication scenarios, and such choices have risen over the years. FEC can be addressed as memory-based and memoryless FEC (or Block Codes). This section aims to provide a state-of-the-art of them, moreover suggesting some FEC candidates for FA wireless systems.

### A. BLOCK CODES

Block codes are a class of FEC in which the data stream turns into a block of  $K$  bits; subsequently, by using a generating matrix, further  $N - K$  bits, known as redundancy bits, have been included. The code rate  $R = \frac{K}{N}$  specifies the number of these bits.

A primary classification proposed for these techniques consists of distinguishing between linear and nonlinear techniques. Linear block codes are less complex than nonlinear ones and offer commonly good decoding performances. The nonlinear block codes are characterized by a very high complexity that does not allow their consideration in low latency communications nowadays [40]. On the contrary, the respective counterpart shows many applicative examples in numerous standards.

The linear block codes can be classified as a function of the generating matrixes and attainable performance. On this basis, the linear block codes are grouped as follows: LDPC, algebraic, fountain, and compressive sensing based. Table 5 compares the block code techniques using reliability in short packet regime and parallel decoding capability. Parallel decoding is a crucial parameter for achieving the stringent latency requirements for FA.

LDPC codes were discovered by Gallager in the 60s [41], and rediscovered in the late 90s by Mackay and Davey [42]. The remarkable decoding performance of this family have fostered their use in many standards since the first decade of XXI century. Some examples are IEEE 802.11 [43], WiMax [44], 5G NR [45], ATSC3.0 [46], 10GBase-T [47], WiGig [48], DVB-T2 [49], [50], DVB-S2 [51], and Consultative Committee for Space Data Systems (CCSDS) [52]. Generally the LDPC are classifiable into three main subfamilies: Random LDPC [41], Quasi-Cyclic (QC) LDPC [53], and Cyclic LDPC [54], among these QC-LDPC are suitable for communications in FA scenarios; indeed, the possibility of a full parallelization secures low latencies. Nevertheless, QC-LDPC shows error floors in BLER-based



**TABLE 5. Block Codes and FEC Comparison**

Typology	Family	Subfamily	Parallel decoding	High reliability in short packet transmission	Ref
Linear	LDPC	Cyclic		X	[54]
Linear	LDPC	Quasi-Cyclic	X	X	[53]
Linear	LDPC	Random		X	[41]
Linear	Algebraic	Hamming	X		[63]
Linear	Algebraic	Golay	X		[64]
Linear	Algebraic	Reed Muller	X		[68]
Linear	Algebraic	BCH	X		[65]–[67], [69], [70]
Linear	Algebraic	5G-NR	X	X	[71]
Linear	Fountain	LT	X		[80]
Linear	Fountain	Raptor	X		[81]
Linear	Fountain	Tornado	X		[82], [83]
Linear	Compressive Sensing Based	SVC		X	[88]–[92]
Non Linear		Preparata		X	[94]
Non Linear		Kerdock		X	[95]
Non Linear		Delsarte-Goethais		X	[96]

analysis [20] in short packet transmissions. This problem can be partially solved by the combination with CRC [55], [56].

Algebraic codes include a wide set of FEC techniques that, due to their mathematical properties, exhibit two main advantages: easy implementation and generally high decoding performance [20]. WPAN [57], DVB-T [58], DVB-T2 [50], IEEE 802.11ad [59], CCSDS [60], [61], MediaFLO [62], and 5G NR [45] are examples of standards that employ this FEC family. Among the several FEC grouped as algebraic, the authors of this article have identified four main subfamilies: the Hamming codes [63], Golay codes [64], the BCH codes [65], [66], [67], and the Reed–Muller codes [68]. Among the most well-known Algebraic techniques, there are Reed–Solomon (RS) [69], and Gabidulin [70] that belong to BCH, whereas the Reed–Muller subfamily includes the recently developed Polar codes [71]. Regarding the algebraic codes in the short packet regime, on the one hand, their decoding performance worsens [20]. On the other hand, the use of parallel decoding is possible [20]. However, a few exceptions, suitable for short packet transmissions, have been introduced recently in the literature, as the cases of Polar codes [72], [73], [74], and BCH

codes with OSD decoding [75]. A negative aspect concerned OSD decoding is the increased decoding latency [75].

Fountain codes were introduced in the late 90s by Bayers et al. [76] to propose an efficient solution in multicast communications, in particular, to enhance the efficiency of ARQ [77]. Indeed standards employed in multicast and broadcast communications, such as 3GPP MBMS [78], and ATSC3.0 [79] use these FECs. The large number of Fountain techniques developed over the years can be categorized into three main subfamilies: the LT codes [80], the Raptor codes [81], and the Tornado codes [82], [83]. Fountain codes present a high complexity [84] which prevents their use in URLLC and especially for FA [20]. However, recent versions of Fountain have been proposed for URLLC scenarios, such as in [85] and [86], where the transmission scheme is significantly simplified. The proposed scheme in [86] does not offer error floors for BLER values below  $10^{-7}$ .

Sparse vector codes (SVC) are a novelty within the world of FEC techniques. Based on compressive sensing [87], their studies started around 2017. The first results are promising for ultrasmall values of  $K$ . In particular, for  $K$  below 100 bits, they show comparable performance with Polar codes [88], [89],

**TABLE 6. Memory Codes and FEC Comparison**

Family	Subfamily	Parallel decoding	High reliability in short packet transmission	Ref
Turbo	SCCC		X	[103], [104]
Turbo	PCCC	X	X	[103], [104]
Turbo	TPC		X	[105]
Convolutional	No Tailbiting	X		[97]
Convolutional	ZTBCC	X		[101]
Convolutional	TBCC	X	X	[102]

[90]. However, the properties related to their generation matrix show worsened decoding performance at high Code Rates ( $R \leq \frac{1}{4}$ ). Furthermore, the required representation of data into sparse vector form limited the use of SVC exclusively to ultrasmall  $K$  values [88]. Recently, the literature proposed some implementations related to these new techniques: [91] where also is estimated computational complexity, and [92] where are given reliability and decoding latency performance.

Finally, the non-linear block codes provide excellent decoding performance in decoding, but at the cost of a complex hardware implementation [93]. Among the best-known non-linear codes, there are the Preparata codes [94], the Kerdock codes [95], and the Delsarte–Goethals codes [96].

Nevertheless, the recent binarization for Preparata and the Kerdock codes proposed in [40] opens new frontiers for their application within low latency communications.

## B. MEMORY-BASED FEC CODES

Since the 1960s, memory-based codes have been applied in numerous systems. The behavior of these techniques is comparable to a state machine, where the data stream passes through different states. Each state is associated with the value of a memory register of the FEC module. A generator polynomial defines the connection between the registers and the relative operations. The encoding process finishes when the last bit of the data stream passes through. It is possible to distinguish two families among the different techniques: convolutional codes (CC) and turbo codes. Table 6 shows a comparison between these techniques by taking into account the reliability performance in short packet regime and the possibility of parallel decoding.

CC codes were introduced by Elias [97] in 1955. CC consists of the convolution operation between bitstreams containing the data and a bit sequence, resulting from the passage of such data in dedicated shift registers. These later constitute a finite-state machine. Unlike block codes, CC allows faster decoding since the encoding/decoding is enabled after the detection of a bitstream, whereas, in block codes, encoding/decoding requires the entire block bit sequence. Nevertheless, block codes give better decoding performance. Principally for its simplicity, CC has achieved wide success from the sixties; indeed, several standards, such as

IEEE 802.11 [43], DVB-T [58], UMTS [98], LTE [99], CCSDS [61], and the Mars Reconnaissance Orbiter NASA Mission [100] utilize CC techniques. There are two main subfamilies of CC: without padding and with padding. CC without padding requires simpler architectures than the counterpart, and as a consequence, this technique is faster. However, the absence of a padding sequence impacts the decoding performance. Indeed, these techniques provide poor decoding performance during the passage of the first bits of the stream caused by the absence of correlation between the initial and the final state. CC with padding improves the decoding performance by including a known sequence for these states, and consequently, a correlation is provided since the first transmissions. CC with padding can be grouped into zero tailbiting convolutional codes (ZTBCC) and tailbiting convolutional codes (TBCC) [101]. ZTBCC has padding composed of zero bits, which on the one hand, improves the performance. However, this option affects the effective code rate [102]. In TBCC, the initial and final states of the encoder are identical. However, this strategy increases the decoding performance in short packet regimes at the expense of complexity.

Berrou et al. [103] proposed Turbo codes in 1993, one of the best performing codes up to date. They have been incorporated into many standards since 1990s. Examples are LTE [99], WiMAX [44], MediaFLO [62], and the Mars Reconnaissance Orbiter NASA Mission [100]. Generally, the Turbo codes can be grouped into parallel concatenated convolutional codes (PCCC), serial concatenated convolutional codes (SCCC) [103], [104], and turbo product codes (TPC) [105]. PCCC and SCCC present similar performance in terms of complexity and reliability. Comparisons between these two architectures are encountered in both [106] and [107]. The authors in [106] shows the better decoding performance of SCCC for BLER below  $10^{-6}$ . In more detail, SCCC achieves the mentioned performance at 7 dB, assuming the AWGN channel model. On the contrary, [107] suggests the use of PCCC over SCCC analyzing the results of complexity and reliability, assuming a BLER of  $10^{-2}$ , also in this study, under the AWGN channel. Analyzing the Turbo subfamilies, TPC is considered as the most promising from a theoretical analysis standpoint [20]. However, nowadays, no hardware

**TABLE 7. Wireless Systems for FA**

Year	System	PHY techniques	MAC techniques	FEC	System performance		Ref.
					E2E	PER	
					Latency [ms]		
2004	IEEE 802.15.4a	UWB+FEC, PSSS+FEC, DSSS+FEC	Deterministic	CC, RS+CC	< 3	$10^{-7}$	[119]
2015	WIA-FA	DSSS+FEC, PHSS+FEC, OFDM+FEC	TDMA	CC, LDPC	8		[4], [20]
2017	5G New Radio	OFDM+FEC	TDMA, OFDMA	LDPC, POLAR	2	$10^{-5}$	[45], [124], [127], [128]
2017	WirelessHP	OFDM+FEC	TDMA	RS+CC, RS, CC	0.44	$10^{-6}$	[4], [32], [125]
2018	SHARP	OFDM+FEC, OFDMA+FEC	TDMA, OFDMA	CC	< 30	$10^{-7}$	[10], [36], [118]
2019	IEEE 802.11ax	OFDM+FEC, OFDMA+FEC	OFDMA	CC, LDPC	10-100	$10^{-5}$	[112]
2020	IEEE 802.15.4z	UWB+FEC	Deterministic	CC	< 3	$< 10^{-7}$	[123]
TBA	IEEE 802.11be	OFDMA+FEC	OFDMA	LDPC	< 1	$< 10^{-5}$	[111]

implementations are found in the literature, despite the presence of parallel decoding scheme proposals [108]. Among the three subfamilies, only PCCC has several hardware implementations with parallel decoding architectures, such as [109] and [110].

## V. FEC SOLUTIONS FOR INDUSTRIAL WIRELESS SYSTEMS

### A. WIRELESS SYSTEMS FOR FA

The literature on wireless communication schemes in FA covers systems based on IEEE 802.11, IEEE 802.15.4, 5G NR, or stand-alone proprietary proposals. Nevertheless, these proposals partially meet the FA requirements as gathered in Table 7.

#### 1) IEEE 802 FAMILIES

IEEE 802.11 is a family of standards for WLAN communications initially designed to operate in the 5-GHz Industrial Scientific and Medical (ISM) band, specifically with the IEEE 802.11a release. The 2.4-GHz band was included in the IEEE 802.11b/g. The introduction of IEEE 802.11n incorporates the opportunity of switching between these two options. Finally, the recent release of IEEE 802.11ax, facilitates the operation in the 6-GHz band also [111]. One of the main characteristics of the IEEE 802.11 standard family is the lack of determinism in packet arrival times. This aspect prevents their use for real-time communications, and consequently, does not guarantee a controlled latency required in FA use cases. Another negative aspect regards reliability performance. Existing systems are distant from securing PER values below  $10^{-7}$ .

Regarding the PHY layer design, almost all standard releases use orthogonal frequency-division multiplexing

(OFDM) and FEC techniques. OFDM is related to the waveform structure, and it changes with the typology of application. For example, IEEE 802.11 g proposes OFDM spectra in 20-MHz channels composed of 64 subcarriers (52 data carriers). In turn, IEEE 802.11ax has 256 subcarriers available within the same channel width (234 data carriers).

The first IEEE 802.11 standards had FEC modules based on CCs, while more sophisticated algorithms such as LDPC were introduced as an option in the IEEE 802.11n [112]. LDPC has become mandatory for the first time in the standard IEEE 802.11ax. IEEE 802.11ax introduced additional novelties, such as multiuser communications based on OFDMA and a new PPDU design. The new PPDU design introduced in IEEE 802.11ax is nowadays a candidate for the standardization of the upcoming IEEE 802.11be [113]. This standard, also known as extremely high throughput, apart from focusing on high data rate profiles, also targets ultralow latency communications and is, therefore, a good candidate for industrial environments [113].

The worldwide success of the IEEE 802.11 standards has supported various modifications and deterministic MAC approaches over the last decade. These proposals attempt to provide time-aware scheduling by the use of time-division multiple access (TDMA) techniques at the MAC layer, such as RT-WiFi [114], IsoMAC [115], Priority MAC [116], or the recent HAR2D-Fi [117]. Another proposal for FA is SHARP, which attempts to optimize also the PHY of the IEEE 802.11 releases. It proposes the optimization of the PHY of IEEE 802.11 g, while at the MAC layer, it proposes a TDMA frame [36], [118]. Recent updates of SHARP are proposed in [10], where OFDMA is introduced to improve the latency performance further.

Another IEEE 802 family considered for industrial environments is the IEEE 802.15.4 standard, which focuses on high-density networks and very short-distance communication ranges. IEEE 802.15.4 was initially sketched for operating in the 2.4 GHz, and 868/916 MHz ISM [119] bands. On the contrary to IEEE 802.11 standards, the IEEE 802.15.4 support deterministic communications. The PHY of 802.15.4 includes direct spread spectrum (DSSS), and ultrawideband (UWB) techniques [120], [121]. UWB combines two modulations known as burst position modulation (BPM) and binary phase-shift keying (BPSK). Concerning FEC, IEEE 802.15.4a introduced both CC and RS+CC [122], whereas, in the newest standard IEEE 802.15.4z, only CC [123] has been adopted. Several FA and PA communication systems such as ZigBee, WirelessHART, ISA100.11a, and WIA-FA rely on IEEE 802.15.4 PHY.

## 2) 5G NEW RADIO (5G NR)

5G NR is the RAN standard for the 5G mobile network (including the PHY layer), developed by 3GPP for the 5G mobile network, and it was introduced in 2017 in Rel-15 [45]. 5G NR is the first 3GPP standard targeted for several communication scenarios. Indeed, the previous 3GPP standards only have been developed for broadband communications. One of the covered verticals, the URLLC, was designed to cover verticals requiring real-time applications. Among these, FA is considered one of the most demanding scenarios [124]. 5G NR for covering such verticals includes two operative frequency ranges for short and large-distance communications. The first one, known as FR1, includes 410 MHz–7.125 GHz, while the second, the FR2, incorporates the frequencies from 24.250 to 52.600 GHz.

The 5G NR PHY layer design partially meets the FA requirements for many applications. Some current limitations are the subframe length, which duration currently spans to 1 ms. However, this new standard improves previous releases' robustness with a combination of OFDMA/TDMA MAC techniques and FEC techniques, i.e., LDPC and POLAR. Regarding latency improvement, some new approaches have been recently proposed. For example, in [26], simulations have demonstrated that FDMA provides latency of 1 ms, while in [27], 2–3 ms is achieved.

## 3) WIRELESSHP

WirelessHP is a standalone standard proposal for FA applications based on IEEE 802.11 PHY [32], [125]. Initially, the system only operated in the 5-GHz frequency range [32], while for future work, millimeter wave is also being considered, in particular, the 60-GHz license-free band [4]. Regarding the system design, MAC techniques allow for WirelessHP time-aware scheduling, and hence, the achievement of very low latencies, around 0.5 ms. Nevertheless, considering the reliability, such performance has currently been reached up to PER of  $10^{-7}$  [126]. The adopted FEC are RS, CC, and RS+CC.

## B. EXISTING FEC SCHEMES WITHIN INDUSTRIAL WIRELESS SYSTEMS

In industrial wireless communications, the use of *ad hoc* FEC is necessary for providing highly reliable communications with reduced latencies. Currently, the most popular schemes applied in these environments are based on RS, CC, LDPC, and Polar. Information about their structure and related published research is provided here.

### 1) WIRELESSHP RS+CC

Several FEC candidates have been considered for the WirelessHP [20]. Among the alternatives, the RS+CC based on [129] and [130] has been adopted for the first laboratory trials focused on the PHY layer [11]. RS is the outer code, while CC is the inner code. There are two main reasons. First, the RS achieves high decoding performance. Second, the concatenation between RS and CC allows high throughput transmission at reduced decoding latencies, considering the Viterbi decoding algorithm.

The FEC has been evaluated considering different configurations. For RS has been proposed two different code lengths, which are 15 and 31 B. The first has been applied for coding data sizes between 9 and 13 B, whereas the other has a range between 19 and 29 B. Three different code rates have been used for the outer code (CC) and are the following: 5/6, 3/4, 2/3.

In [11], these configurations have been adopted for the data transmission between two nodes implemented with two Universal Software Radio Peripherals (USRPs), considering a bandwidth of 5 MHz. The better performances have been obtained considering CC (2/3), where low values of PER (below  $10^{-7}$ ) were obtained assuming periods for the packet transmissions less than 100  $\mu$ s.

### 2) IEEE 802.11 CC

The IEEE 802.11 CC is ZTBCC and is based on [131]. A tail bit sequence of 6 bits set at zero is included in the data block before the encoder and is used to improve the decoding performance. The convolutional encoder is designed for offering a default code rate of 1/2. For offering multiple code rate choices, puncturing is applied after the encoding. Two different puncturing modes are included. The first allows  $1/2 < R < 5/6$ , while the other is used for  $R = 5/6$ . The use of the Viterbi decoding algorithm allows extremely reduced decoding latencies.

The authors in [36] show the results of SHARP obtained by OMNET++ simulations. These results show that, without the use of retransmissions, IEEE 802.11 CC helps in obtaining PER values less than  $10^{-6}$  for latencies close to 500  $\mu$ s.

### 3) 5G NR CA-POLAR

5G NR CA-Polar are used within the 5G NR control channel due to the high decoding performance for short packets. Such performances are improved for coupling the CRC sequence with the information block at the PHY layer. This approach is



twofold. First, they are used for improving the error detection performance. Second, their combination with the SCL decoding algorithm also allows error correction [132].

Multiple data size and code rates are available with 5G NR Polar. Data range from 30 to a maximum of 1024 bits. At the same time, the code rate could vary from 1/5 to 5/6 due to the use of the following rate matching operations: puncturing, shortening, or repetition.

In [33], it is shown that CA-Polar outperforms the IEEE 802.11 CC for data with reduced sizes (in the order of 100 b). Moreover, many SCL decoding proposals based on semiparallelism offer reduced decoding latencies [22].

#### 4) 5G NR LDPC

5G NR QC LDPC codes are used for the data transmission and are designed to be applied for many scenarios. Among these, also FA is included. Many advantages are associated with this technique. First, the error floors are detectable for PER values below  $10^{-5}$  for a large set of code rates. Second, reduced decoding latencies due to the high degree of parallelism. The reliability performance is improved for using CRC as outer code, while the block segmentation before the encoding allows significantly reduced latency performances [132].

5G NR QC LDPC offers many data sizes, which vary from less than 100 to 8448 bit. Two base matrices (BMs) are proposed. BM1 is usually applied with large data, while on the contrary is used BM2. Puncturing and shortening are applied to achieve code rate flexibility, varying from 19/20 to 1/5.

In [38], it is shown that due to the parallel decoding, 5G NR QC LDPC could achieve decoding latencies below  $1 \mu\text{s}$  for achieving PER values below than  $10^{-5}$ .

### C. CANDIDATE CODES FOR WIRELESS COMMUNICATIONS IN FA

This section proposes FEC candidates for FA scenarios. The choice is based on the techniques proposed in Tables 5 and 6. Among all the analyzed techniques, the choice falls on QC-LDPC, Polar, PCCC, and TBCC, due to their high reliability in short packet regime and the opportunity to implement parallel decoding.

#### 1) QC-LDPC

QC-LDPC is a subfamily of LDPC. The linear relationships between the information block with  $K$  bits and the one encoded with  $N$  bits are defined using a parity check matrix ( $H$ ).  $H$  has dimension  $N \times N - K$ , and it is composed only by elements with one or zero as values. Its principal property is sparsity, which means that most of the matrix element values corresponding to zero, allowing, as a consequence, its representation using the Tanner graph. This graph comprises  $N$  nodes, the variable nodes, and further  $N - K$  nodes, the check nodes. Comparing QC-LDPC with the other subfamilies, its  $H$  presents the quasi-cyclic property, enabling full parallel decoding. Indeed, such property derives from the high sparsity

of the matrix, allowing to divide  $H$  into several submatrices. The literature offers two methods for generating  $H$  in the case of QC-LDPC. By probabilistic approach such as the Photograph method [53], or based on the power edge growth (PEG) method [133], which is an iterative algorithm used for the graph generation.

The Photograph method consists of repetition techniques applied to a base matrix [134]. The main benefits are high reliability for variable lengths of both  $K$  and code rate, as demonstrated by the version implemented in 5G NR [135]. The only disadvantage related to the short packet transmissions is the presence of error floors at higher SNR levels. Nevertheless, this problem can be solved by concatenation with CRC [55], [56]. Among the obtained FEC by the Photograph method, there are the *accumulate-repeat-3-accumulate* (AR3A) and *accumulate-repeat-by4-jagged-accumulate* (AR4JA) proposed by the Jet Propulsion Laboratory [136], [137].

The second proposal, the PEG method, is an iterative form for generating  $H$ , which aims to establish connections between the Tanner Graph nodes. These iterations produce girth maximization, which allows high-decoding performance in short packet communications. The term girth defines the largest cycle in the Tanner Graph. For more details about the algorithm, see [77]. However, their performance tends to deteriorate as the size of the information increases. The QC-PEG-LDPC have been considered as potential candidates in 5G NR for URLLC [13] assuming  $K$  of 40 and 200 bits. The results recognize benefits by using this method in the 40-bit case. In [135], the authors recommend the use of the PEG within the QC-LDPC structure adopted in 5G NR for ensuring a better performance in the short packet regime. Table 8 summarizes the main features of the proposed methodologies. Among them, this article recommended the use of the photograph within FA wireless systems. Indeed, high-reliability performance occurs for a wider variety of data sizes, and code rates respect the PEG method.

#### 2) POLAR

Polar codes were designed in the late 2000s by Arikan [138], providing for the first time a FEC technique able to achieve the channel capacity. The main feature of Polar is the use of binary-input discrete memoryless channels (B-DMC)  $W$ , where a method known as channel polarization is applied. Channel polarization splits  $W$  into a perfect channel and a noisy channel, allowing the transmission of the  $K$  information through the perfect channels. At the same time, the redundant  $N - K$  bits pass along the noisy channels. The noisy channel bits are known as Frozen bits. Such sequence is also known to the receiver. Then, a generator matrix  $G$  encodes the generated data vector.

Early Polar results did not provide the expected performance [143], in particular in the short packet regime [72]. This problem was solved by the use of concatenation techniques. There are currently two proposals, one consists of



**TABLE 8. Encoding Methodologies**

Candidate	Method	General advantages	General disadvantages	Ref.
QC-LDPC	PEG	High reliability for reduced payload size	Reduced reliability from payload sizes > 200 b	[133]
QC-LDPC	Photograph	High reliability for every payload size	CRC concatenation is required in Short Packet Regime	[53]
Polar	Arikan's Polar	High Decoding Performance for large packets	Poor decoding performance for short packet transmissions	[138]
Polar	CA-POLAR	High decoding Performance for short packet transmissions	More latency than Arikan's Polar	[72]–[74]
Polar	PAC POLAR	High decoding Performance for short packet transmissions	Actually no hardware implementations are published	[139]
PCCC	Narayan's Model	Reduced Complexity	Poor decoding performance, High latency	[140]
PCCC	Souza's Model	Reduced Complexity	Poor decoding performance	[141]
PCCC	LTE Encoder	High decoding performance	High complexity	[142]
CC	TBCC	High Decoding Performance	High Complexity	[102]
CC	ZTBCC	High decoding performance, Reduced Complexity	Reduced Code Rate	[102]

concatenation with CRC, known as CRC-aided Polar (CA-POLAR) [72], [73], [74], while the other proposes CC and is known as PAC [139]. Recently, in [144] and [145], an optimal Polar code design for industrial environments is presented.

The high performance achievable by CA-POLAR codes allows its consideration within the design of wireless systems for FA communications. As observable in Table 8, such techniques offer, on the one hand, high reliability in short packet regime, and there are hardware implementations with encouraging results.

### 3) PCCC

PCCC codes are a subfamily of Turbo codes [103]. The encoder is designed to connect two convolutional encoders, which produces the parity bits. In addition, a puncturing block ensures the encoding for several code rates. The PCCC encoder includes one or more interleaving blocks to improve the decoding performance. In a survey on Turbo Coding for HARQ, Chen et al. [146] identifies three main Turbo Encoders: Narayanan model [140], Souza model [141], and LTE Turbo encoder [142], which differ in the number and placement of interleaves.

The Narayan model foresees the use of two interleavers: one placed before the encoders and the other before the second encoder. The Souza model involves using a single interleaved set before the second encoder. However, these models do not show successful decoding during the first frames transmission [146]. In the LTE Turbo model, four interleavers solve this issue, the first one placed between the two parallel encoders and the others in correspondence with the systematic bit sequence and the obtained parity bits. Moreover, LTE Turbo presents a circular buffer that solves the decoding problems encountered in the other models.

Table 8 summarizes the main features of the encoder models for PCCC. Among the proposals, LTE turbo shows better

decoding performances compared with its counterparts, and for this reason, the authors propose this model as a candidate.

### 4) PADDED CC

CC with padding reduces the typical high decoding probability that occurs during the first data stream transmitted [102]. Two main padding strategies permit the distinction of this subfamily into TBCC and ZTBCC. TBCC requires that encoder and decoder structures have the same initial and final states. Consequently, the padding sequence is included in the encoded block, showing benefits in the decoding performance, particularly for short packet transmissions, moreover avoiding the code rate loss, defined as follows:

$$R = \frac{K}{N + \text{padding bit}} \quad (2)$$

In ZTBCC, the padding is an additional element of the encoded stream. The decoded block is composed of stream and padding bits in this case. This structure affects the code rate described as follows:

$$R = \frac{K}{N} \quad (3)$$

Table 8 summarizes the main features of the models of CC with padding. Among these models, the authors recommend using the TBCC codes for their high decoding performance in the short packet regime and the absence of code rate loss.

## VI. ANALYSIS AND COMPARISON OF DECODING ALGORITHMS

As highlighted in previous sections, the integration of FEC techniques can be a crucial element for guaranteeing the performance of wireless systems in FA use cases. One reason is associated with the properties of the propagation channels in industrial environments. The high time coherence of industrial

propagation channels makes the use of some MAC layer techniques useless, such as time retransmission techniques [34]. The usage of robust FEC techniques could improve the MAC-layer performance [144], [145]. The FECs are techniques that detect and correct the erroneous bit included in the received data. Many propagation effects correlated to the channel models cause these errors during the data transmission, such as noise, interference, and fading. Among these, fading is particularly critical within industrial environments. More specifically, the encoder located in the transmitter converts a block of  $K$  information bits into a longer block of  $N$  bits, which contains  $N-K$  redundant bits. Such redundancy helps the decoding architecture, located in the receiver, detect and correct the erroneous bits. After these corrections, the original  $K$  information is ultimately reconstructed. The literature offers numerous decoding architecture proposals to obtain specific reliability, latency, or energy consumption goals. For example, faster decoding is typically allowed by a low complex structure despite the expense of reliability. Commonly, many industrial scenarios, such as process automation, adopt low-complex decoding architectures. In these cases, high density node networks are required to control and monitor the processes, where the nodes must communicate fast and at the same time, maintain a reduced energy consumption. On the contrary, the FA processes demand complex decoding architectures to meet the strict requirements of the use cases. High reliability and low latencies are achievable with decoding architectures that include a high level of parallelism and sophisticated decoding algorithms [20]. To further improve the reliability, typically, the demodulated  $N$  bits are estimated by using the logarithmic likelihood ratio (LLR) method [147].

Tables 9 and 10 show a comparison of the decoding algorithms developed for short packet transmissions over the years. The comparison considers both the algorithmic complexity and the reliability. In contrast, the latency is not included in the analysis because the hardware performance advances in recent years, not allowing a fair comparison.

In this work, the definition of Algorithmic complexity refers to the number of required clock cycles during the decoding. The presence of parallel decoding reduces the number of cycles needed. In the analyzed literature, parallel decoding can be semiparallel or fully parallel. Among the reviewed works, in [148], the case of full parallel decoding is defined as available. Moreover, if the algorithms are iterative, another parameter is the number of iterations.

The clock cycle complexity allows the estimation of decoding latency in short packet transmissions, and thus, in FA, as highlighted in [14], [22], and [149]. In this survey, the complexity is related to the parameters  $N$ ,  $P$ ,  $L$ ,  $R$ ,  $K$ , and finally,  $m$ .  $N$  defines the block length and  $R$  is the code rate, whereas  $K = NR$ .  $P$  defines the number of updated nodes in the decoder. Considering full parallel decoding,  $N = P$ . The parameters  $L$  and  $m$  define the number of lists used in the SCL algorithm and the memory length in WAVA. Finally, the reliability analysis consists of both BLER and BER. BLER values differ from BER ones for the presence of the symbol\*. The

presence of blanks defines the absence of information in the literature regarding the specific parameters. Most decoding algorithms are evaluated with the AWGN channel, whereas in [150], is included a Rayleigh channel.

### A. LOW DENSITY PARITY CHECK (LDPC)

In LDPC codes, the literature suggests using iterative decoding algorithms. Such algorithms allow the message passing between variable nodes and check nodes. The message passing can also be defined as message exchange. Min-Sum and belief propagation (BP) are the algorithms adopted in QC-LDPC. Both algorithms have a complexity tending to  $\frac{N}{P}$  per iteration due to the full parallel decoding. Broulim et al. [151] and Balatsouka-Stimming and Dollas [152] offer an implementation of MIN-SUM with full parallel decoding. In the case of BP, full parallel decoding is proposed in [153], [154], and [155]. Other MIN-SUM implementations in which semiparallel decoding is proposed are [156], [157], and [158], while for the BP case, there is the proposal of [159]. In terms of reliability, BER of  $10^{-6}$  at SNR values close to 4 dB are achieved in [152] and [158] via FPGA implementation. Nevertheless, [153] offers a BER of  $10^{-9}$  at equal SNR. BP-based algorithms offer higher reliability than MIN-SUM-based algorithms due to the higher number of required operations [160]. However, the number of operations does not affect the number of clocks required per iteration, as shown in Table 9. In conclusion, BP, and in particular, the model [153] are optimal, from the complexity point of view, offers full parallel decoding. In contrast, in terms of reliability, [153] is the best performing model among the proposals analyzed.

### B. POLAR

Polar implementations for short packet communications scenarios use algorithms based on the concept of erasure, i.e., the message decoding consists of erasing the interference affecting the received  $K$  LLRs and the iterative reconstruction of the message. Cancellation-based algorithms include successive cancellation (SC), successive cancellation list (SCL), and successive cancellation flip (SCP), while the iterative algorithms proposed by the lettering are BP, OSD, and Sphere. The proposals with SC show semiparallel decoding, moreover, the clock complexity varies from a value tending to  $2\log_2(N/P)$ , as in the case of Kam [161] and Ercan's 2017 [162] models, up to a maximum tending to  $N/P$ , as in the case of Leroux's model [163], Yuan's 2014 [164], and Giard's [165]. Regarding reliability, the 2017 Ercan model is the best result up to date, offering a BLER of  $10^{-5}$  at SNR of 4 dB (FPGA implementation). Even in the case of SCL have been proposed semiparallel decoding architectures. These models show complexities ranging from  $N/2 + (N/P)\log_2(N/4P)$  clock cycles, as in the case of Yuan's 2015 model [166], up to a complexity tending to  $2N + (N/P)\log_2 N$ . In this last case, the models of Balatsoukas-Stimming [167], Xiong [168], Lin [169], and Fan [170] have been included. Concerning reliability, Balatsoukas-Stimming and Lin offer the best performance for a block length of 1024 bits. Both of them are implemented

**TABLE 9. Hardware Implementation Part I**

Author	FEC	Decoding algorithm	Block length [Bit]	Code Rate	Hardware implementation	Parallel decoding	Number of iterations (MAX)	Required clock cycles	BER/BLER*	SNR [dB]	Ref
Park et al	LDPC	MIN-SUM	672	0.5	ASIC	Semi-Parallel	10	$\frac{5N}{P}$	$10^{-7}$	4	[156]
Xiang et al	LDPC	MIN-SUM	2304	0.5	ASIC	Semi-Parallel	10	$\frac{N}{P}$	$10^{-6}$	3	[157]
Broulim et al	LDPC	MIN-SUM	64	0.5	FPGA	Full			$10^{-7}$	6.75	[151]
Broulim et al	LDPC	MIN-SUM	128	0.5	FPGA	Full			$10^{-7}$	6	[151]
Broulim et al	LDPC	MIN-SUM	256	0.5	FPGA	Full			$10^{-7}$	4.75	[151]
Chandrasetty et al	LDPC	MIN-SUM	576	0.5	FPGA	Semi-Parallel	10	$\frac{N}{P}$	$10^{-6}$	4.25	[158]
Chandrasetty et al	LDPC	MIN-SUM	1152	0.5	FPGA	Semi-Parallel	10	$\frac{N}{P}$	$10^{-6}$	3.75	[158]
Chandrasetty et al	LDPC	MIN-SUM	2304	0.5	FPGA	Semi-Parallel	10	$\frac{N}{P}$	$10^{-6}$	3.5	[158]
Balatsoukas-Stimming et al	LDPC	MIN-SUM	1000	0.5	FPGA	Full	10	$\frac{2N}{P}$	$10^{-6}$	3.5	[152]
Balatsoukas-Stimming et al	LDPC	MIN-SUM	1152	0.5	FPGA	Full	10	$\frac{2N}{P}$	$10^{-6}$	3.5	[152]
Balatsoukas-Stimming et al	LDPC	MIN-SUM	1152	0.5	FPGA	Full	10	$\frac{2N}{P}$	$10^{-6}$	4.25	[152]
Petrovic et al	LDPC	Layered BP	2304	22/68	FPGA	Semi-Parallel	10	$\sim \frac{N}{P}$	$10^{-4*}$	0.75	[159]
Yesil et al	LDPC	Layered BP	2304	0.5	FPGA	Full	10	$\frac{N}{P}$	$10^{-8}$	3.25	[154]
Petrovic et al	LDPC	Flooding BP	2304	22/68	FPGA	Semi-Parallel	10	$\sim \frac{N}{P}$	$10^{-5*}$	0.25	[159]
Yen et al	LDPC	BP Based	672	0.5	ASIC	Full	11	$\frac{N}{P}$	$10^{-7}$	6	[155]
Li et al	LDPC	BP	576	0.5	FPGA	Full	10	$\frac{NR}{P}$	$10^{-9}$	4.5	[153]
Wu et al	POLAR	OSD	128	0.5					$10^{-4*}$	4	[16]
Wu et al	POLAR	OSD	256	0.5					$10^{-3*}$	4	[16]
Kam et al	POLAR	SC	1024	0.5	ASIC	Semi-Parallel		$2\log(\frac{N}{4P})$	$\frac{10^{-4}}{10^{-5*}}$	3.5	[161]
Leroux et al	POLAR	SC	1024	0.5	FPGA	Semi-Parallel		$\frac{N}{P} \log_2(\frac{N}{4P})$	$\frac{10^{-5}}{10^{-4*}}$	3.75	[163]
Yuan et al	POLAR	SC	1024	0.5	FPGA	Semi-Parallel		$1, 5N - 2$			[164]
Giard et al	POLAR	SC	1024	0.5	FPGA ASIC	Semi-Parallel		$\sim \frac{N}{P} + 4$	$\frac{10^{-6}}{10^{-4*}}$	3.5	[165]
Giard et al	POLAR	SC	2048	0.5	ASIC	Semi-Parallel		$\sim \frac{N}{P} + 4$	$\frac{10^{-6}}{10^{-4*}}$	3	[165]
Ercan et al	POLAR	SC	1024	0.5	FPGA	Semi-Parallel		$\frac{\log_2 N + 1}{P}$	$\frac{10^{-7}}{10^{-5*}}$	4	[162]
Ercan et al 2020	POLAR	SC	1024	0.5	ASIC	Semi-Parallel		$\frac{N}{3P}$	$10^{-6*}$	3.5	[171]
Tajima et al	POLAR	BP	128	0.5			8	$\sim 2N + 2NR$	$10^{-4*}$	6	[174]

on ASIC and provide BLER of  $10^{-6}$  for SNR close to 4 dB. Ercan in 2020 offers an alternative to SCL by introducing the SCF algorithm, which provides similar reliability to Lin and Fan models, with a reduced complexity  $N/3P$  [171]. The Ercan model is currently the first implementation of SCF. In

the specific, an ASIC has been used for the model [171]. Also, the implementation of the Sphere algorithm [148], [172], [173] reveals promising for reduced block lengths. However, the information on the hardware implementation of this approach is scarce. Similarly addressed is the use of the OSD

**TABLE 10. Hardware Implementation Part II**

Author	FEC	Decoding algorithm	Block length [Bit]	Code rate	Hardware implementation	Parallel decoding	Number of iterations (MAX)	Required clock cycles	BER/BLER*	SNR [dB]	Ref
Husmann et al	POLAR	Sphere	128	0.5		Avaiable		$\frac{2^K}{P}$	$10^{-6}$	4	[148]
Piao et al	POLAR	Sphere	64	0.5				$LN \log N$	$10^{-5*}$	2	[172]
Hashemi et al	POLAR	List Sphere	1024	0.5	ASIC	Semi-Parallel		$N \log_2 N - 1$	$10^{-5}/10^{-4*}$	3	[173]
Yuan et al	POLAR	SCL	1024	0.5	ASIC			$\sim \frac{N}{2} + (\frac{N}{P}) \log_2(\frac{N}{4P})$	$10^{-4*}$	2.5	[166]
Yuan et al	POLAR	SCL	1024	0.5	ASIC			$\sim N + (\frac{N}{P}) \log_2(\frac{N}{4P})$	$10^{-4*}$	2.5	[166]
Balatsoukas-Stimming et al	POLAR	SCL	1024	0.5	ASIC	Semi-Parallel		$(2 + R)N + (\frac{N}{P}) \log(\frac{N}{4P})$	$10^{-6*}$	4	[167]
Xiong et al	POLAR	SCL	1024	0.5	ASIC			$3\frac{N}{NR} + \frac{NL}{P} \log \frac{NL}{8P}$	$10^{-4}/10^{-2*}$	2.6	[168]
Lin et al	POLAR	SCL	1024	0.5	ASIC	Semi-Parallel		$\sim 2N + \frac{N}{P} \log_2 \frac{N}{4P} + \frac{R}{N}$	$10^{-6*}$	3.6	[169]
Fan et al	POLAR	SCL	1024	0.5	ASIC	Semi-Parallel		$3N + \frac{N}{P} \log_2 \frac{N}{4P}$	$10^{-5*}$	2.5	[170]
ZTE	TBCC	WAVA	100			Semi-Parallel	2	$\frac{N}{P} + 60$			[179]
Wang et al	TBCC	CVA	40				20		$10^{-6*}$	5	[181]
Zhou et al	TBCC	ML+OSD	144	0.5					$10^{-6*}$	1.75	[182]
Liang et al	TBCC	WAVA	128	0.5			10	$\sim N2^m$	$10^{-6*}$	3.5	[180]
Shin et al	Turbo	Log Map	1024	0.3	ASIC	Semi-Parallel	6	$\sim \frac{N}{P}$	$10^{-5}$	0.8	[178]
Bougard et al	Turbo	SW Map	128	0.3	FPGA		6		$10^{-7}$	6	[175]
Bougard et al	Turbo	SW Map	64	0.3	FPGA	Semi-Parallel	6		$10^{-8}$	5.5	[175]
Wong et al	Turbo	SW MAP	512	0.3	ASIC	Semi-Parallel	8	$\sim \frac{2N}{P}$	$10^{-5}$	1.75	[176]
Wong et al	Turbo	SW MAP	256	0.3	ASIC	Semi-Parallel	8	$\sim \frac{2N}{P}$	$10^{-5}$	2.25	[176]
Wong et al	Turbo	SW MAP	128	0.3	ASIC	Semi-Parallel	8	$\sim \frac{2N}{P}$	$10^{-5}$	3	[176]
Xiang et al	Turbo	APTD	64	0.3		Semi-Parallel	8	$\sim \frac{2N}{P}$	$10^{-5*}$	5.25	[177]
Xiang et al	Turbo	APTD	512	0.3		Semi-Parallel	8	$\sim \frac{2N}{P}$	$10^{-5*}$	2.5	[177]
Xiang et al	Turbo	ML-MAP	64	0.3		Semi-Parallel	8	$\sim \frac{2N}{P}$	$10^{-5*}$	7.25	[177]
Xiang et al	Turbo	ML-MAP	512	0.3		Semi-Parallel	8	$\sim \frac{2N}{P}$	$10^{-5*}$	2	[177]
Maunder et al	Turbo	Log MAP	480	0.3		Full	8	$\sim \frac{2N}{P}$	$10^{-5*}$	3	[150]
Maunder et al	Turbo	Log MAP	48	0.3		Full	8	$\sim \frac{2N}{P}$	$10^{-5*}$	7	[150]

TABLE 11. Proposed Decoding Algorithm

FEC	Decoding algorithm	Author	Decoding architecture	Required clock cycles	Iterations	P	Ref
QC-LDPC	BP	Li et al	Full parallel	$\frac{NR}{P}$	10	N	[153]
CA-POLAR	SCL	Fan et al	Semi parallel	$\frac{N}{P} \log_2 \frac{N}{4P}$		64	[170]
LTE TURBO	Log-MAP	Maunder et al	Full parallel	$\frac{2N}{P}$	8	N	[150]
TBCC	WAVA	ZTE	Semi parallel	$\frac{N}{P} + 60$	2	128	[179]

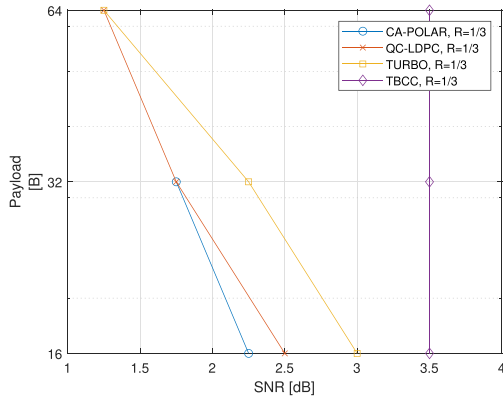


FIGURE 3. Reliability results for  $R=1/3$ .

algorithm [16]. Among the various proposals examined, the BP algorithm [174] appears to be the least efficient for Polar codes. In conclusion, SCL-based implementations are the most efficient in complexity and reliability. Nevertheless, SCF is just a promise, and further investigation regarding this novelty is necessary.

### C. PARALLEL CONCATENATED CONVOLUTIONAL CODES (PCCC)

PCCC code implementations support the use of Log-MAP-based algorithms that enable iterative decoding. Generally, all of the models allow semiparallel decoding, with complexities tending to  $2N/P$ . Such models are Bougard's [175], Wong's [176], and Xiang's [177]. Further implementations are Shin's model, with complexity tending to  $N/P$  [178], and Maunder's model [150] resulting so far the only proposed full parallel decoding for PCCC. Both models implement MAP. Among the different models, Wong's model performs better in terms of reliability due to an ASIC implementation ensuring a BLER of  $10^{-5}$  at SNR of 1.75, 2.25, and 3 dB, for 512-, 256-, and 128-bit block sizes, respectively.

### D. TAILBITING CONVOLUTIONAL CODES (TBCC)

In the TBCC case, iterative algorithms such as WAVA [179] [180], CVA [181], and OSD [182] are proposed for short packet transmissions. However, performance results are only available for WAVA-based proposals. In particular, the ZTE

model suggested for the 5G NR standard provides a semiparallel architecture with a complexity per iteration tending to  $N/P$  [179].

## VII. RELIABILITY AND LATENCY PERFORMANCE COMPARISONS FOR THE FEC CANDIDATES

This section compares the candidate codes presented in Section III, i.e., QC-LDPC, Polar, TBCC, and PCCC. The analysis is based on a comparison of their reliability and latency performances. Reliability is analyzed using MATLAB simulations based on BLER metrics. Finally, latency is evaluated as decoding latency, following the approach proposed by previous works [33], [38], [39]. The decoding algorithms were previously suggested in Section IV.

### A. PRELIMINARIES

The suggested metrics are applicable to comparisons among different FEC techniques, offering reliability and latency performances for various payload sizes. The BLER represents the reliability metric. For the latency evaluation, the decoding latency is optimal for focusing on the PHY layer performance. Finally, the proposed payload lengths are 16, 32, and 64 B. Concerning the decoding latency evaluation, its calculation is available by counting the number of clocks required in the decoding complexity. For this analysis, the results offered in Section VI are the reference. The FEC candidates compared in this section are QC-LDPC, CA-POLAR, LTE TURBO, and TBCC. QC-LDPC and CA-POLAR are in the 5G NR standard, while TURBO and TBCC are part of LTE. Furthermore, QC-LDPC has coupled to the Belief Propagation algorithm, CA-Polar to an SCL with  $L=2$ , and a CRC of 24 bits, while LTE Turbo uses Log-MAP finally, TBCC with WAVA.

### B. RELIABILITY

The reliability analysis discussed in this section aims to evaluate the performance of the candidates expressed in terms of BLER at different payload lengths. The BLER threshold value is taken by the reliability comparisons proposed in [20], which surveyed and analyzed different FEC techniques candidates for WirelessHP. BLER values have been obtained with a specifically developed MATLAB workbench, which provides simulation results to compare different FEC techniques with code rates 1/3 and 1/2. The code rate at 1/2 is a well-known configuration for industrial communications [20], whereas the



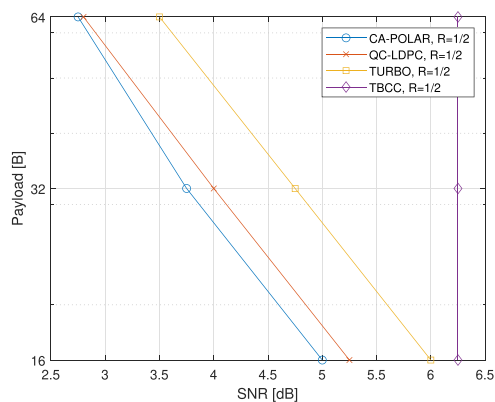


FIGURE 4. Reliability results for  $R = 1/2$ .

case of  $1/3$  is a configuration proposed for 5G NR for the signaling transmission of the Physical Broadcast Channel [183], also targeted for short packet communications. In this case, the data size varies between 40 and 100 bits. The simulations assume QPSK modulation over an AWGN channel. Further simulation parameters are the number of transmissions per simulation point ( $3 \cdot 10^6$  to obtain a BLER threshold of  $10^{-6}$ ). The SNR curve is obtained with a step of 0.25 dB. Figs. 3 and 4 display the simulation results. The curves show the variation of reliability as a function of the payload size. The vertical axis represents the payload values, while the horizontal axis shows the SNR values obtained for each BLER threshold.

Fig. 3 presents the threshold values for code rate  $1/3$ . The figure shows how the SNR for different payload sizes varies according to the FEC employed. It is possible to observe how for the range 16–32 B QC-LDPC, and CA-POLAR provide similar performance, while CA-POLAR is better for 16-B payloads. CA-POLAR lacks the threshold for 64 B due to its specific design in the 5G NR standard. In the 64-B case, QC-LDPC and LTE TURBO have comparable performance. Finally, analyzing TBCC, a constant threshold can be observed as a function of the different payload lengths because it is a CC type.

Fig. 4 shows the threshold values for code rate  $1/2$ . First, it is observed that CA-POLAR provides the best performance in all considered ranges. However, QC-LDPC gets closer when the payload is 64 B. LTE TURBO offers 16 dB lower performance than CA-POLAR, whereas TBCC only offers comparable performance to LTE TURBO for 16 B.

The most relevant conclusions deduced from the results are the following. First, CA-Polar and QC-LDPC outperform the other candidates. Nevertheless, CA-Polar shows slightly better performances. Among the candidates, TBCC offers the worst decoding performance. Second, the variation of payload sizes affects the decoding performances of the candidates, except for TBCC.

### C. LATENCY

Decoding latency is defined using (1). However, this definition requires a previous step, which regards the estimation of the

algorithmic complexity in terms of cycle clocks. Table 11 shows required clock cycles associated with the decoding algorithm choices ( $It$  and  $P$  correspond to the number of iterations and parallel processes, respectively). BP and Log-MAP enable full parallel decoding, while SCL and WAVA only allow semiparallel decoding. For CA-POLAR,  $P = 32$  was assumed for payloads of 16 B, since [170] does not consider such low payload sizes. Table 12 shows both the count of clocks required by the decoding algorithm and the corresponding decoding latencies. The number of clock cycles respects the values of the parameters shown in Table 11. The decoding latency calculation is performed as defined in [39]. The clock frequency is considered at 300 MHz. This choice is motivated by the similar clock frequencies performed by the FPGA models used in [10] and [32]. In [32] a Spartan DS610 is used, whereas [10] proposes a Xilinx 7035i Zynq SoC.

The results show that QC-LDPC and LTE TURBO provide very low decoding latency due to the full parallel decoding, ensuring constant values as the block length varies. QC-LDPC provides a decoding latency of  $0.017\mu s$  and  $0.01\mu s$ , respectively, for code rates of  $1/2$  and  $1/3$ , while LTE TURBO provides a constant decoding latency of  $0.053\mu s$ . Although CA-POLAR does not offer a fully parallel architecture, it allows low latency decoding for 16 and 32 B. In the case of 16 B, it guarantees  $0.027\mu s$  for code rate  $1/2$  and  $0.13\mu s$  for code rate  $1/3$ , while for 32 B, it offers  $0.05$  and  $0.13\mu s$  respectively. Finally, in the case of 64 B, the decoding latency obtained is  $0.11\mu s$ . In conclusion, the best performing choice in terms of latency is the QC-LDPC.

### VIII. FUTURE CHALLENGES

Nowadays, current industrial wireless systems adopt classical FEC techniques with reduced complexity, such as CC and RS. Nevertheless, the numerous contributions in short packet communications risen in URLLC have introduced valid alternatives for these scenarios. Many of these proposals achieve the decoding latency performance of these classic solutions due to the property of parallel decoding typical of the adopted decoding algorithms. Examples are LDPC and Polar codes applied in 5G NR and TBCC and Turbo applied in LTE as observed in Section V-C. Moreover, the recent novelties SVC [88], [91], [92] and PAC Polar [139], whose research is in a preliminary phase, could offer more alternatives for URLLC and FA future developments.

Therefore, based on the results obtained in this study, we discuss some open issues that emerged for FEC techniques in FA environments as follows.

- 1) *MAC layer aspects*: Wireless systems for FA need to ensure stringent performance at the MAC layer. Due to the characteristics of industrial environments, the MAC must provide deterministic communications with a reduced number of retransmissions to ensure low latencies and high reliability, particularly for safety applications, as discussed in Section I-A. In this case, a wireless

**TABLE 12. Decoding Latency Results for a Decoding Clock Frequency of 300 MHz**

FEC	Clock cycles						Decoding latency [ $\mu$ s]					
	16B		32B		64B		16B		32B		64B	
	R=1/2	R=1/3	R=1/2	R=1/3	R=1/2	R=1/3	R=1/2	R=1/3	R=1/2	R=1/3	R=1/2	R=1/3
QC-LDPC	5	3	5	3	5	3	0.017	0.01	0.017	0.01	0.017	0.01
CA-POLAR	8	20	16	20	32		0.027	0.067	0.05	0.13	0.11	
LTE TURBO	16	16	16	16	16	16	0.053	0.053	0.053	0.053	0.053	0.053
TBCC	124	126	128	132	136	144	0.41	0.42	0.43	0.44	0.45	0.48

system design that combines a reduced number of re-transmissions at the MAC layer with high-performant FECs at the PHY layer could achieve the desired performance for critical scenarios.

- 2) *FEC candidates*: Future directions are addressed here for the FEC candidates. The mathematical property of QC-LDPCs allows high performance (as observed in [53]) and a reduced decoding latency due to the full parallel decoding. The literature mainly offers proposals based on MIN-SUM and BP regarding decoding algorithms for short packets. The results proposed within the survey are proposed for AWGN channels, proposing both implementations on FPGAs and ASICs. CA-Polars show high performance for short packets when SCL is adopted. The proposals surveyed in this work allow semiparallel decoding and reduced decoding latencies. However, the decoding latencies are higher than QC-LDPC. Numerous trials published in the literature adopt ASIC [22]. Moreover, new decoding algorithms for CA-Polar have been proposed recently, offering interesting results (SCF, Sphere) [148], [171], [172], [184]. However, only preliminary results are provided. The proposed Log-Map decoding algorithm for Turbo codes in [150] offers a full-parallel solution for the first time in these FECs. Finally, TBCC with WAVA seem to cope with the high decoding latencies characteristic of this FEC technique [179]. The authors have detected the following future directions for the proposed solutions. On the one hand, the combination with the FEC and the suggested algorithms must be tested with simulations to evaluate their performance with industrial channels. On the other hand, field trials within industrial environments must be conducted.
- 3) *Noveloneous decoding algorithms for the FEC candidates*: CA-Polar is a hot topic concerning the coding theory due to its demonstrated performance for short packet transmissions. Traditionally, SCL is the decoding algorithm adopted with this FEC. Nevertheless, novelties such as SCF [171] and sphere decoding algorithms [148], [172], [184] could achieve SCL performance with lower latencies. Therefore, further studies in this direction are needed. Analyzing the contents of these articles is possible addressing the following challenges. For [148], [171], and [172] the algorithms structure is described, and preliminary results obtained

by simulations are given. Therefore, the subsequent hardware implementation for these proposals must be proposed considering FPGA or ASIC to compare with the previous proposals' results. Finally, the authors in [184] offer a detailed description of the proposal with a guideline for its hardware implementation. Nevertheless, this work lacks comparable results; consequently, preliminary studies must be conducted to evaluate the algorithm's performance with simulations, considering AWGN and industrial channel models.

- 4) *Novelties on FEC techniques*: SVC has recently emerged as a potential FEC technique for extremely short packet transmission (payloads below 100 bits), offering performance comparable to CA-Polar [88], [89], [90], [91], [92]. Preliminary studies show that SVC has limitations in code rate values (lower or equal than 1/4) and modulations. Nevertheless, SVC could be considered an excellent candidate for future FA applications, particularly in safety communications. Therefore, its hardware implementation toward ultralow latency communications is a future challenge.
 

PAC, recently introduced by Arikian [139], also presents capabilities as a future candidate for FA communications, potentially outperforming CA-Polar. Nevertheless, the studies presented are preliminary, showing a few contributions focused on decoding algorithms. Potentially, PAC could be a potential FA candidate if combined with decoding algorithms designed for low-latency communications. Therefore, the development of decoding algorithms will be a hot topic and raise interest in future studies.
- 5) *Toward the use of nonlinear codes in FA applications*: The binarization of the Preparata and Kerdock codes combined with low complex decoding algorithms addresses future challenges for low latency communications [40]. In this first proposal, only the MAP decoding algorithm has been considered. Therefore, the following challenges have been detected. First, a hardware implementation must be conducted as it could open new frontiers for low latency communications and FA. Second, different decoding algorithms suitable for FA environments, such as BP or SCL, must be tested and compared with the results of adopting MAP, as this research topic shows only this preliminary contribution.

## IX. CONCLUSION

FEC techniques within FA wireless systems are crucial for meeting FA requirements. Several articles on URLLC identify FEC as the tool for ensuring high reliability and low latency wireless communications when short payloads are transmitted. However, there is a gap in the literature on the method for applying FEC techniques for FA communications, which, compared to URLLC, have more demanding requirements.

In this work, the aim was to satisfy this need. This article has studied the FA background at a high level and several proposals related to the design of wireless systems for FA. Subsequently, the study focused on a general overview of the use cases proposed. One relevant conclusion is the lack of focus on the PHY layer. As a result, the use cases exclusively offer requirements for the MAC layer. However, the PHY layer design is not negligible in this particular family of wireless communications. The properties of the propagation model typical of the industrial channel models complicate the exclusive use of retransmission techniques to fulfill the FA requirements. Such requirements refer to the inherent criticality of industrial processes, where the protection of workers, machinery, and production is essential.

After discussing the problems related to the FA requirements, the focus shifts to the in-depth study concerning the FEC techniques. The first part of this study has consolidated a comprehensive state-of-the-art of FEC techniques. The proposed techniques are considered the most suitable for short packet communications. The chosen parameters are parallel decoding, which benefits the latency performance and high reliability in short packet communications. The identified FEC candidates are QC-LDPC, POLAR, TBCC, and PCCC. In particular, in POLAR, CA-POLAR is considered, while LTE TURBO for the case of PCCC.

Another relevant aspect regarding the FEC techniques is the choice of decoding algorithms. These methodologies strongly influence the PHY layer performance and are essential to meet the requirements. The suggested combinations are BP for QC-LDPC, SCL for CA-POLAR, WAVA for TBCC, and Log-MAP for LTE TURBO. These choices arise from the performance analysis of several proposals encountered in the literature.

A further element resulting from this work is the absence of specific metrics in the analysis of FEC for short packet communication scenarios. Consequently, the desired PHY layer performance for FA use cases is not precise. One result of this work is the proposals of PHY layer metrics. It was then possible to compare the FEC candidates through their use. The results show that QC-LDPC and CA-POLAR are suitable for meeting the FA requirements. In particular, QC-LDPC is a potential candidate for critical communications, while CA-POLAR for safety communications.

Finally, based on the study proposed in this survey, we have pointed out further future research for developing FEC techniques in short packet transmissions, and particularly, for FA scenarios. On the one hand, we have addressed the studies for the proposed candidates. On the other hand, we have detected

the novelties recently introduced in the literature potentially applicable to the considered scenarios.

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